Contention and memory controllers

An introduction to (ideas on) tracking multi-core contention in DRAM

Asier Fernández de Lecea
Francisco J. Cazorla

Presentation outline

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Executive summary

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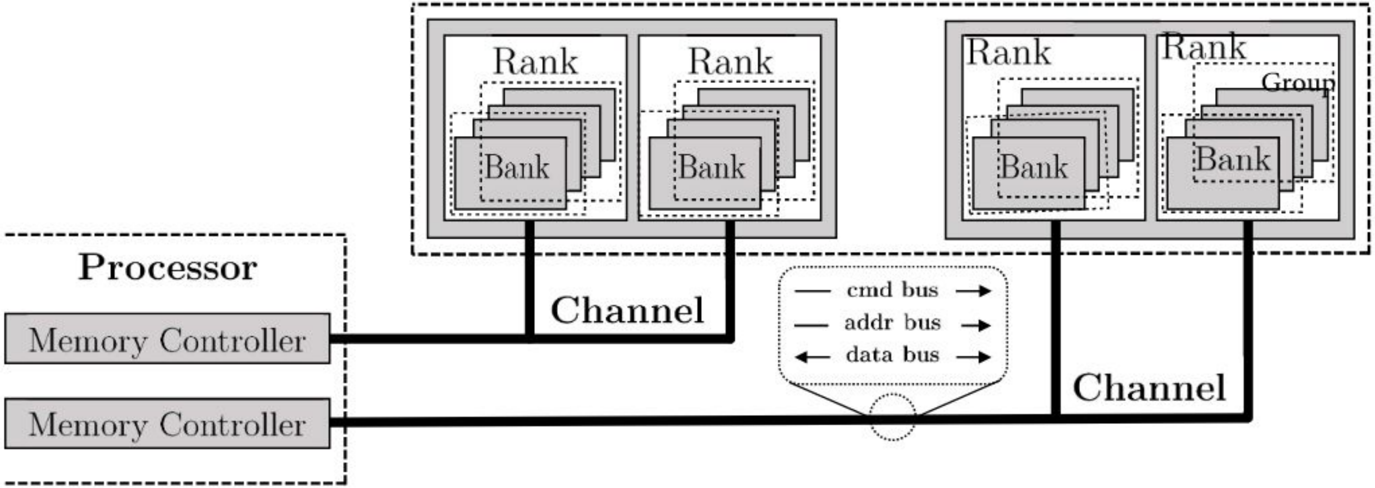
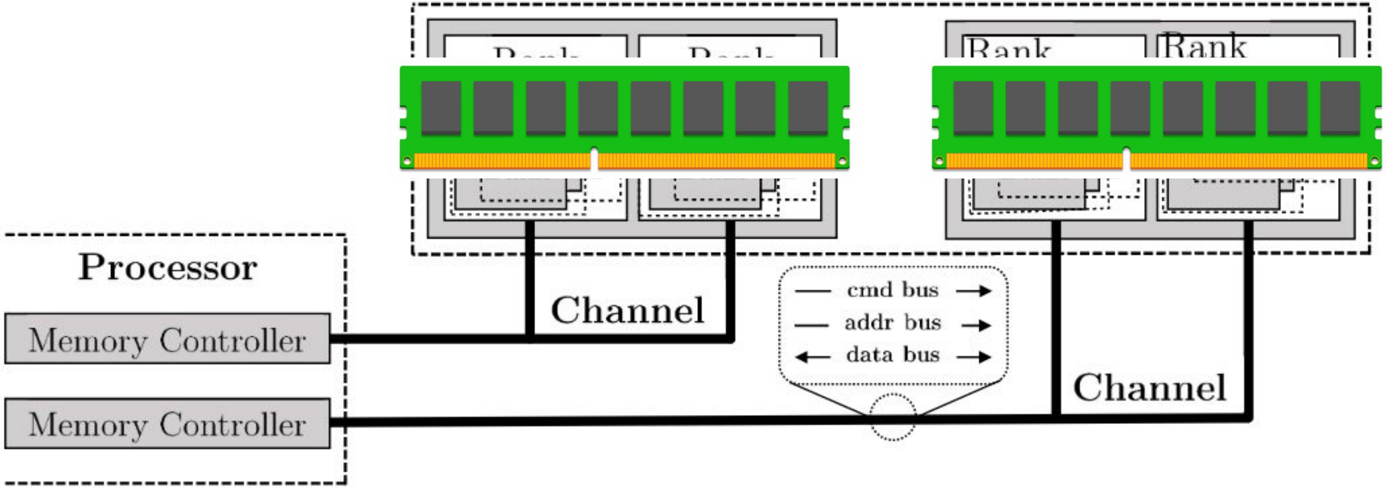
- We propose an extension of an MC’s timing-constraints table that regulates the execution of DRAM commands
- The timing-constraints table can be expanded-upon to incorporate different levels of contention specificity
- This extension is compatible with static- and dynamic-command-scheduling controllers

Memory controllers



Memory controllers



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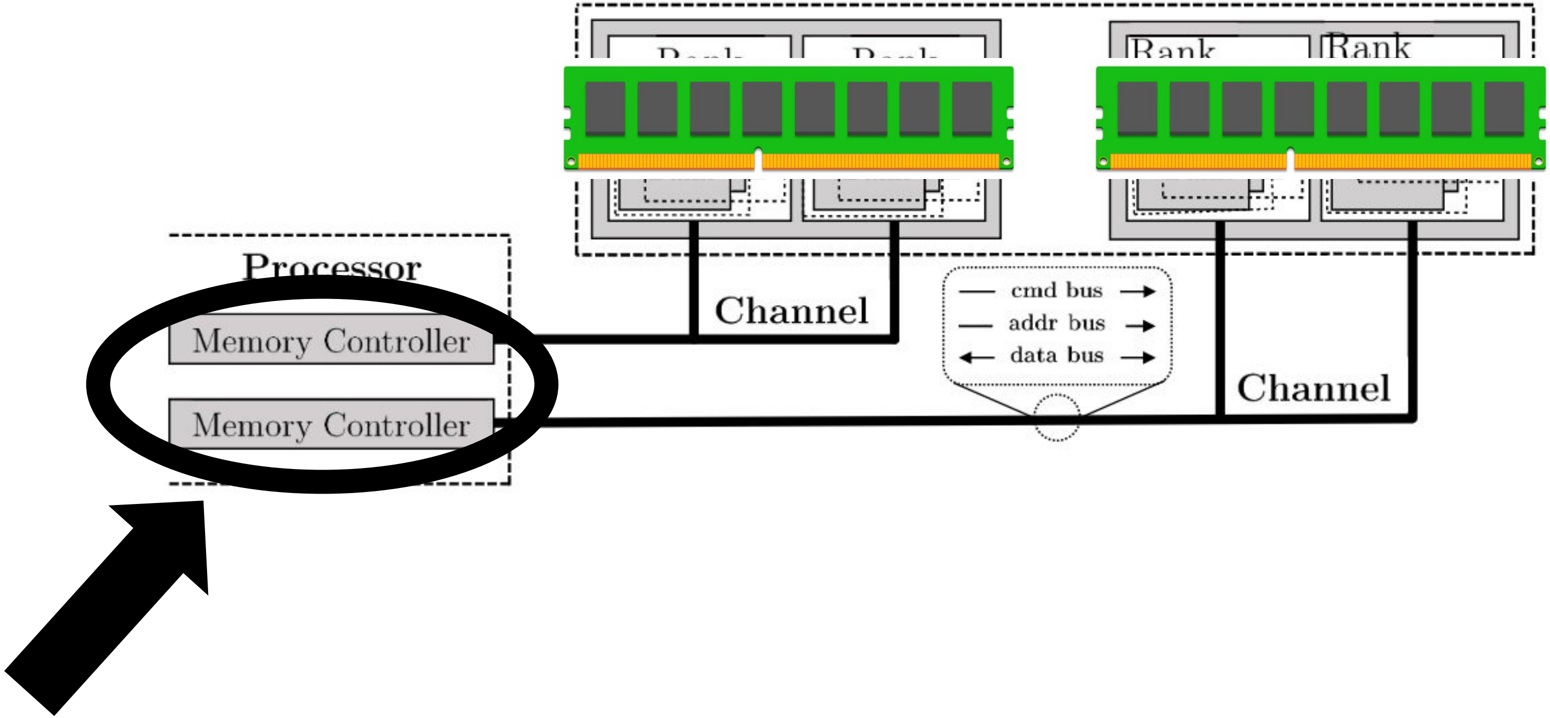
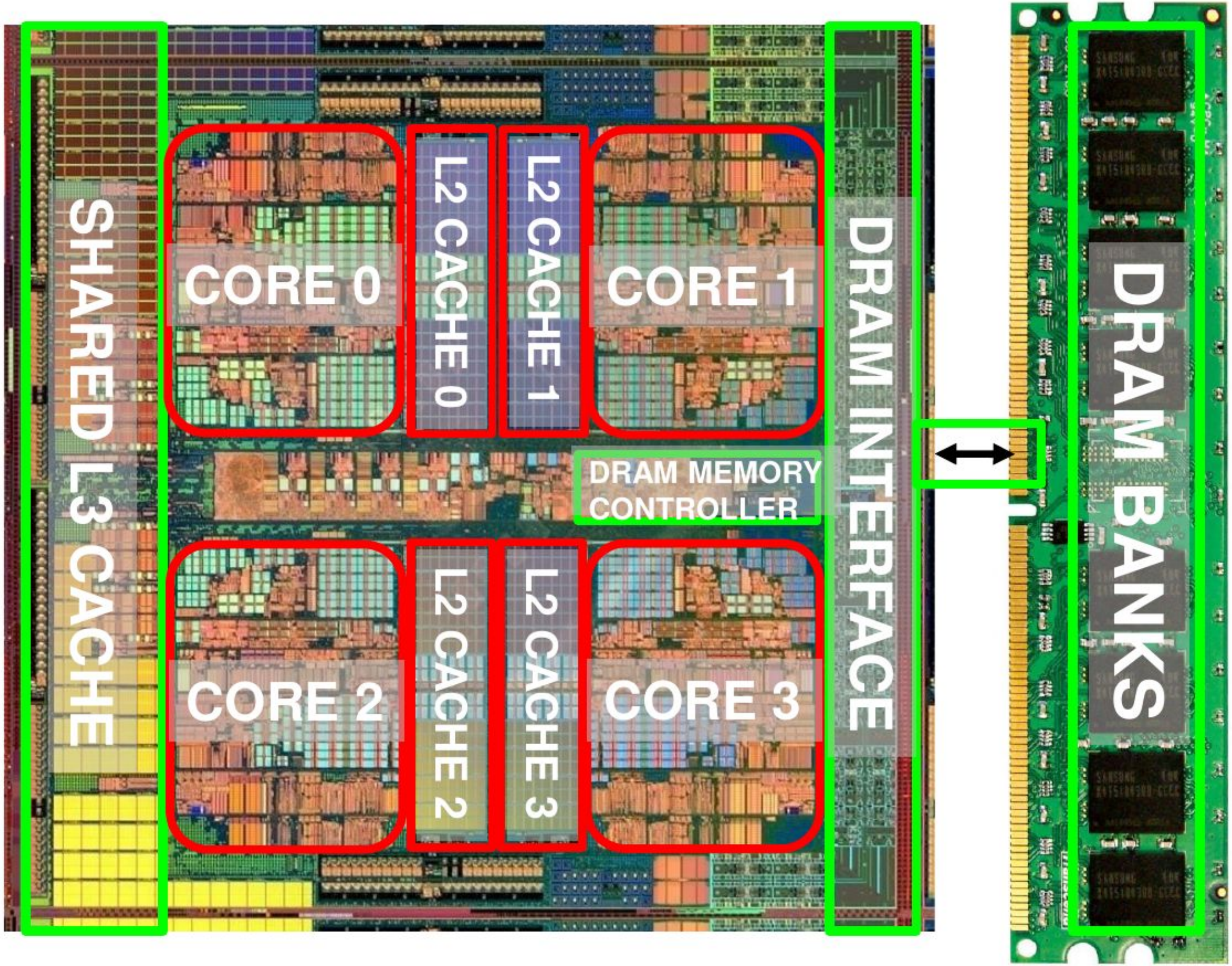
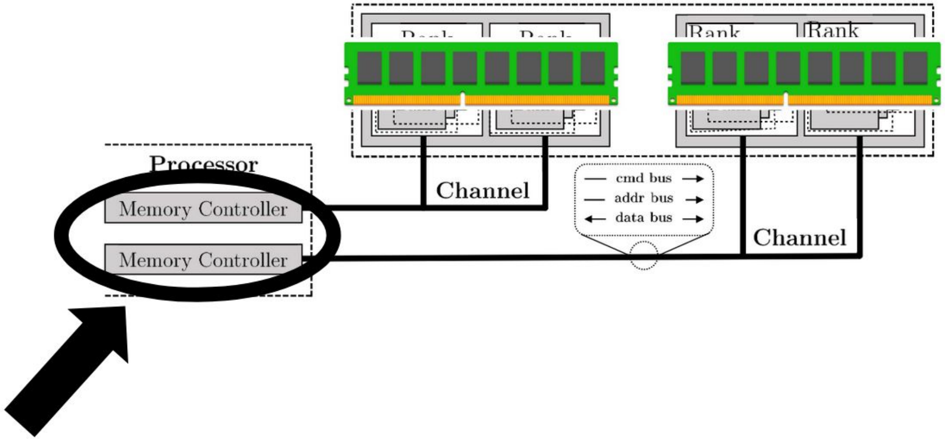




AMD Barcelona, 2006

Memory controllers

DRAM MCs manage **read** and **write transactions** from CPU to DRAM



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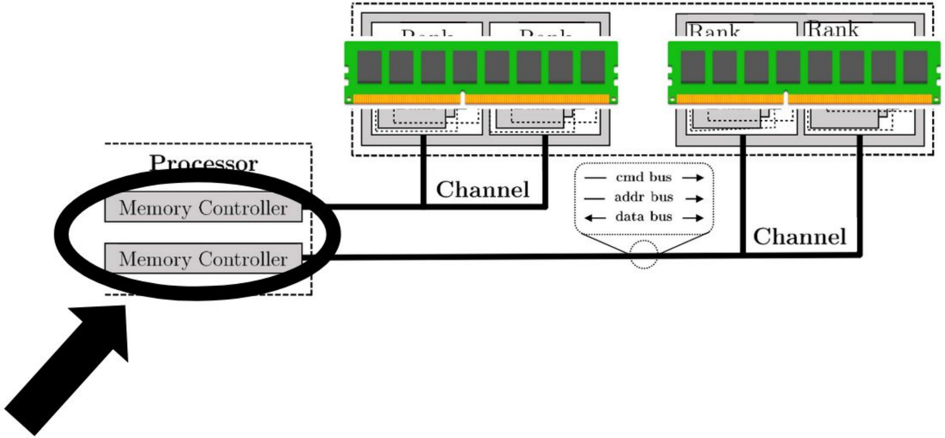

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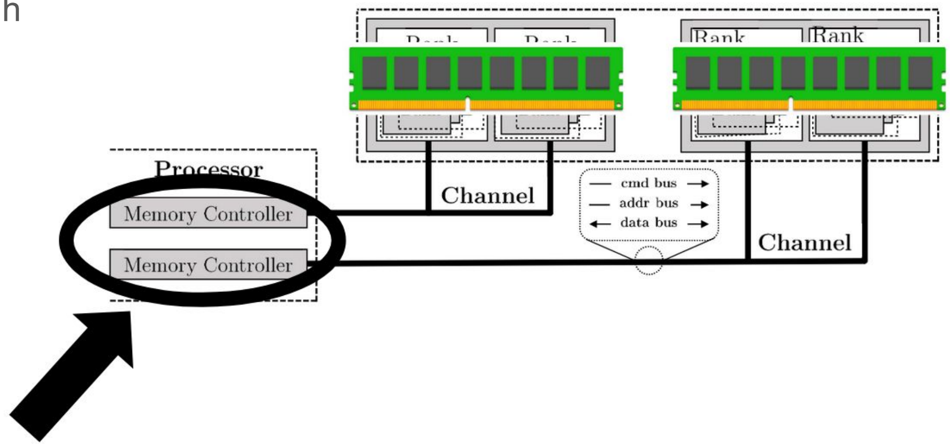

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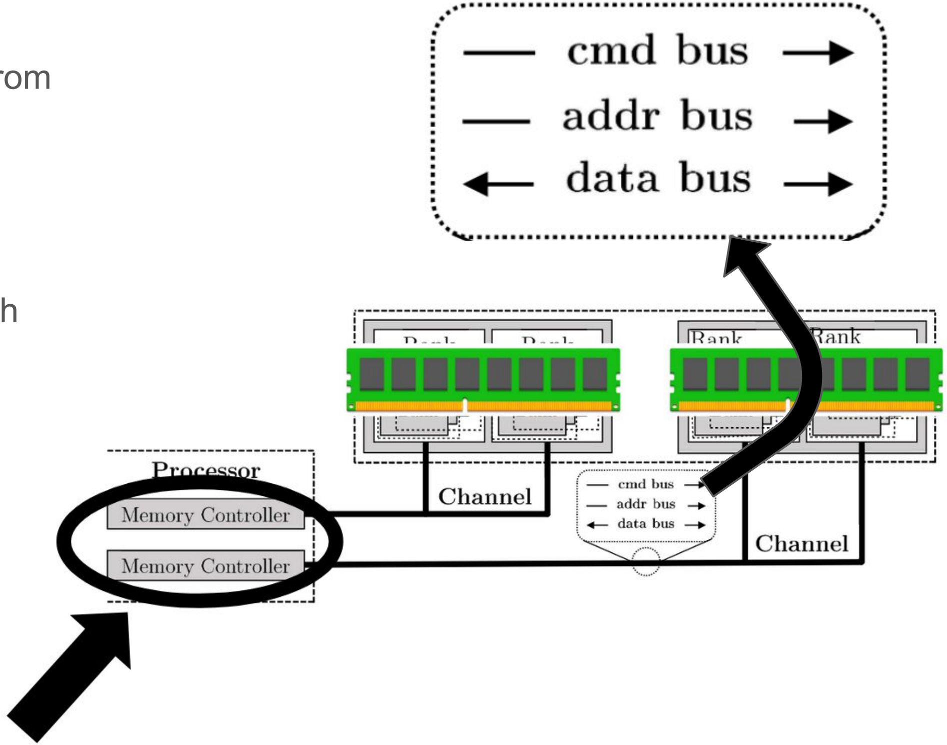

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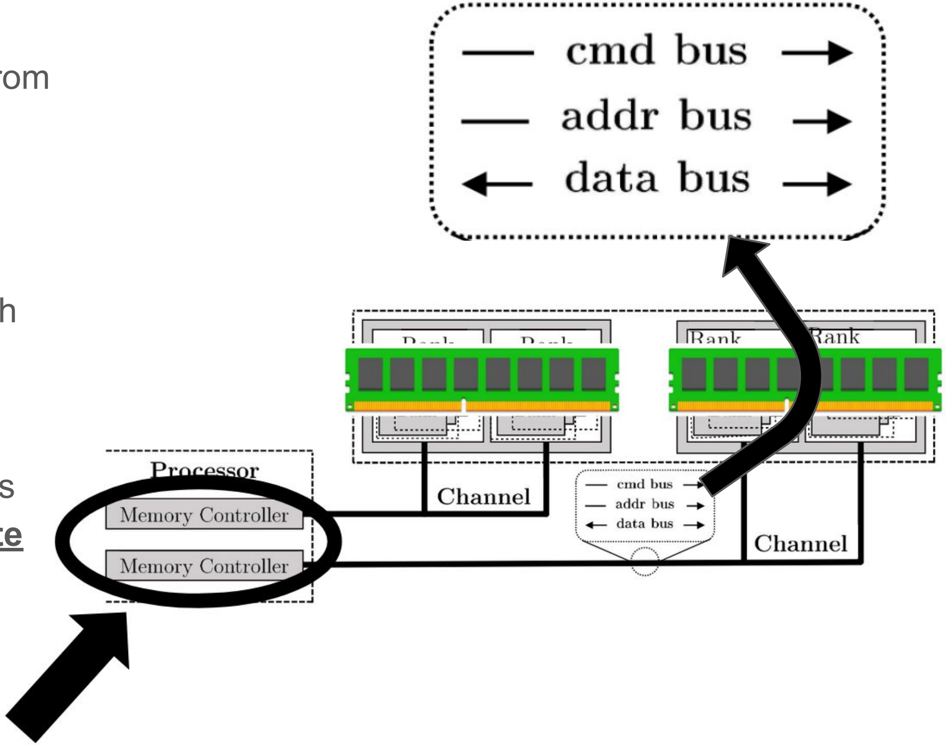

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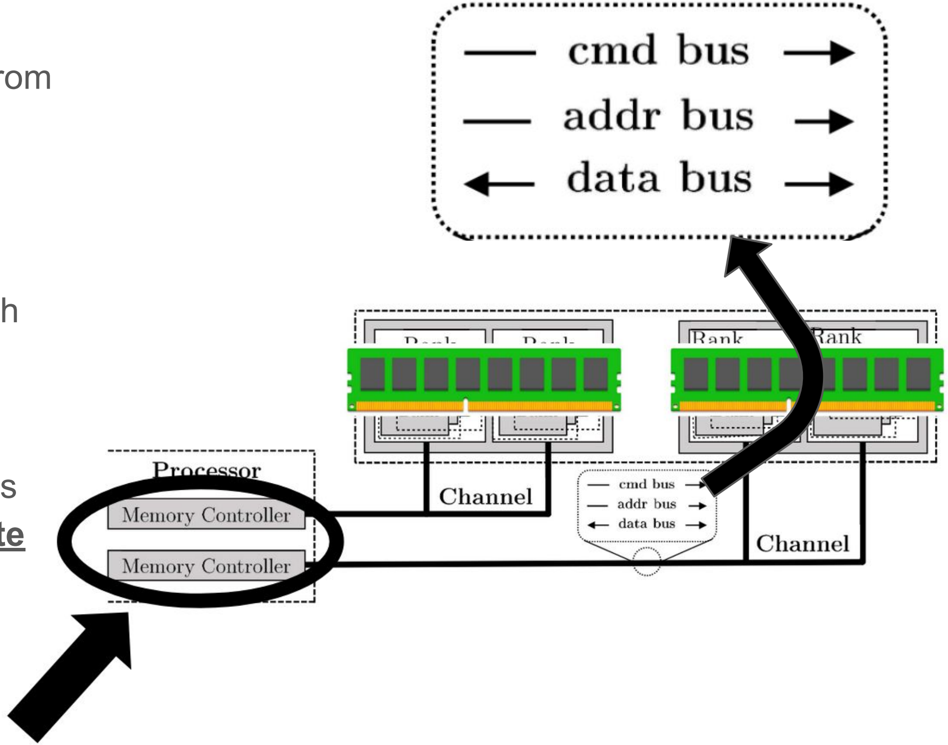
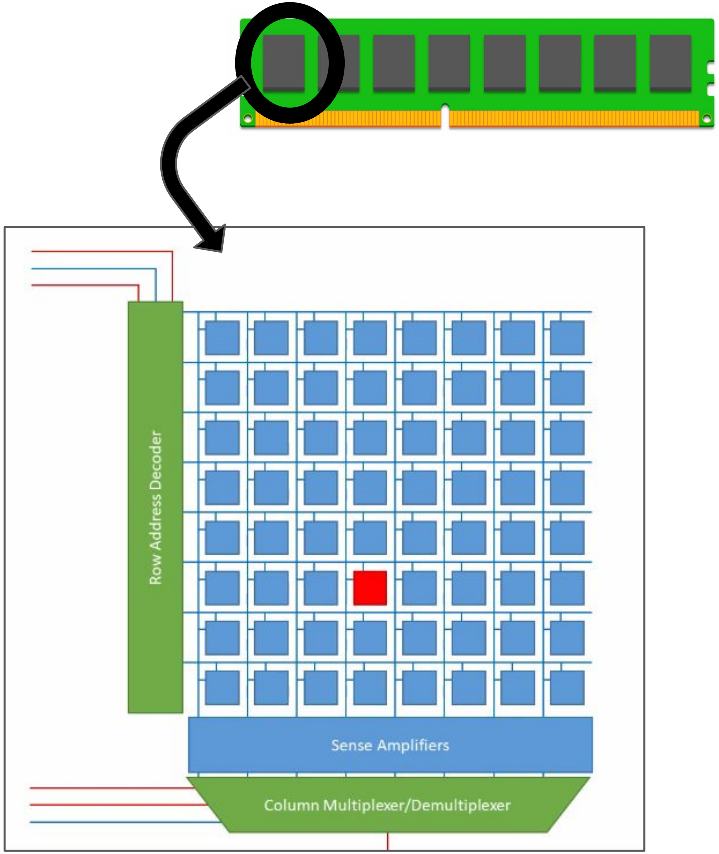
Wait… DRAM commands???



DRAM protocol speedrun

Let’s get into DRAM commands and JEDEC timing constraints!! :)



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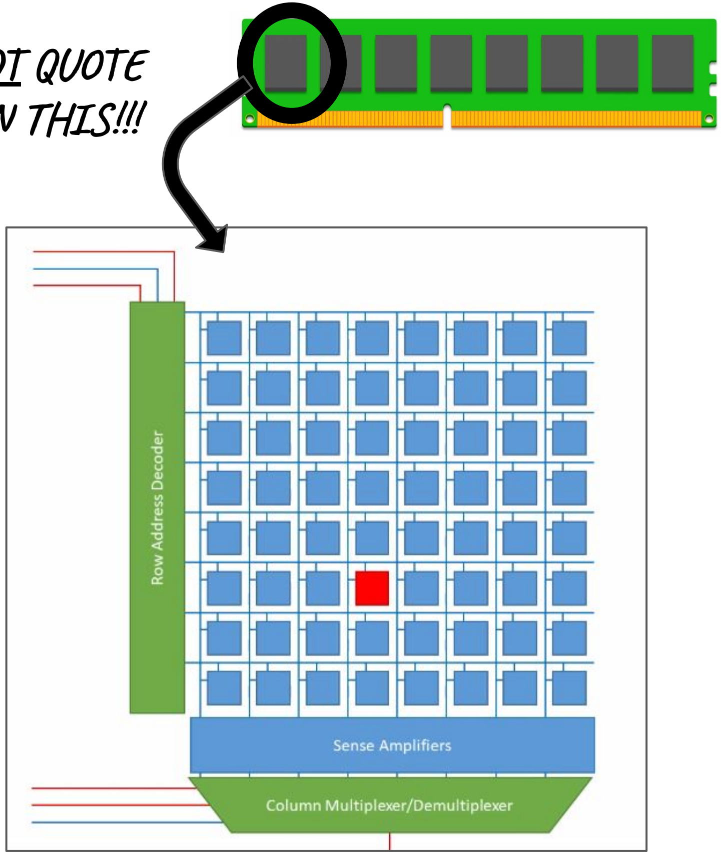

DO NOT QUOTE ME ON THIS!!!

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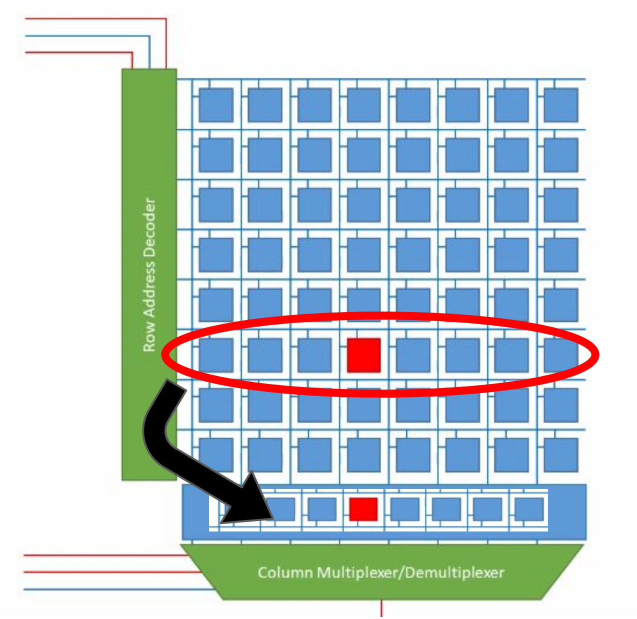

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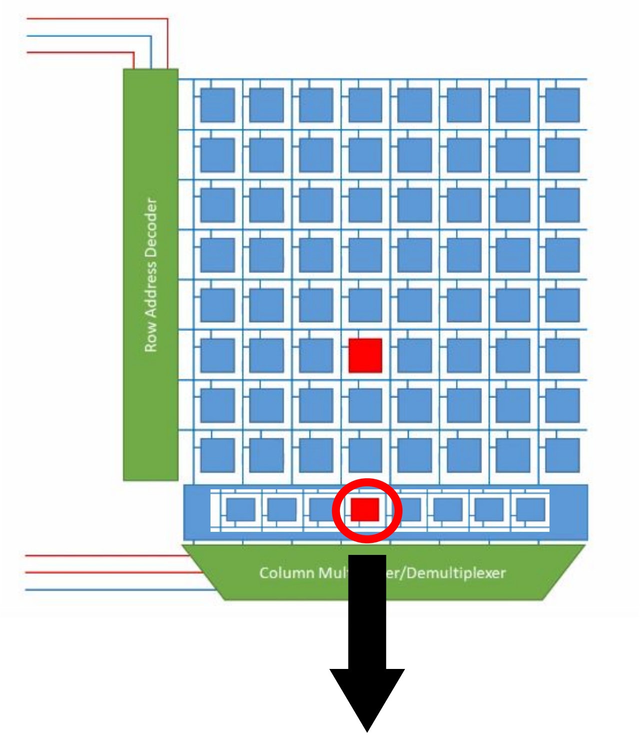

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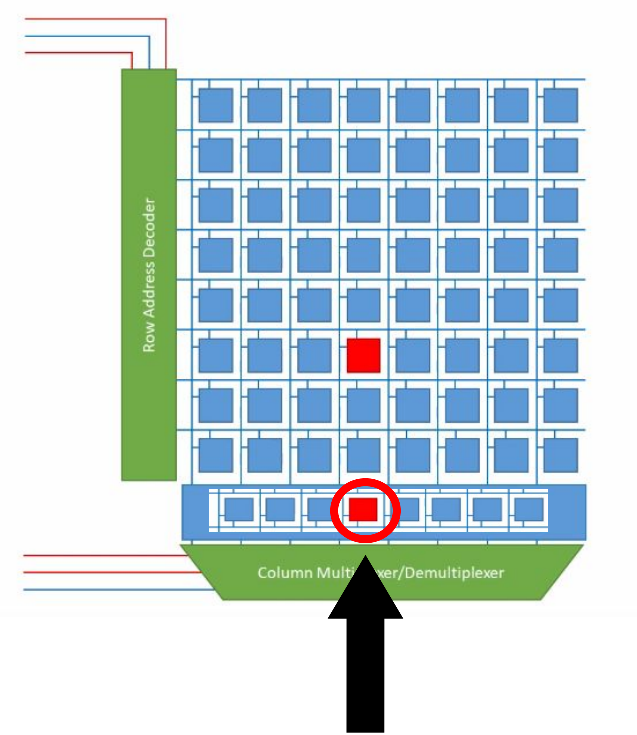

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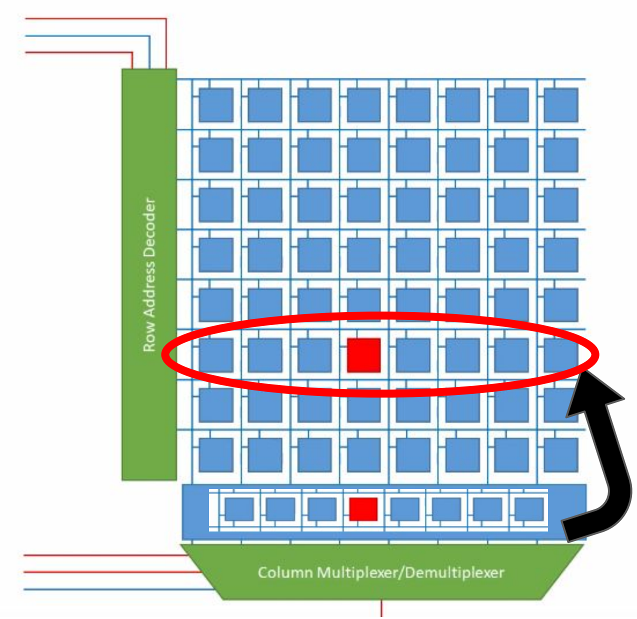

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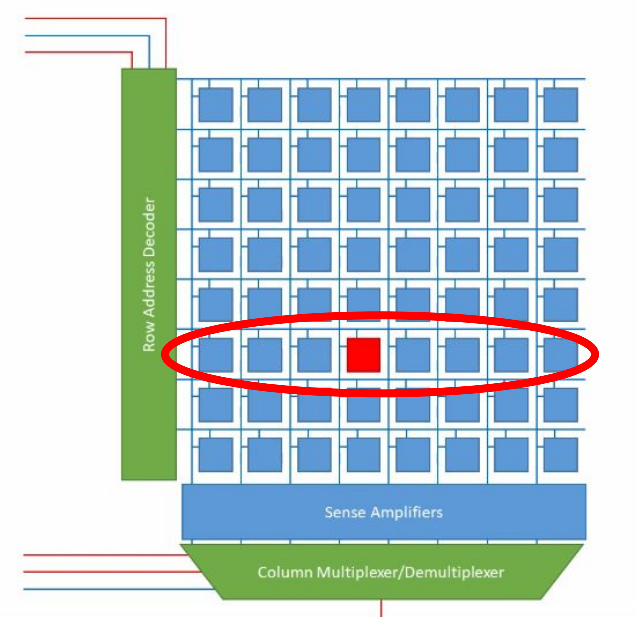

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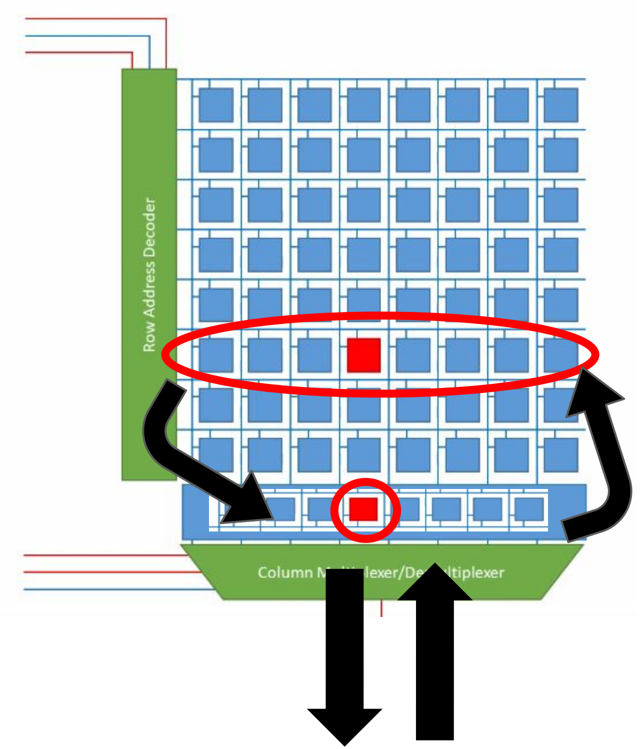

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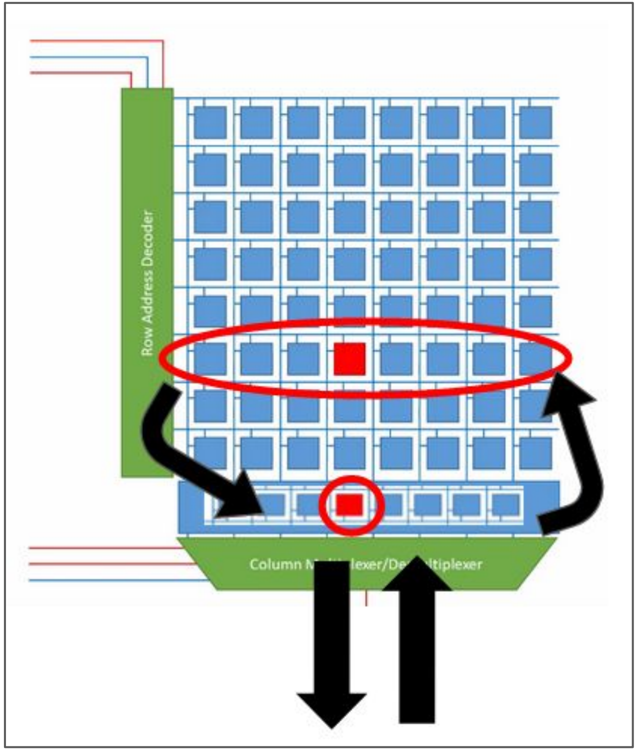

KEY IDEA: DRAM commands must respect certain timing constraints between each other to ensure integrity of data

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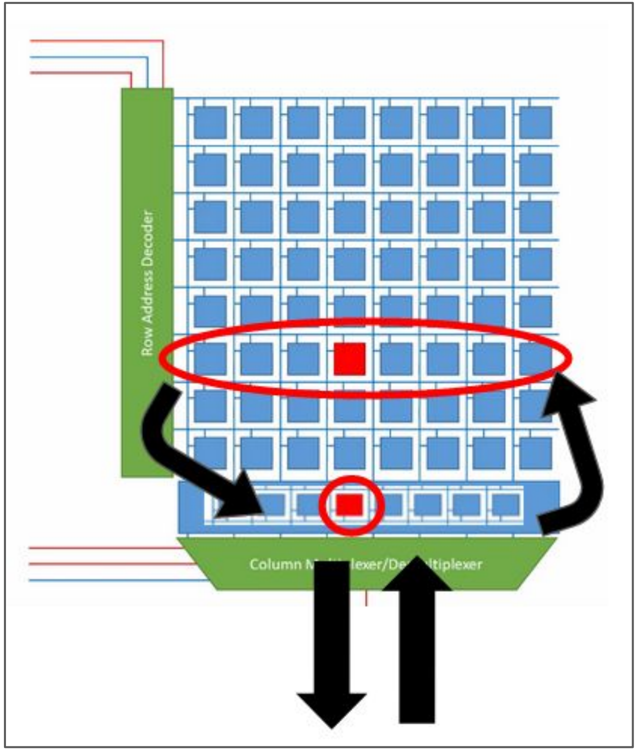

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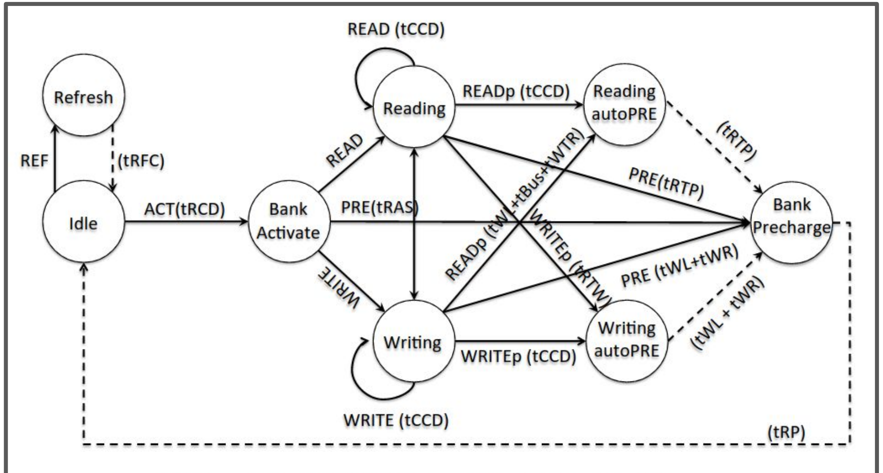
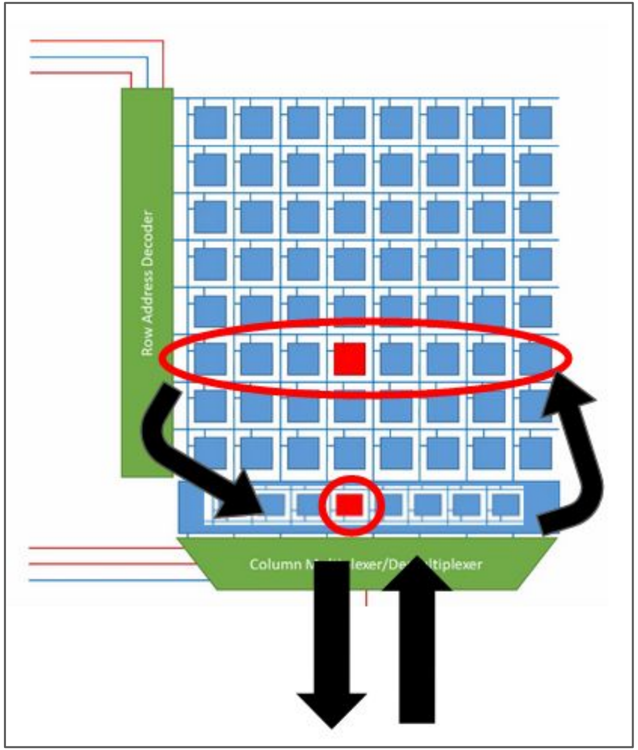


Figure 2.2: DRAM Operation State Machine.

DRAM protocol speedrun



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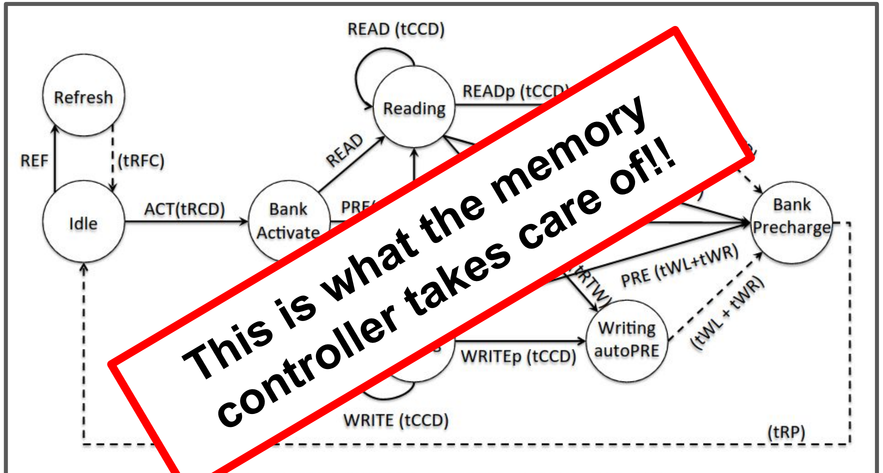
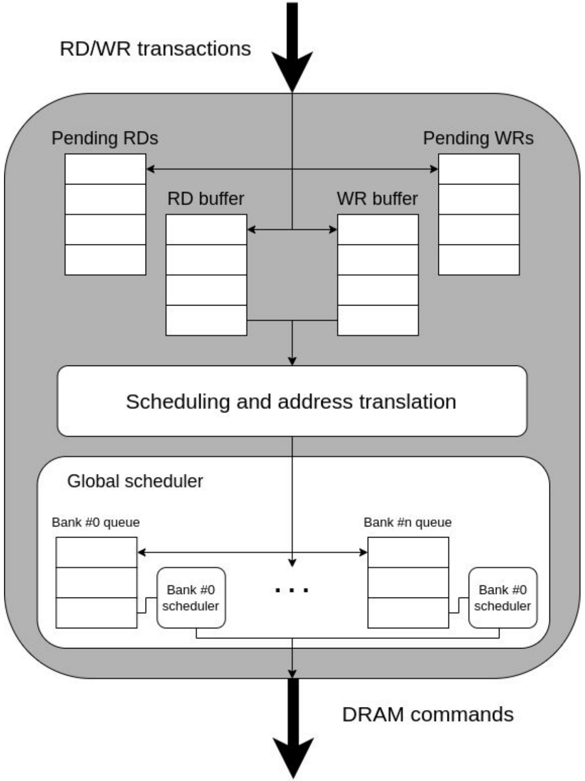


This is what the memory controller takes care of!!

Figure 2.2: DRAM Operation State Machine.

Structure (logical) of a memory controller



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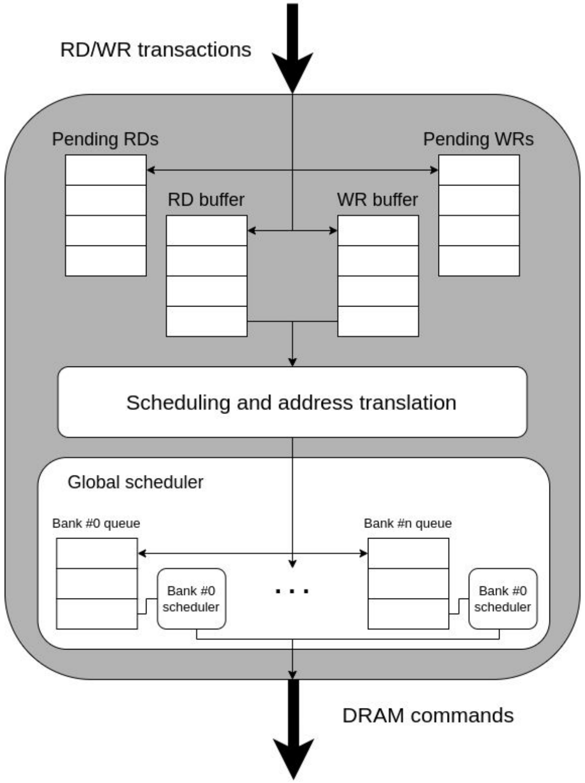

Front-end:
transaction-level
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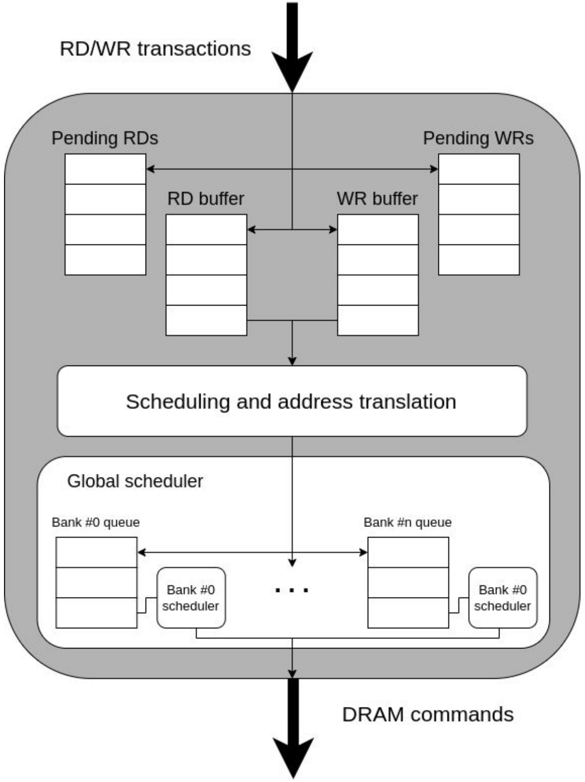
Structure (logical) of a memory controller



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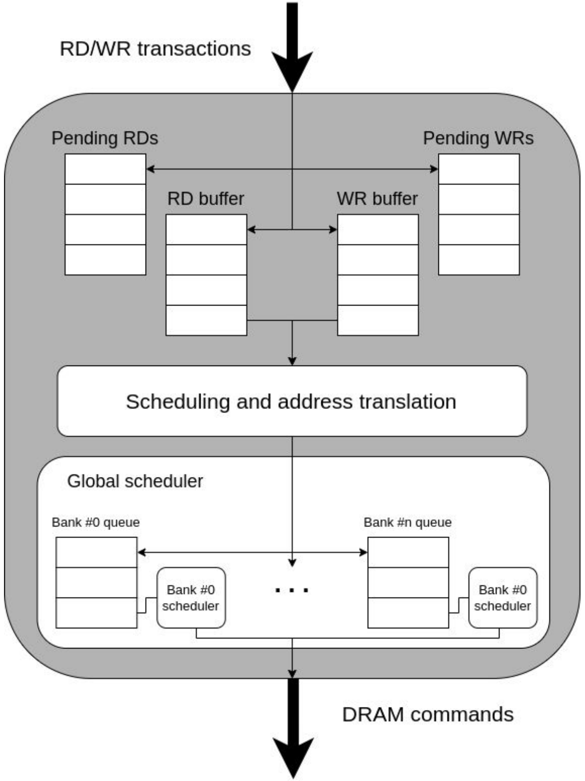
Back-end: DRAM command generation



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Not so relevant, contention-wise

Structure (logical) of a memory controller

This is where the magic happens!!

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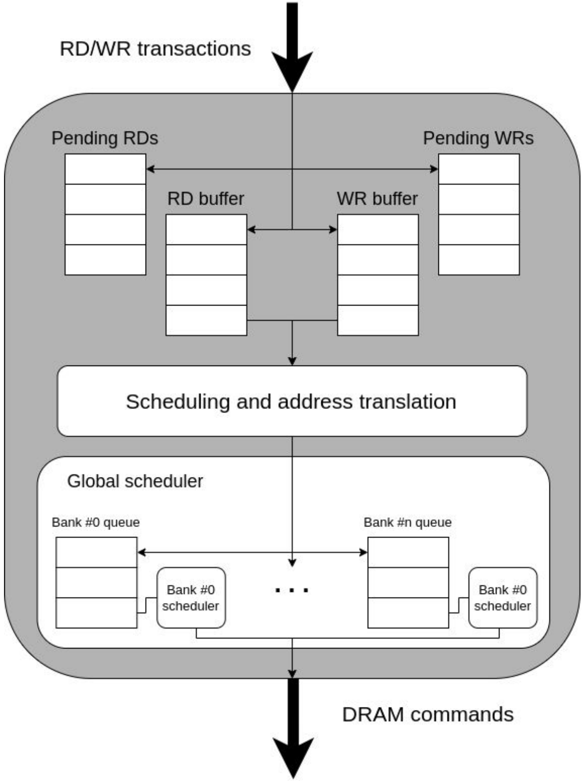

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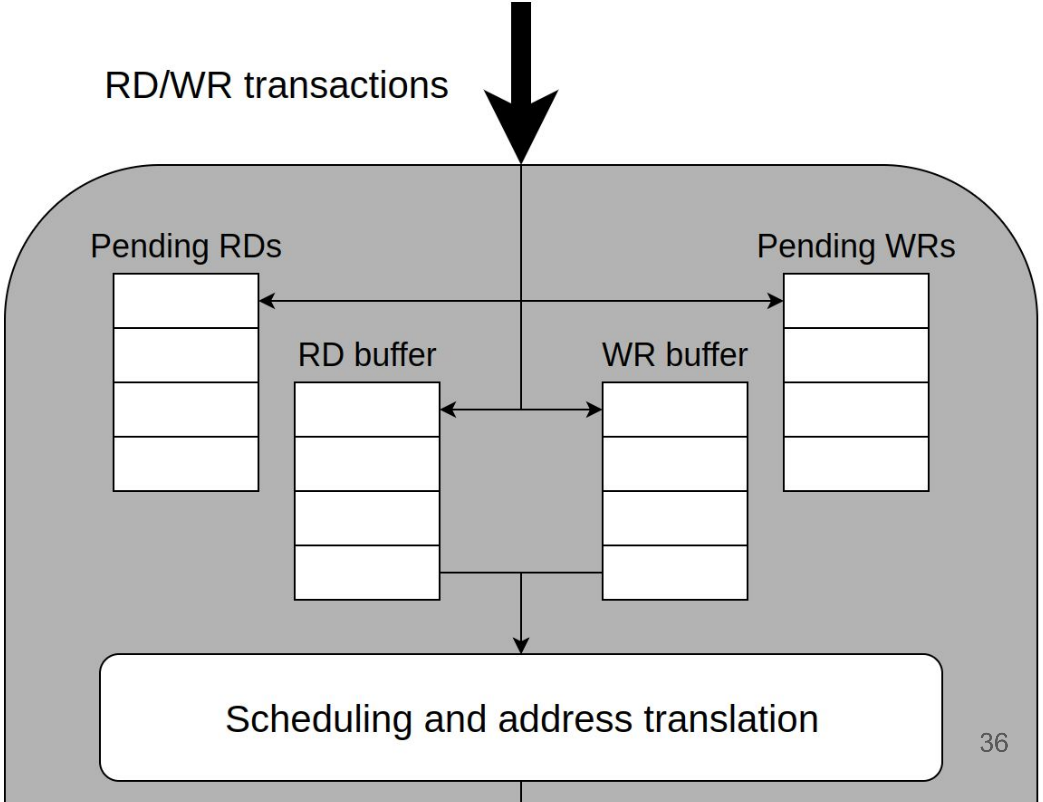

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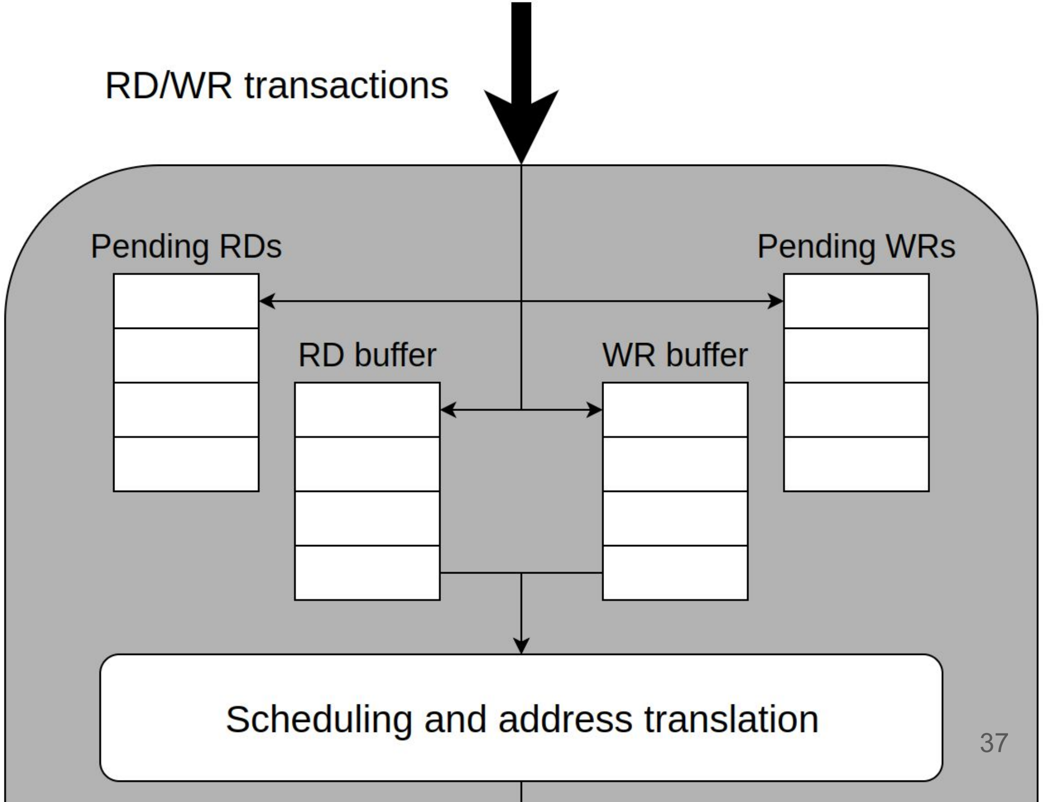

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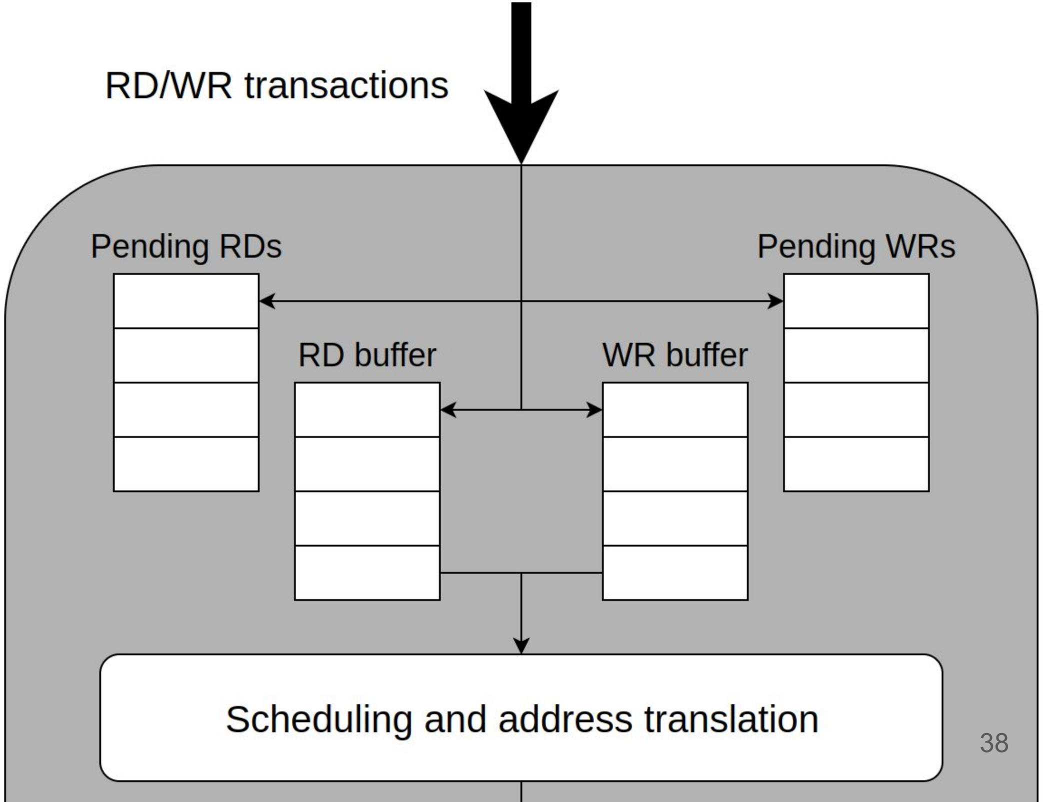

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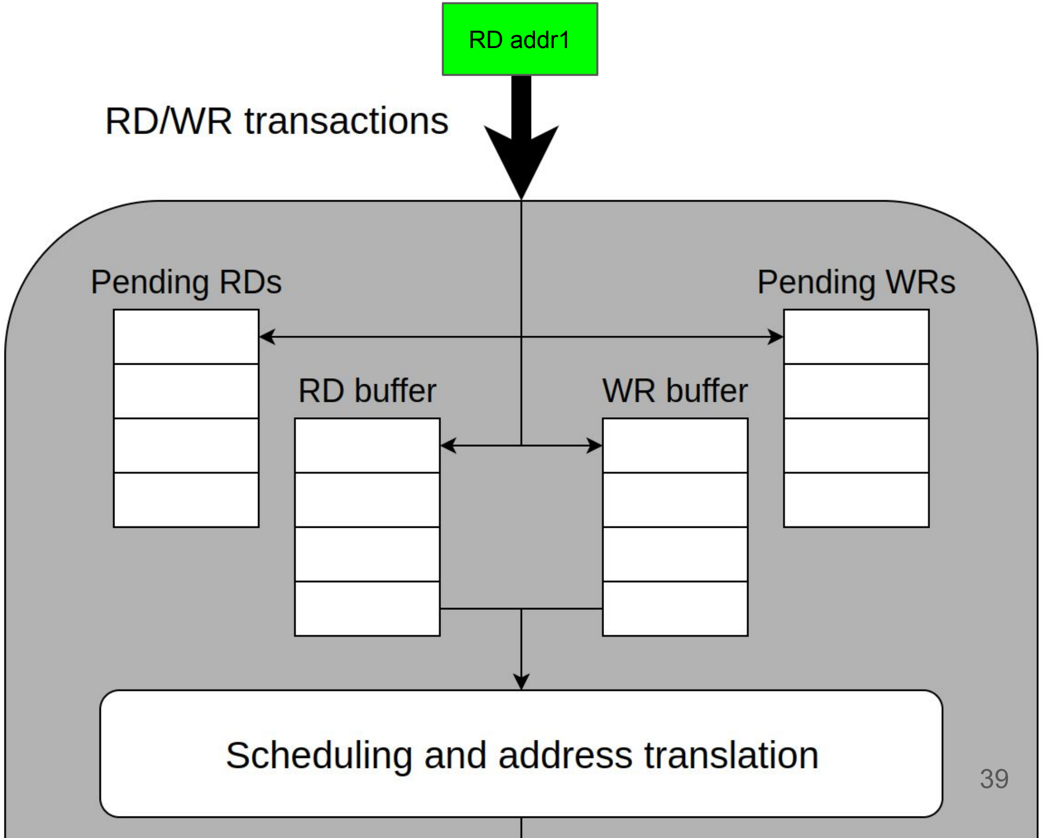

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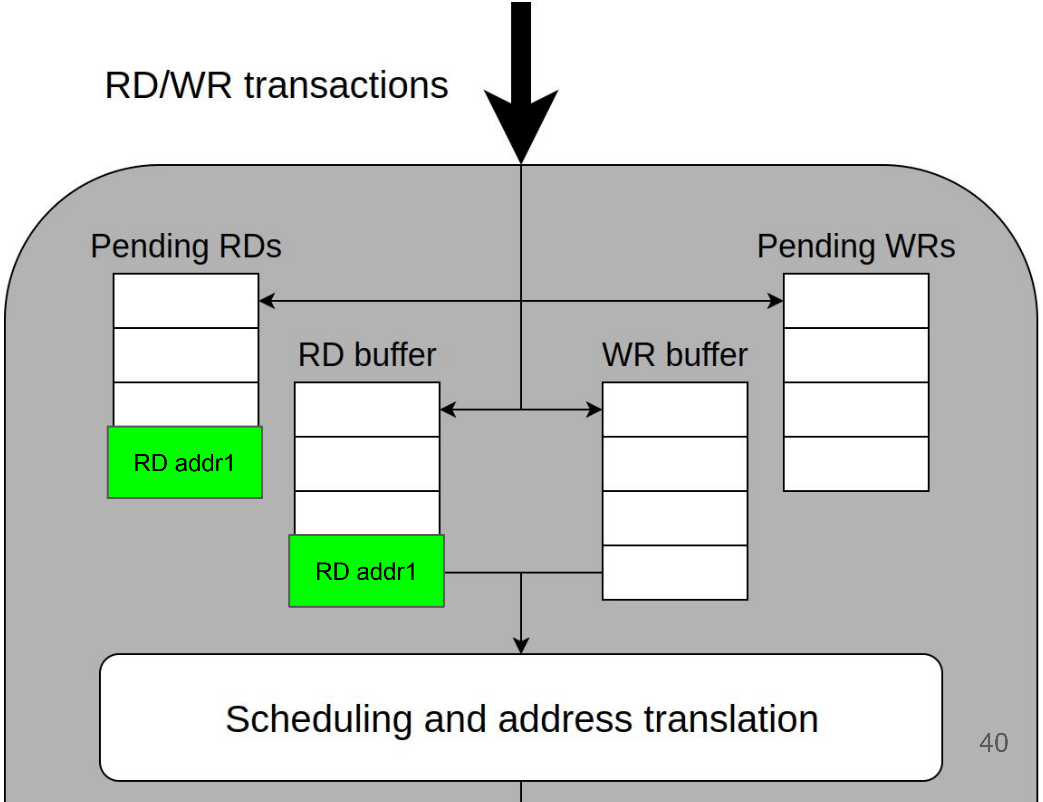

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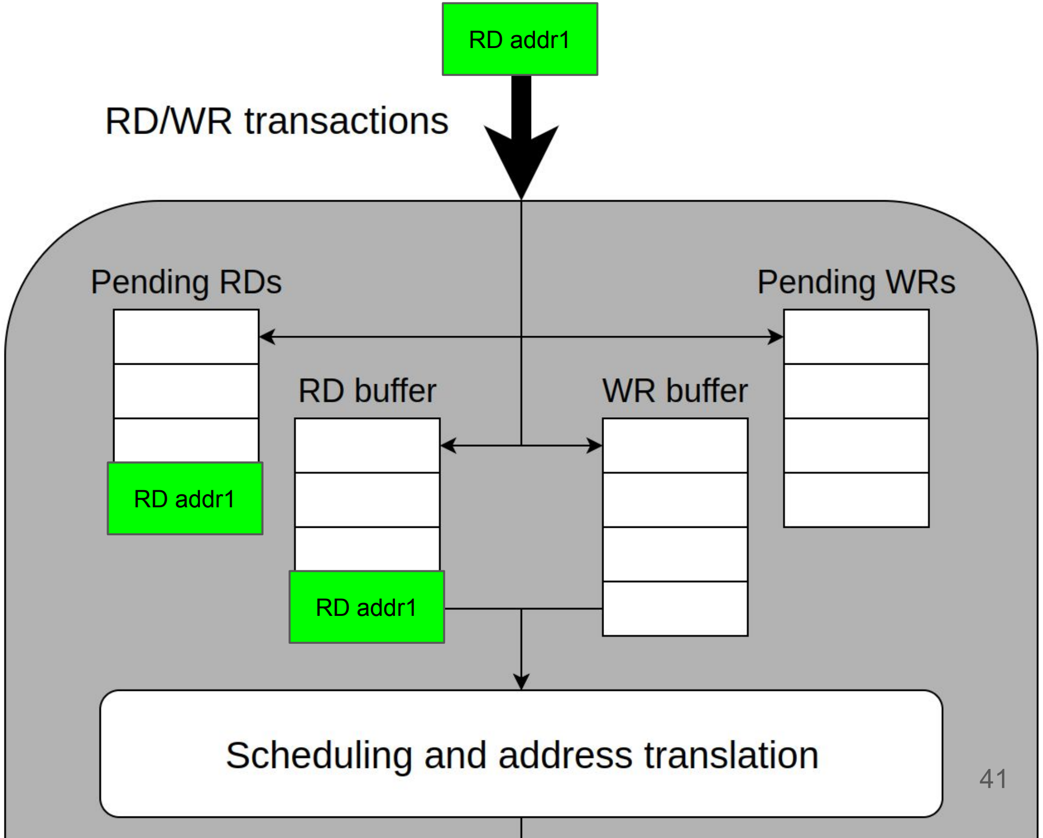

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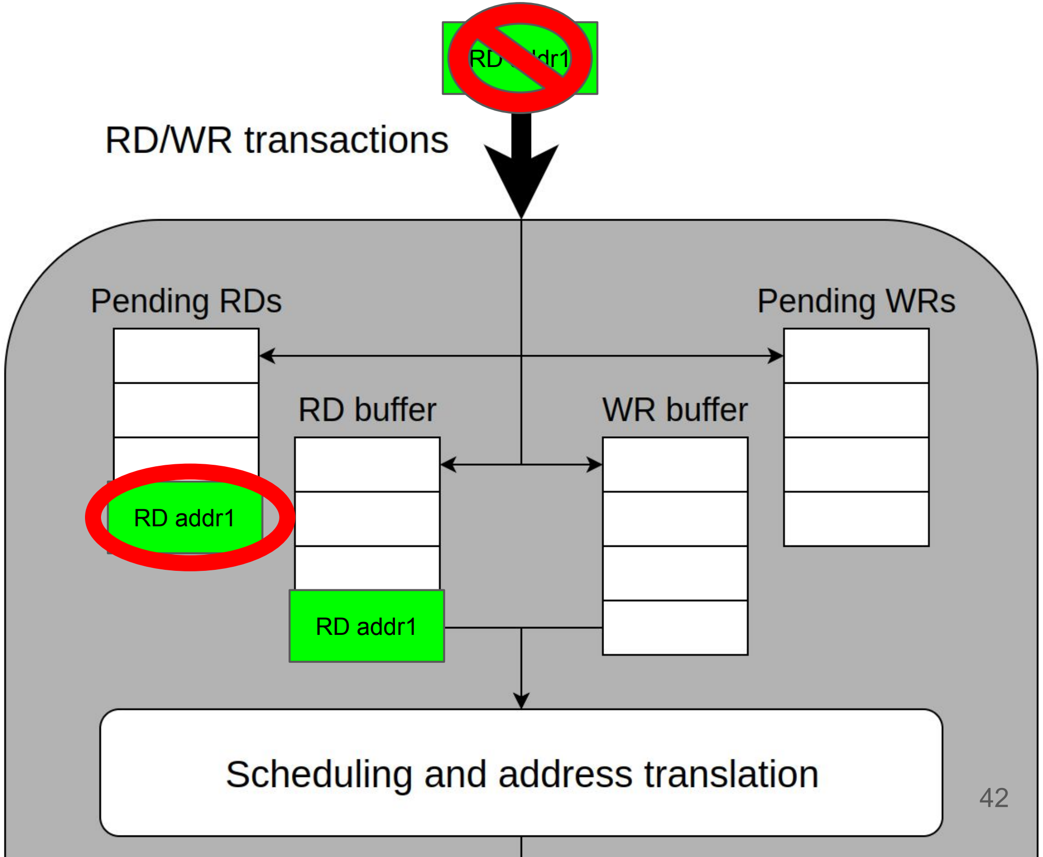

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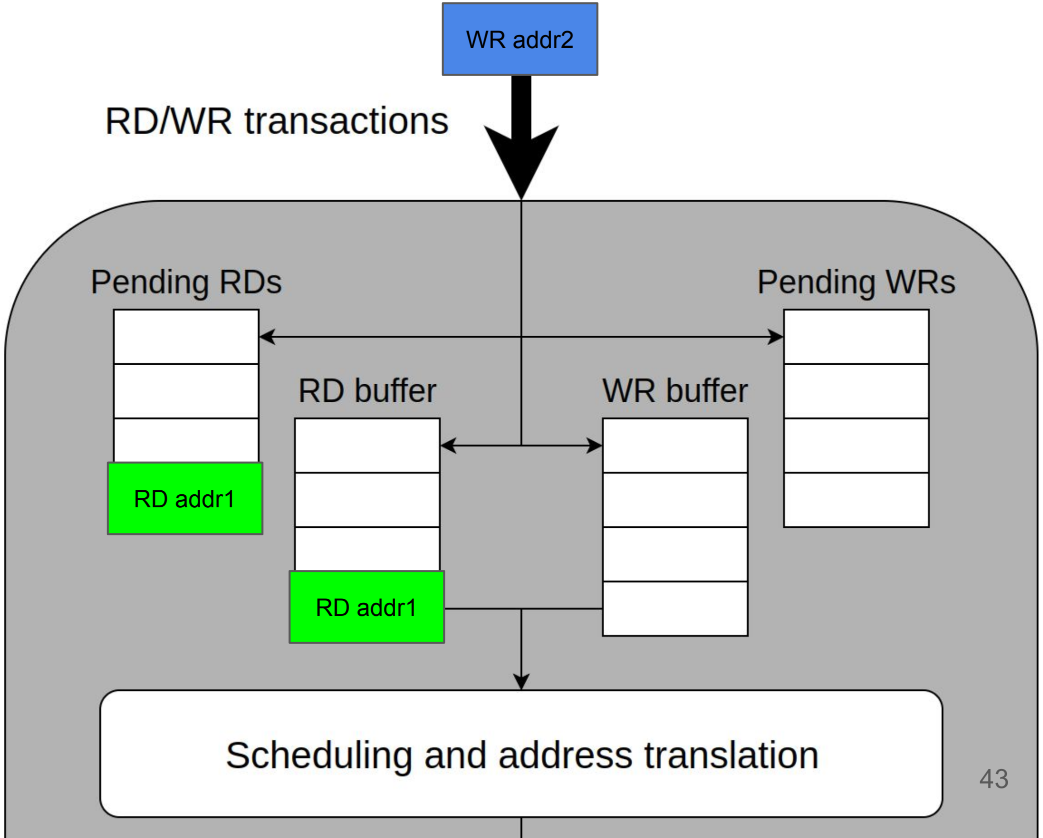

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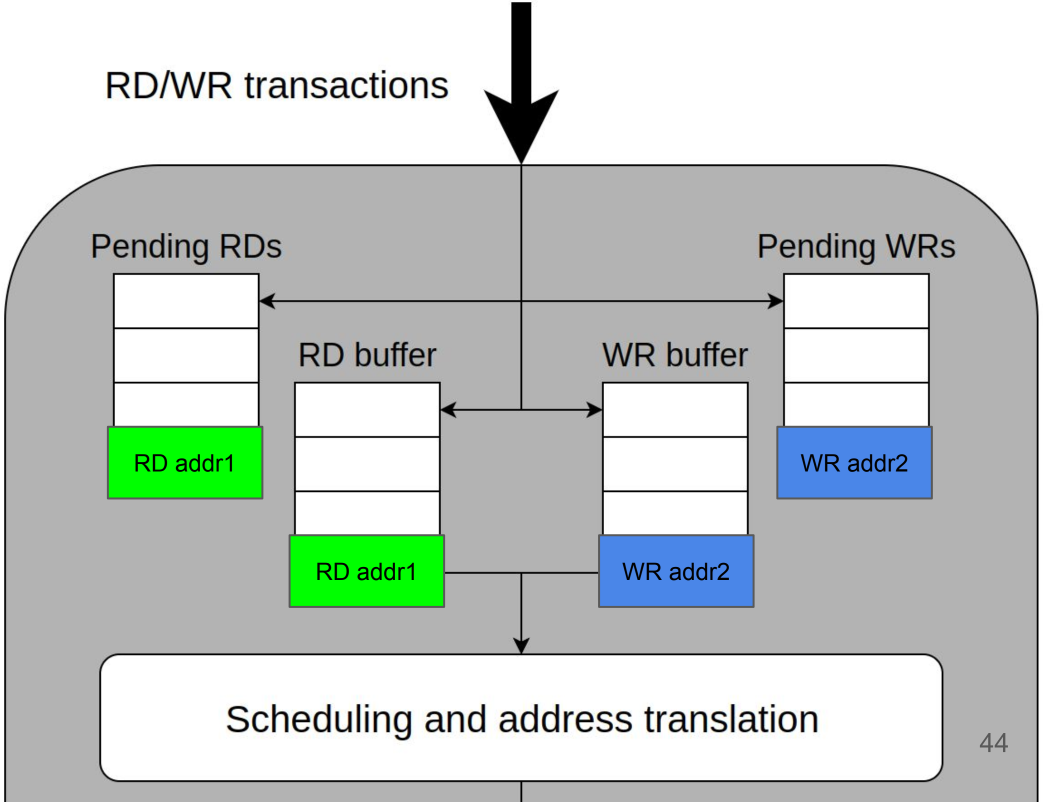

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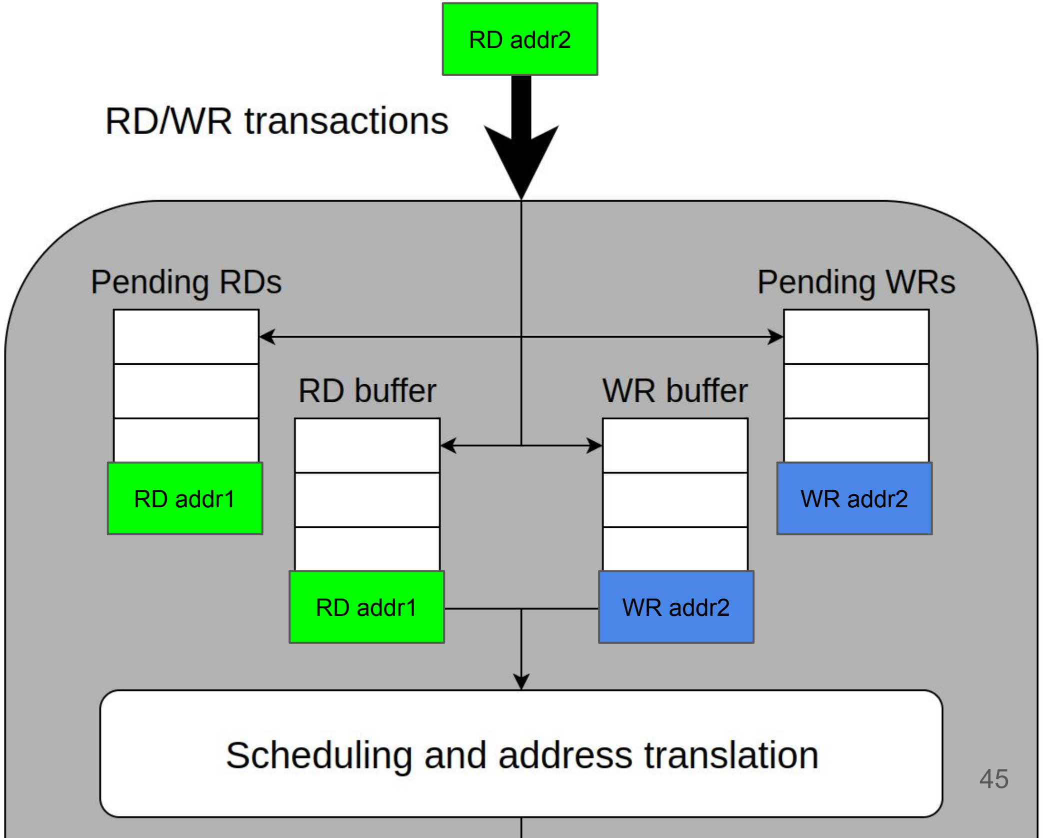

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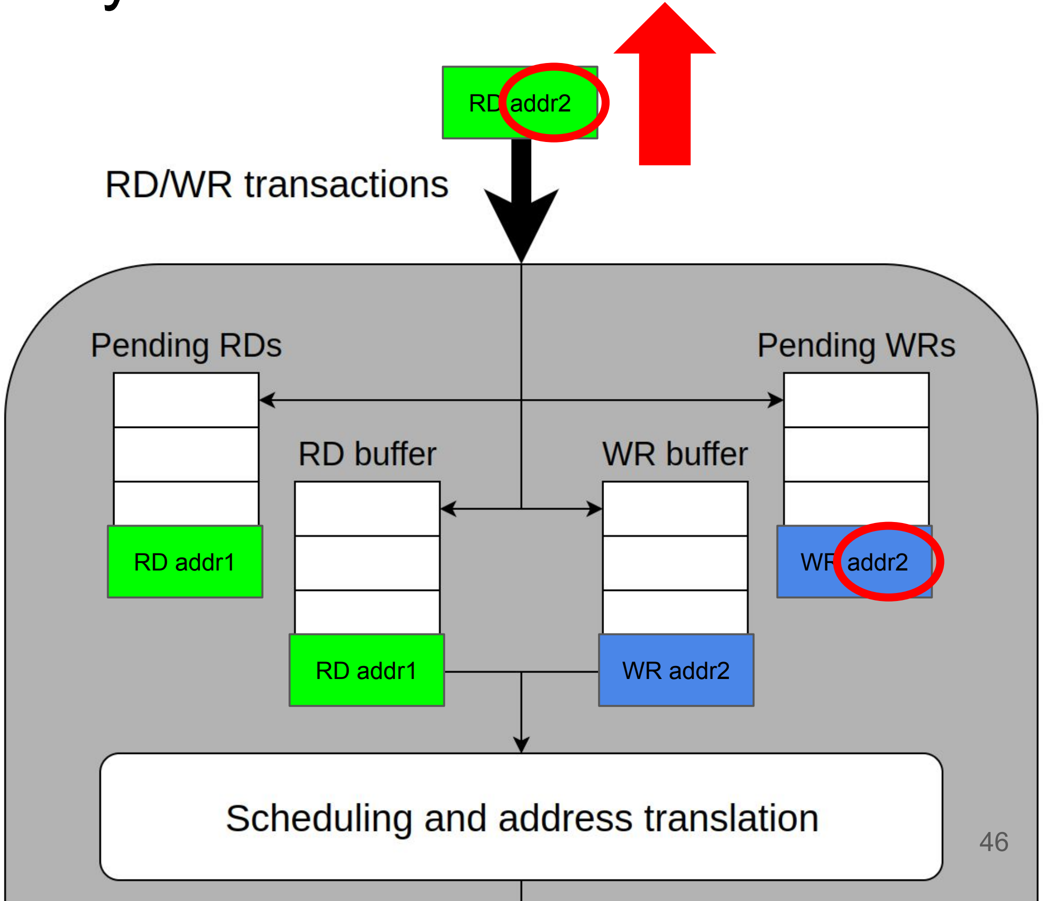

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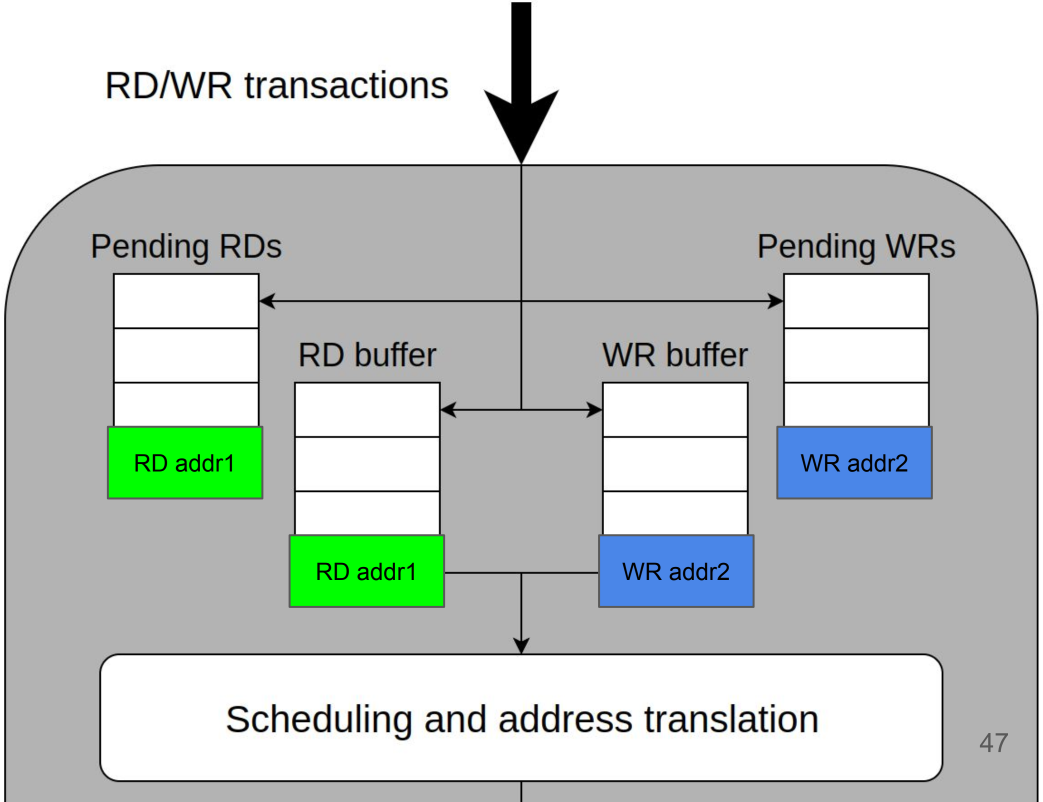

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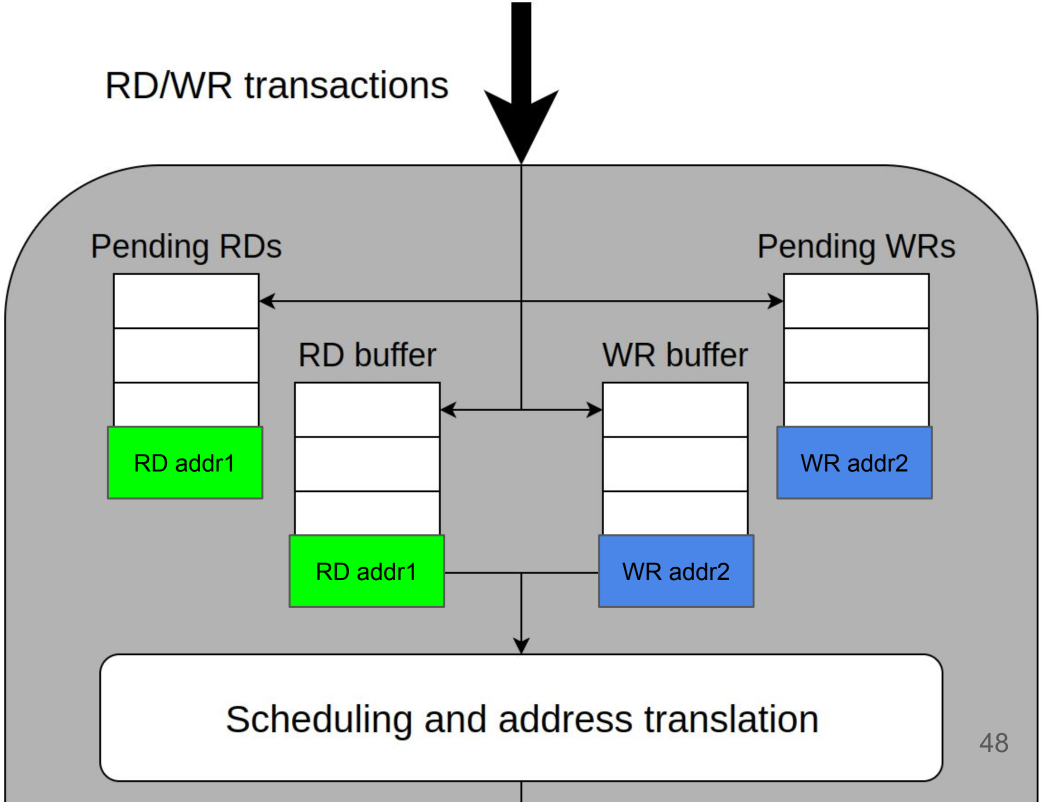

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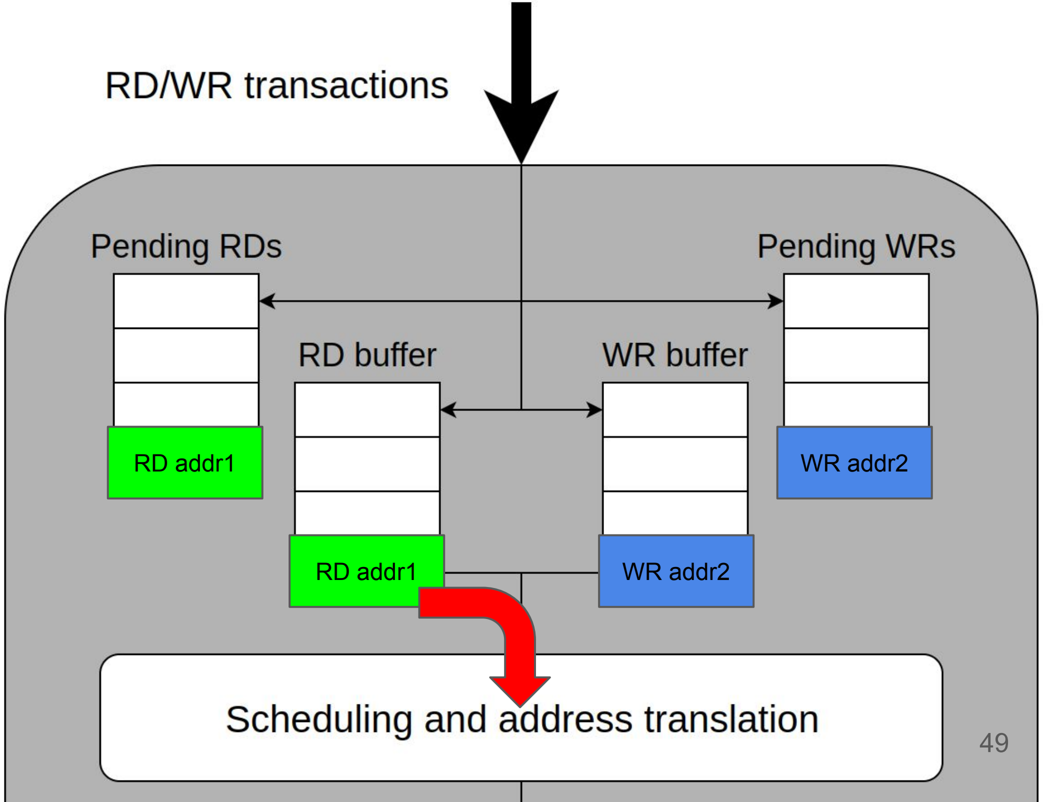

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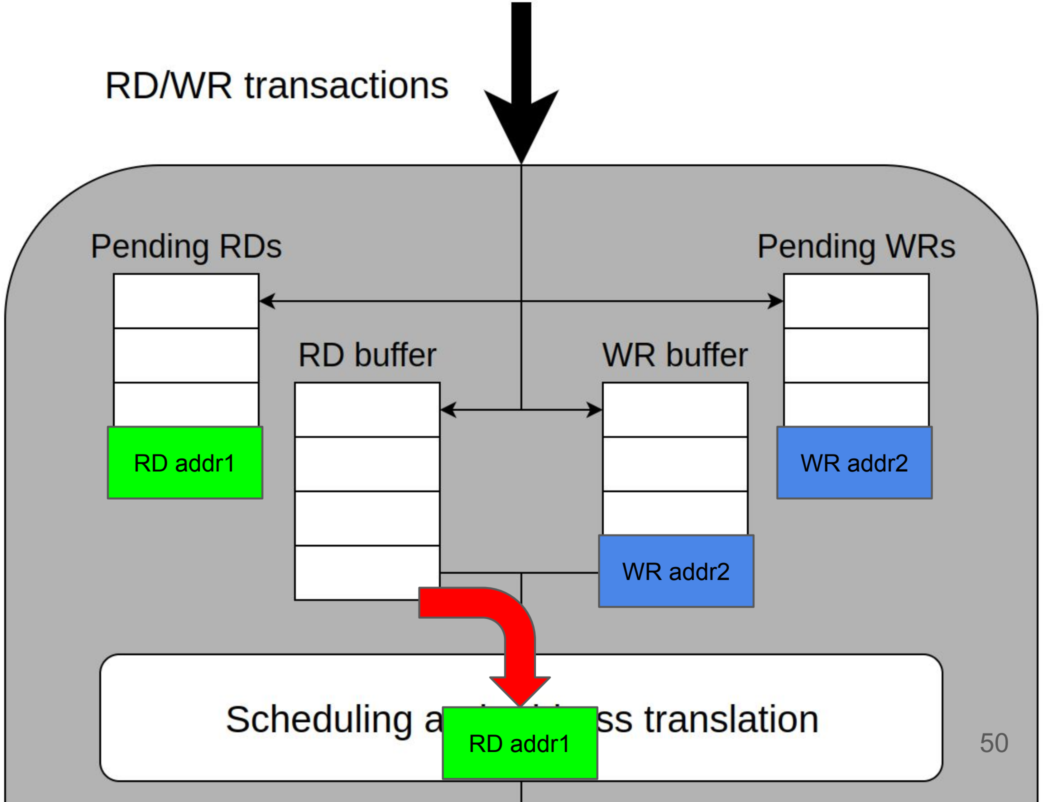

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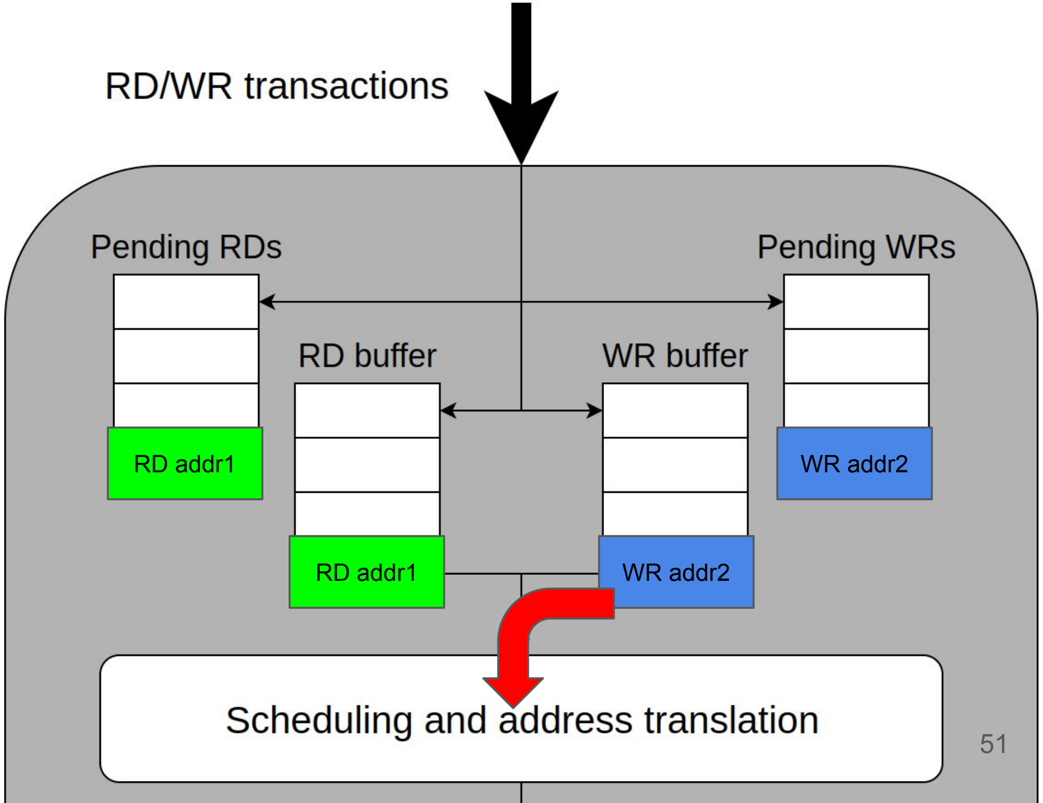

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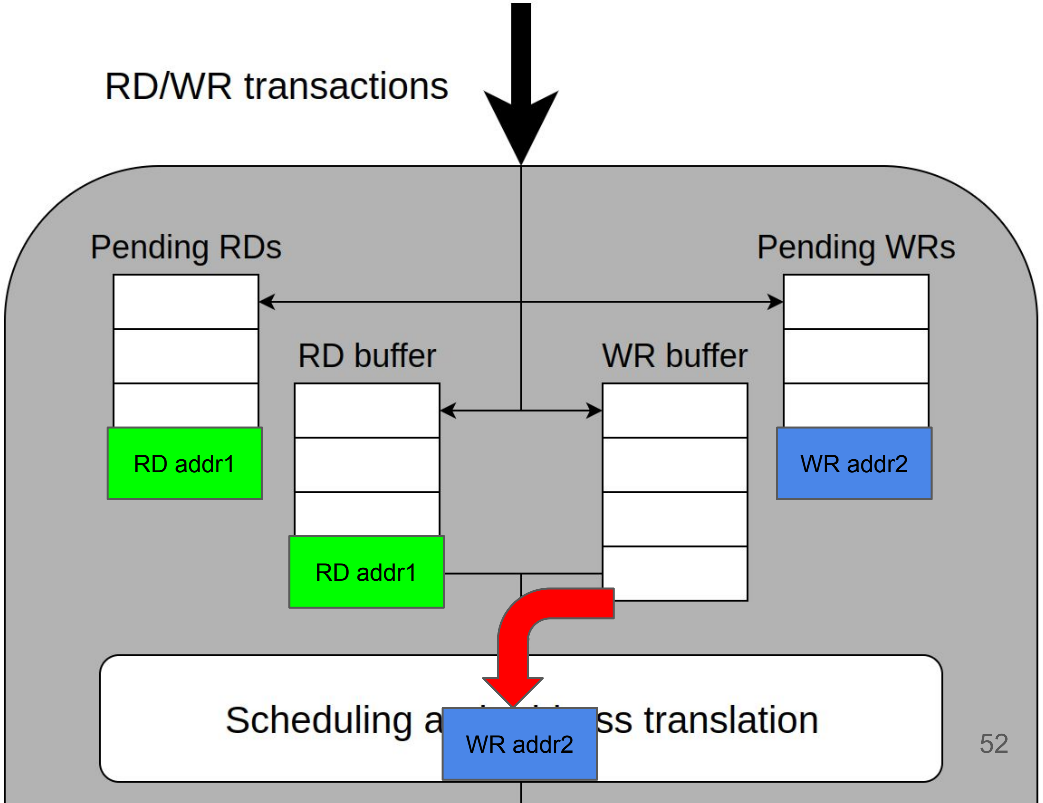

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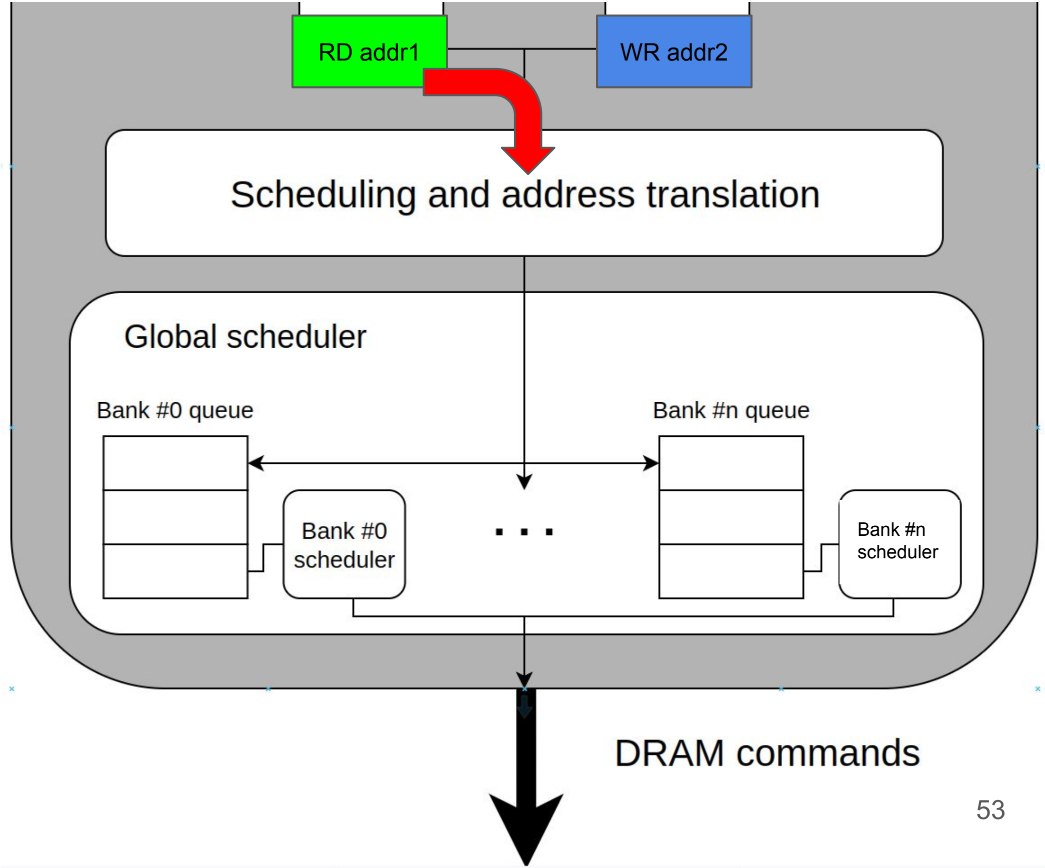

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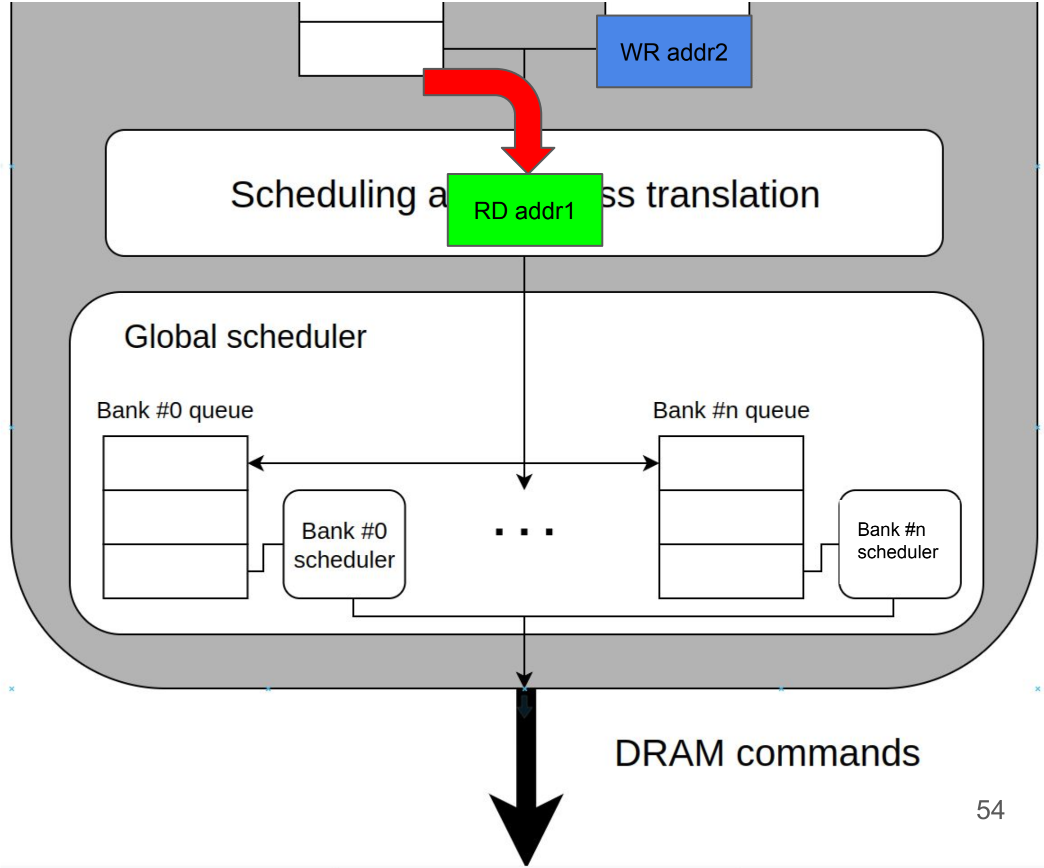

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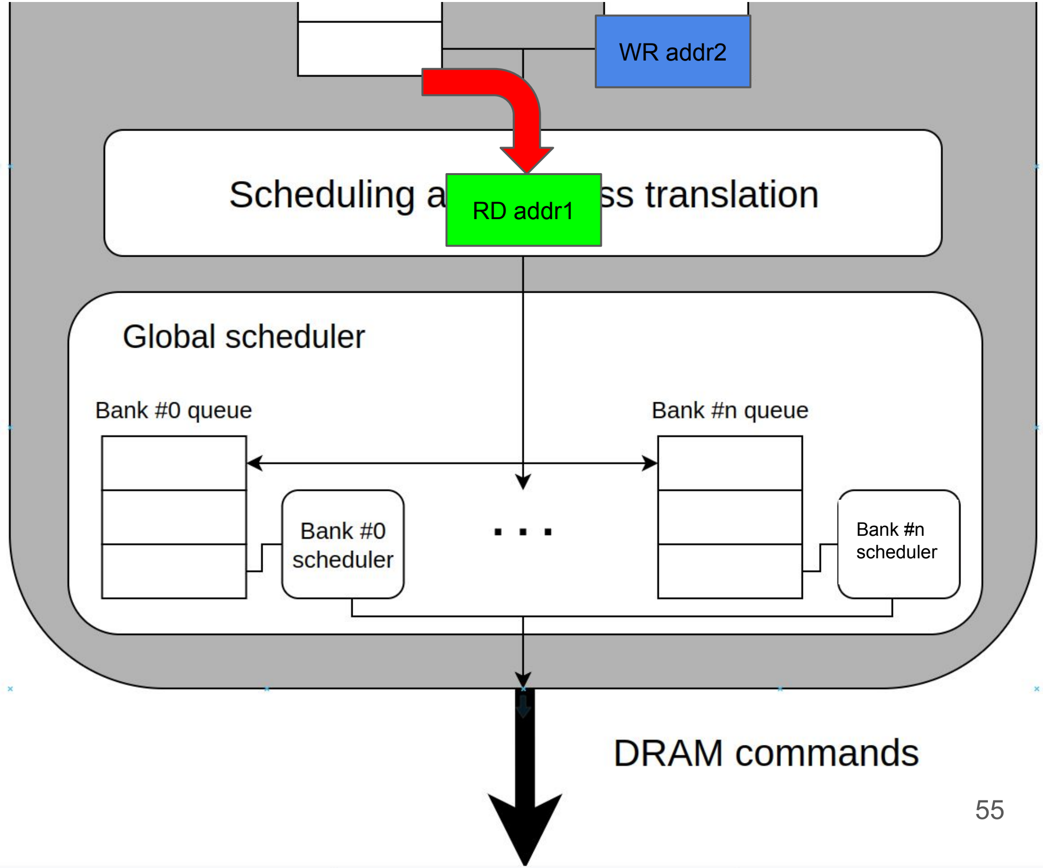

Structure (logical) of a memory controller

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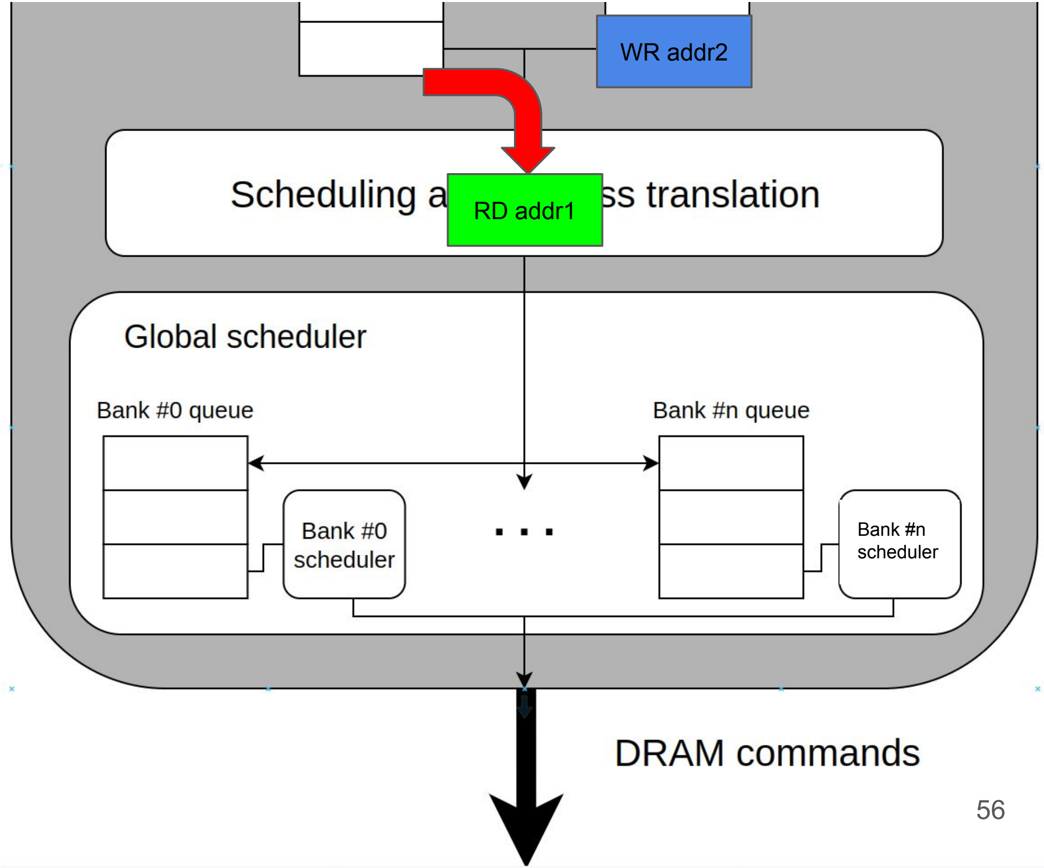

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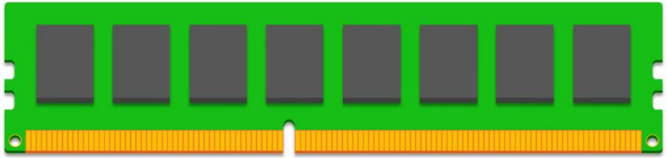

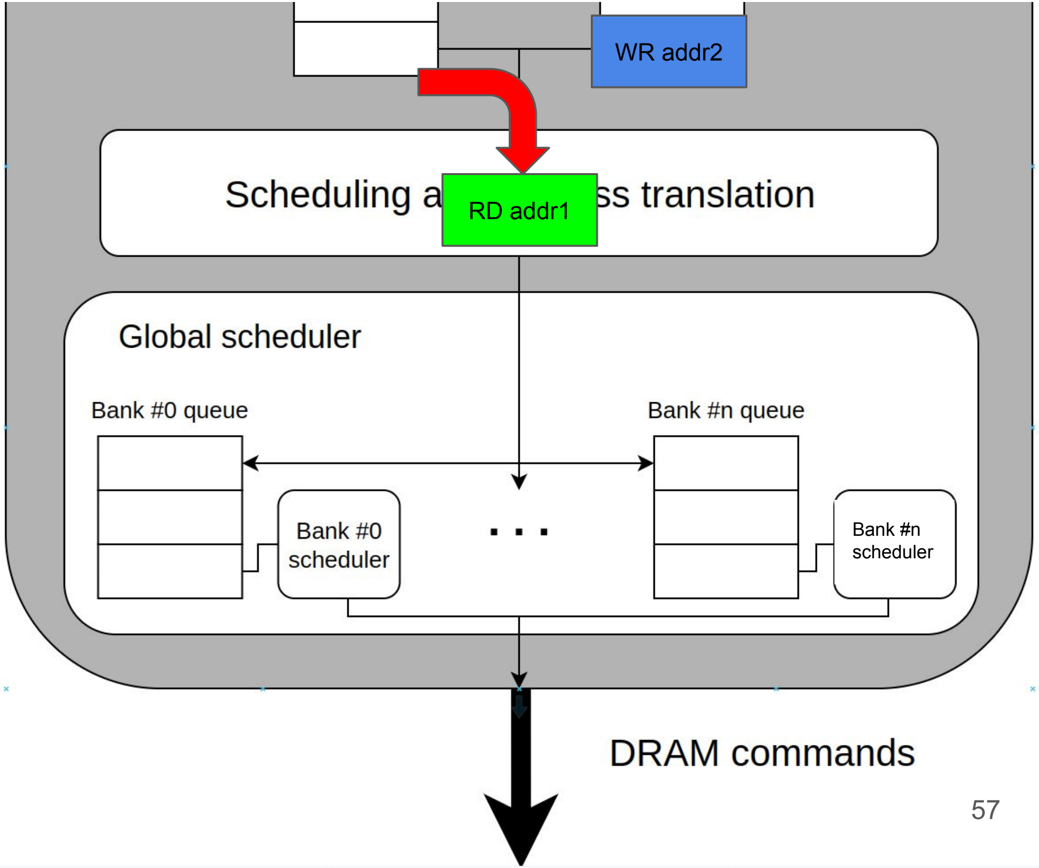

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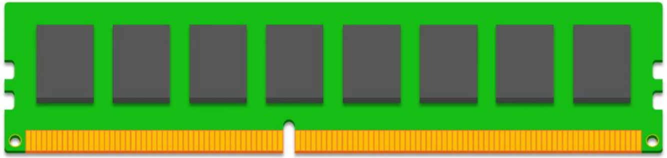

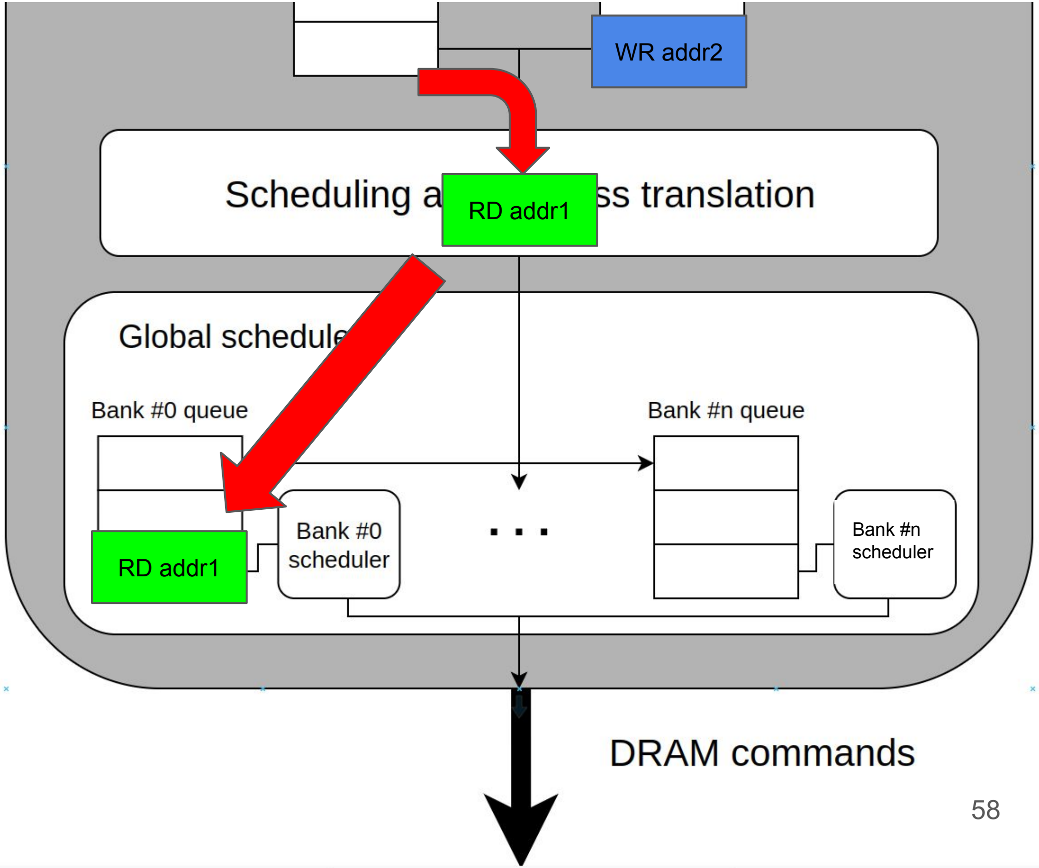

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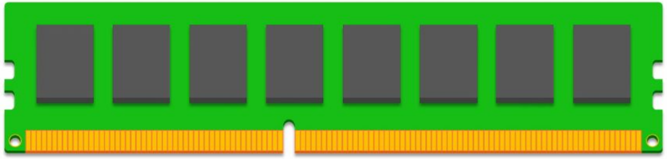

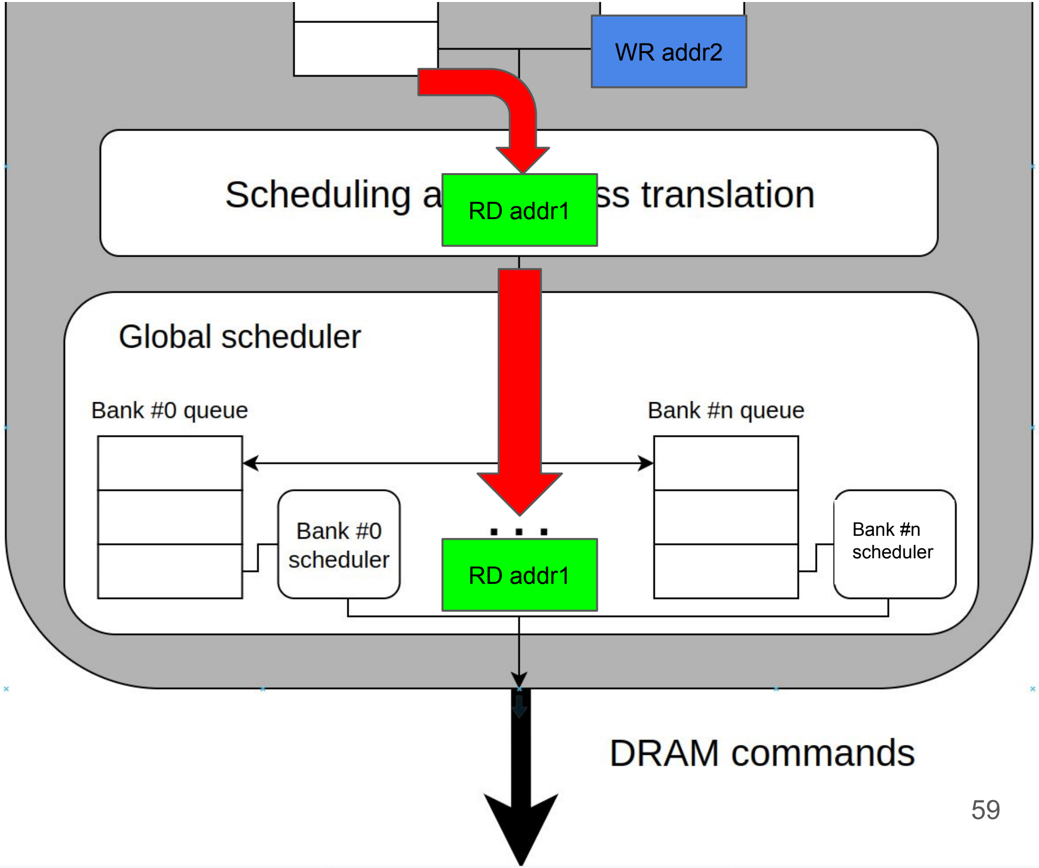

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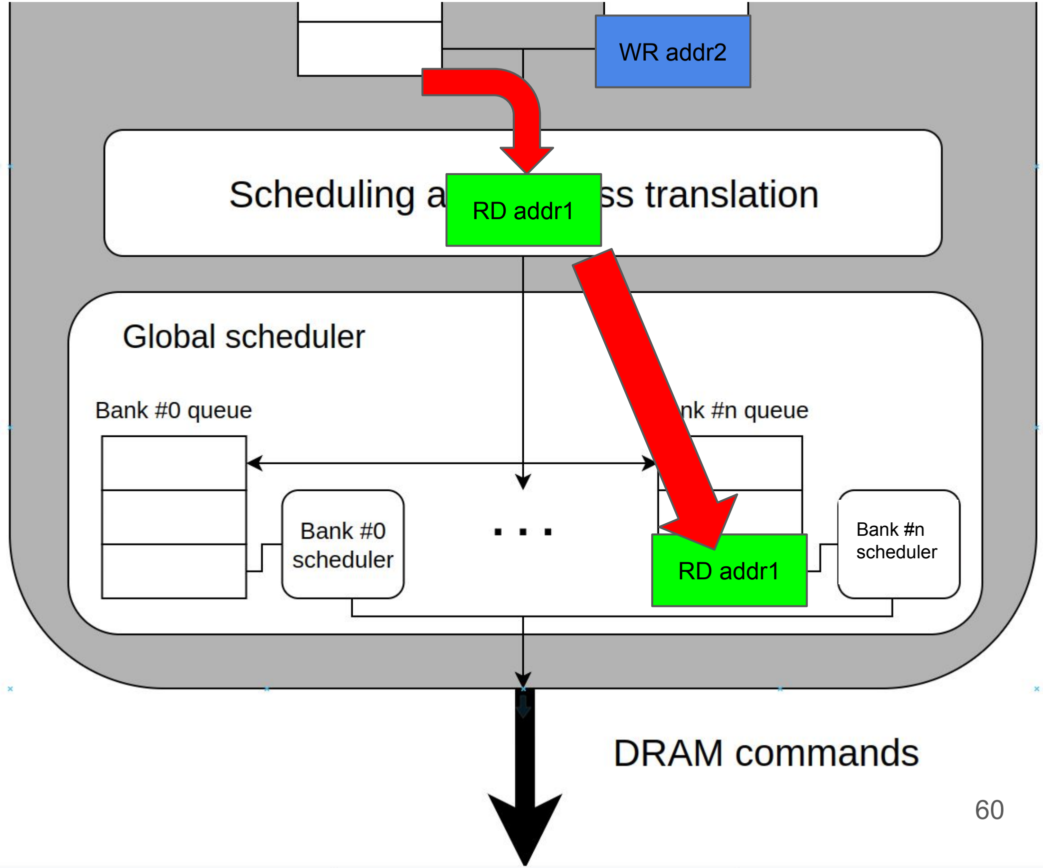
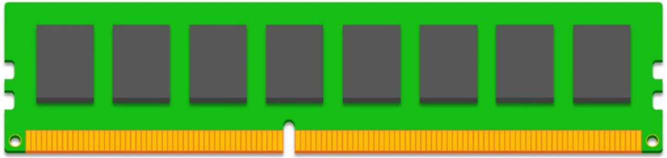
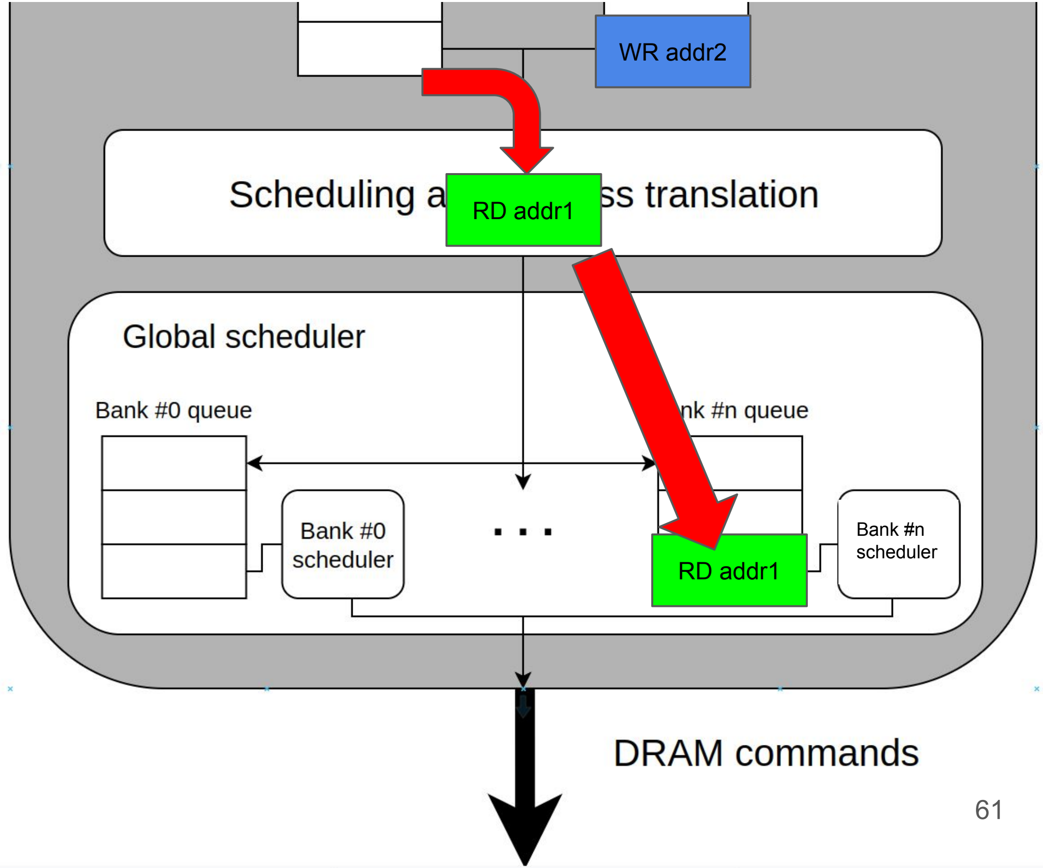




Structure (logical) of a memory controller

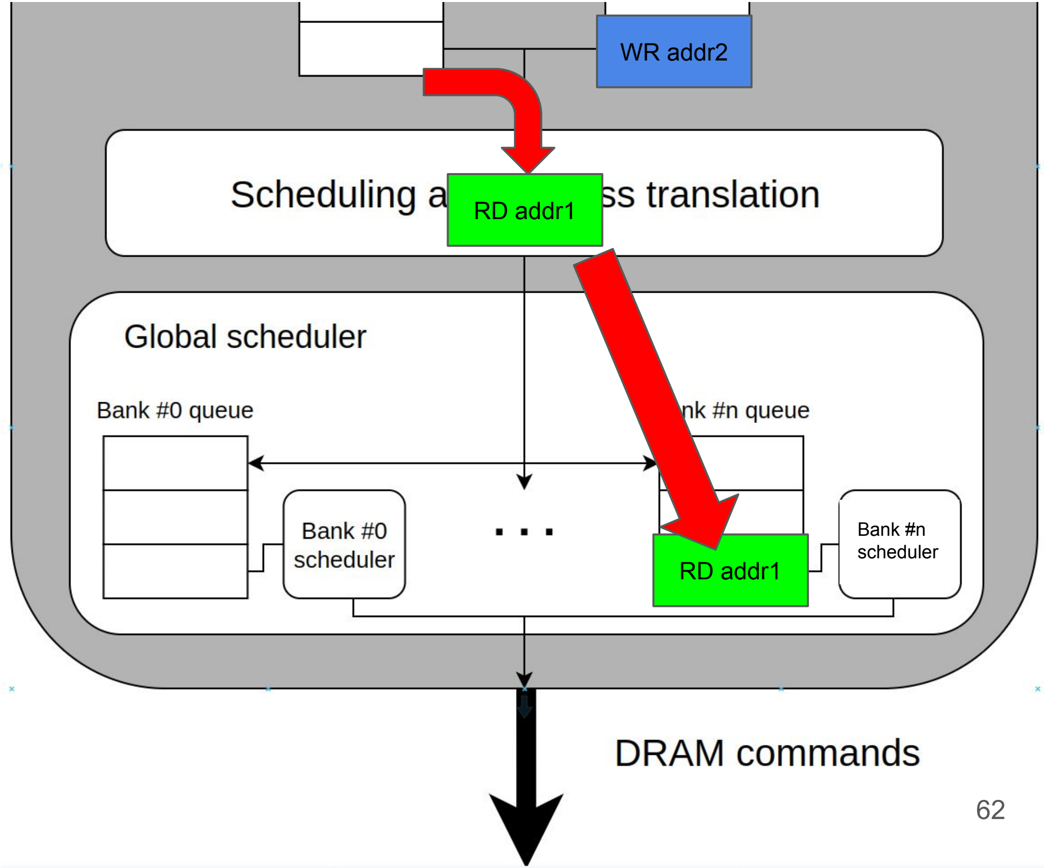
Where are the DRAM commands though??



Structure (logical) of a memory controller

Where are the DRAM commands though??

- This is where the bank schedulers come in…



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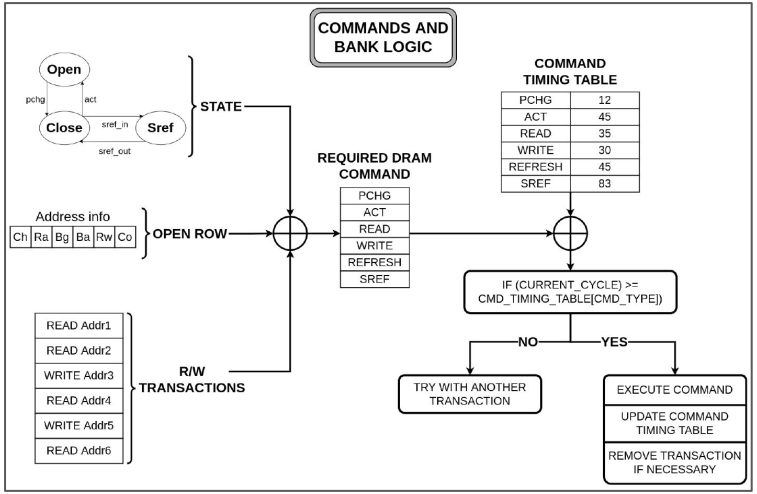
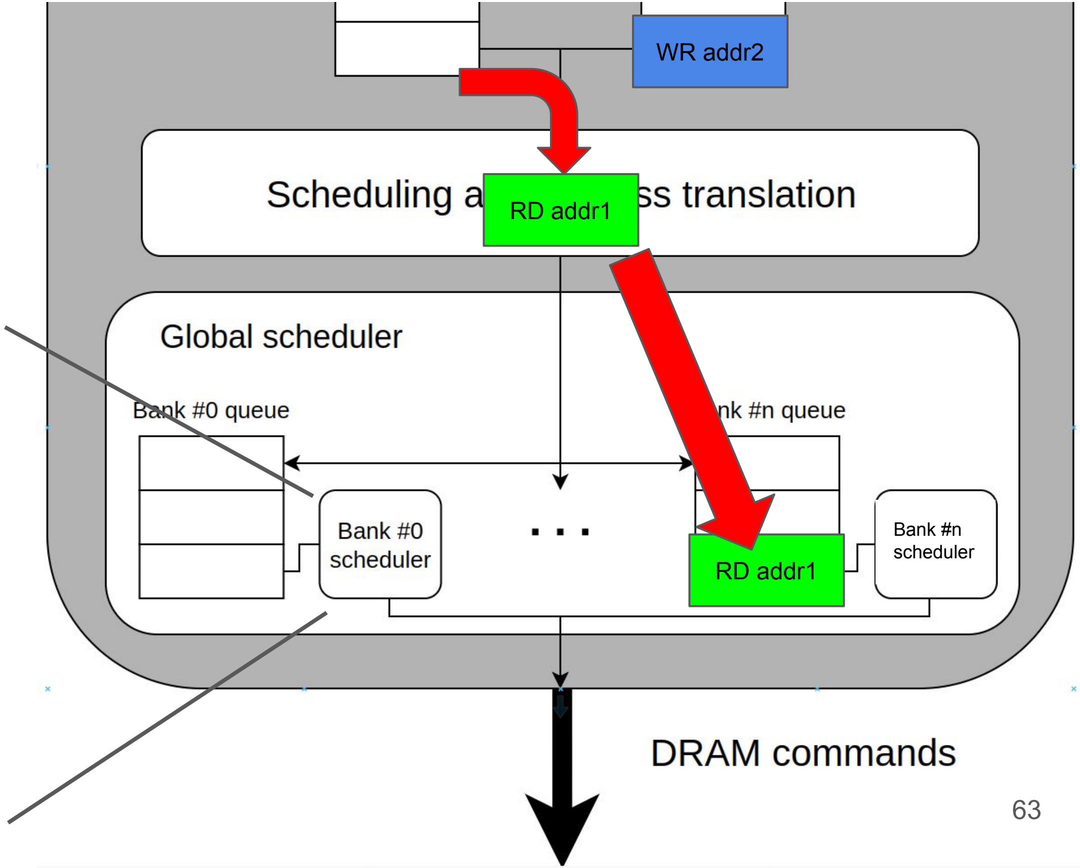


PCHG	12
ACT	45
READ	35
WRITE	30
REFRESH	45
SREF	83

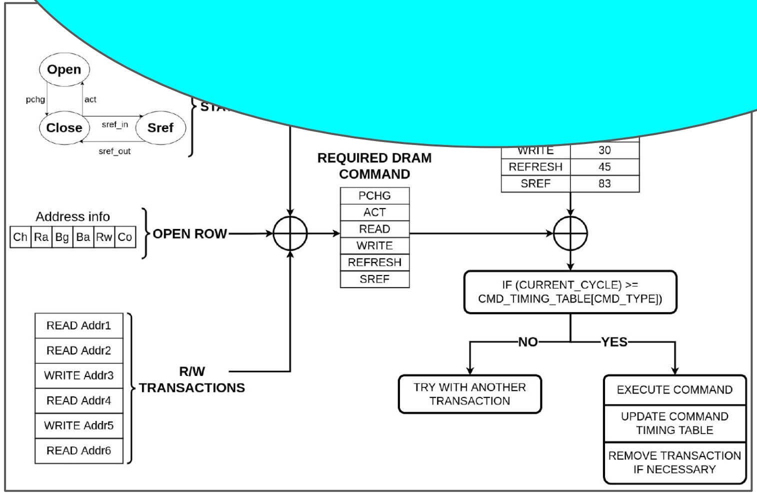


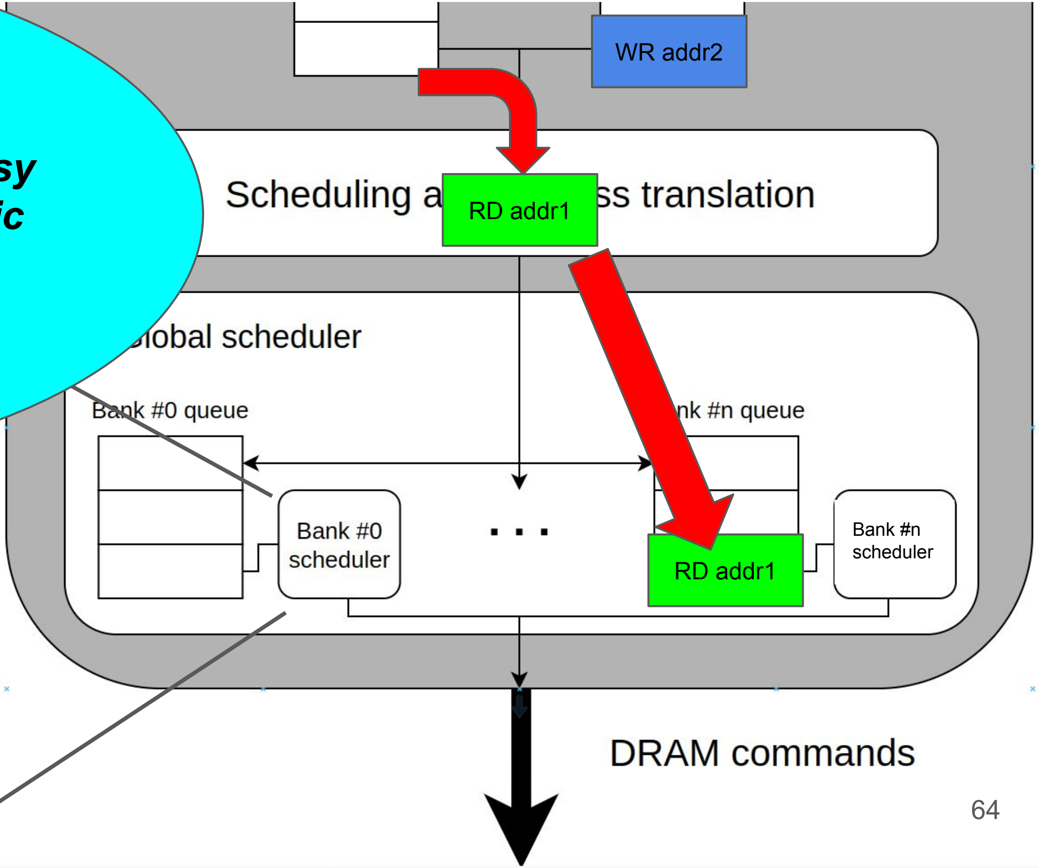
Structure (logical) of a memory controller

Whe

●

We won't be looking into the messy details of the bank scheduler logic today…



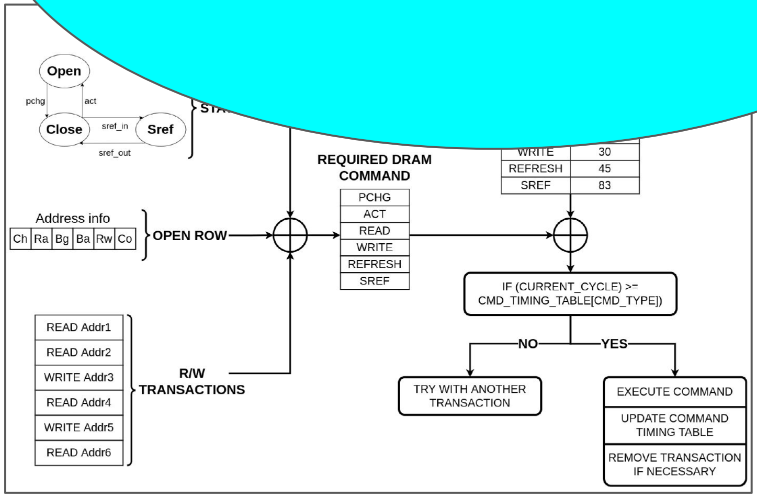


Structure (logical) of a memory controller

Instead, we'll just consider the following relevant points:

Whe

-



WRITE	30
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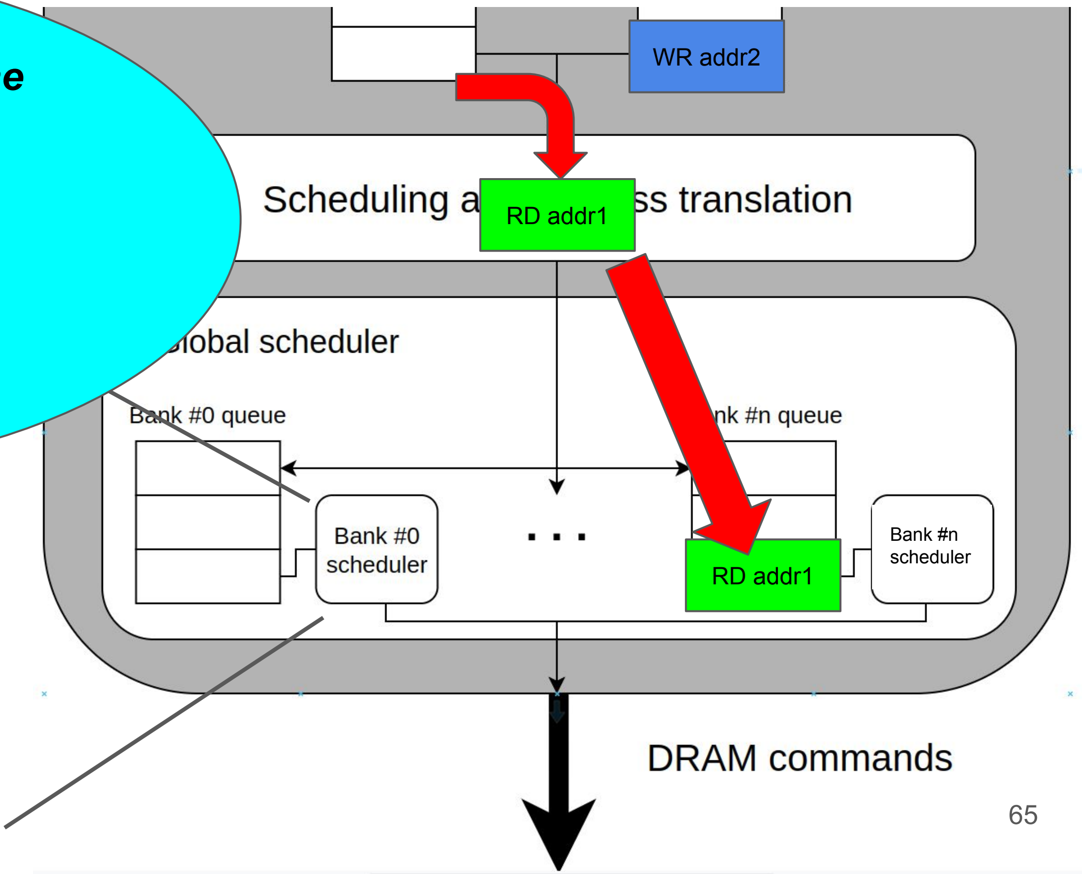

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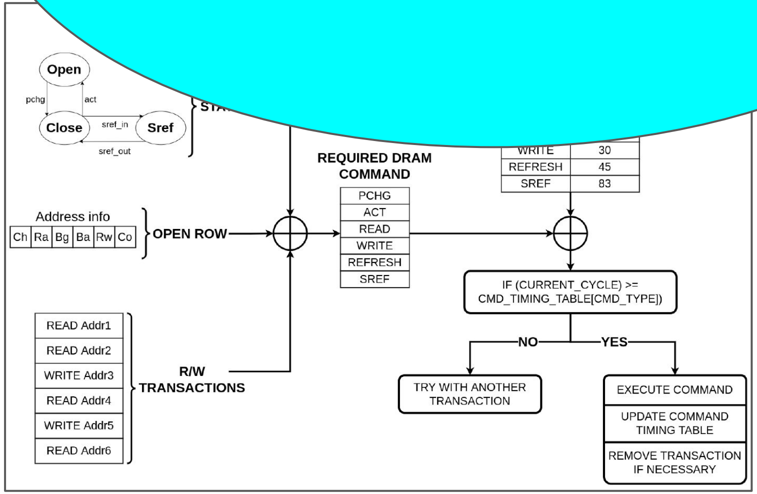

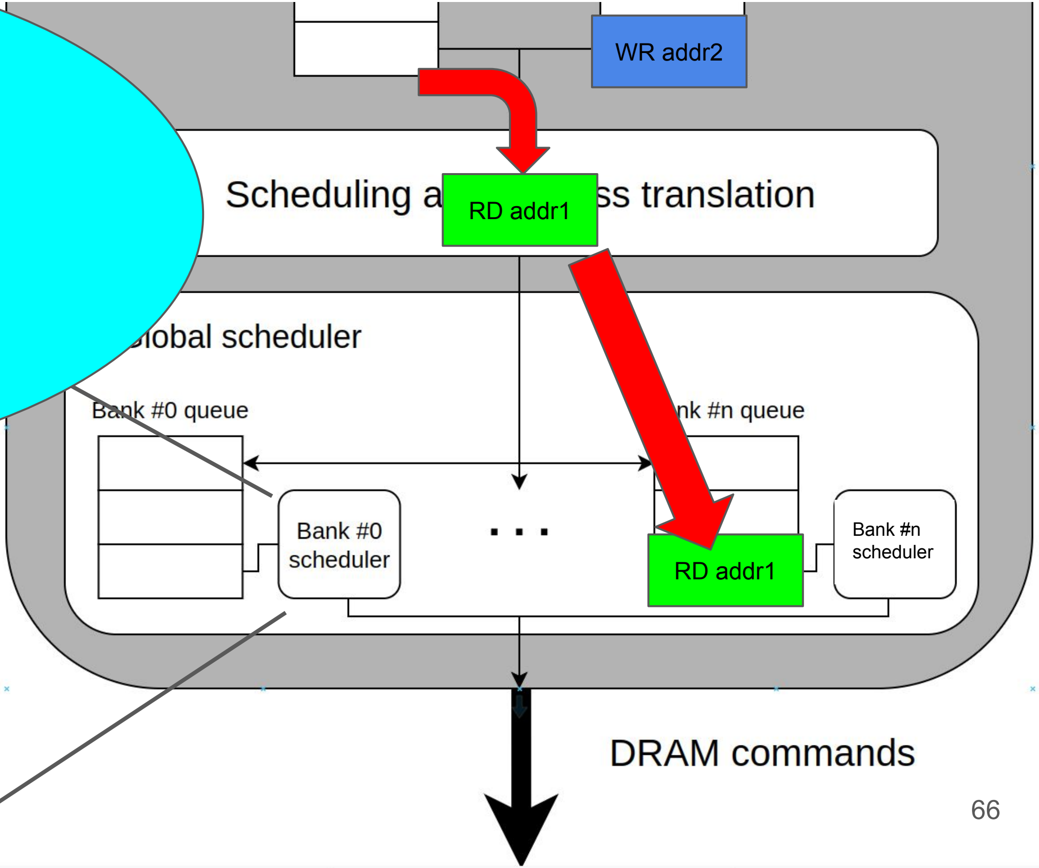

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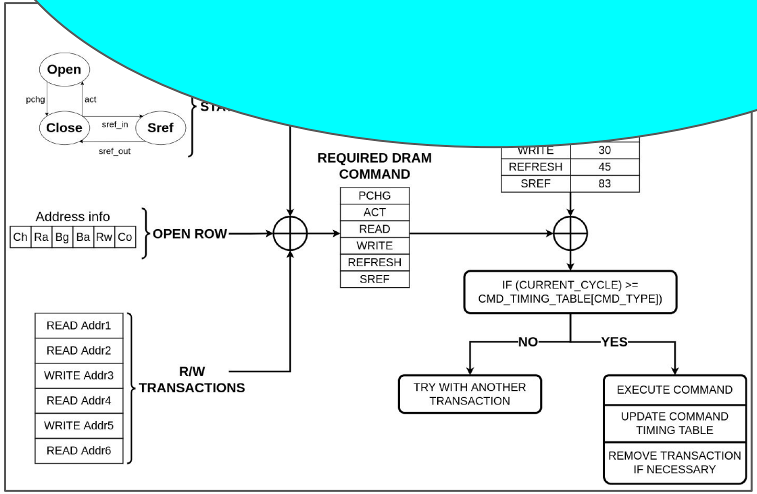

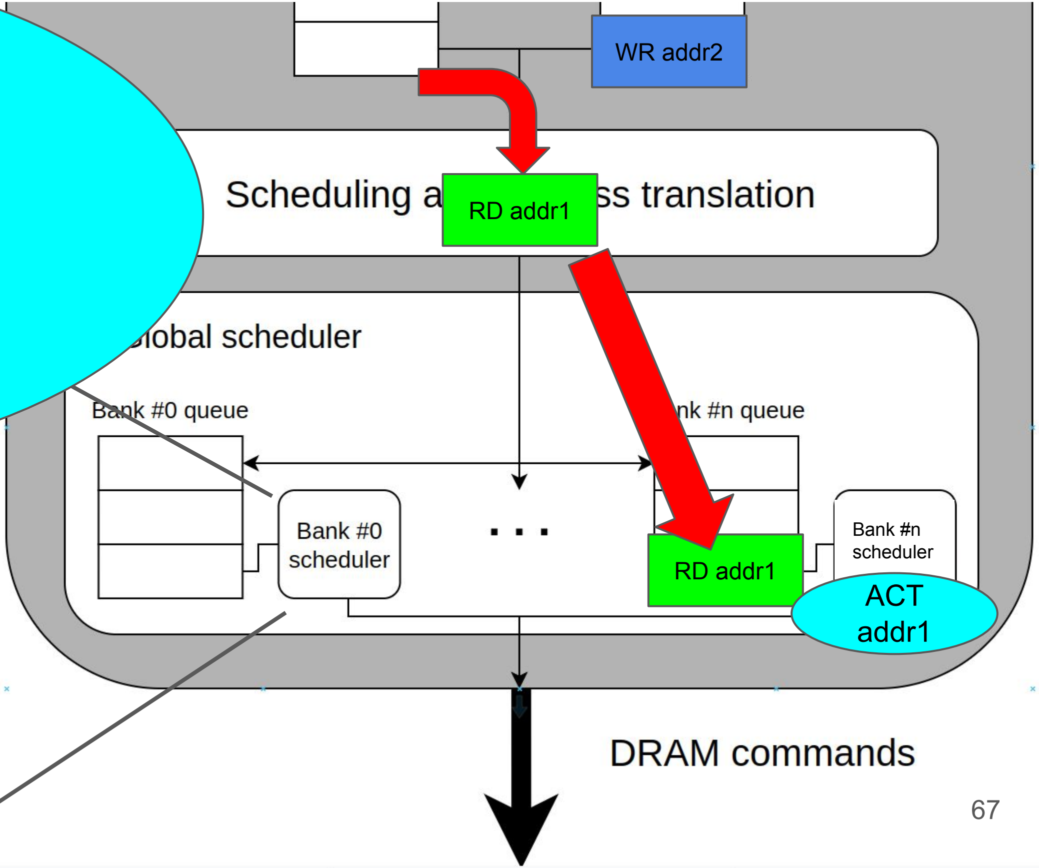

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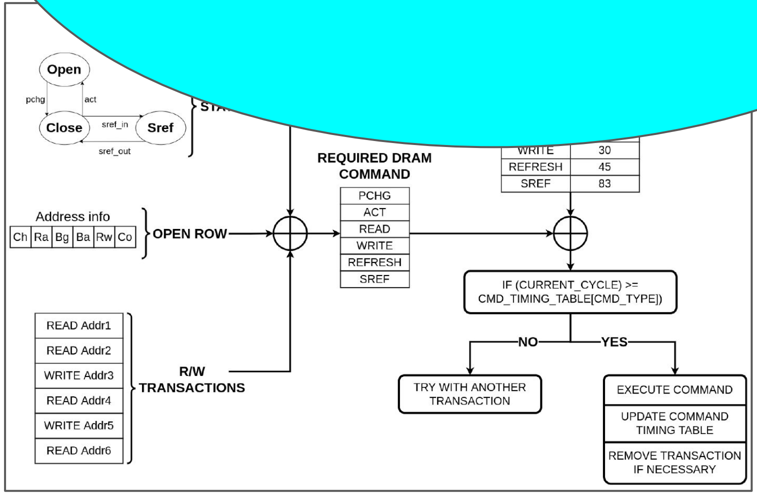

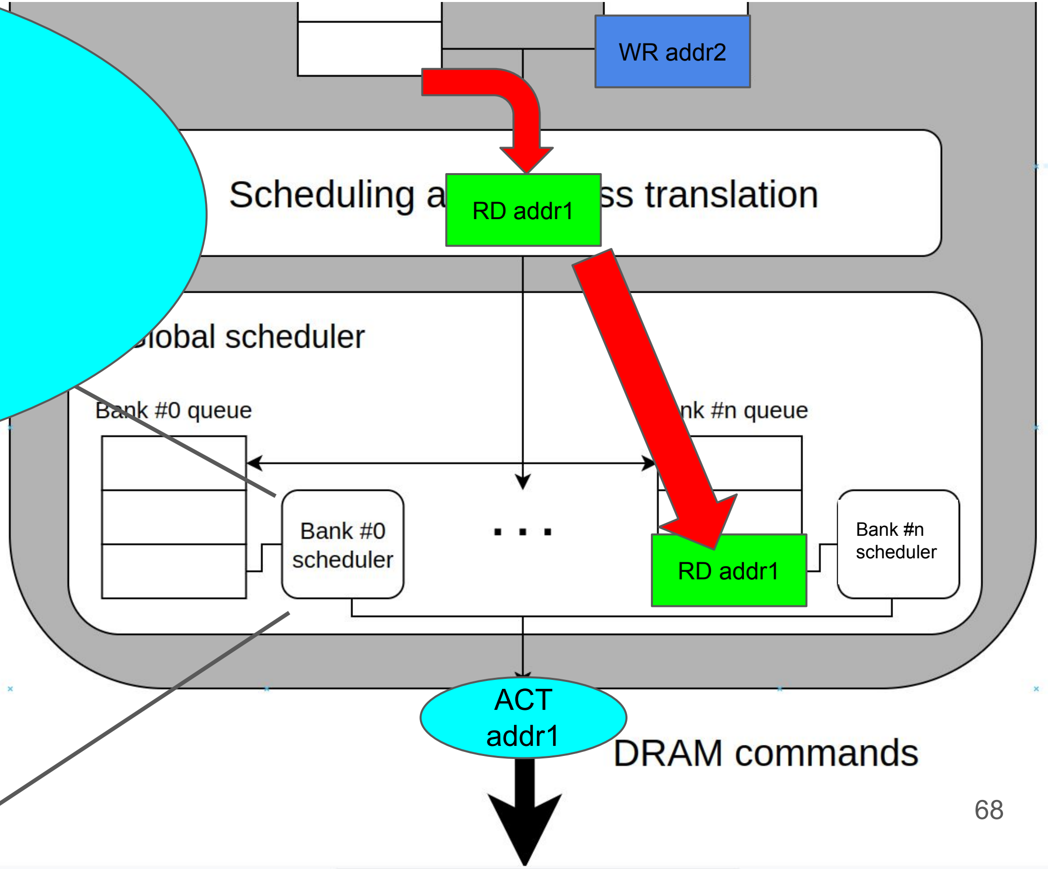

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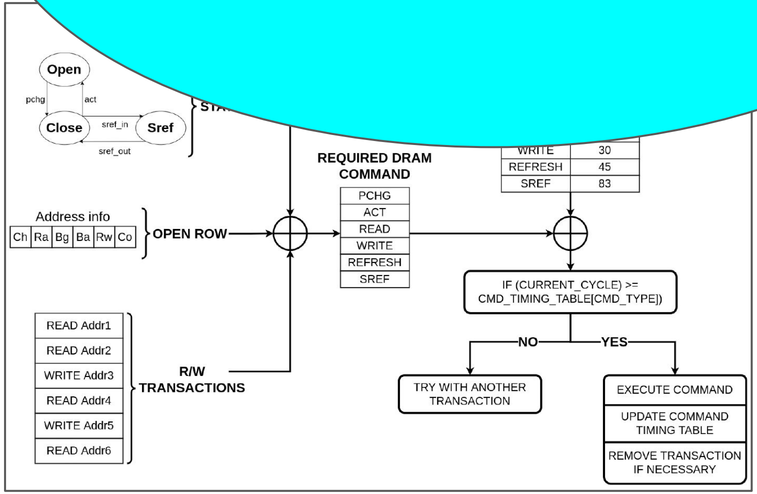

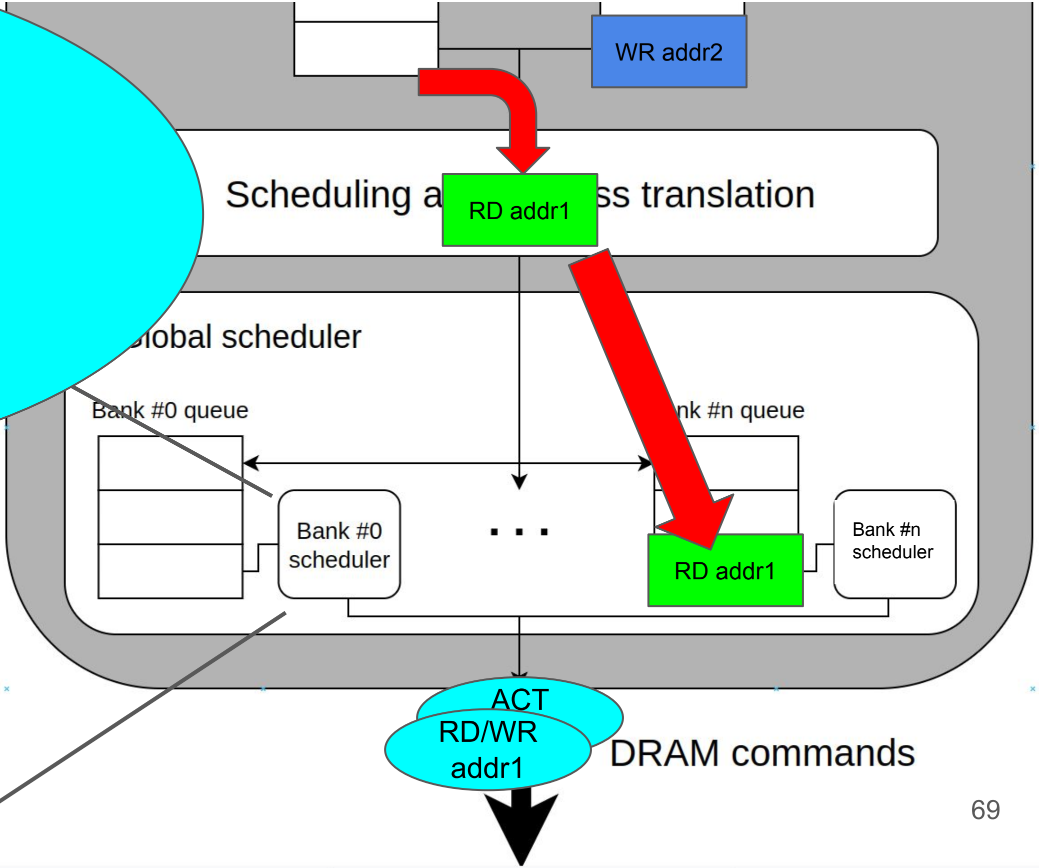

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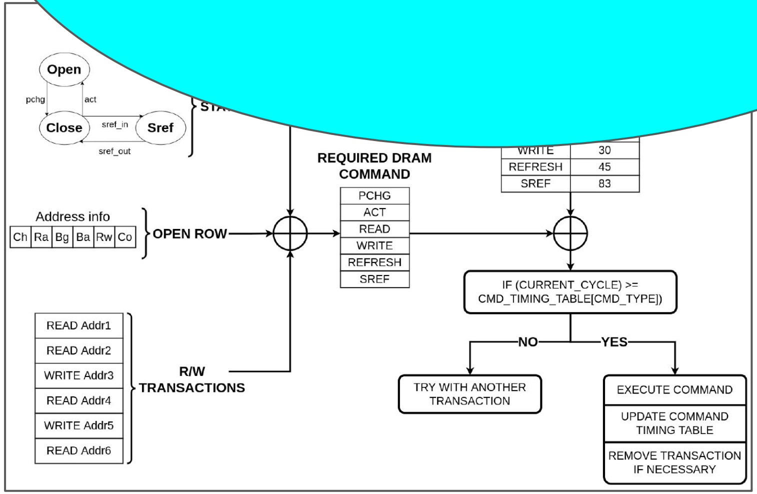

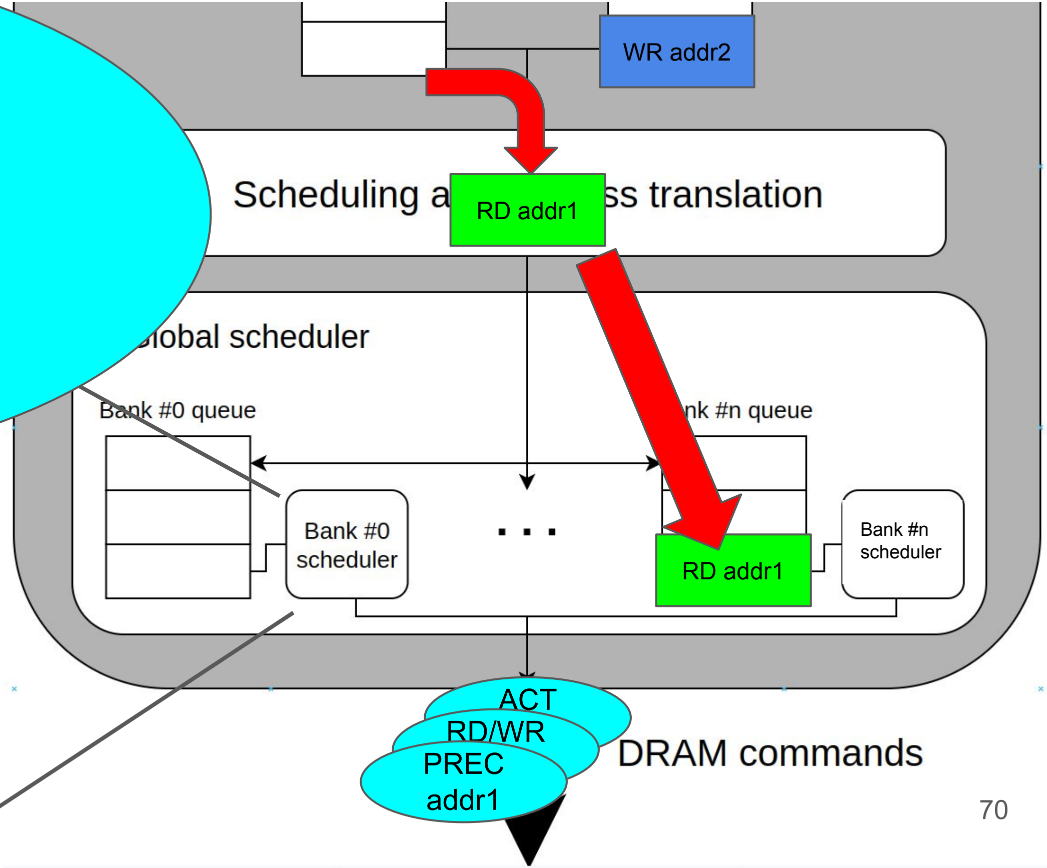

Structure (logical) of a memory controller

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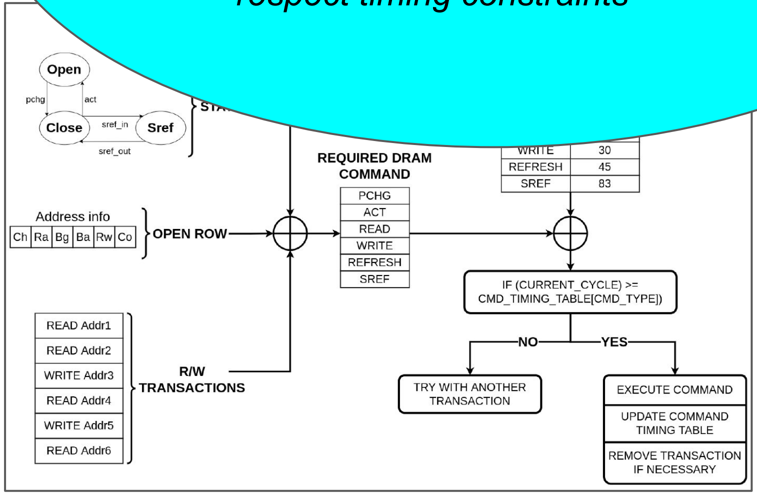
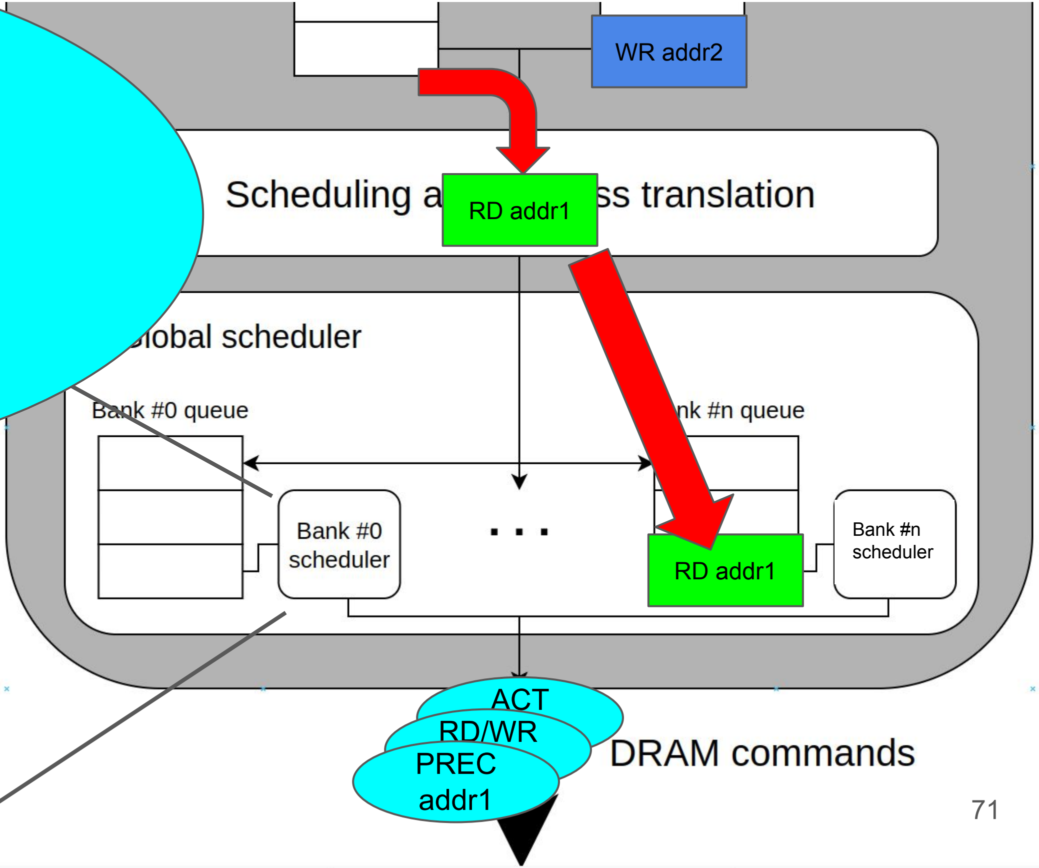
Instead, we'll just consider the following relevant points:

1. *Scheduler transforms requests into DRAM commands*
2. *DRAM command generation must respect timing constraints*





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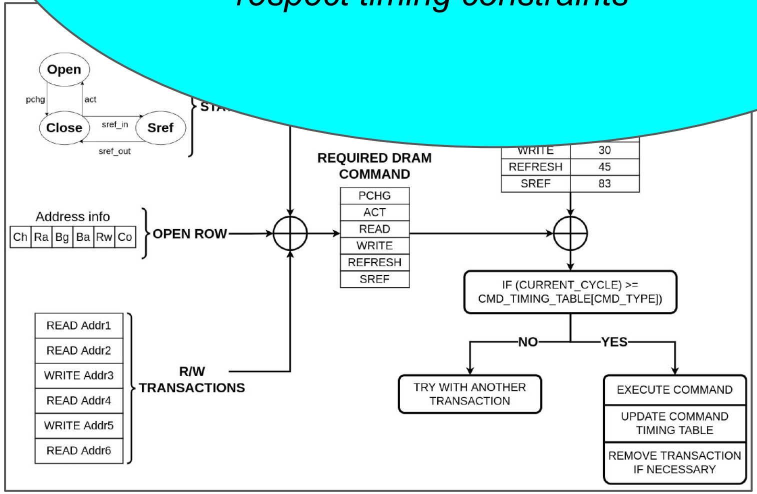

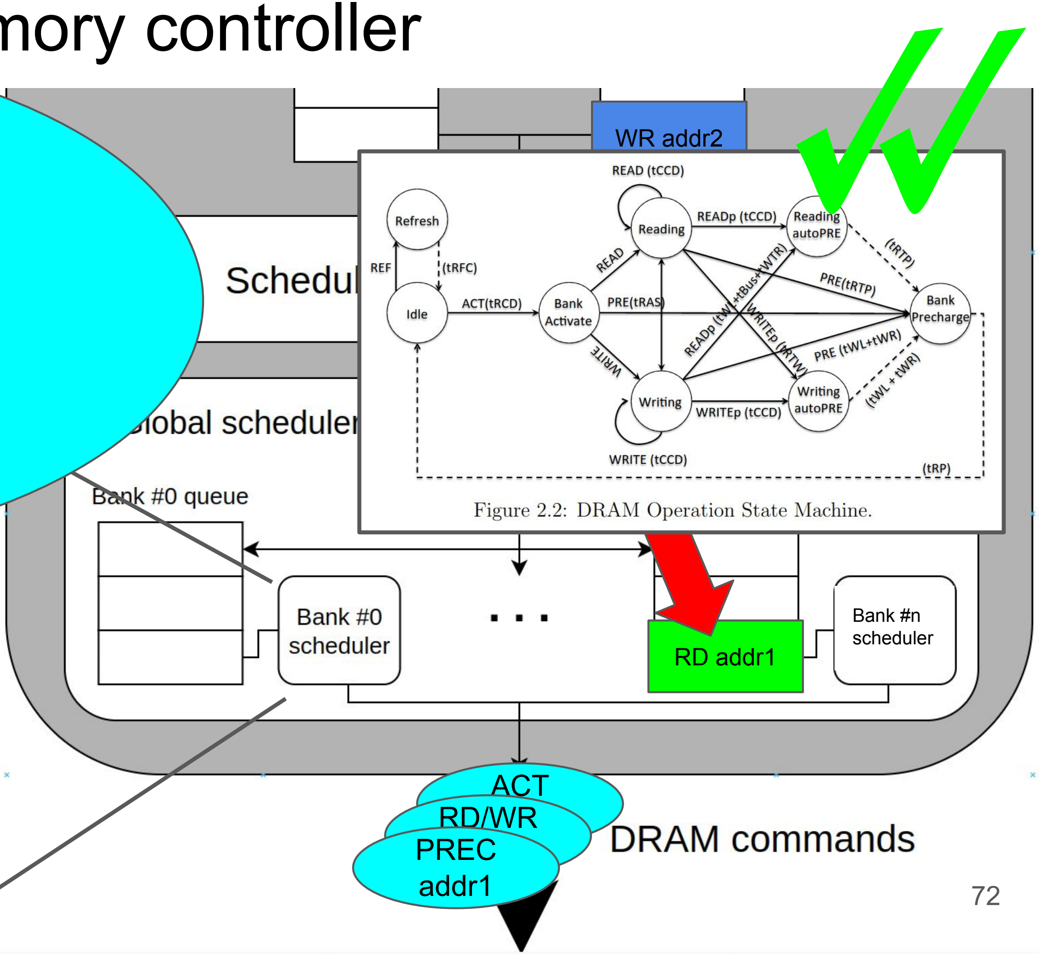

Figure 2.2: DRAM Operation State Machine.

Structure (logical) of a memory controller

Whe

Instead, we'll just consider the following relevant points:

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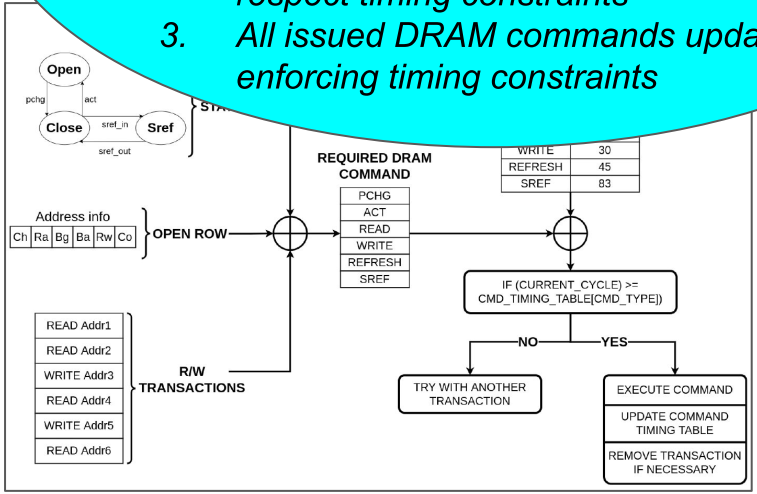
3. *All issued DRAM commands update the enforcing timing constraints*



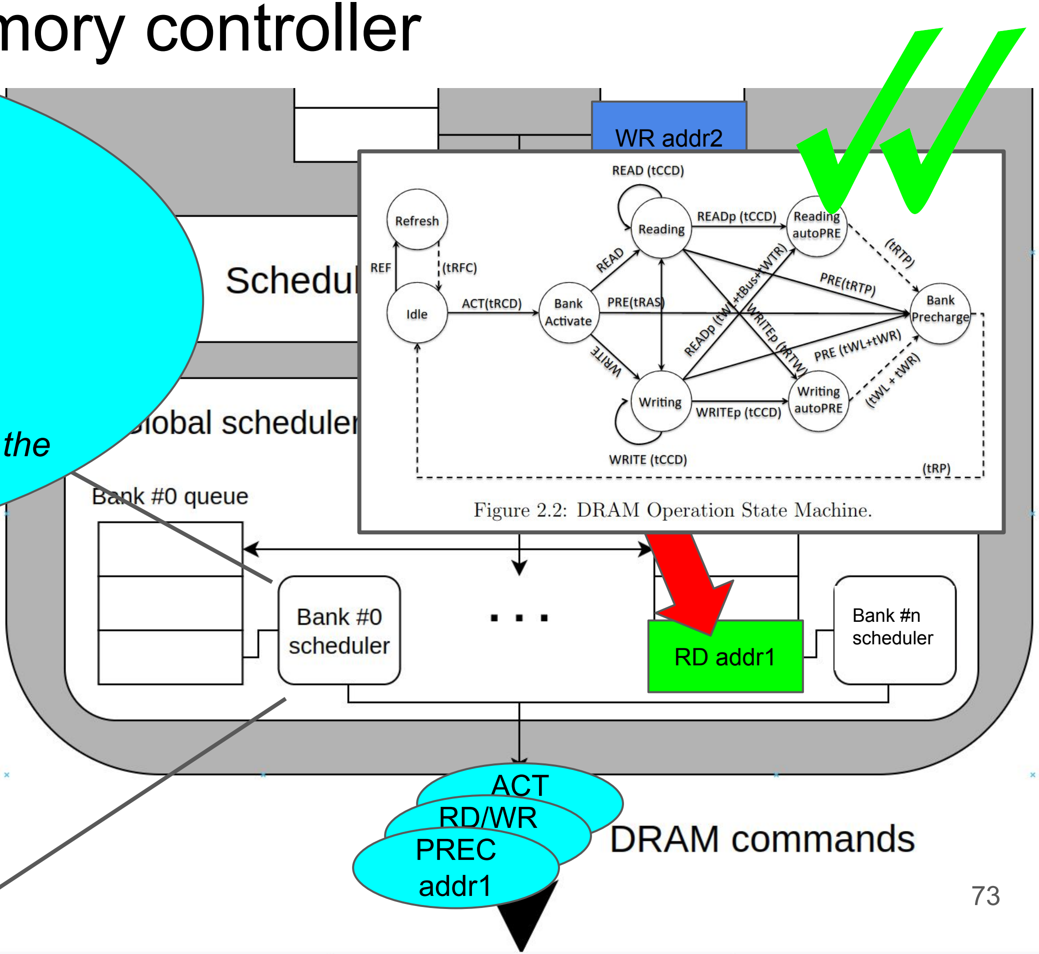
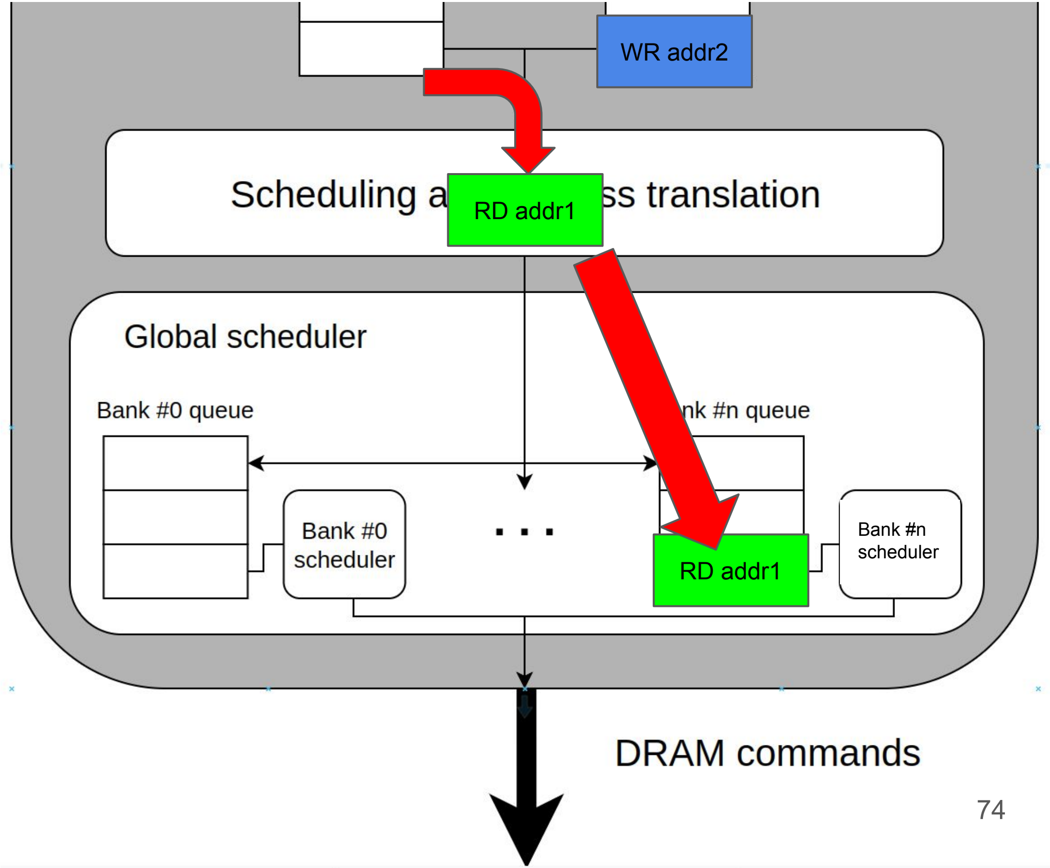


Figure 2.2: DRAM Operation State Machine.

Structure (logical) of a memory controller

Current clock value:
N+1

DRAM cmd type	OK clock cycle
PCHG	…
ACT	N
READ	…
WRITE	…
REFRESH	…
SREF	…



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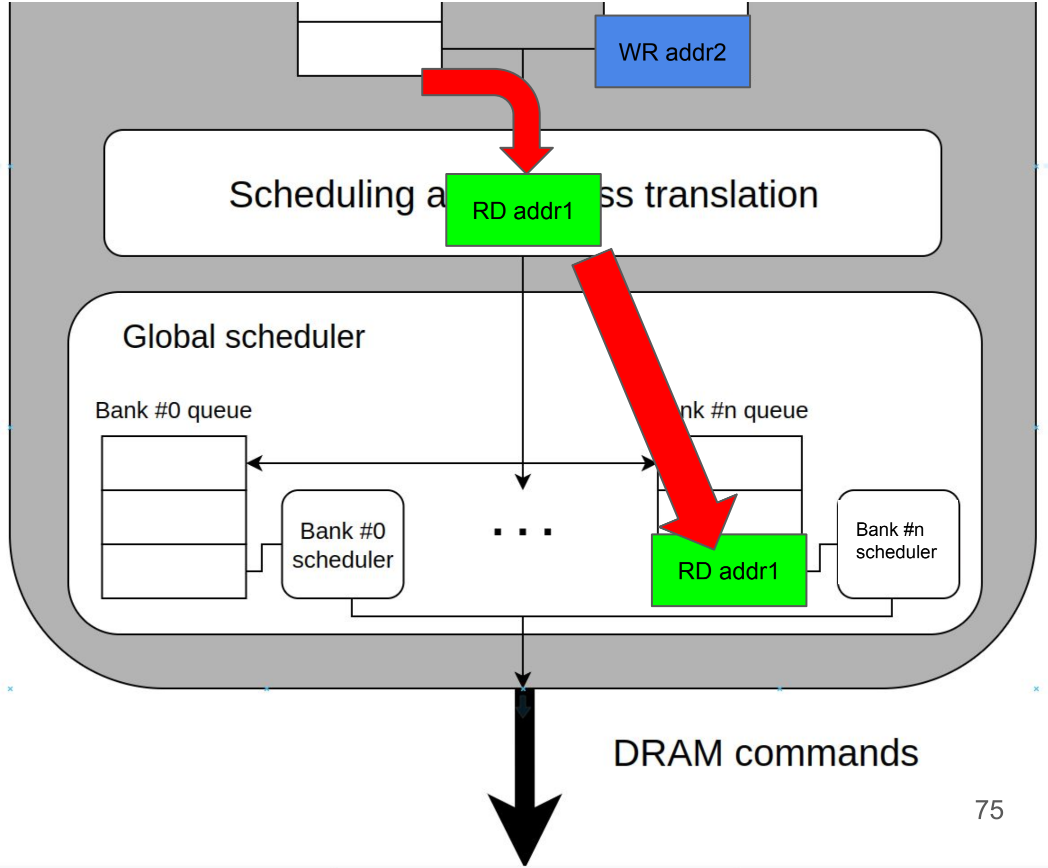
DRAM cmd type	OK clock cycle
PCHG	…
ACT	N
READ	…
WRITE	…
REFRESH	…
SREF	…



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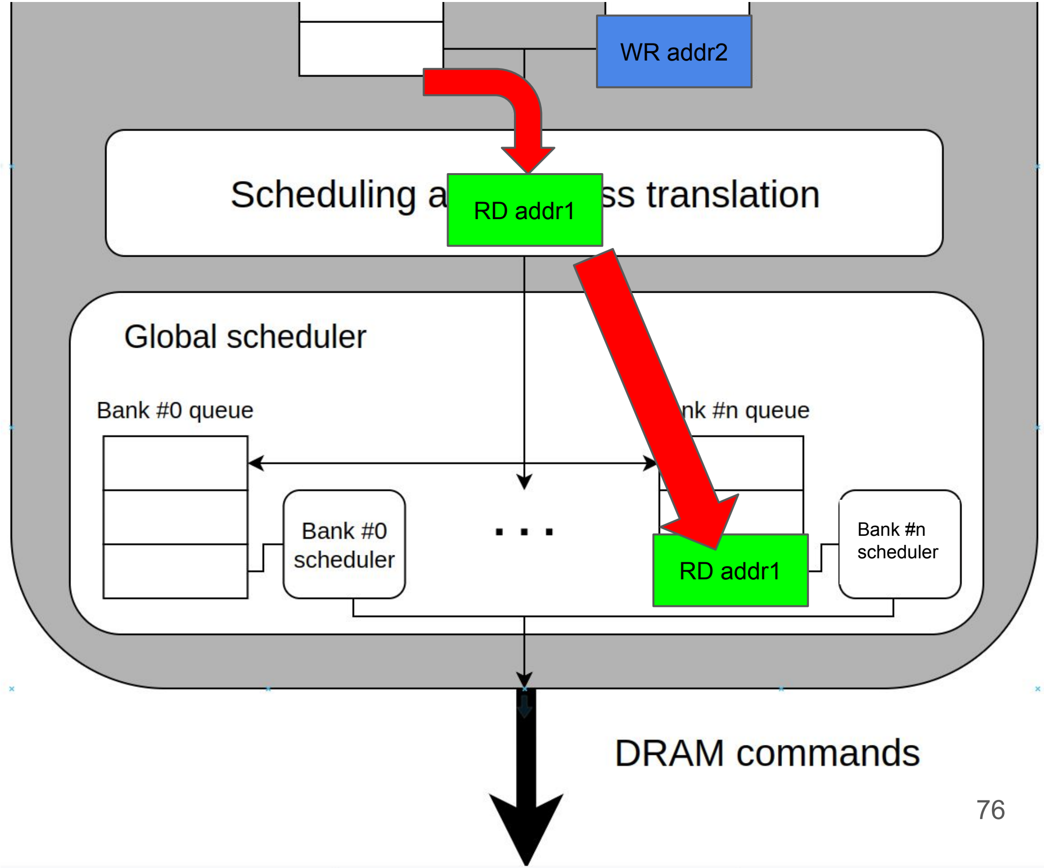
DRAM cmd type	OK clock cycle
PCHG	…
ACT	N
READ	…
WRITE	…
REFRESH	…
SREF	…



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DRAM cmd type	OK clock cycle
PCHG	…
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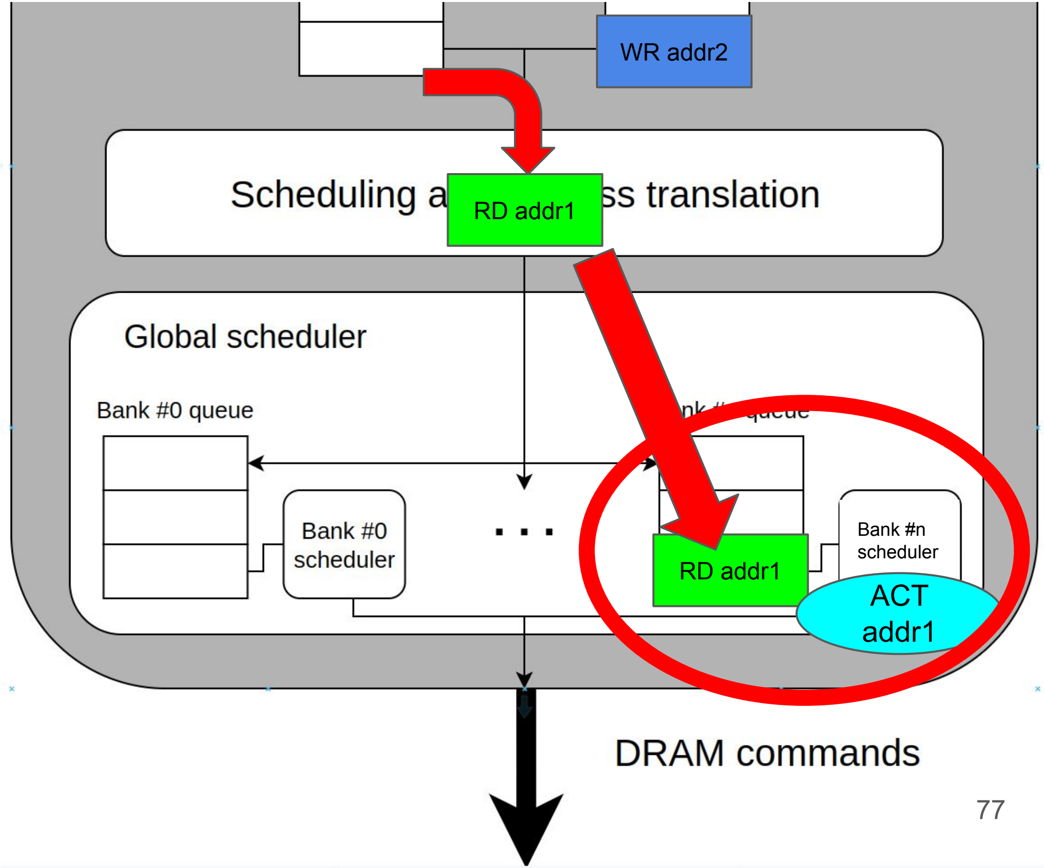

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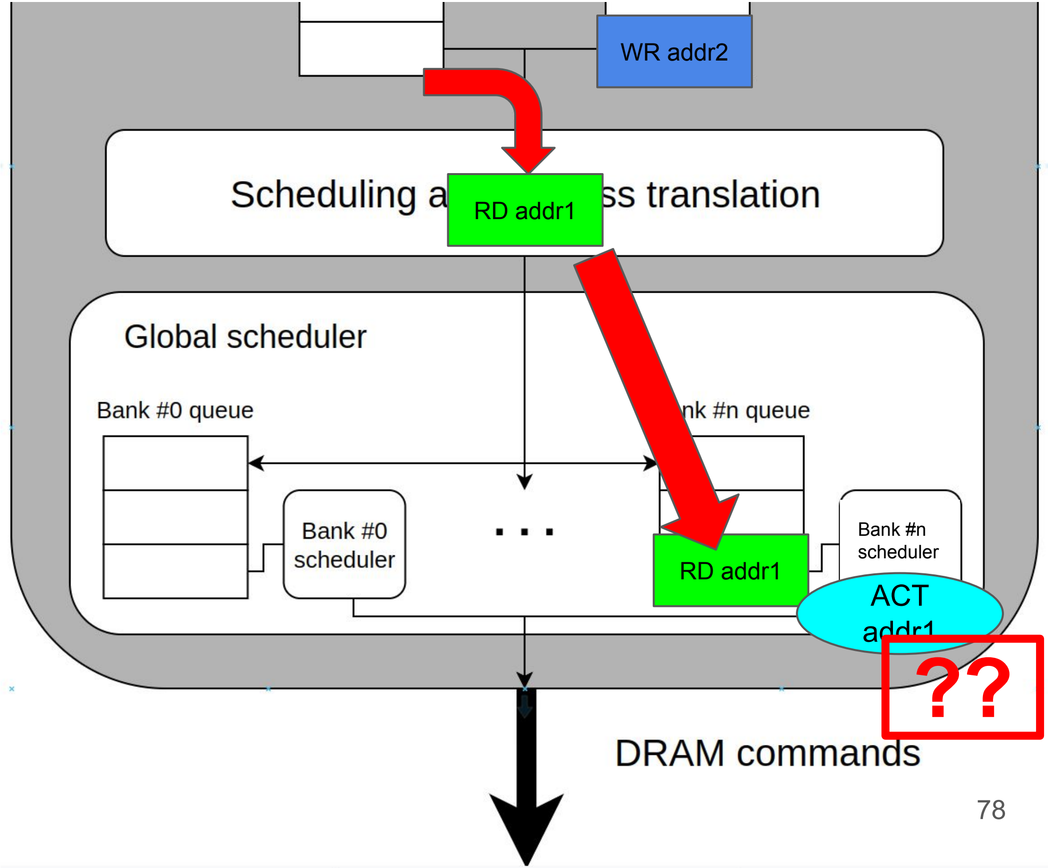

Structure (logical) of a memory controller

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??

DRAM cmd type	OK clock cycle
PCHG	…
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SREF	…

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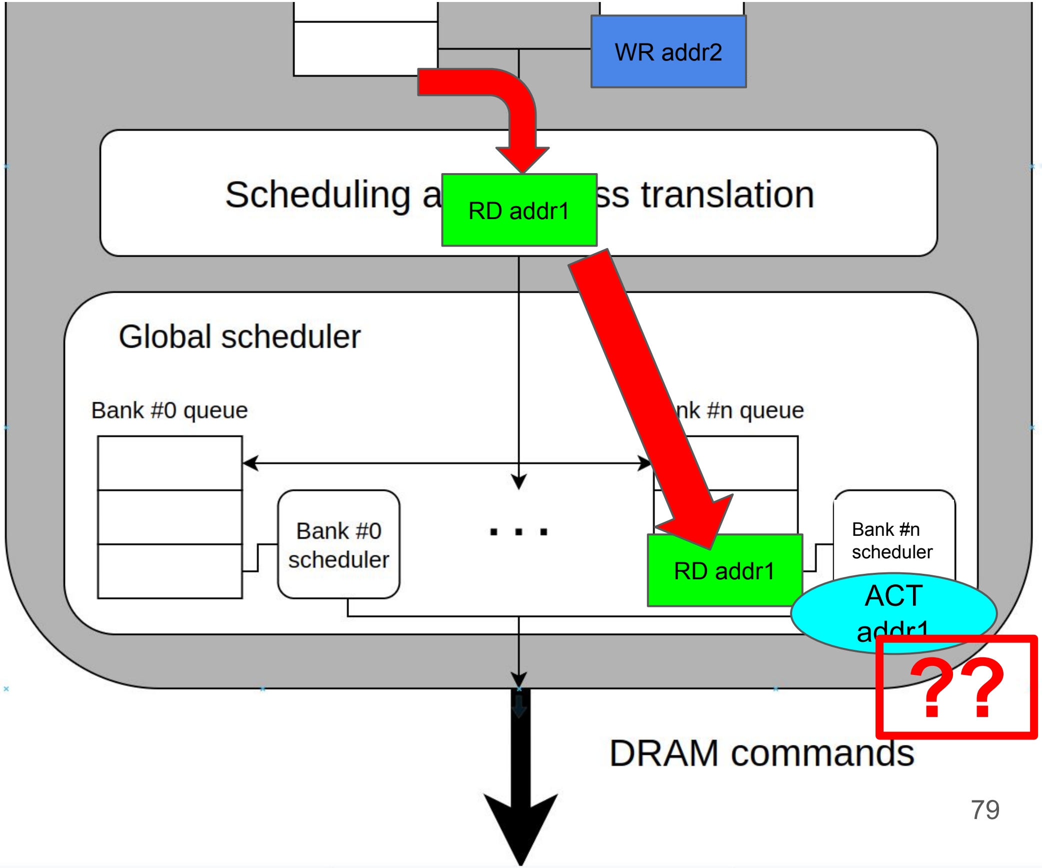


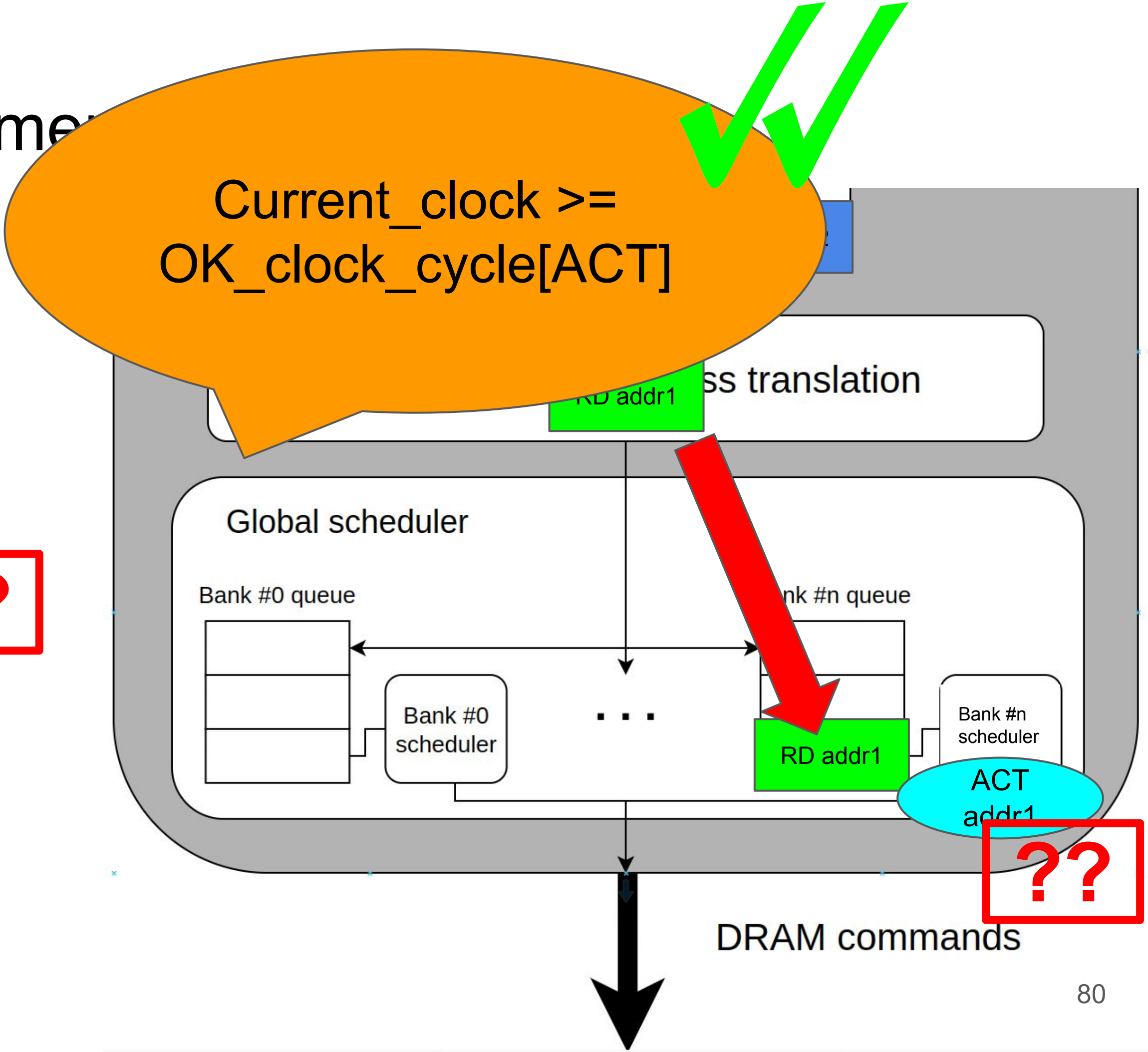
Structure (logical) of a me

Current clock value:
N+1

??

DRAM cmd type	OK clock cycle
PCHG	…
ACT	N
READ	…
WRITE	…
REFRESH	…
SREF	…

??

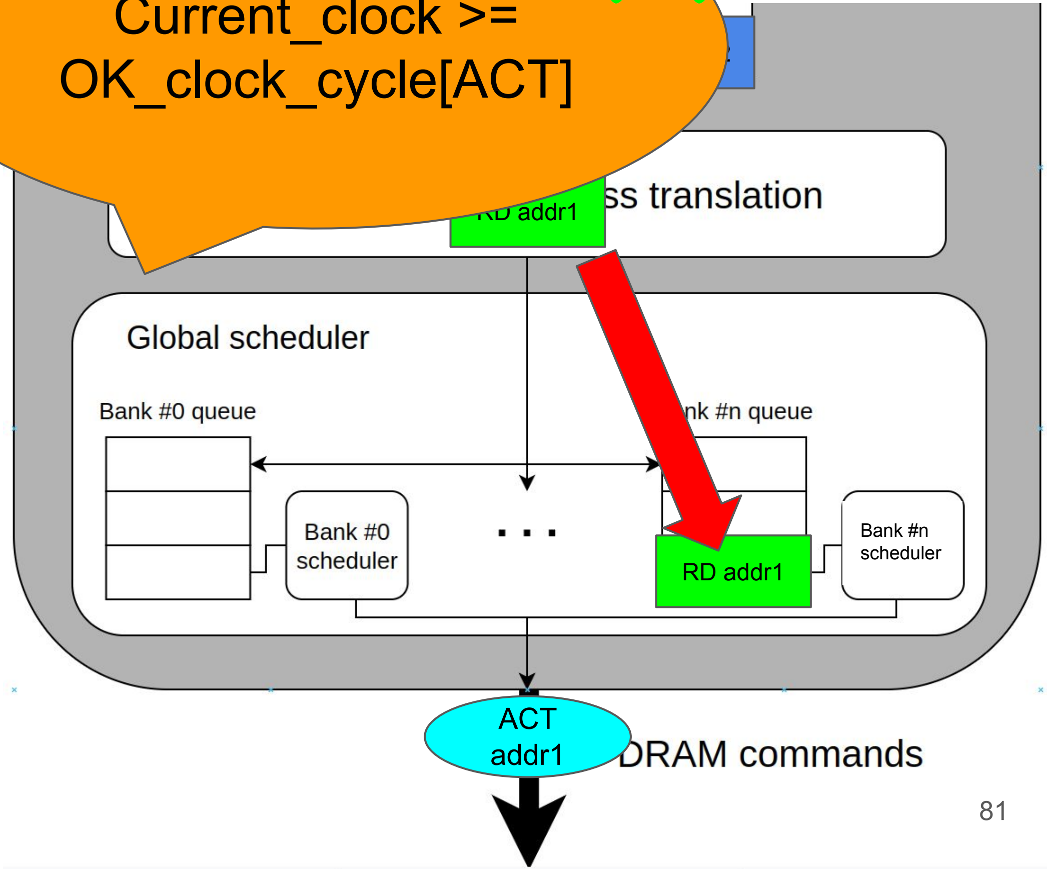


Current_clock >=
OK_clock_cycle[ACT]

Structure (logical) of a me

***Current clock value:
N+1***

DRAM cmd type	OK clock cycle
PCHG	…
ACT	N
READ	…
WRITE	…
REFRESH	…
SREF	…



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✓✓

Structure (logical) of a me

***Current clock value:
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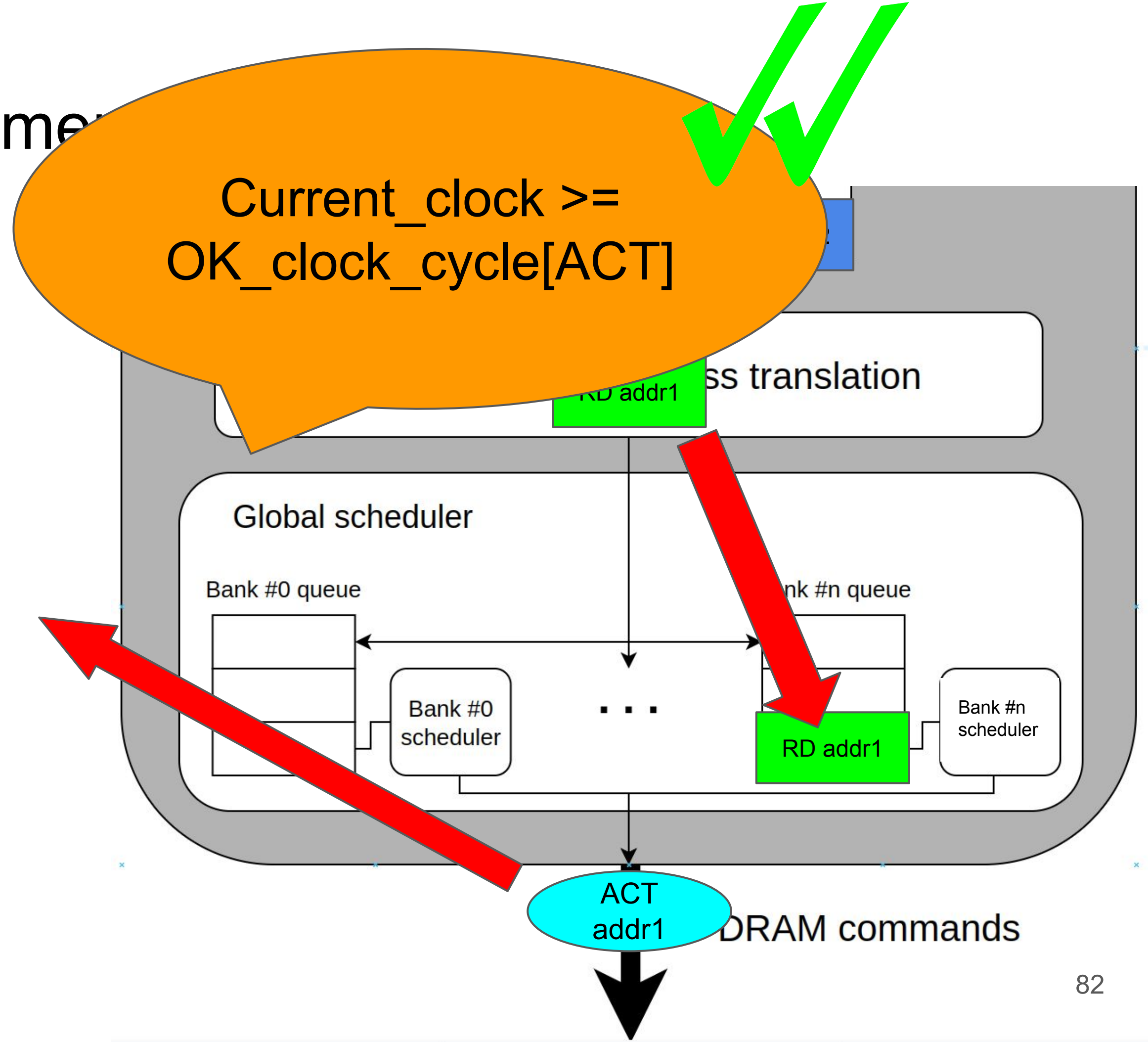
READ	…
WRITE	…
REFRESH	…
SREF	…

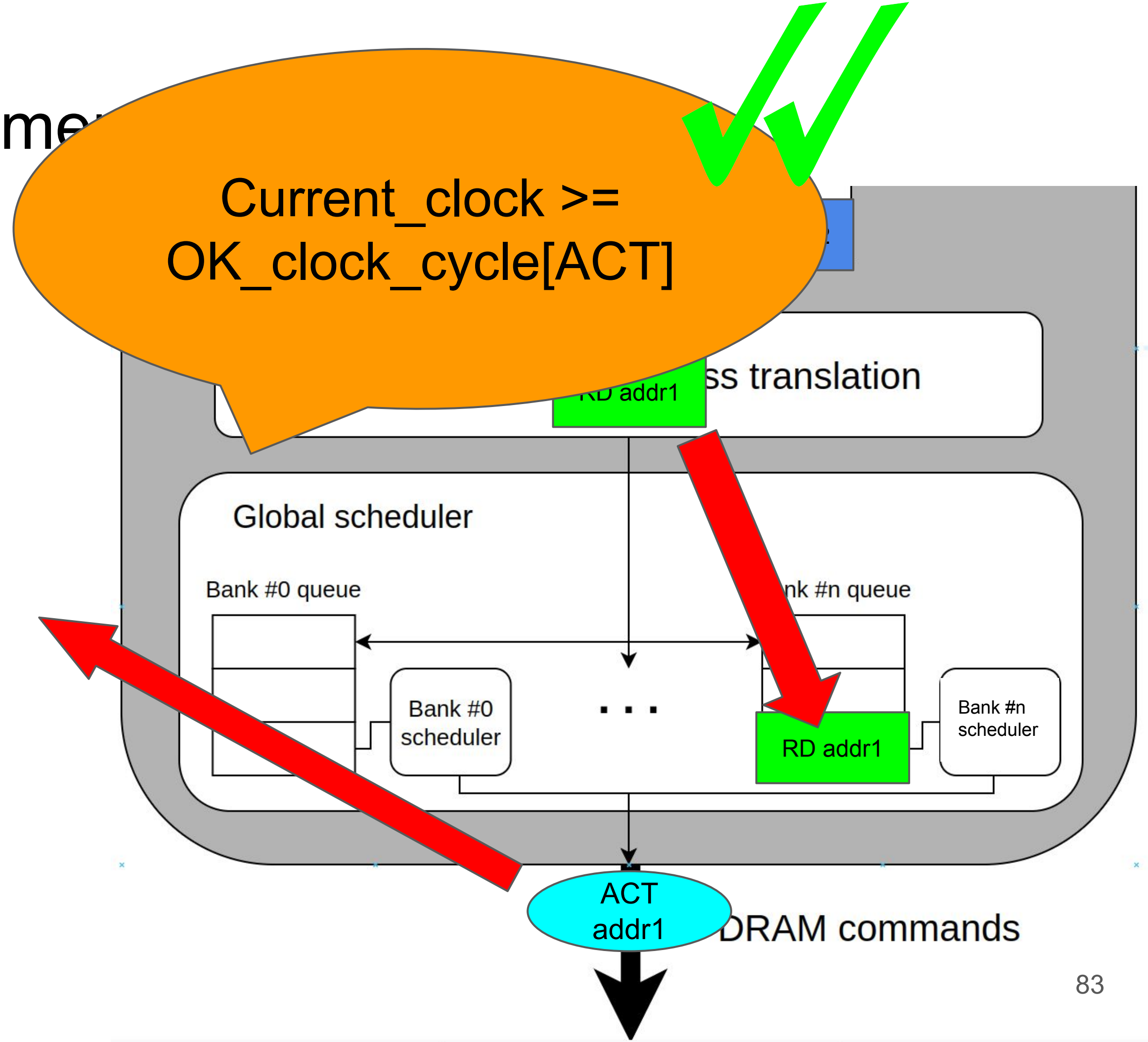


Current_clock >=
OK_clock_cycle[ACT]

Structure (logical) of a me

Current clock value:
N+1

DRAM cmd type	OK clock cycle
PCHG	… + tXXX
ACT	N + tYYY
READ	… + tZZZ
WRITE	… + tAAA
REFRESH	… + tBBB
SREF	… + tCCC

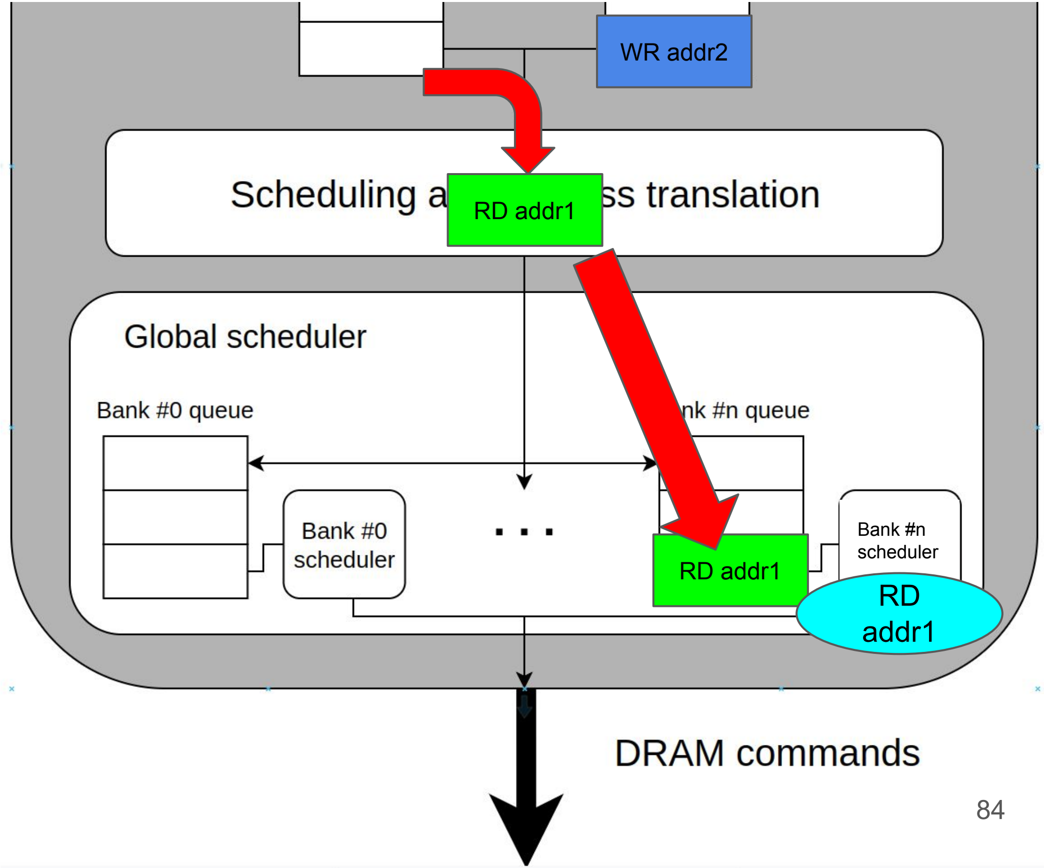


Current_clock >=
OK_clock_cycle[ACT]

Structure (logical) of a memory controller

Current clock value:
N+130

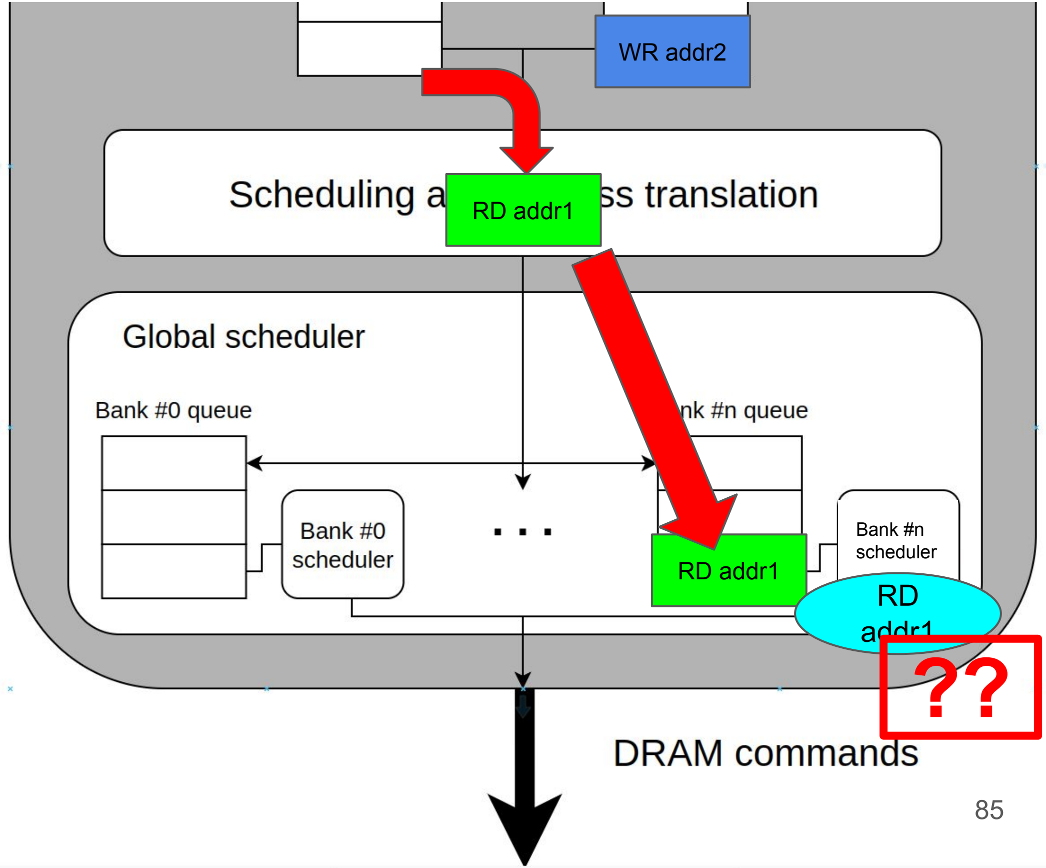
DRAM cmd type	OK clock cycle
PCHG	… + tXXX
ACT	N + tYYY
READ	N + 150
WRITE	… + tAAA
REFRESH	… + tBBB
SREF	… + tCCC



Structure (logical) of a memory controller

Current clock value: N+130

DRAM cmd type	OK clock cycle
PCHG	… + tXXX
ACT	N + tYYY
READ	N + 150
WRITE	… + tAAA
REFRESH	… + tBBB
SREF	… + tCCC



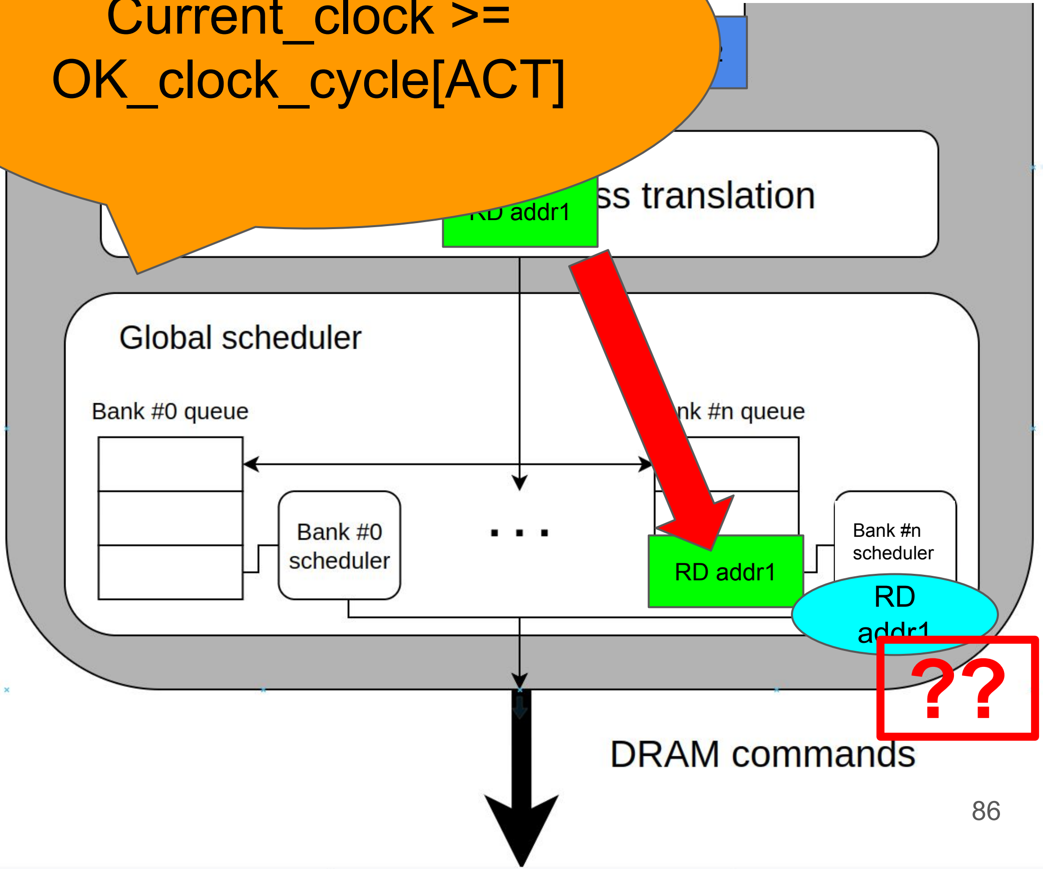
Structure (logical) of a me

Current clock value:
N+130

Current_clock >=
OK_clock_cycle[ACT]

XX

DRAM cmd type	OK clock cycle
PCHG	… + tXXX
ACT	N + tYYY
READ	N + 150
WRITE	… + tAAA
REFRESH	… + tBBB
SREF	… + tCCC



Structure (logical) of a me

Current clock value:
N+130

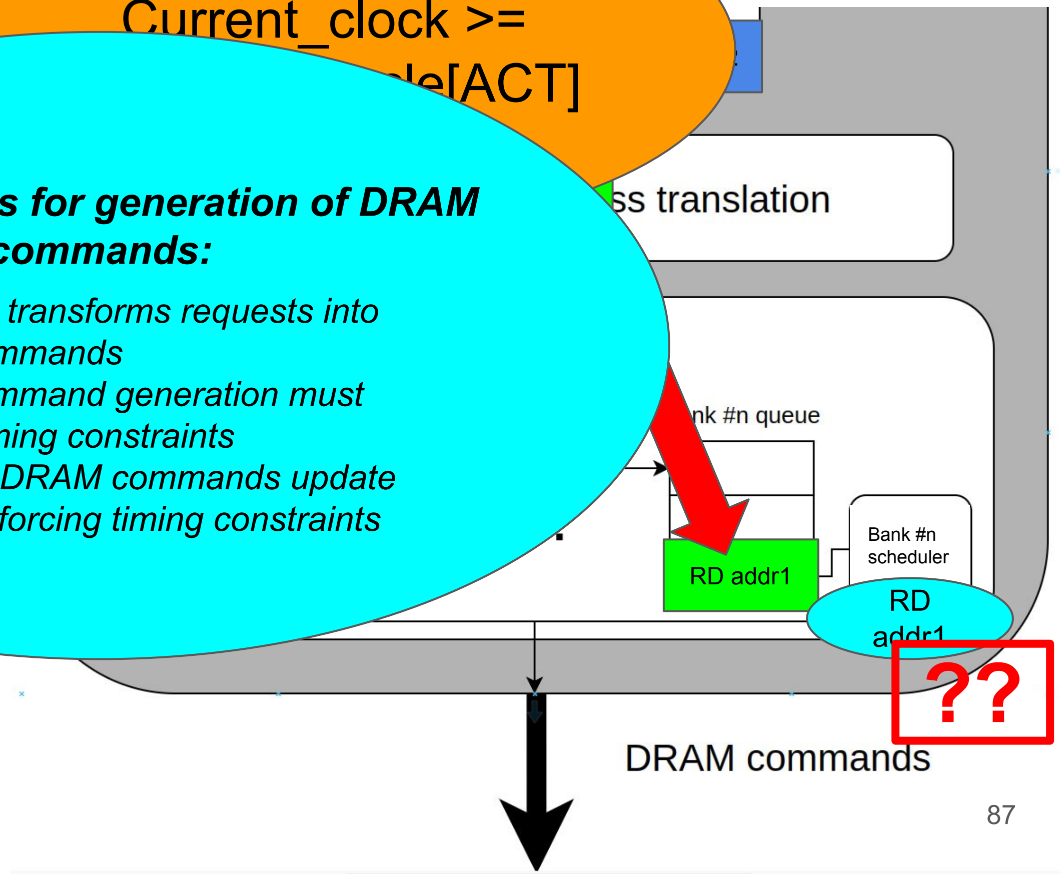
DRAM cmd type	
PCHG	
ACT	
READ	
WRITE	… + tAA
REFRESH	… + tBBB
SREF	… + tCCC

Current_clock >=
le[ACT]

XX

Relevant points for generation of DRAM commands:

1. *Scheduler transforms requests into DRAM commands*
2. *DRAM command generation must respect timing constraints*
3. *All issued DRAM commands update (some) enforcing timing constraints*



This is where our HW proposal comes into full view

Motivation for our proposal (following slides)

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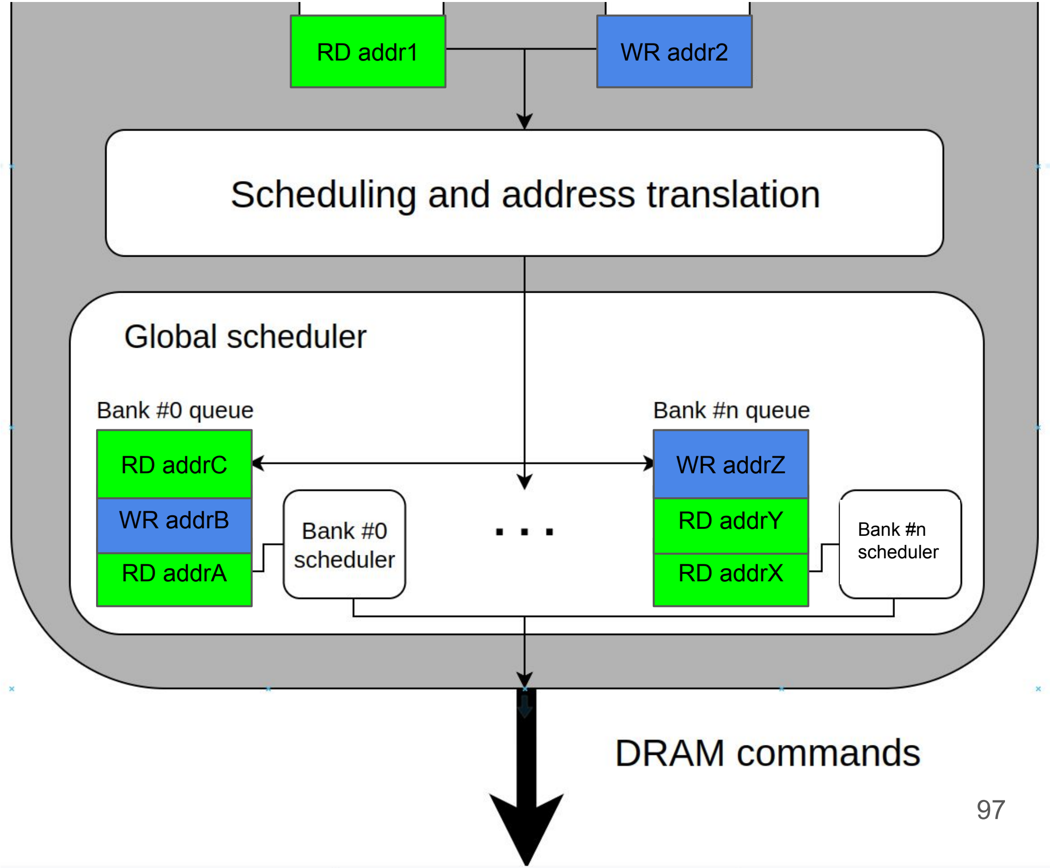
    - Page-write counters
- More information on interactions and delays between memory transactions could be used for the following:
    - Optimizing core usage/pinning within main memory
    - Verification of stress tests or workloads through dedicated HW counters
    - Utilization metrics of different parts of main memory (bank, bankgroup, rank…)

Back-end view

Current clock value:
N+130

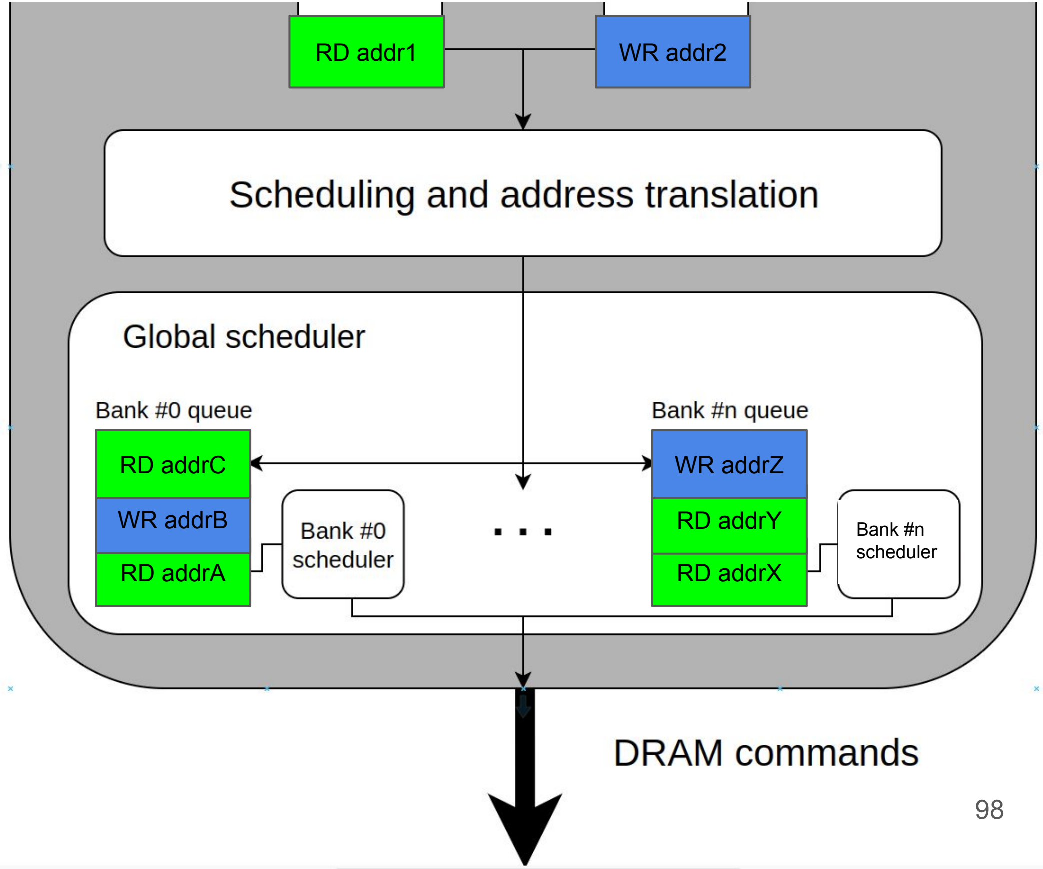
DRAM cmd type	OK clock cycle
PCHG	… + tXXX
ACT	N + tYYY
READ	N + 150
WRITE	… + tAAA
REFRESH	… + tBBB
SREF	… + tCCC



Back-end view, **NOW** with core info

Current clock value:
N+130

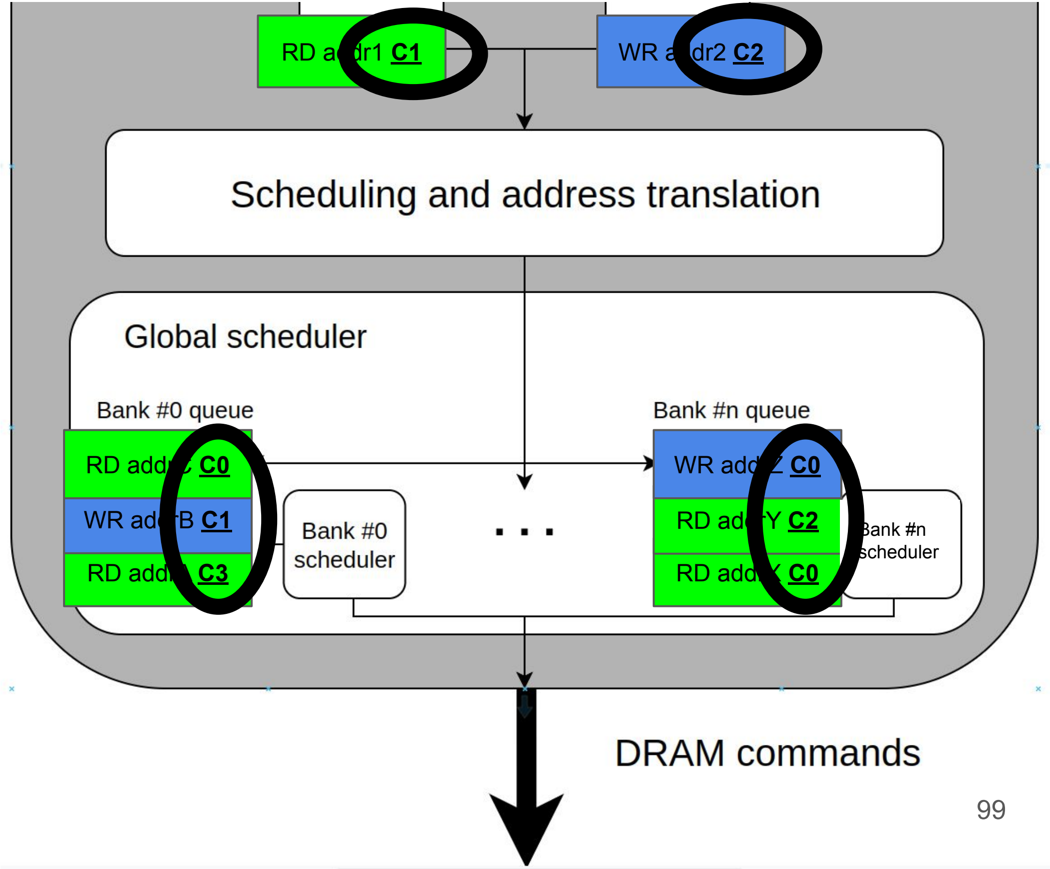
DRAM cmd type	OK clock cycle
PCHG	… + tXXX
ACT	N + tYYY
READ	N + 150
WRITE	… + tAAA
REFRESH	… + tBBB
SREF	… + tCCC



Back-end view, **NOW** with core info

Current clock value:
N+130

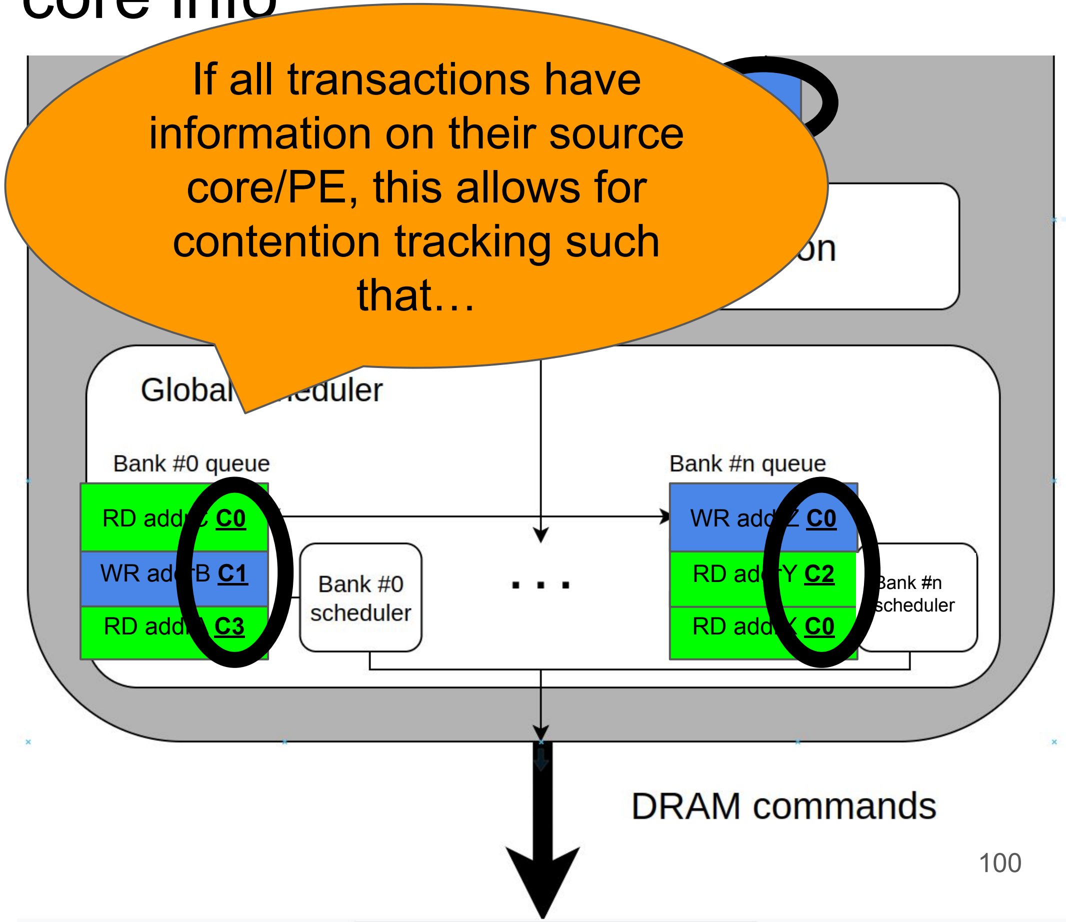
DRAM cmd type	OK clock cycle
PCHG	… + tXXX
ACT	N + tYYY
READ	N + 150
WRITE	… + tAAA
REFRESH	… + tBBB
SREF	… + tCCC



Back-end view, **NOW** with core info

Current clock value: N+130

DRAM cmd type	OK clock cycle
PCHG	… + tXXX
ACT	N + tYYY
READ	N + 150
WRITE	… + tAAA
REFRESH	… + tBBB
SREF	… + tCCC

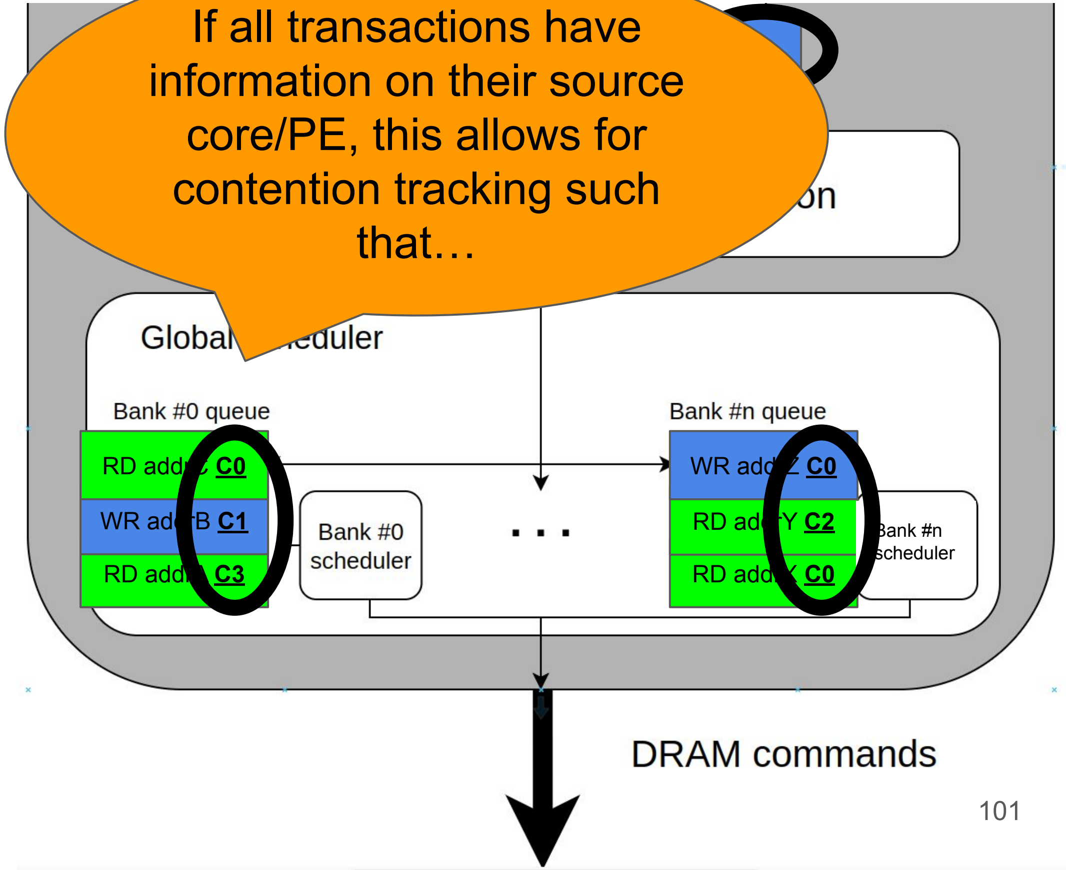


If all transactions have information on their source core/PE, this allows for contention tracking such that…

Back-end view, **NOW** with core info

Current clock value: N+130

DRAM cmd type	**OK clock cycle**	**Last core to update**
PCHG	… + tXXX	C0
ACT	N + tYYY	C1
READ	N + 150	C2
WRITE	… + tAAA	C2
REFRESH	… + tBBB	C3
SREF	… + tCCC	C3



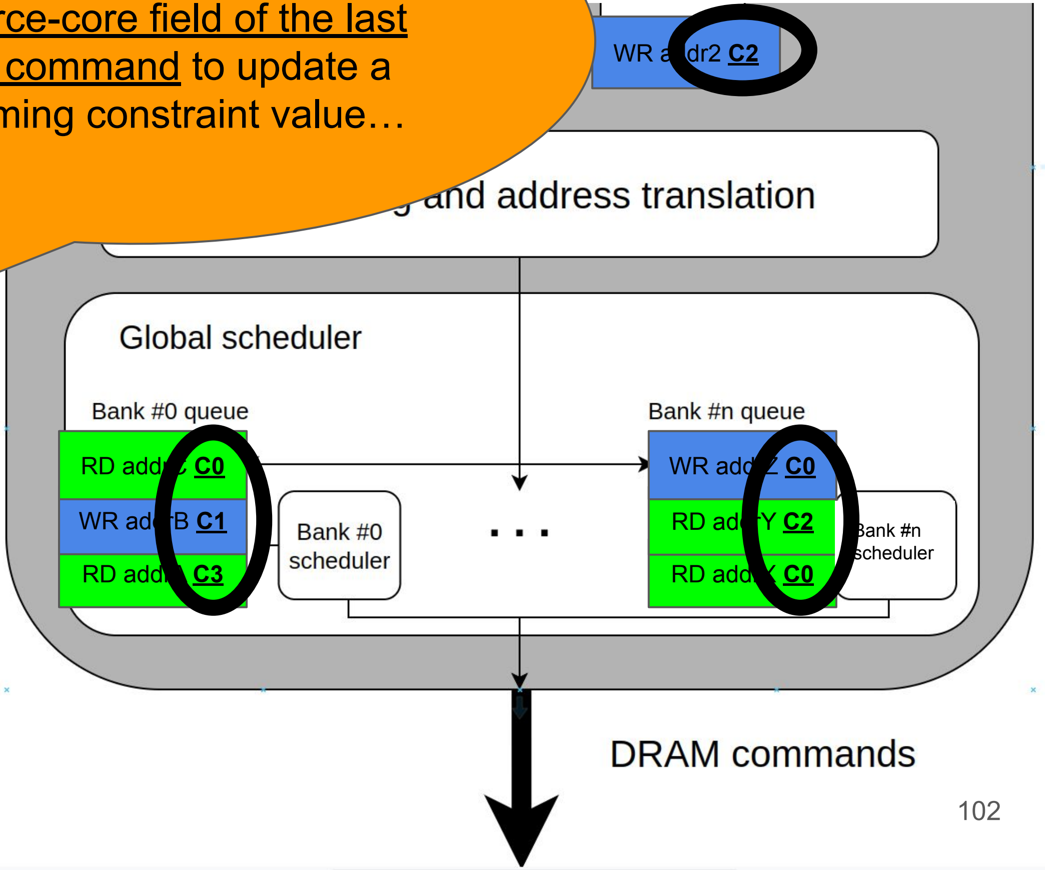
If all transactions have information on their source core/PE, this allows for contention tracking such that…

Back-end view, **N**

Current clock valu
N+130

This column holds information on the <u>source-core field of the last DRAM command</u> to update a given timing constraint value…

DRAM cmd type	OK clock cycle	Last core to update
PCHG	… + tXXX	C0
ACT	N + tYYY	C1
READ	N + 150	C2
WRITE	… + tAAA	C2
REFRESH	… + tBBB	C3
SREF	… + tCCC	C3

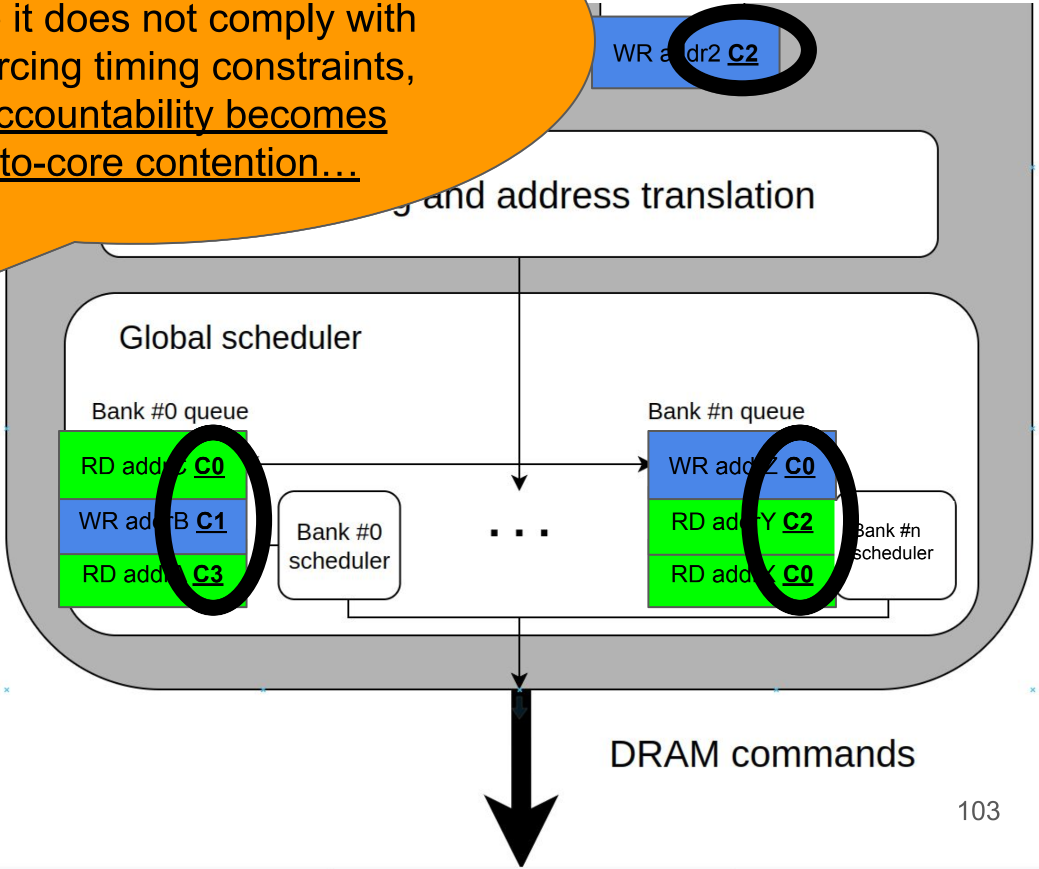


Back-end view, **N**

Current clock valu
N+130

As such, whenever a DRAM command cannot be issued because it does not comply with the enforcing timing constraints, <u>core-accountability becomes core-to-core contention…</u>

DRAM cmd type	OK clock cycle	Last core to update
PCHG	… + tXXX	C0
ACT	N + tYYY	C1
READ	N + 150	C2
WRITE	… + tAAA	C2
REFRESH	… + tBBB	C3
SREF	… + tCCC	C3



Back-end view, **N**

Current clock valu
N+130

As such, whenever a DRAM command cannot be issued because it does not comply with the enforcing timing constraints, <u>core-accountability becomes core-to-core contention…</u>

DRAM cmd type	OK clock cycle	Last core to update
PCHG	… + tXXX	C0
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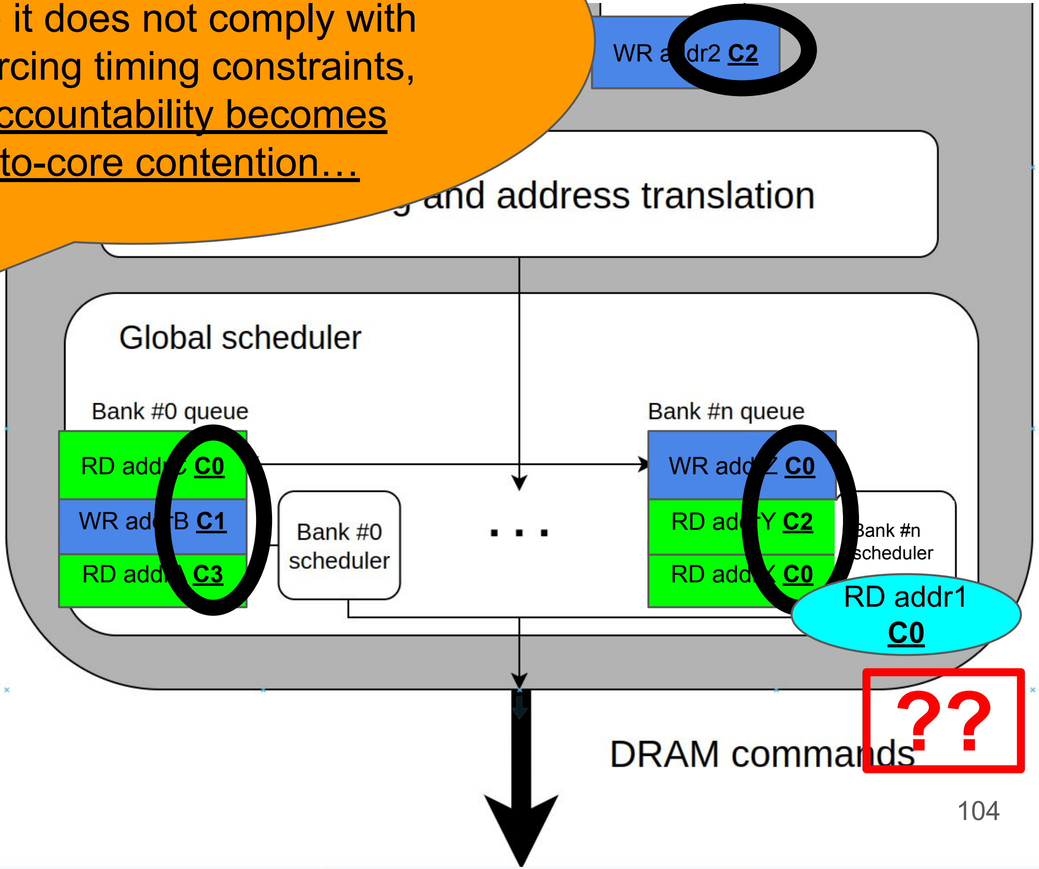
WRITE	… + tAAA	C2
REFRESH	… + tBBB	C3
SREF	… + tCCC	C3

!!



Source-core info traceability

KEY IDEA: the extension of the timing constraint table with source-core information allows core-to-core contention tracking whenever a memory transaction tries to issue its corresponding DRAM commands

DRAM cmd type	OK clock cycle	Last core to update
PCHG	… + tXXX	C0
ACT	N + tYYY	C1
READ	N + 150	C2
WRITE	… + tAAA	C2
REFRESH	… + tBBB	C3
SREF	… + tCCC	C3

Source-core info traceability

KEY IDEA: the extension of the timing constraint table with source-core information allows core-to-core contention tracking whenever a memory transaction tries to issue its corresponding DRAM commands

This holds true for the presented model of the memory controller (MC)

DRAM cmd type	OK clock cycle	Last core to update
PCHG	… + tXXX	C0
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REFRESH	… + tBBB	C3
SREF	… + tCCC	C3

Source-core info traceability

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This holds true for the presented model of the memory controller (MC), which could be interpreted as:

1. MC with a static command scheduling policy, aka closed-page policy

DRAM cmd type	OK clock cycle	Last core to update
PCHG	… + tXXX	C0
ACT	N + tYYY	C1
READ	N + 150	C2
WRITE	… + tAAA	C2
REFRESH	… + tBBB	C3
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1. MC with a static command scheduling policy, aka closed-page policy
   a. Typical in predictable MCs and the WCET world in general

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PCHG	… + tXXX	C0
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REFRESH	… + tBBB	C3
SREF	… + tCCC	C3

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1. MC with a static command scheduling policy, aka closed-page policy
   a. Typical in predictable MCs and the WCET world in general
2. MC with dynamic command scheduling policy, aka open-page policy

More on this later…

DRAM cmd type	OK clock cycle	Last core to update
PCHG	… + tXXX	C0
ACT	N + tYYY	C1
[illegible]	N + 150	C2
[illegible]	… + tAAA	C2
[illegible]	… + tBBB	C3
SREF	… + tCCC	C3

Source-core info traceability

How is any of this relevant?

DRAM cmd type	**OK clock cycle**	**Last core to update**
PCHG	… + tXXX	C0
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SREF	… + tCCC	C3

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The only obtainable data related to main-memory contention is limited to page-hits and page-misses (if at all, shout out to the T2080), with no sort of insight into finer-level details as to who/why are memory requests being delayed.

DRAM cmd type	OK clock cycle	Last core to update
PCHG	… + tXXX	C0
ACT	N + tYYY	C1
READ	N + 150	C2
WRITE	… + tAAA	C2
REFRESH	… + tBBB	C3
SREF	… + tCCC	C3

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Main memory, in terms of contention, is an inscrutable black box of black magic of nasty contention we cannot get a proper understanding of right now.

DRAM cmd type	OK clock cycle	Last core to update
PCHG	… + tXXX	C0
ACT	N + tYYY	C1
READ	N + 150	C2
WRITE	… + tAAA	C2
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DRAM cmd type	OK clock cycle	Last core to update
PCHG	… + tXXX	C0
ACT	N + tYYY	C1
READ	N + 150	C2
WRITE	… + tAAA	C2
REFRESH	… + tBBB	C3
SREF	… + tCCC	C3

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ACT	N + tYYY	C1
READ	N + 150	C2
WRITE	… + tAAA	C2
REFRESH	… + tBBB	C3
SREF	… + tCCC	C3

Core-to-core

✓✓

Source-core info traceability

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In fact, this “extending-of-the-timing-table” approach can be expanded upon…

DRAM cmd type	OK clock cycle	Last core to update	Address of request
PCHG	… + tXXX	C0	addr1
ACT	N + tYYY	C1	addr2
READ	N + 150	C2	addr3
WRITE	… + tAAA	C2	addr4
REFRESH	… + tBBB	C3	addr5
SREF	… + tCCC	C3	addr6

Core-to-core ✓✓

Type of contention ✓✓

Source-core info traceability

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DRAM cmd type	OK clock cycle	Last core to update	Address of request	Enforced time constr.
PCHG	… + tXXX	C0	addr1	tXXX
ACT	N + tYYY	C1	addr2	tYYY
READ	N + 150	C2	addr3	tZZZ
WRITE	… + tAAA	C2	addr4	tAAA
REFRESH	… + tBBB	C3	addr5	tBBB
SREF	… + tCCC	C3	addr6	tCCC

Core-to-core	Type of contention	Time constraint analysis
✓✓	✓✓	✓✓

Source-core info traceability

How is any of this relevant?

Level 0

The only obtainable data related to main-memory contention is limited to page-hits and page-misses (if at all, shout out to the T2080), with no sort of insight into finer-level details as to who/why are memory requests being delayed.

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DRAM cmd type	OK clock cycle	Last core to update	Address of request	Enforced time constr.
PCHG	… + tXXX	C0	addr1	tXXX
ACT	N + tYYY	C1	addr2	tYYY
READ	N + 150	C2	addr3	tZZZ
WRITE	… + tAAA	C2	addr4	tAAA
REFRESH	… + tBBB	C3	addr5	tBBB
SREF	… + tCCC	C3	addr6	tCCC

Core-to-core ✓✓

Type of contention ✓✓

Time constraint analysis ✓✓

Source-core info traceability

Level 0 performance counters:

- Page hits
- Page misses
- Page reads
- Page writes

How is any of this rel

The only obtainab
contention is lim
at all, shout ou
into finer-level
requests being

Main memory, in
inscrutable black b
contention we cannot g
right now.

In fact, this “extending-of-the-timing-tab
can be expanded upon…

Address of request	Enforced time constr.
ddr1	tXXX
dr2	tYYY
r3	tZZZ
dr4	tAAA
addr5	tBBB
addr6	tCCC

✓✓

ype of contention

✓✓

Time constraint analysis

✓✓

Source-core info traceability

How is any of this relevant?

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DRAM cmd type	OK clock cycle	Last core to update	Address of request	Enforced time constr.
PCHG	… + tXXX	C0	addr1	tXXX
ACT	N + tYYY	C1	addr2	tYYY
READ	N + 150	C2	addr3	tZZZ
WRITE	… + tAAA	C2	addr4	tAAA
REFRESH	… + tBBB	C3	addr5	tBBB
SREF	… + tCCC	C3	addr6	tCCC

Core-to-core	Type of contention	Time constraint analysis
✓✓	✓✓	✓✓

Source-core info traceability

How is any of this relevant?

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In fact, this "extending-of-the-timing-table" approach can be expanded upon…

Level 1

DRAM cmd type	OK clock cycle	Last core to update	Address of request	Enforced time constr.
PCHG	… + tXXX	C0	addr1	tXXX
ACT	N + tYYY	C1	addr2	tYYY
READ	N + 150	C2	addr3	tZZZ
WRITE	… + tAAA	C2	addr4	tAAA
REFRESH	… + tBBB	C3	addr5	tBBB
SREF	… + tCCC	C3	addr6	tCCC

Core-to-core ✓✓

Type of contention ✓✓

Time constraint analysis ✓✓

Level 0 performance counters:

Page hits
Page misses
Page reads
Page writes

ceability

Ho

The only obtaina contention is li at all, shout ou into finer-level requests being

Main memory, in inscrutable black b contention we cannot right now.

In fact, this “extending-of-the-timing-tab can be expanded upon…

Level 1 performance counters:

- Level 0’s perf. counters
- Core-to-core delays at MC’s back-end
- Core-to-core delays also at MC’s front-end

Address of request	Enforced time constr.
ddr1	tXXX
dr2	tYYY
r3	tZZZ
dr4	tAAA
addr5	tBBB
addr6	tCCC

ype of contention ✓✓

Time constraint analysis ✓✓

✓✓

Source-core info traceability

How is any of this relevant?

Level 0

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In fact, this “extending-of-the-timing-table” approach can be expanded upon…

Level 1

DRAM cmd type	OK clock cycle	Last core to update	Address of request	Enforced time constr.
PCHG	… + tXXX	C0	addr1	tXXX
ACT	N + tYYY	C1	addr2	tYYY
READ	N + 150	C2	addr3	tZZZ
WRITE	… + tAAA	C2	addr4	tAAA
REFRESH	… + tBBB	C3	addr5	tBBB
SREF	… + tCCC	C3	addr6	tCCC

Core-to-core	Type of contention	Time constraint analysis
✓✓	✓✓	✓✓

Source-core info traceability

How is any of this relevant?

Level 0

The only obtainable data related to main-memory contention is limited to page-hits and page-misses (if at all, shout out to the T2080), with no sort of insight into finer-level details as to who/why are memory requests being delayed.

Main memory, in terms of contention, is an inscrutable black box of black magic of nasty contention we cannot get a proper understanding of right now.

In fact, this “extending-of-the-timing-table” approach can be expanded upon…

Level 2

Level 1

DRAM cmd type	OK clock cycle	Last core to update	Address of request	Enforced time constr.
PCHG	… + tXXX	C0	addr1	tXXX
ACT	N + tYYY	C1	addr2	tYYY
READ	N + 150	C2	addr3	tZZZ
WRITE	… + tAAA	C2	addr4	tAAA
REFRESH	… + tBBB	C3	addr5	tBBB
SREF	… + tCCC	C3	addr6	tCCC

Core-to-core	Type of contention	Time constraint analysis
✓✓	✓✓	✓✓

ceability

<u>Level 0 performance counters:</u>

Page hits
Page misses
Page reads
Page writes

<u>Level 1 performance counters:</u>

Level 0
CX-CY back-end
CX-CY front-end

<u>Level 2 performance counters:</u>

- Level 1’s perf. counters
- Core-to-core delays with information on their placement in DRAM memory:
  - Within-bank dependencies
  - Within-bankgroup dependencies
  - Within-rank dependencies
  - …

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requests being

Main memory, in
inscrutable black b
contention we cannot g
right now.

In fact, this “extending-of-the-timing-tabl
can be expanded upon…

request	Enforced time constr.
ddr1	tXXX
dr2	tYYY
r3	tZZZ
dr4	tAAA
addr5	tBBB
addr6	tCCC

✓✓

ype of contention

✓✓

Time constraint analysis

✓✓

Source-core info traceability

How is any of this relevant?

Level 0

The only obtainable data related to main-memory contention is limited to page-hits and page-misses (if at all, shout out to the T2080), with no sort of insight into finer-level details as to who/why are memory requests being delayed.

Main memory, in terms of contention, is an inscrutable black box of black magic of nasty contention we cannot get a proper understanding of right now.

In fact, this “extending-of-the-timing-table” approach can be expanded upon…

Level 2

Level 1

DRAM cmd type	OK clock cycle	Last core to update	Address of request	Enforced time constr.
PCHG	… + tXXX	C0	addr1	tXXX
ACT	N + tYYY	C1	addr2	tYYY
READ	N + 150	C2	addr3	tZZZ
WRITE	… + tAAA	C2	addr4	tAAA
REFRESH	… + tBBB	C3	addr5	tBBB
SREF	… + tCCC	C3	addr6	tCCC

Core-to-core ✓✓

Type of contention ✓✓

Time constraint analysis ✓✓

Source-core info traceability

How is any of this relevant?

Level 0

The only obtainable data related to main-memory contention is limited to page-hits and page-misses (if at all, shout out to the T2080), with no sort of insight into finer-level details as to who/why are memory requests being delayed.

Main memory, in terms of contention, is an inscrutable black box of black magic of nasty contention we cannot get a proper understanding of right now.

In fact, this “extending-of-the-timing-table” approach can be expanded upon…

Level 3

Level 2

Level 1

DRAM cmd type	OK clock cycle	Last core to update	Address of request	Enforced time constr.
PCHG	… + tXXX	C0	addr1	tXXX
ACT	N + tYYY	C1	addr2	tYYY
READ	N + 150	C2	addr3	tZZZ
WRITE	… + tAAA	C2	addr4	tAAA
REFRESH	… + tBBB	C3	addr5	tBBB
SREF	… + tCCC	C3	addr6	tCCC

Core-to-core ✓✓

Type of contention ✓✓

Time constraint analysis ✓✓

Level 0 performance counters:

Page hits
Page misses
Page reads
Page writes

Level 1 performance counters:

Level 0
CX-CY back-end
CX-CY front-end

Level 3 performance counters:

- Level 2’s performance counters
- Core-to-core delays at time-constraint level (finest level of granularity)

Level 2 performance counters:

Level 1
Contention w.r.t. placement

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requests bei

Main memory, i
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request	Enforced time constr.
addr1	tXXX
ddr2	tYYY
ddr3	tZZZ
addr4	tAAA
addr5	tBBB
addr6	tCCC

ore ✓✓

Type of contention ✓✓

Time constraint analysis ✓✓

ceability

Level 0 performance counters:

Page hits
Page misses
Page reads
Page writes

Level 1 performance counters:

Level 0
CX-CY back-end
CX-CY front-end

Lev

Level 0

Ho

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Main memory, in terms of contention, is an inscrutable black box of black magic of nasty con er understanding of

ble” approach

DRAM cmd type	OK clock cycle	Last update	request	Enforced time constr.
PCHG	… + tXXX	C0	addr1	tXXX
ACT	N + tYYY	C1	addr2	tYYY
READ	N + 150	C2	addr3	tZZZ
WRITE	… + tAAA	C2	addr4	tAAA
REFRESH	… + tBBB	C3	addr5	tBBB
SREF	… + tCCC			tCCC

Level 2 performance counters:

Level 1
Contention w.r.t. placement

Core-to-core

✓✓ ✓✓

Level 3 performance counters:

Level 2
Timing constraint analysis

Source-core info traceability

How is any of this relevant?

Level 0

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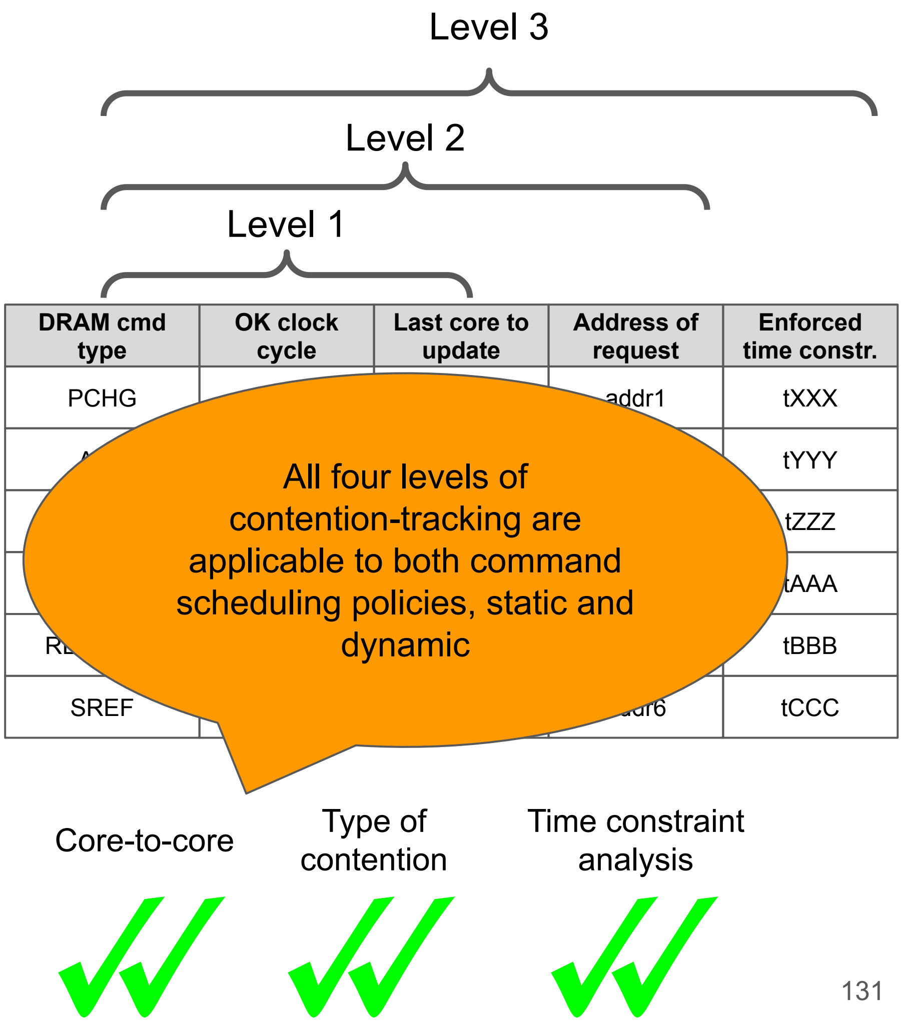
Main memory, in terms of contention, is an inscrutable black box of black magic of nasty contention we cannot get a proper understanding of right now.

In fact, this "extending-of-the-timing-table" approach can be expanded upon…

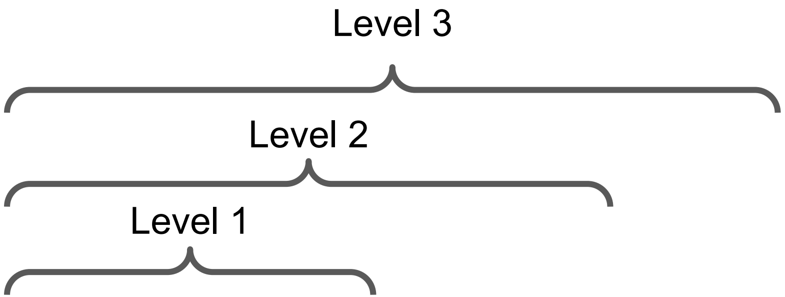


DRAM cmd type	OK clock cycle	Last core to update	Address of request	Enforced time constr.
PCHG			addr1	tXXX
A				tYYY
				tZZZ
				tAAA
RE				tBBB
SREF			ddr6	tCCC

All four levels of contention-tracking are applicable to both command scheduling policies, static and dynamic

Contention proposals

Level 0: page-hits and page-misses
Level 1: core-to-core contention (including inter-queue contention)
Level 2: memory-location-aware contention
Level 3: time constraint analysis



DRAM cmd type	**OK clock cycle**	**Last core to update**	**Address of request**	**Enforced time constr.**
PCHG	… + tXXX	C0	addr1	tXXX
ACT	N + tYYY	C1	addr2	tYYY
READ	N + 150	C2	addr3	tZZZ
WRITE	… + tAAA	C2	addr4	tAAA
REFRESH	… + tBBB	C3	addr5	tBBB
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Core-to-core	Type of contention	Time constraint analysis
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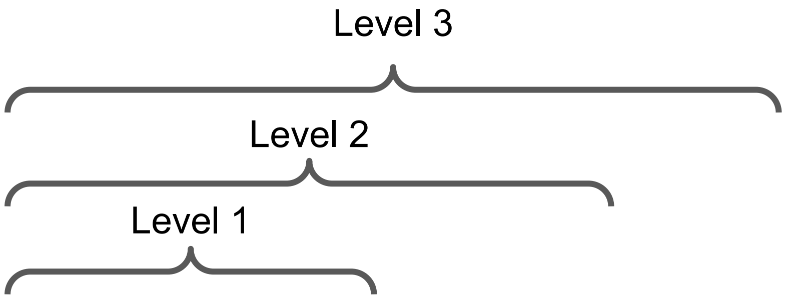

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    - Explanation of contention tracking on a static-command-scheduling MC is almost finished, along with the hardware proposal itself in the form of logical blocks and such