ECC in CVA6-Ariane processor

Sergio García Esteban
Asier Fernández de Lecea Navarro

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- Where ECC modules should go in your processor
  - What to do and where to put them in your processor
- Implementation details: a perilous and headache-ridden path
  - Final account of what we have managed to accomplish

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- You have some important data in memory that is susceptible to corruption (strong radiation environments, for example)
- The integrity of data in memory is essential for programs to run correctly (obviously)
- If that’s the case, how does one (1) detect errors in data words and (2) correct them?

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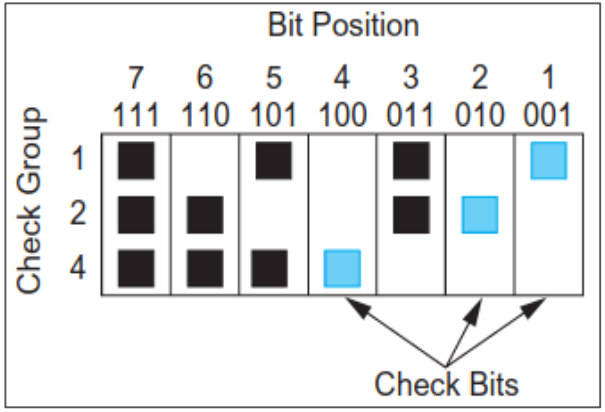

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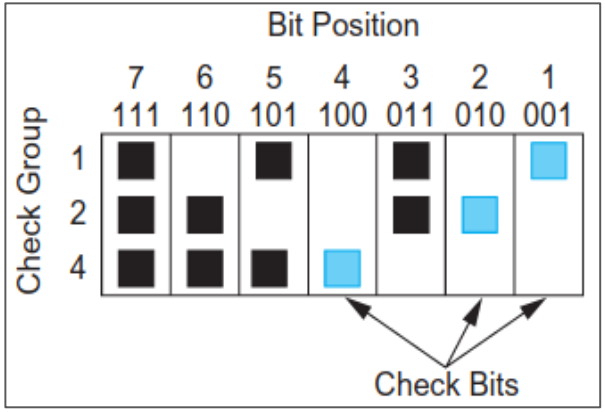

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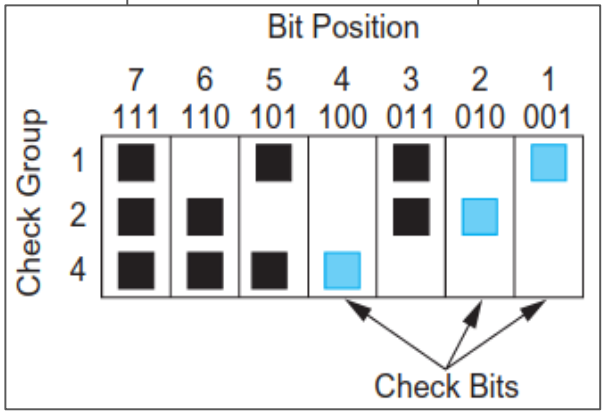

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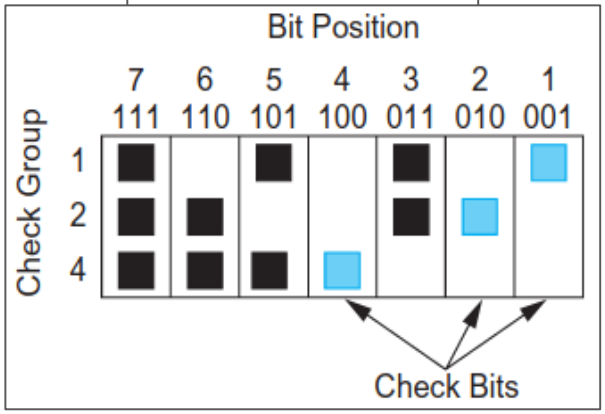

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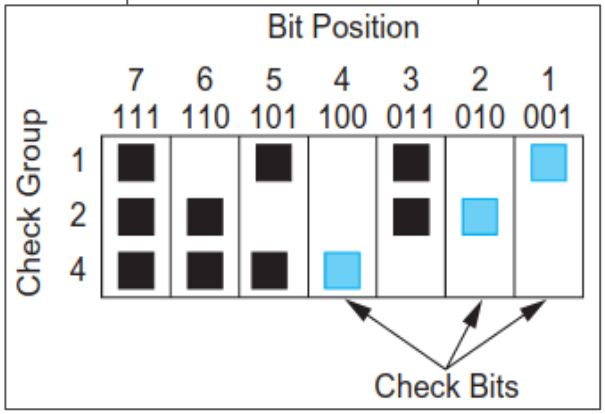

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Bit position		1	2	3	4	5	6	7	8	9	10	11	12
Encoded data bits		p1	p2	d1	p4	d2	d3	d4	p8	d5	d6	d7	d8
Parity bit coverage	p1	X		X		X		X		X		X	
	p2		X	X			X	X			X	X	
	p4				X	X	X	X					X
	p8								X	X	X	X	X

FIGURE 5.23 Parity bits, data bits, and field coverage in a Hamming ECC code for eight data bits.

Source: Computer Organization and Design
The Hardware Software Interface - 2nd Edition - Patterson, Hennessy

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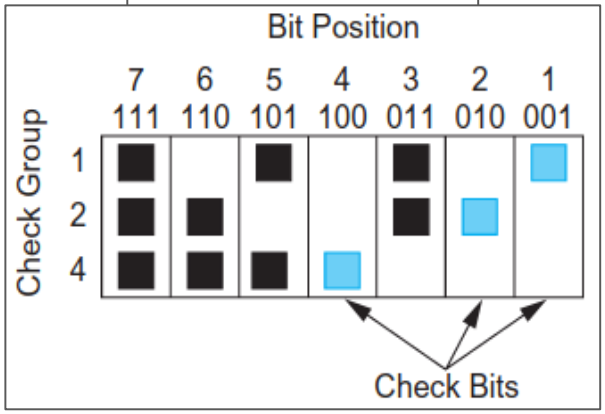

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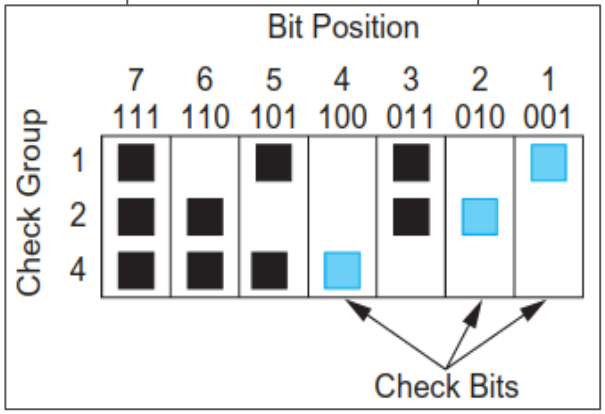

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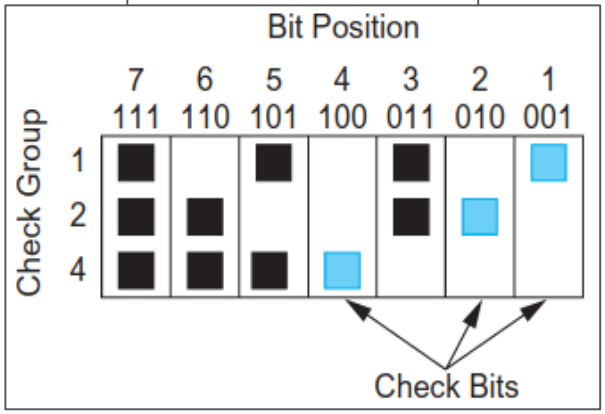

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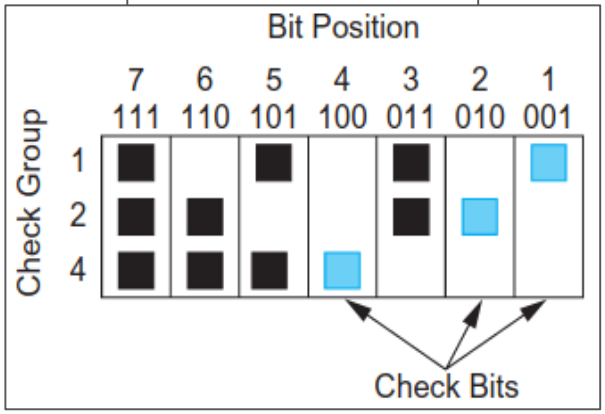

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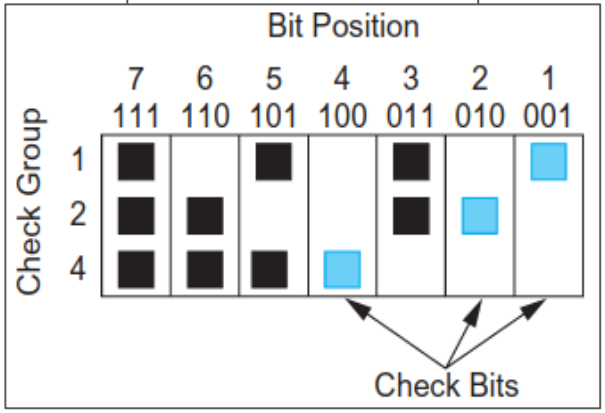

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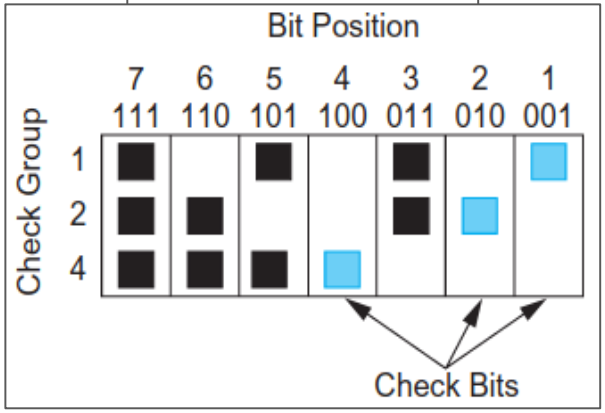

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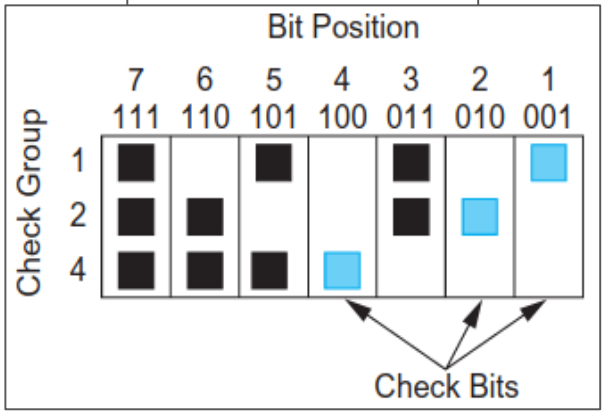

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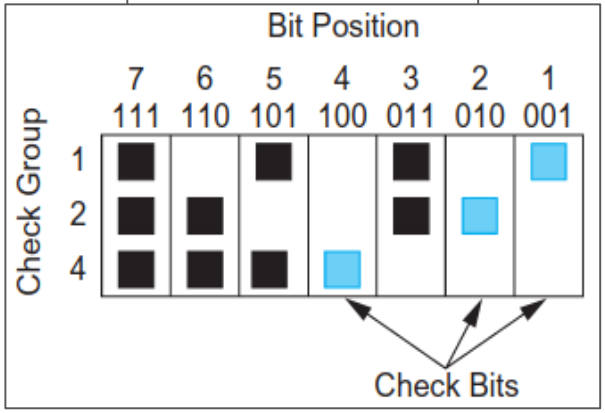

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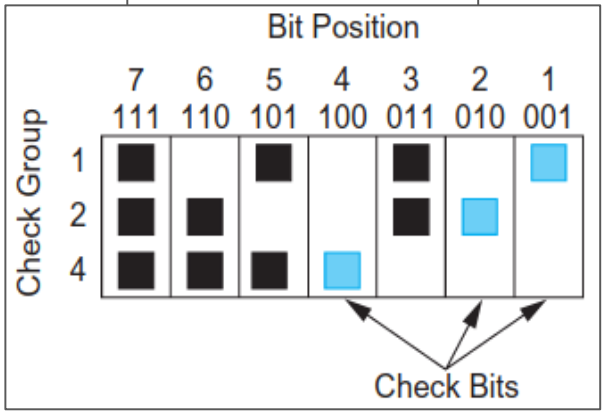

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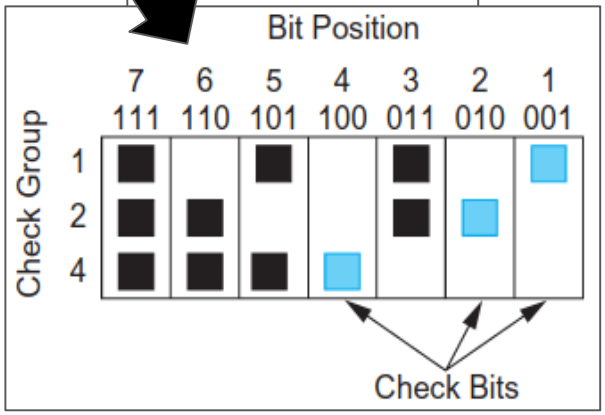

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- XOR-ing the unmodified check bits with the supposed check bits yields the ***<u>SYNDROME: the erroneous bit flipped!!</u>***

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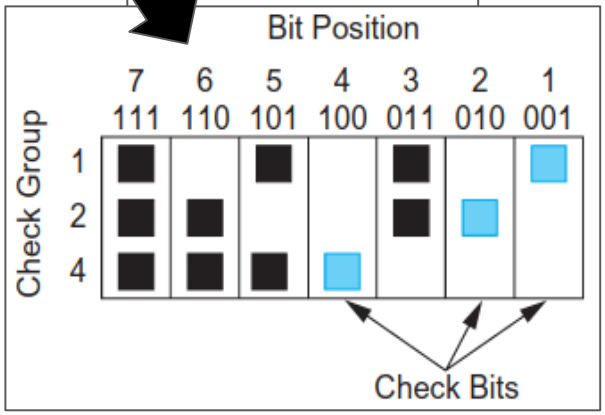

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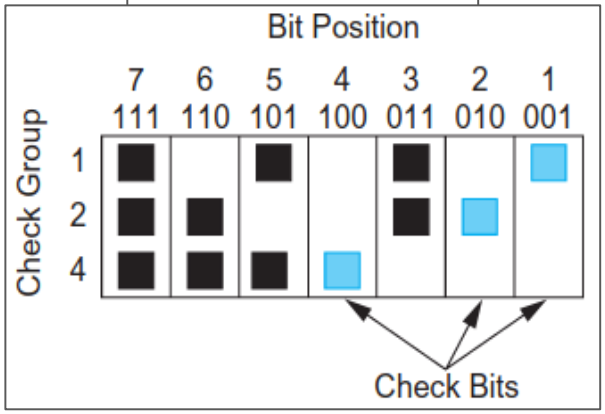

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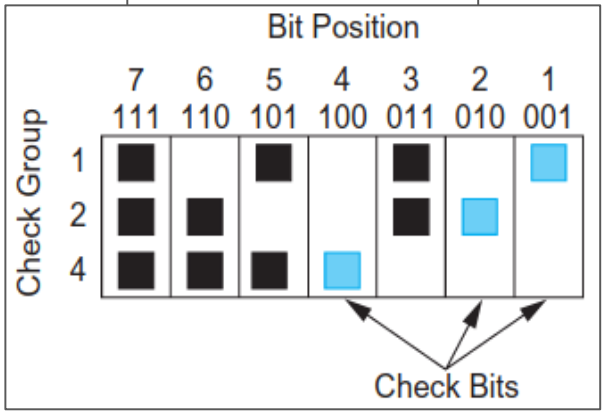

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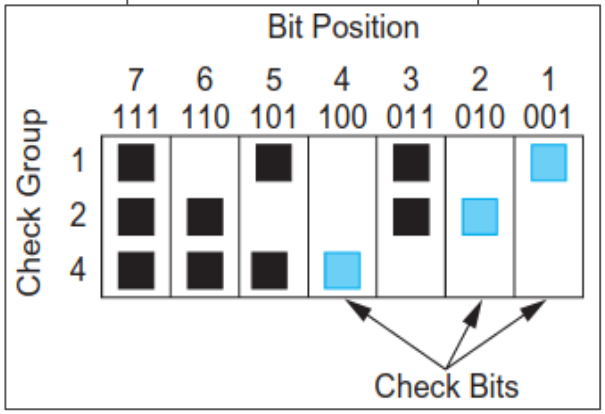

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- If the parity bit of the possibly-erroneous data matches with the supposed parity bit <u>AND</u> the check bits don't match, there has been a double-bit error!

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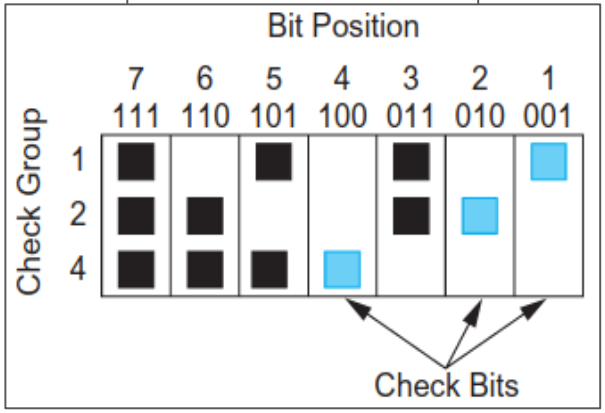

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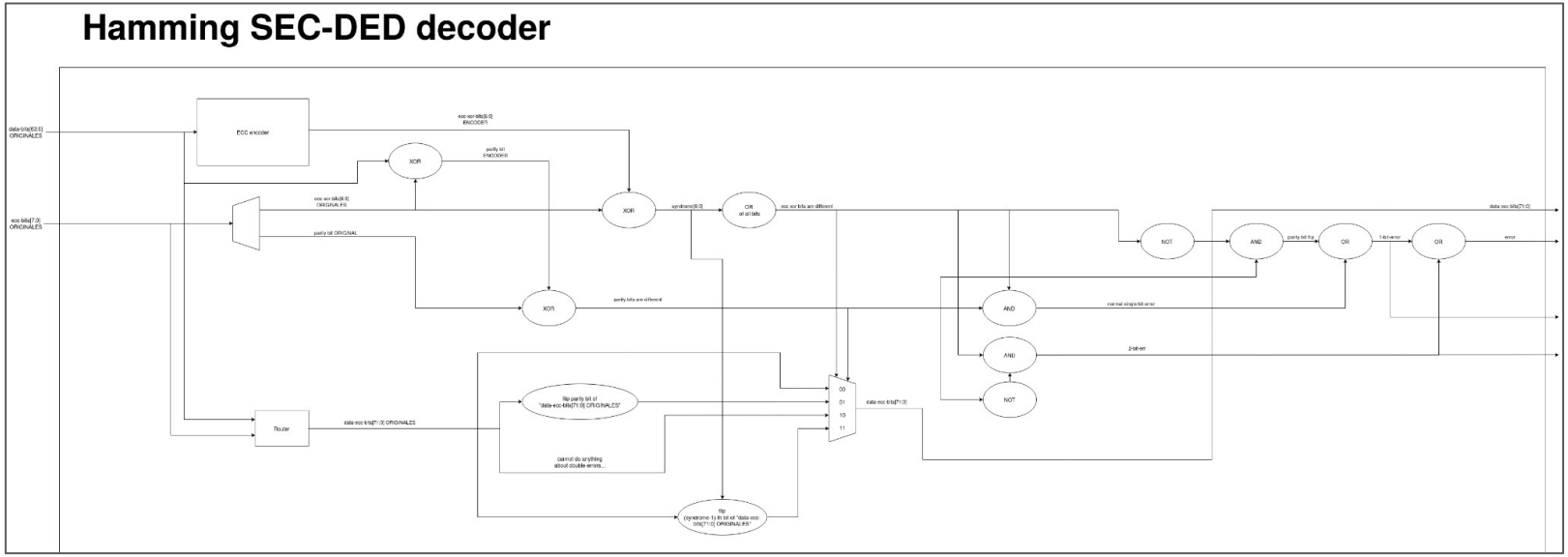
The logic for managing SEC-DED codes is a bit cumbersome…



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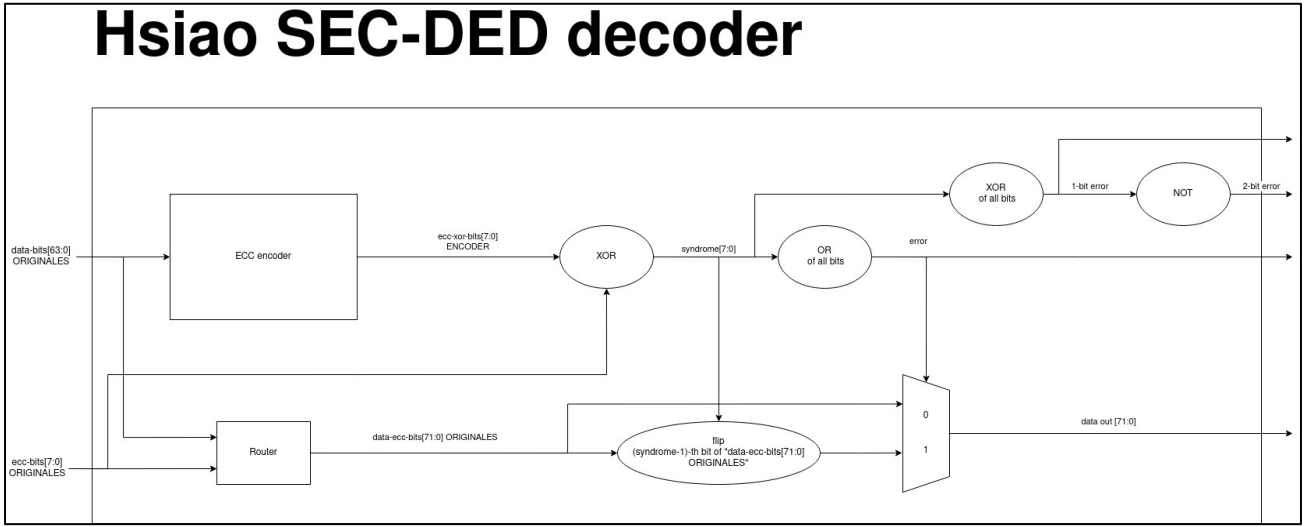

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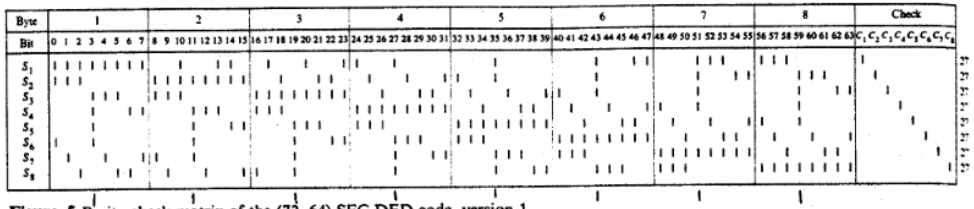
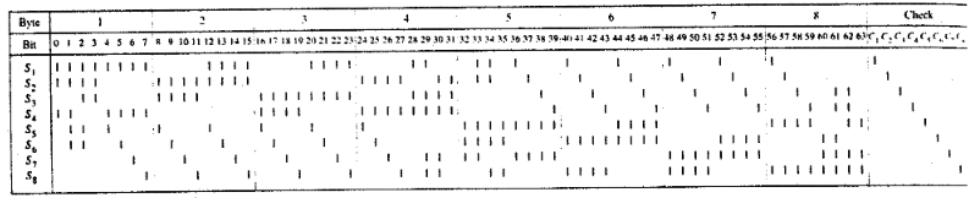


Figure 5 Parity-check matrix of the (72, 64) SEC-DED code, version 1.

Figure 6 Parity-check matrix of the (72, 64) SEC-DED code, version 2.



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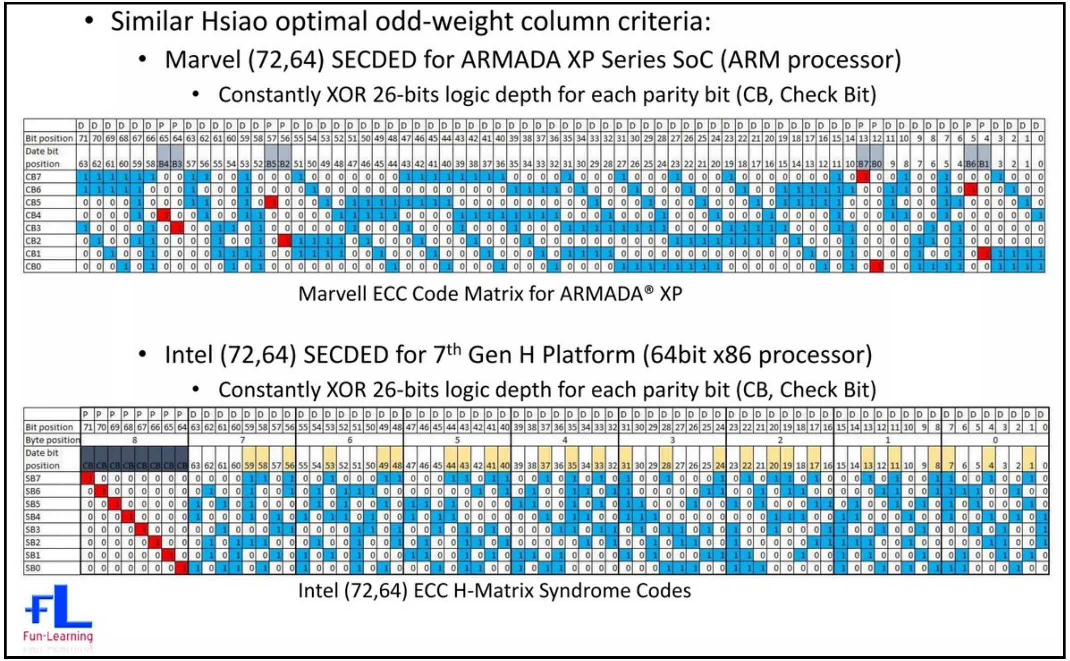
Other check bit patterns also exist…



- Similar Hsiao optimal odd-weight column criteria:
  - Marvel (72,64) SECDED for ARMADA XP Series SoC (ARM processor)
    - Constantly XOR 26-bits logic depth for each parity bit (CB, Check Bit)

	D	D	D	D	D	D	P	P	D	D	D	D	D	D	P	P	D	D
Bit position	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54
Date bit position	63	62	61	60	59	58	B4	B3	57	56	55	54	53	52	B5	B2	51	50
CB7	1	1	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	0
CB6	1	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1
CB5	0	0	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	0
CB4	0	0	0	0	1	0	1	0	0	1	0	0	1	1	0	0	0	0
CB3	1	0	0	0	0	1	0	1	0	0	1	1	0	1	0	0	0	0
CB2	0	1	0	0	1	1	0	0	0	0	1	0	0	1	0	1	1	1
CB1	0	0	1	0	0	1	0	0	0	0	1	1	1	1	0	0	1	1
CB0	0	0	0	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0

	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Bit position	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36
Date bit position	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
CB7	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
CB6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
CB5	1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
CB4	0	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1
CB3	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
CB2	1	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
CB1	1	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
CB0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Bit position	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
Date bit position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14
CB7	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0
CB6	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1
CB5	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	1	1
CB4	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
CB3	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	0
CB2	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
CB1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CB0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0

	D	D	D	D	P	P	D	D	D	D	D	D	P	P	D	D	D	D
Bit position	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Date bit position	13	12	11	10	B7	B0	9	8	7	6	5	4	B6	B1	3	2	1	0
CB7	0	0	1	0	1	0	0	1	0	0	1	0	0	0	1	0	0	0
CB6	1	1	1	1	0	0	1	1	0	0	1	0	1	0	0	1	0	0
CB5	1	1	1	0	0	0	1	0	0	0	1	1	0	0	0	0	1	0
CB4	0	0	1	0	0	0	1	1	0	0	1	0	0	0	0	0	0	1
CB3	0	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0
CB2	0	0	0	1	0	0	0	0	1	1	0	1	0	0	0	0	0	0
CB1	1	0	0	1	0	0	0	0	1	0	0	1	0	1	1	1	1	1
CB0	0	1	0	1	0	1	0	0	1	1	1	1	0	0	1	1	1	1

Marvell ECC Code Matrix for ARMADA® XP

- Intel (72,64) SECDED for 7th Gen H Platform (64bit x86 processor)
  - Constantly XOR 26-bits logic depth for each parity bit (CB, Check Bit)

	P	P	P	P	P	P	P	P	D	D	D	D	D	D	D	D	D	D
Bit position	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54
Byte position	8								7								6	
Date bit position	CB	CB	CB	CB	CB	CB	CB	CB	63	62	61	60	59	58	57	56	55	54
SB7	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
SB6	0	1	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	1
SB5	0	0	1	0	0	0	0	0	1	0	1	0	1	0	0	0	0	1
SB4	0	0	0	1	0	0	0	0	1	0	0	0	1	0	1	0	1	0
SB3	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	1	0	0
SB2	0	0	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0	1
SB1	0	0	0	0	0	0	1	0	0	1	0	1	0	0	1	0	1	0
SB0	0	0	0	0	0	0	0	1	1	0	1	1	0	1	0	0	1	0

	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Bit position	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36
Byte position							5								4			
Date bit position	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36
SB7	1	0	0	0	1	1	0	0	0	1	1	0	1	1	0	0	1	0
SB6	0	1	1	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0
SB5	0	1	0	0	1	0	1	1	0	1	0	0	0	0	1	1	0	0
SB4	1	1	0	1	0	0	1	0	1	1	0	0	0	0	0	0	1	0
SB3	0	0	1	1	0	1	0	0	1	0	1	0	1	0	0	0	0	1
SB2	0	0	1	0	0	1	0	1	0	0	1	1	0	1	0	0	0	0
SB1	1	0	1	0	0	0	1	1	0	0	1	0	1	0	1	1	0	1
SB0	0	0	1	0	1	0	0	0	1	0	1	1	0	0	1	0	1	1

	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Bit position	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
Byte position					3								2					
Date bit position	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
SB7	1	0	1	0	1	0	0	1	0	0	0	1	0	1	0	1	1	0
SB6	1	1	0	1	1	0	0	0	0	0	1	1	0	0	1	0	1	1
SB5	1	0	1	0	1	1	0	0	0	1	0	0	1	0	1	0	0	0
SB4	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1
SB3	1	0	1	1	0	1	0	1	1	0	1	0	1	0	0	1	0	0
SB2	0	1	0	1	0	0	1	0	1	1	0	0	1	0	0	0	0	0
SB1	0	0	0	0	1	0	1	0	0	0	1	1	1	1	0	0	0	1
SB0	0	0	0	0	0	0	0	1	1	1	0	0	1	1	1	0	0	0

	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Bit position	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Byte position			1								0							
Date bit position	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SB7	1	0	0	0	1	0	1	0	0	1	1	0	0	1	0	0	1	0
SB6	0	0	0	0	0	1	1	0	0	1	1	1	1	0	0	1	0	0
SB5	1	1	0	1	0	0	1	0	1	0	1	0	1	0	0	0	1	0
SB4	0	0	1	1	0	0	0	1	0	0	1	0	0	1	0	1	0	1
SB3	0	1	1	0	0	1	0	0	1	0	0	0	1	0	1	0	0	1
SB2	1	1	1	1	1	0	0	1	0	0	0	0	0	1	1	0	0	1
SB1	0	0	1	0	1	0	0	0	1	0	0	1	0	0	1	0	1	0
SB0	0	0	1	0	0	1	0	1	0	1	1	1	0	0	0	1	0	0

Intel (72,64) ECC H-Matrix Syndrome Codes

Fun-Learning

Fundamentals of Error Correction Codes (ECC)

Sources:

CMOS VLSI Design: A Circuits and Systems Perspective - 4th Edition - Weste, Harris

→ pages 468-470

→ pages 543-544

Computer Organization and Design: The Hardware Software Interface - 2nd RISC-V Edition - Patterson, Hennessy

→ pages 433-436

→ pages A-(64-66)

https://people.eecs.berkeley.edu/~culler/cs252-s02/papers/hsiao70.pdf

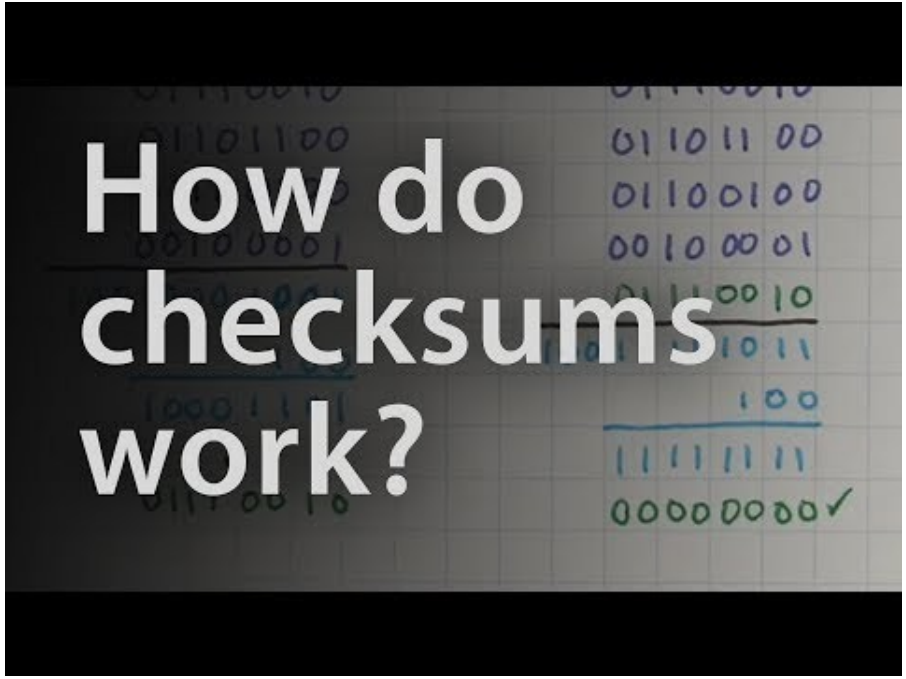
https://www.slideshare.net/SkCheah/memory-ecc-the-comprehensive-of-secded

Fundamentals of Error Correction Codes (ECC)

Video by Ben Eater:

Checksums and Hamming distance

https://www.youtube.com/watch?v=ppU41c15Xho

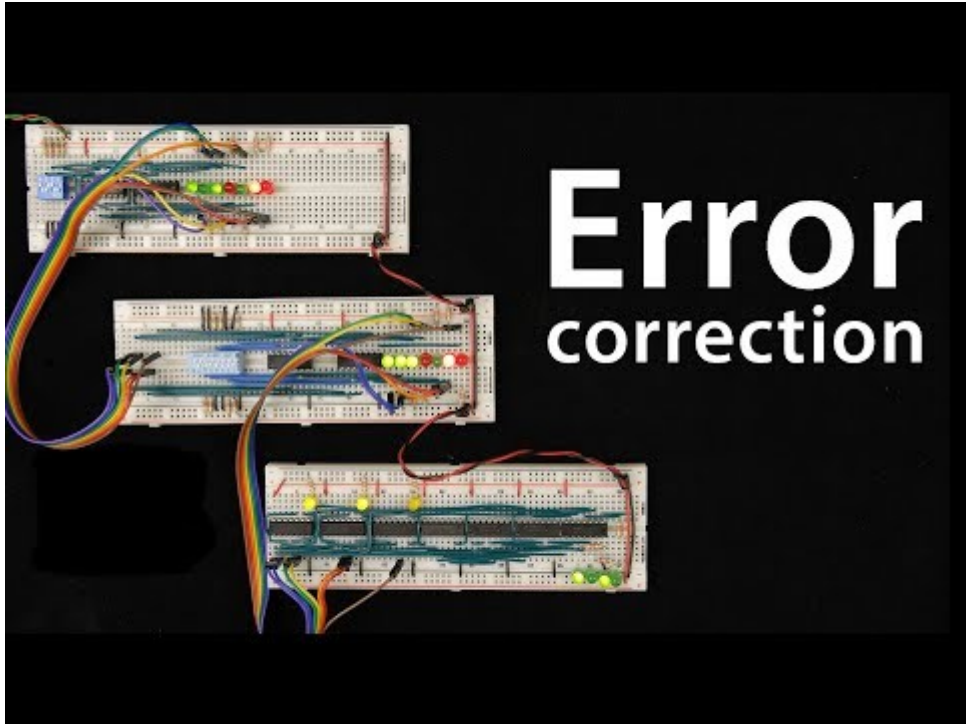


Fundamentals of Error Correction Codes (ECC)

Video by Ben Eater:

What is error correction? Hamming codes in hardware

https://www.youtube.com/watch?v=h0jloehRKas

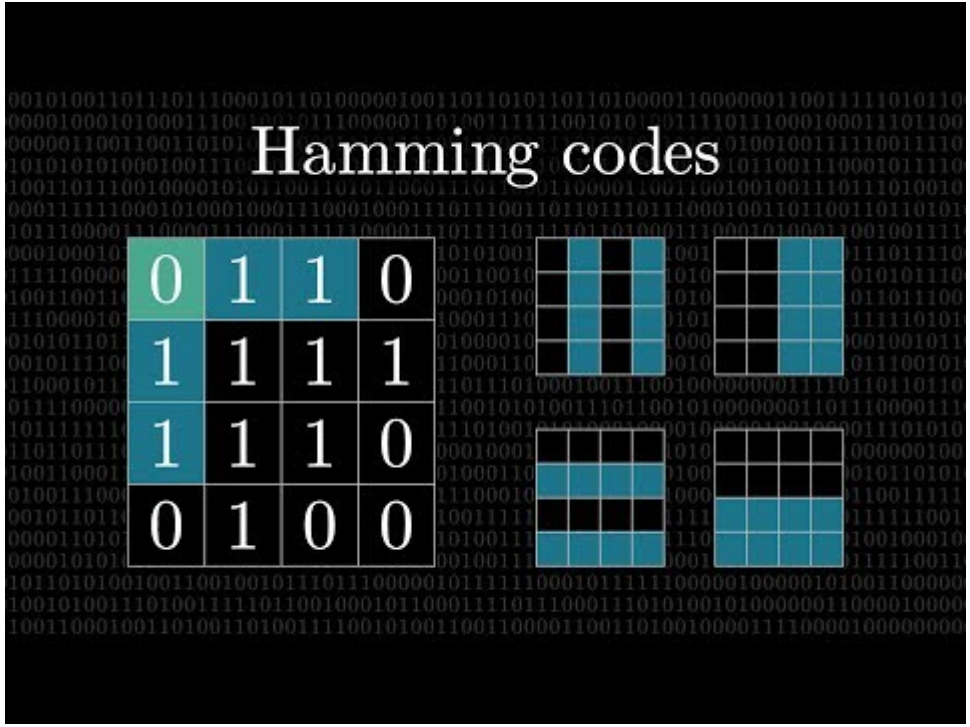


Fundamentals of Error Correction Codes (ECC)

Video by 3Blue1Brown (more math-related):

How to send a self-correcting message (Hamming codes)

https://www.youtube.com/watch?v=X8jsijhllIA

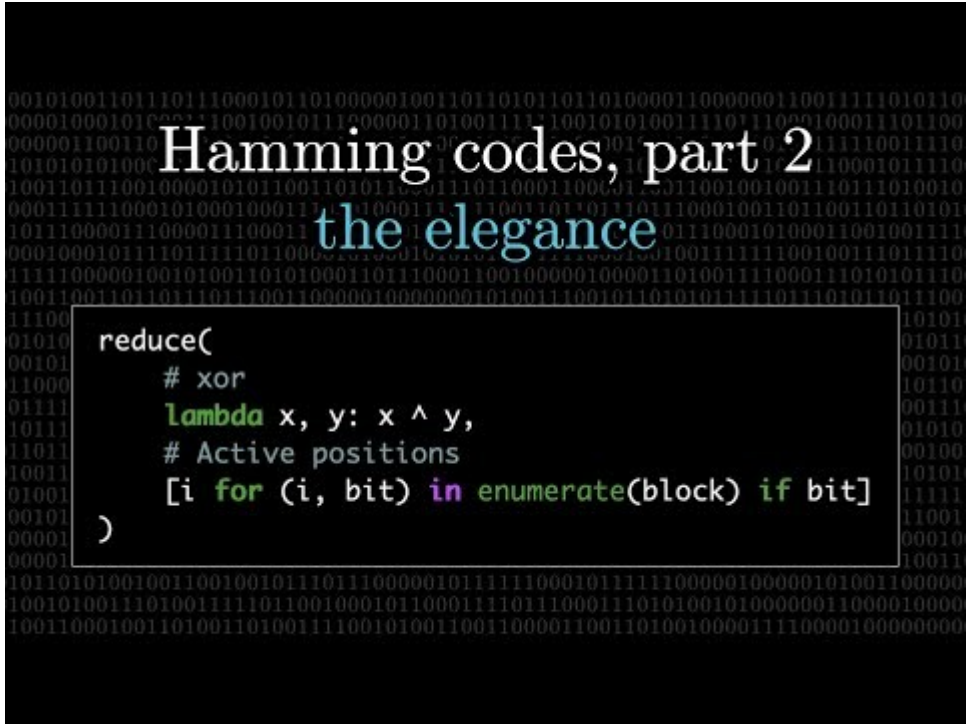


Fundamentals of Error Correction Codes (ECC)

Video by 3Blue1Brown (more math-related):

Hamming codes part 2, the elegance of it all

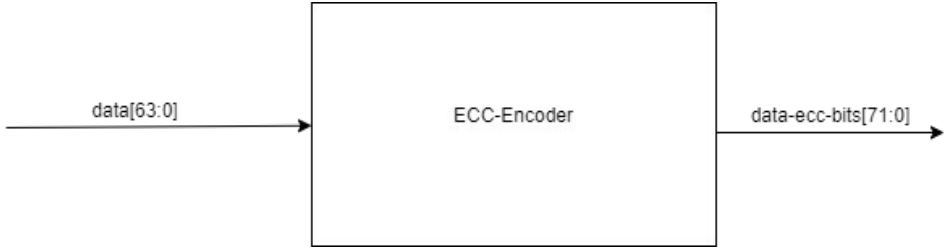
https://www.youtube.com/watch?v=b3NxrZOu_CE



Modules for implementing and testing ECC functionalities

Encoder

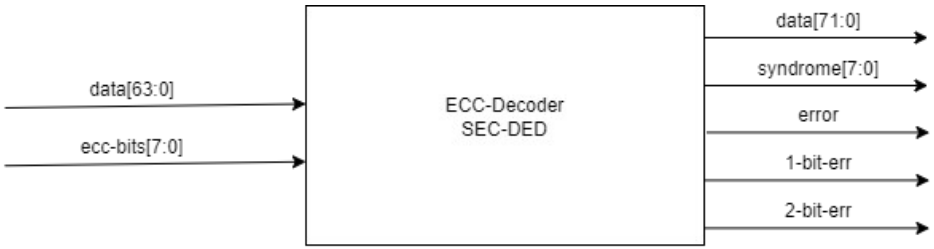
- Generate ECC bits
- Hsiao algorithm

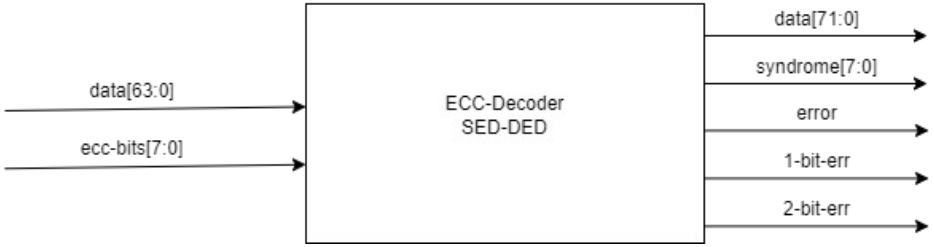


Modules for implementing and testing ECC functionalities

Decoder

- Recalculate syndrome
- Detect/Correct 1-bit errors
- Detect 2-bit errors
- Error signals





Modules for implementing and testing ECC functionalities

Fault Injector

- Functionality test
- Inject errors
  - No error
  - 1-bit error
  - 2-bit error
  - Random

Where ECC modules should go in Ariane

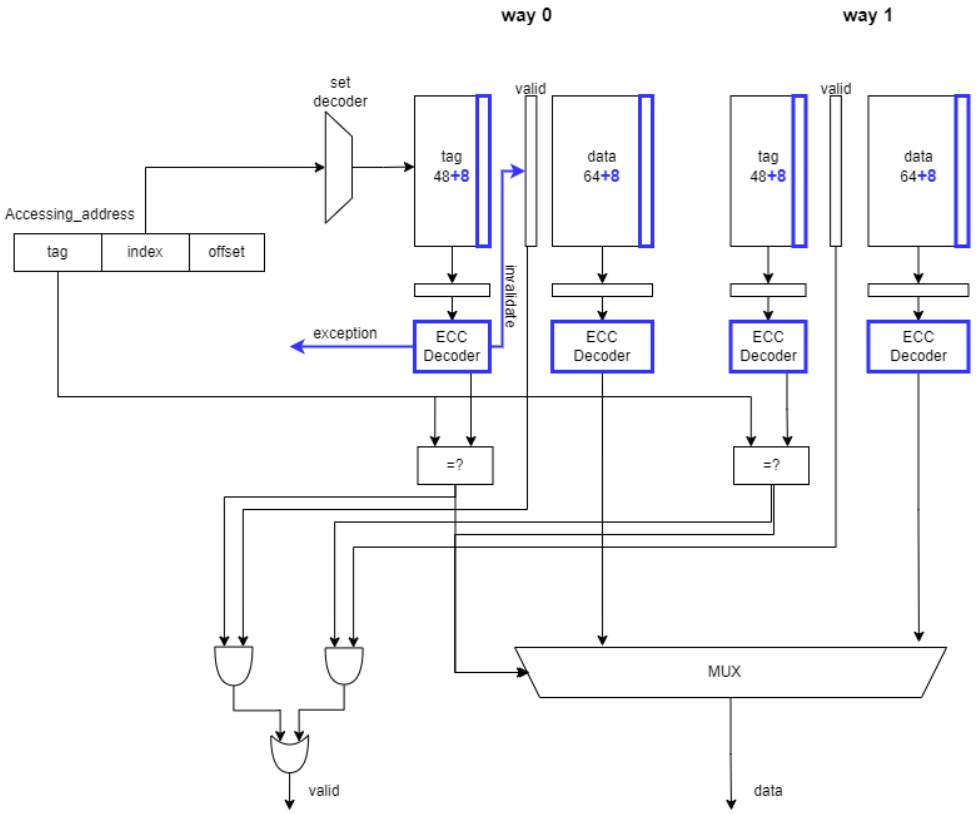
Ariane cache

- 8-way 32 KB associative cache with 16 byte line sizes
- write-back with no write allocation

Where ECC modules should go in Ariane

Simple implementation

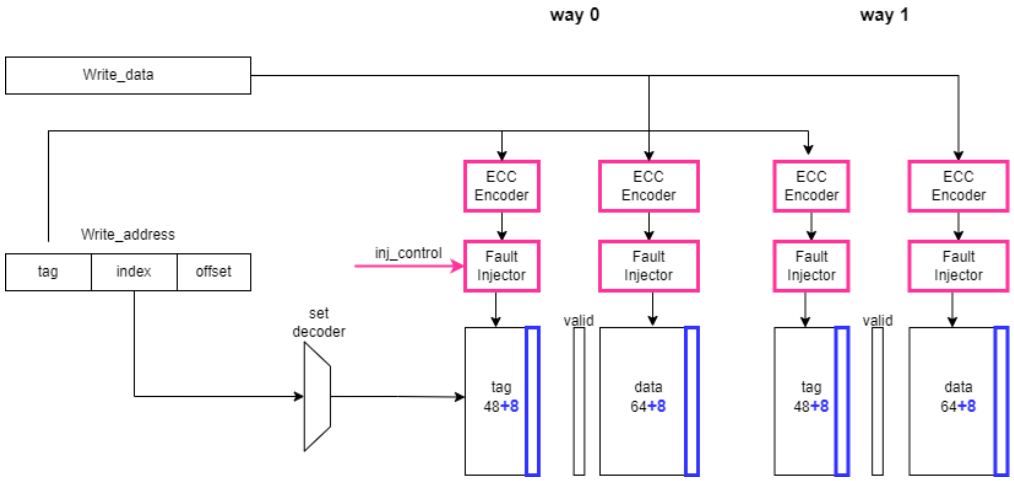
- Extend tag and data sizes to store ecc bits
- Insert Decoder to correct single bit errors
- Connect output signals to invalidate or launch exception in case of double bit errors



Where ECC modules should go in Ariane

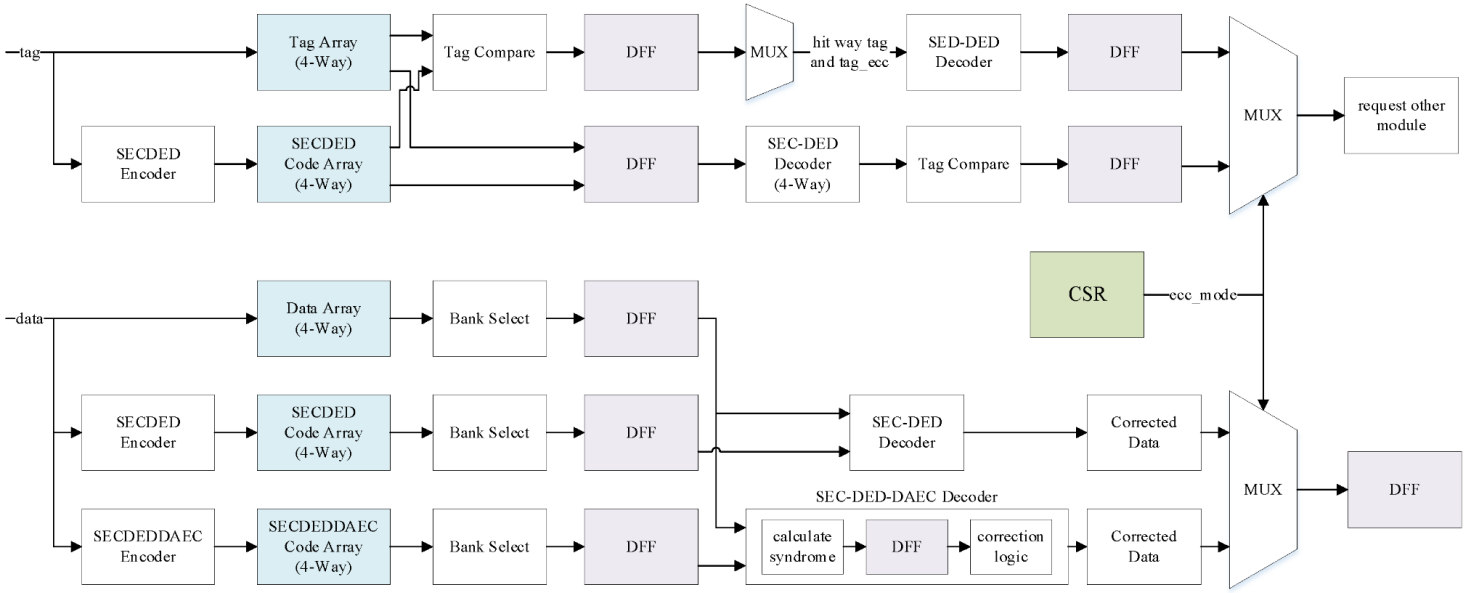
Testing implementation

- Insert Encoder to simulate ECC in top-level cache
- Insert Fault Injector to simulate errors



Where ECC modules should go in Ariane

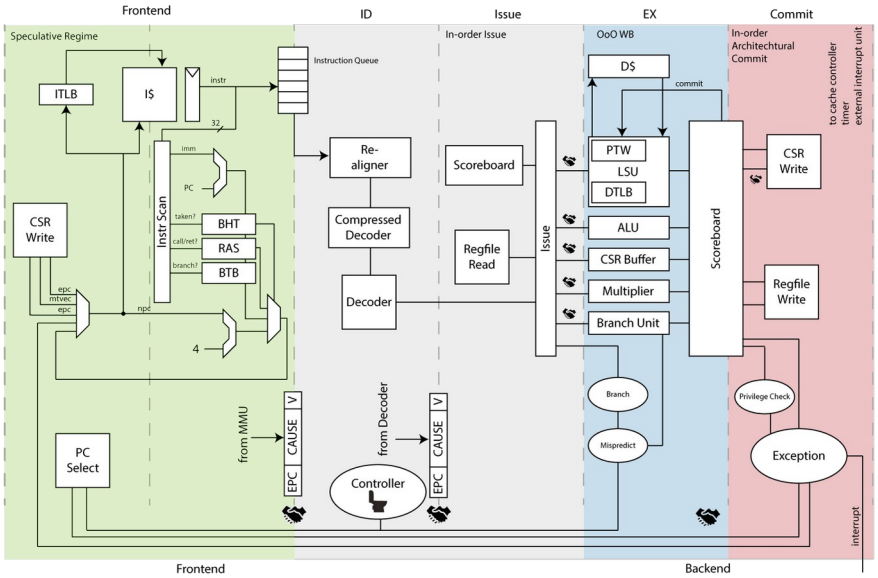
Actual High-End implementation example



Zhou, Y.; Liu, H.; Xiang, Q.; Yin, C. High-Performance and Flexible Design Scheme with ECC Protection in the Cache. *Micromachines* **2022**, *13*, 1931. https://doi.org/10.3390/mi13111931

Implementation details

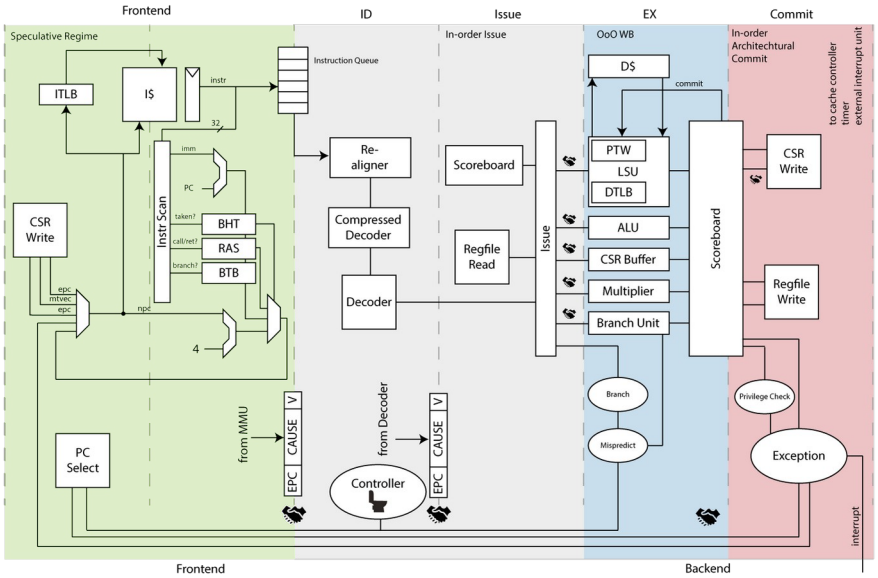
- The Ariane processor (now called CVA6) is one of the seven RISC-V cores developed and maintained by OpenHW Group



CVA6 diagram, from https://github.com/openhwgroup/cva6

Implementation details

- The Ariane processor (now called CVA6) is one of the seven RISC-V cores developed and maintained by OpenHW Group
- Their projects include (all of them “open source”):
  - Two application-class cores in CVA5 and CVA6 (with M, S, U privilege levels for operating system support and the like)
  - Five smaller embedded cores in CV32E40{P,X,S}, CV32E41P and CVE2



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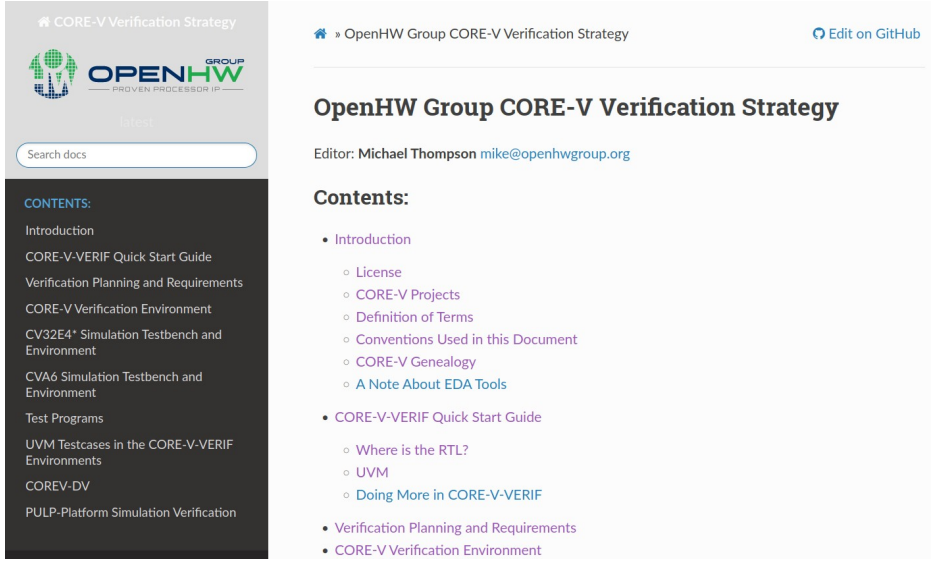
- OpenHW Group maintain separate Github repositories for the RTL and their corresponding verification scripts and utilities



Source: [core-v-verif readthedocs page]

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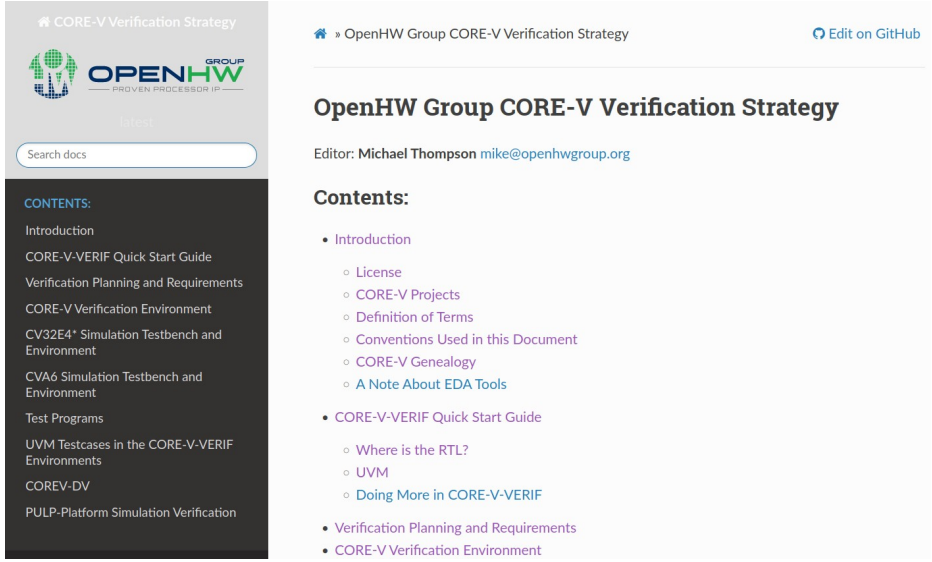
- Source code and RTL for CVA6 in https://github.com/openhwgroup/cva6



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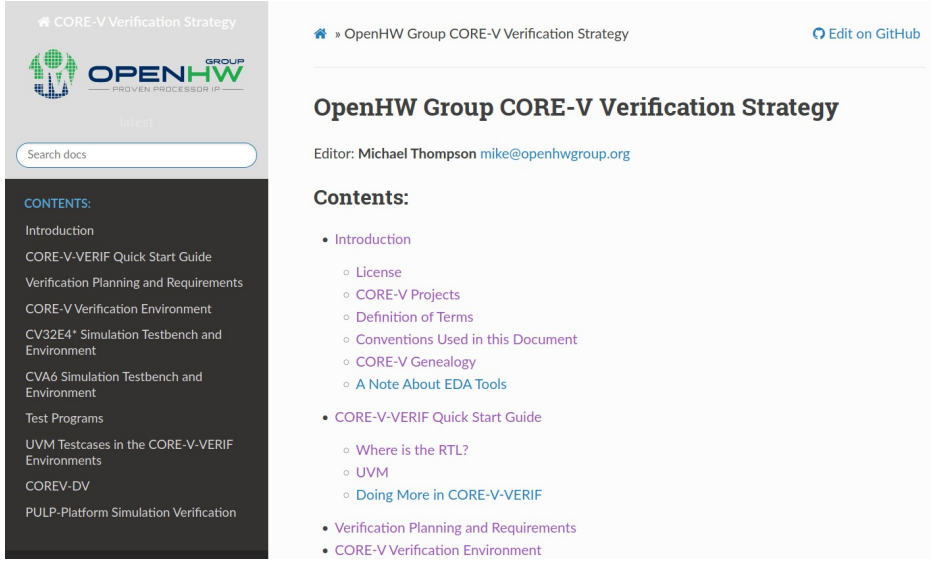
- In the [core-v-verif](https://github.com/openhwgroup/core-v-verif) repository resides the verification part of all the cores
  - CV32E40P core is the more mature and stable of the projects
  - Others not so much, varying levels of progress…



Source: [core-v-verif readthedocs page](https://core-v-verif.readthedocs.io/)

Implementation details

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Source: [core-v-verif readthedocs page]

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- Depending on the type of bit flip introduced (either no errors, single-bit errors or double-bit errors), the results for any and all testbenches are easily predictable
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Also, waveform files from each testbench!!!

Much better and comprehensive than anything we could conceive of…

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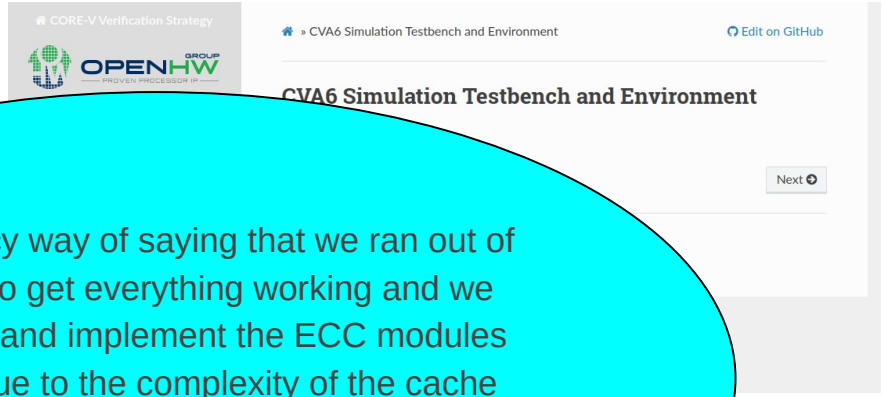
  - A lot of tinkering with Verilator
  - Little time for source-code spelunking

- Our final report consists of a 30-page tutorial on how to modify and “fix” the CVA6 and the core-v-verif repositories to obtain waveform files for all the compliance and instruction tests of the processor, as well as a brief explanation of the cache subsystem within CVA6

Implementation details

Integration-hell bullet points:

- All this results in:
  - Basic tutorials in the documentation not working
  - Modifications to Makefiles and other scripts
  - A lot of tinkering with Verilator
  - Little time for source-code spelunkin
- Our final report consists of a 2
  on how to modify and “fix” t
  core-v-verif repositories to
  files for all the compliance a
  of the processor, as well as a
  of the cache subsystem within C



This is a fancy way of saying that we ran out of time trying to get everything working and we couldn’t test and implement the ECC modules ourselves due to the complexity of the cache subsystem code, but hopefully our findings and explorations save some time for future students that also want to work with the CVA6 processor, either ECC-wise or with other modules…

Questions?