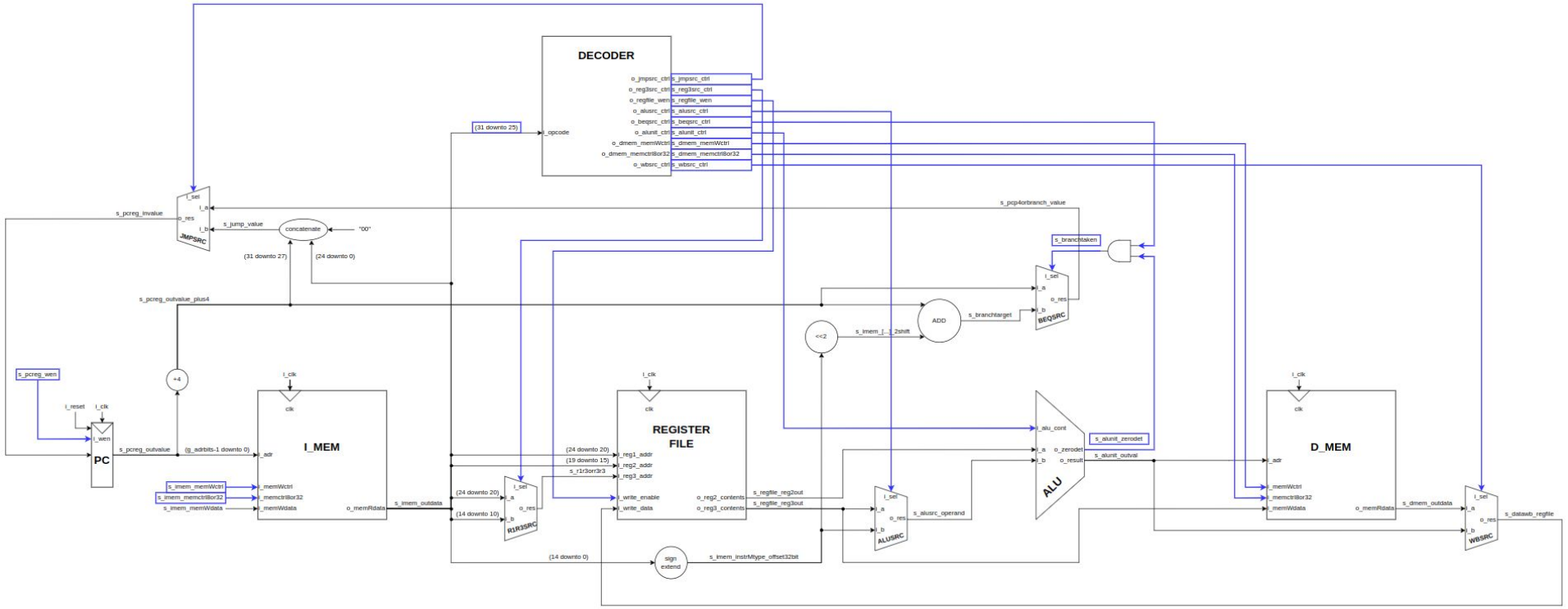
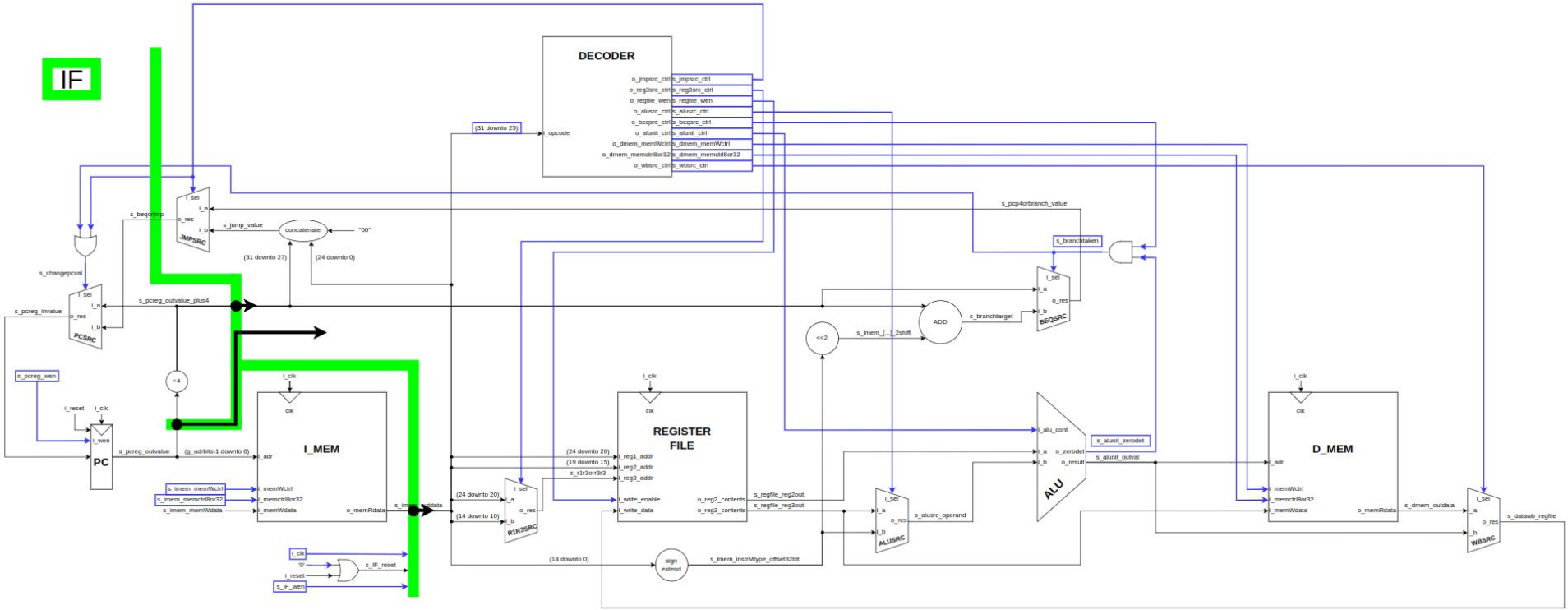
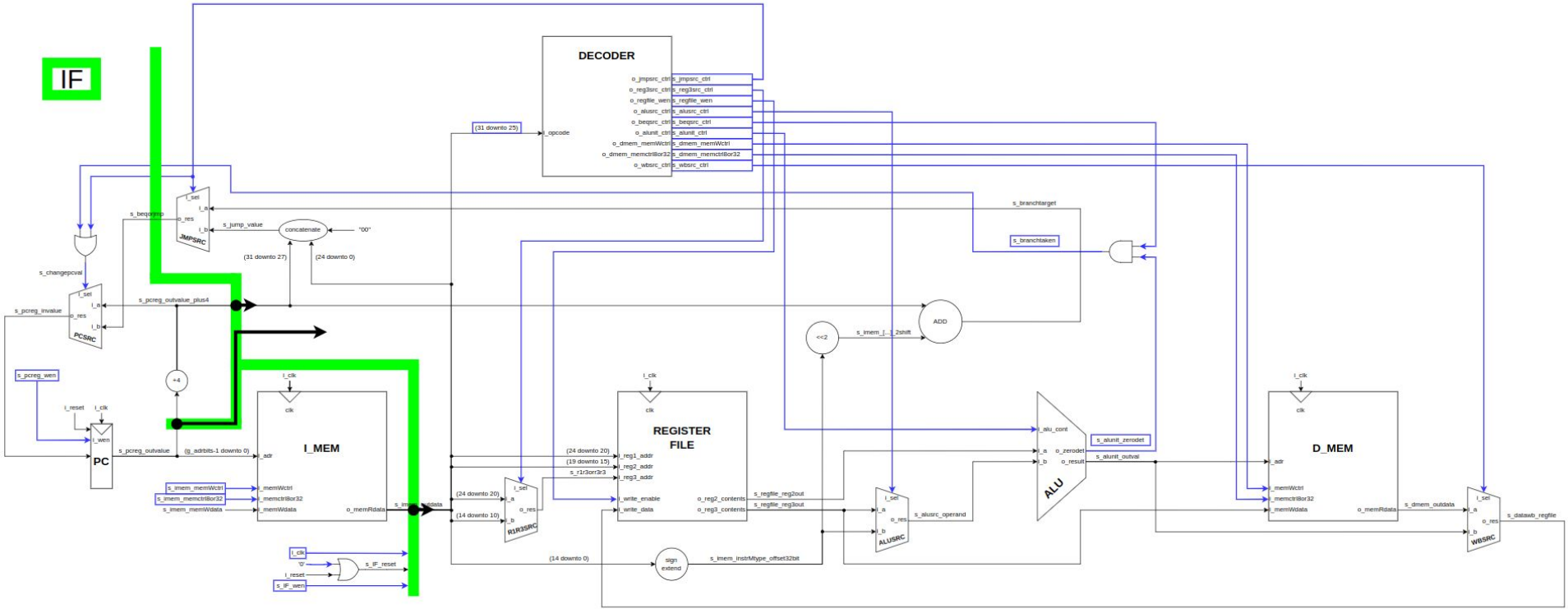
Base processor, single cycle



Instruction-fetch stage, beware PCSRC and BEQSRC muxes…



Instruction-fetch stage, beware PCSRC and BEQSRC muxes…



Thick dots/arrows indicate presence of inter-stage registers for given value/signal

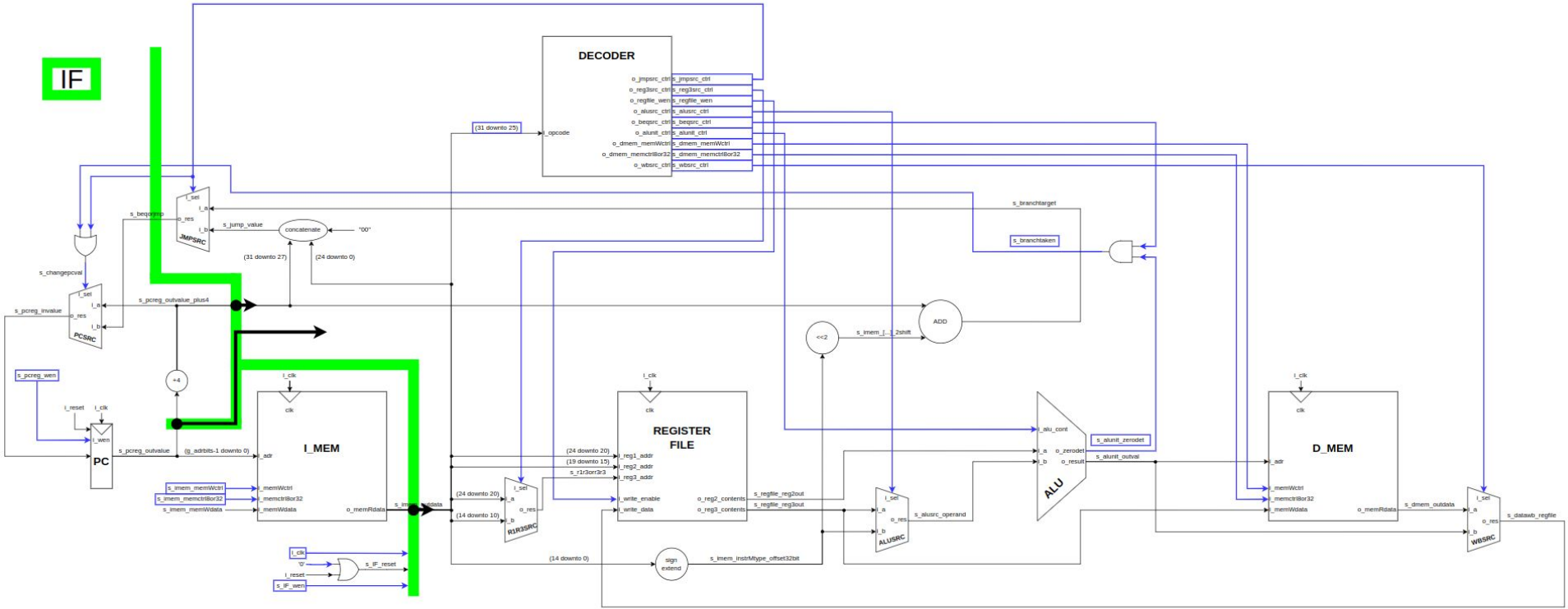
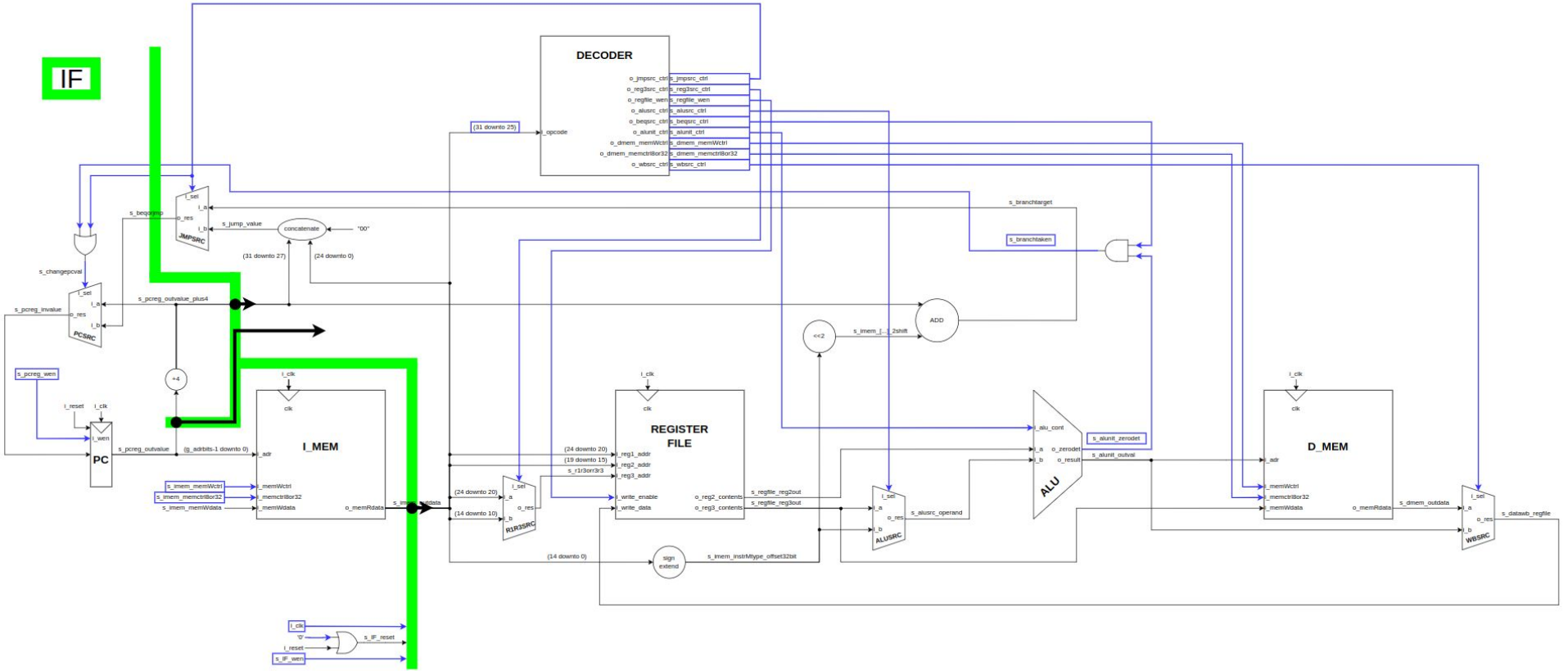
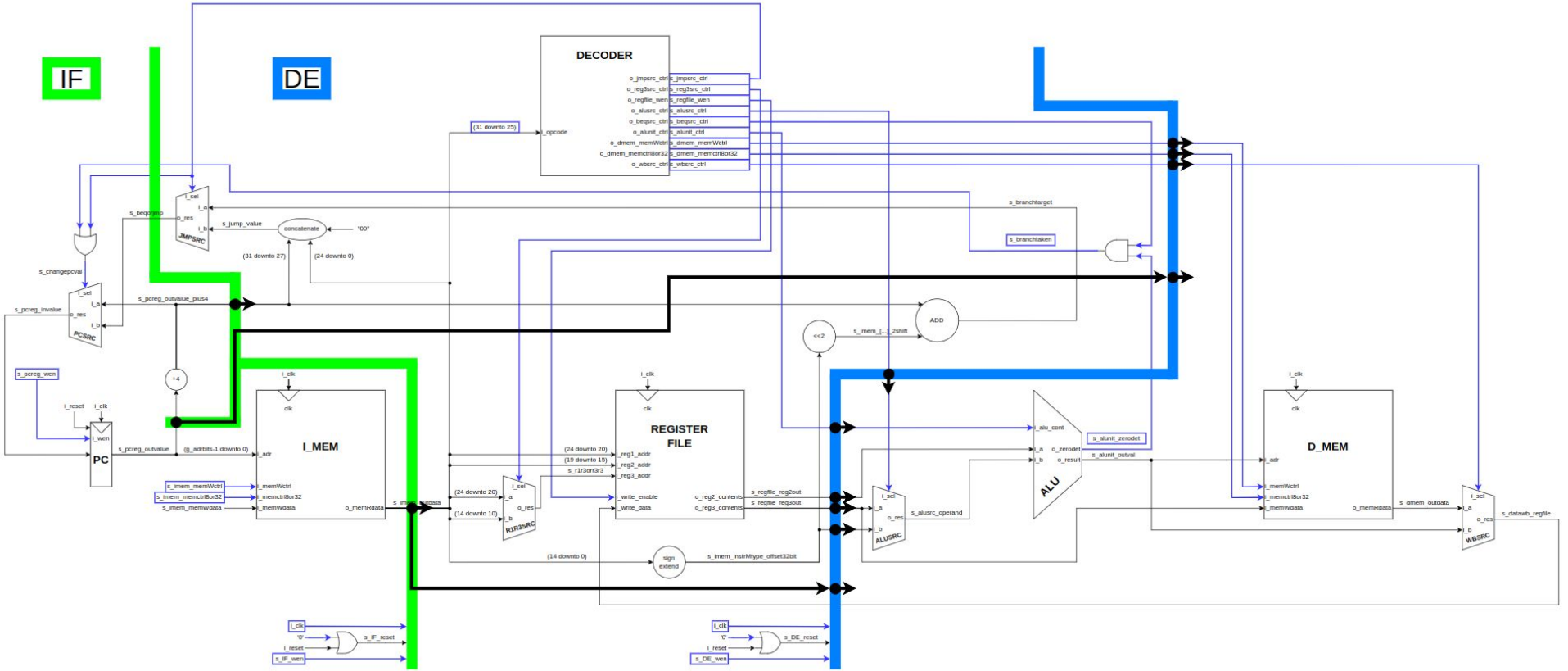


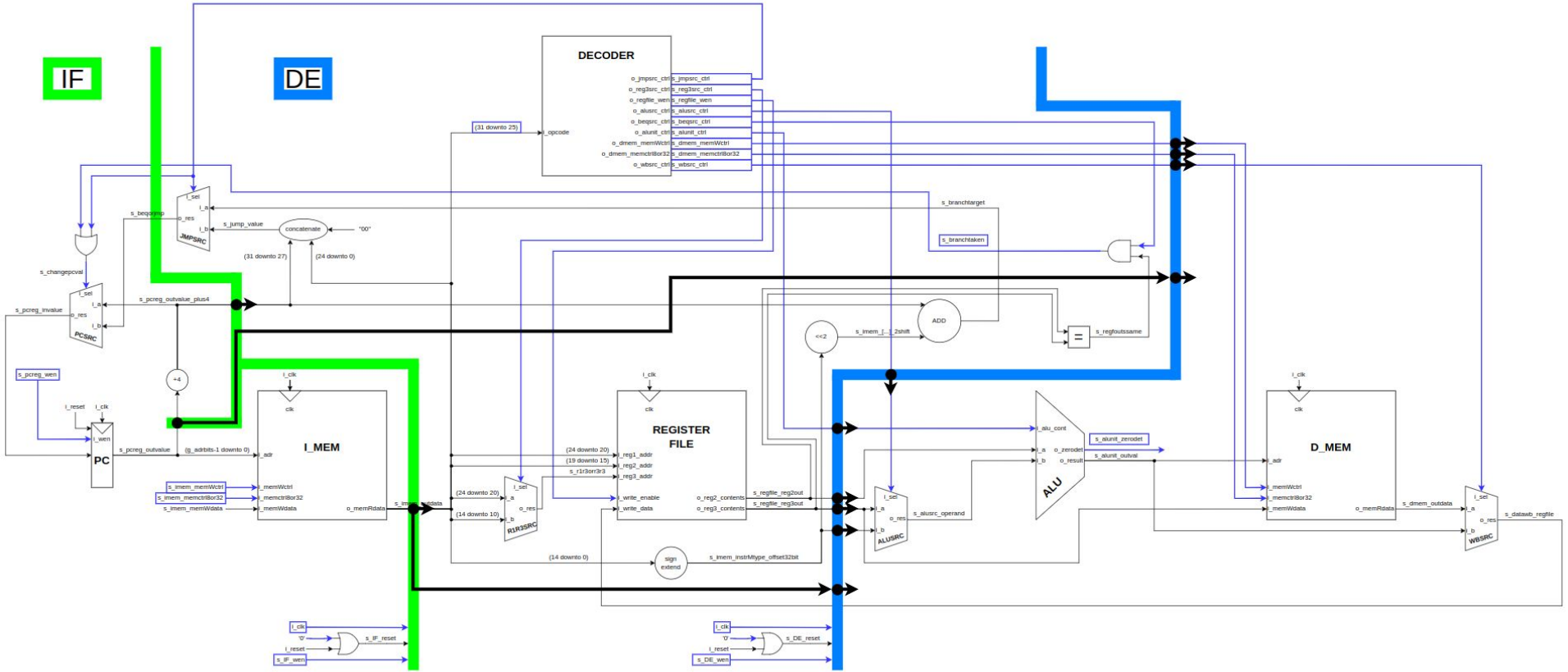
Diagram will get *bigger*, more room at bottom



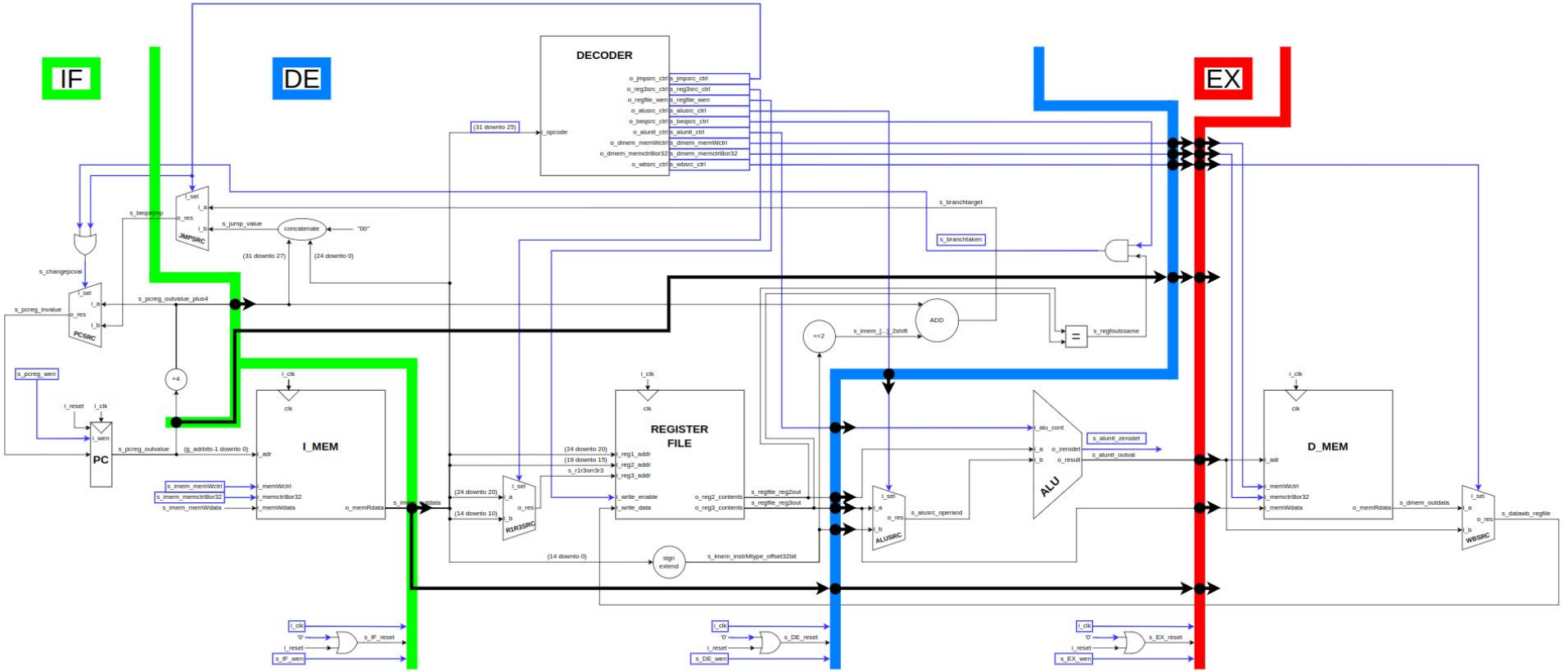
Decode stage, some values from IF to DE and from DE to next stage too



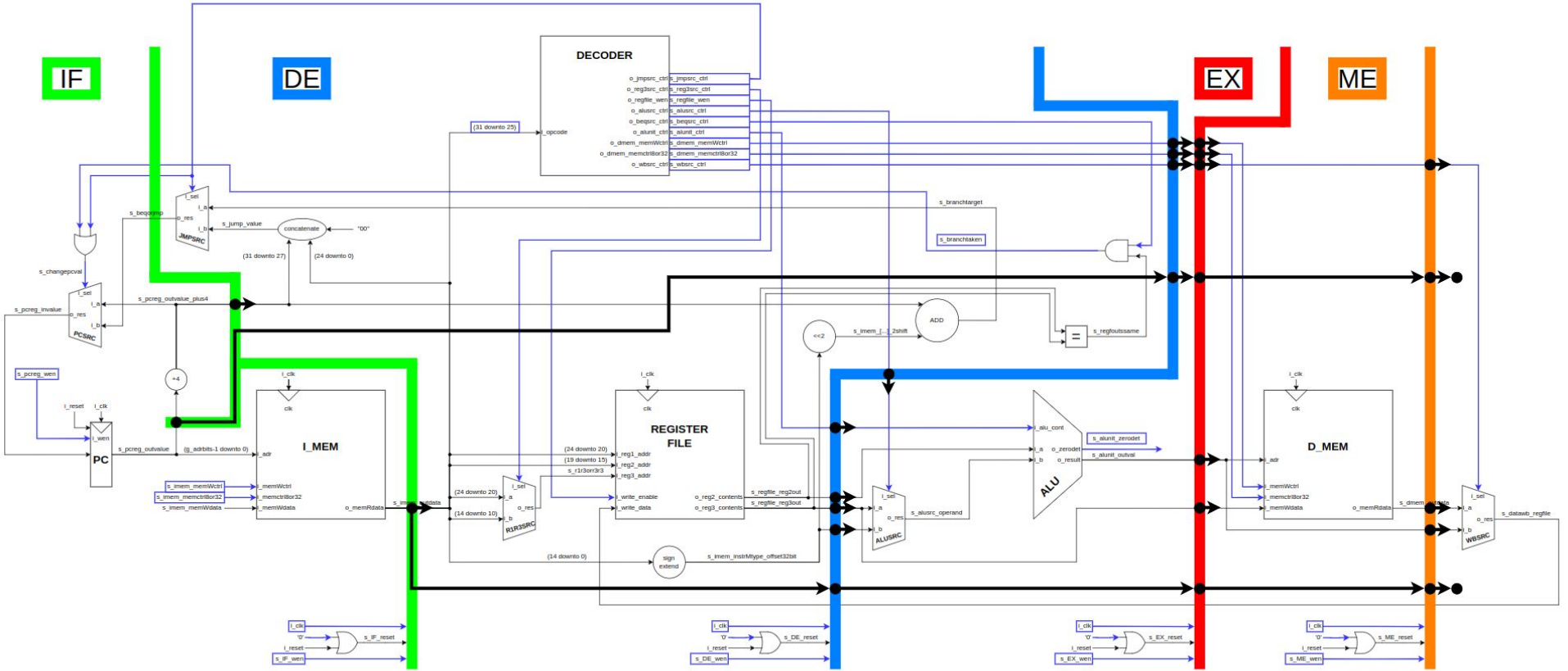
Early branch resolution, branches are resolved as taken/not at DE stage (LOL)



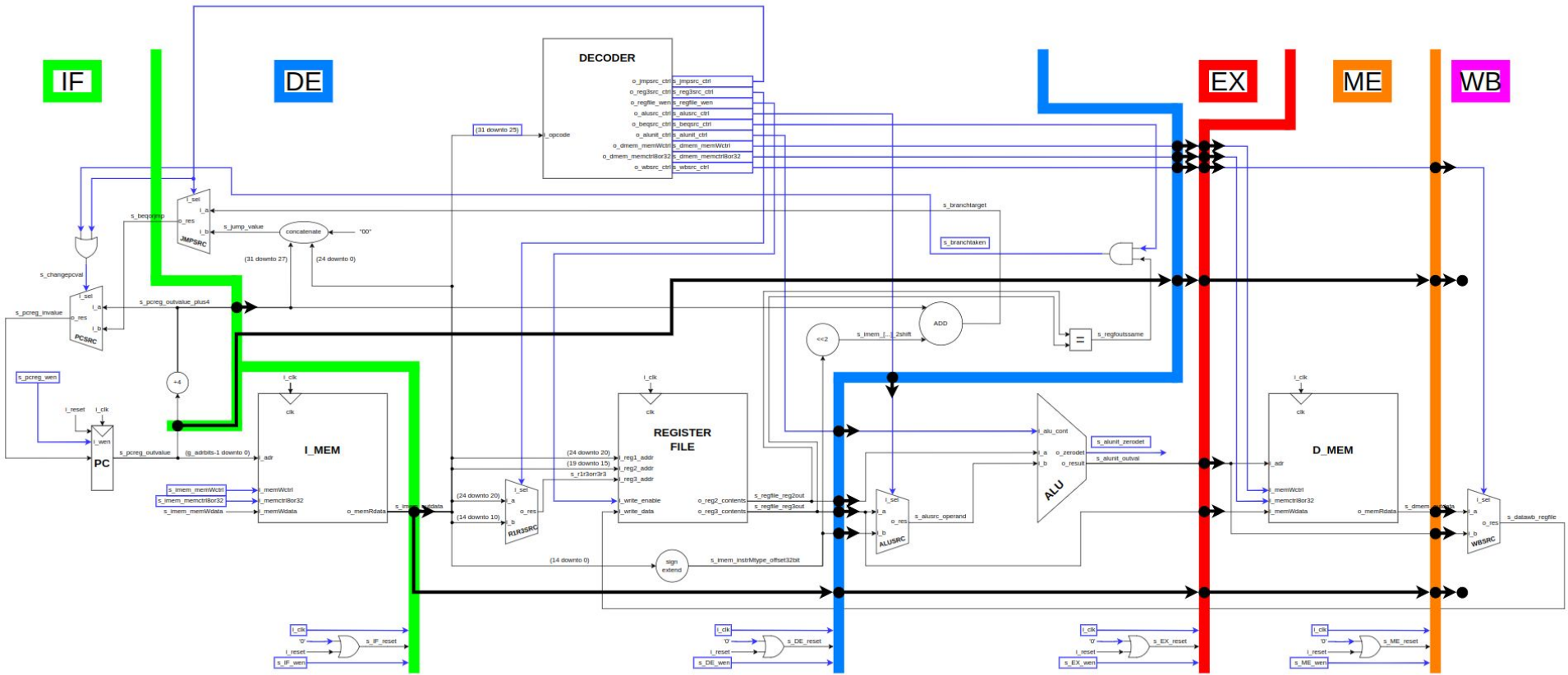
Execution stage, some more values from DE to EX and from EX to next stage



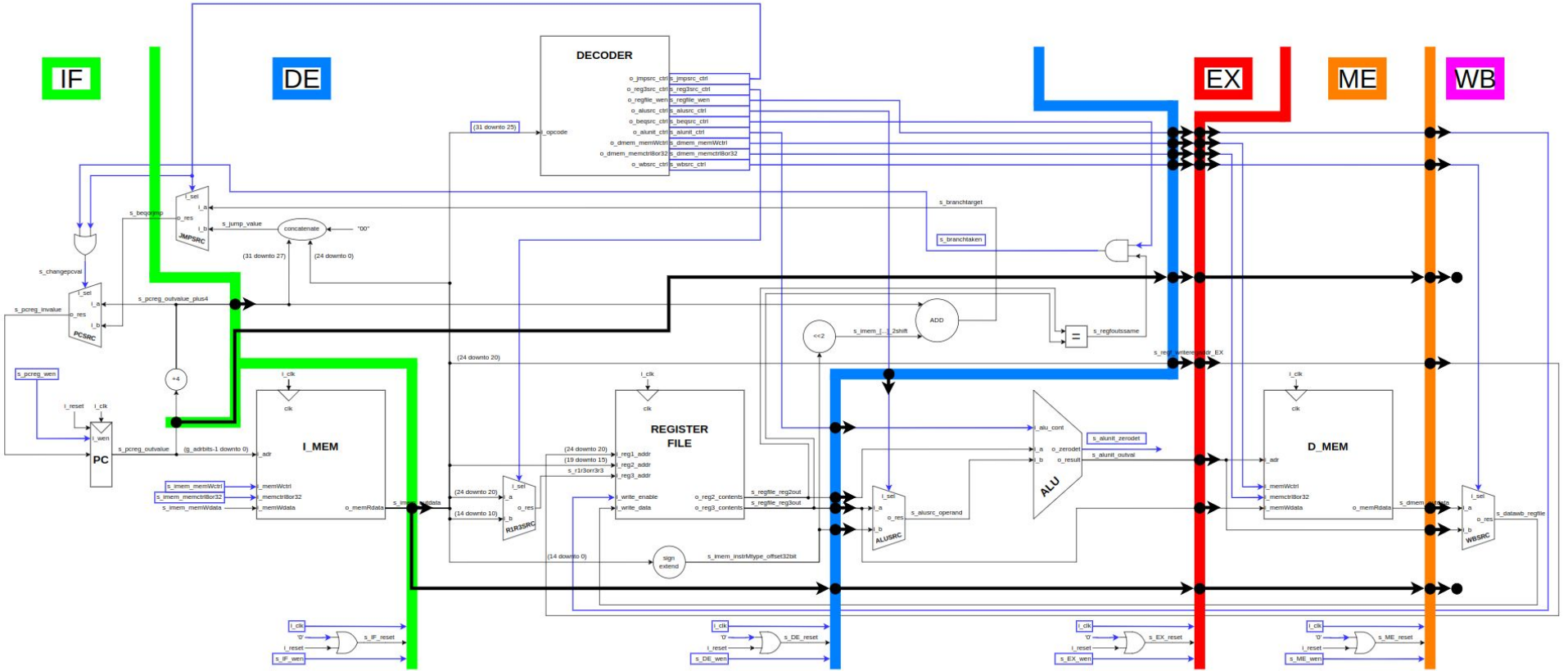
Memory stage, some more values from EX to ME and from ME to next stage



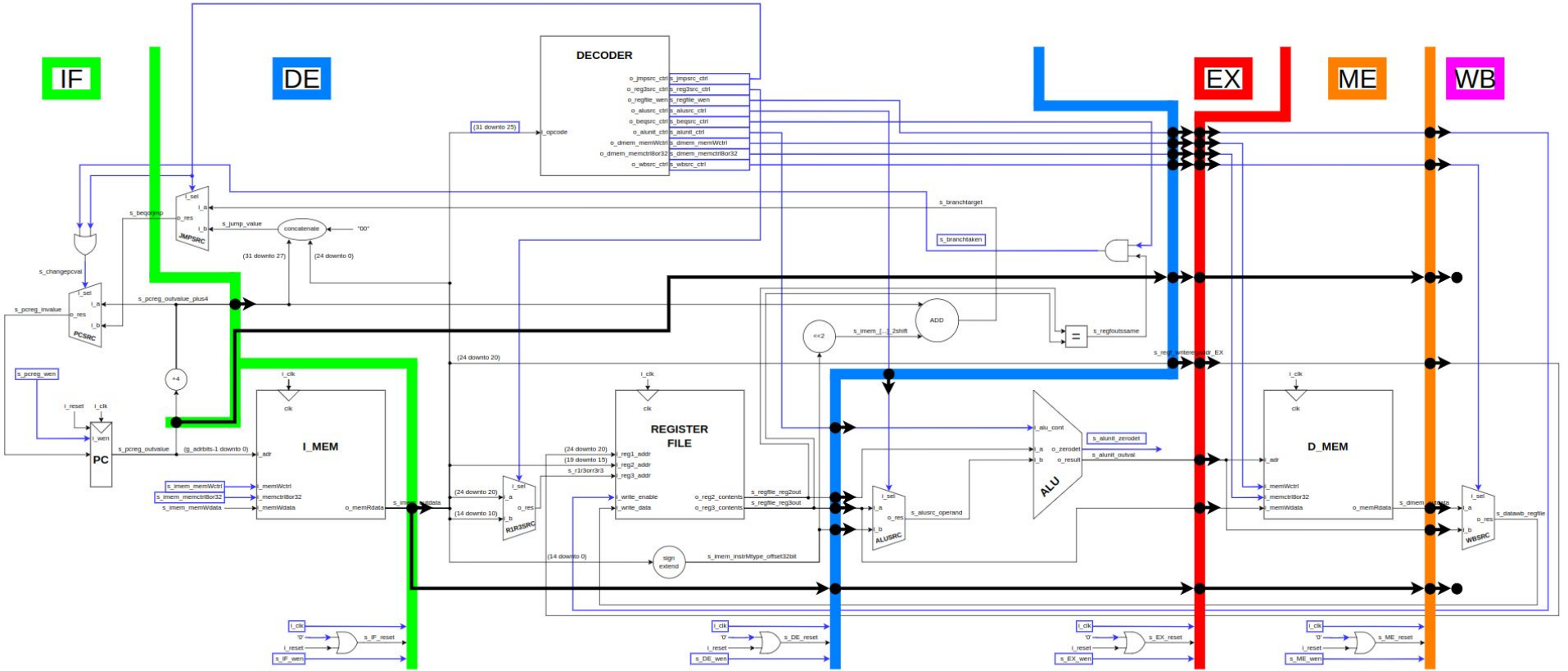
Write-back stage...



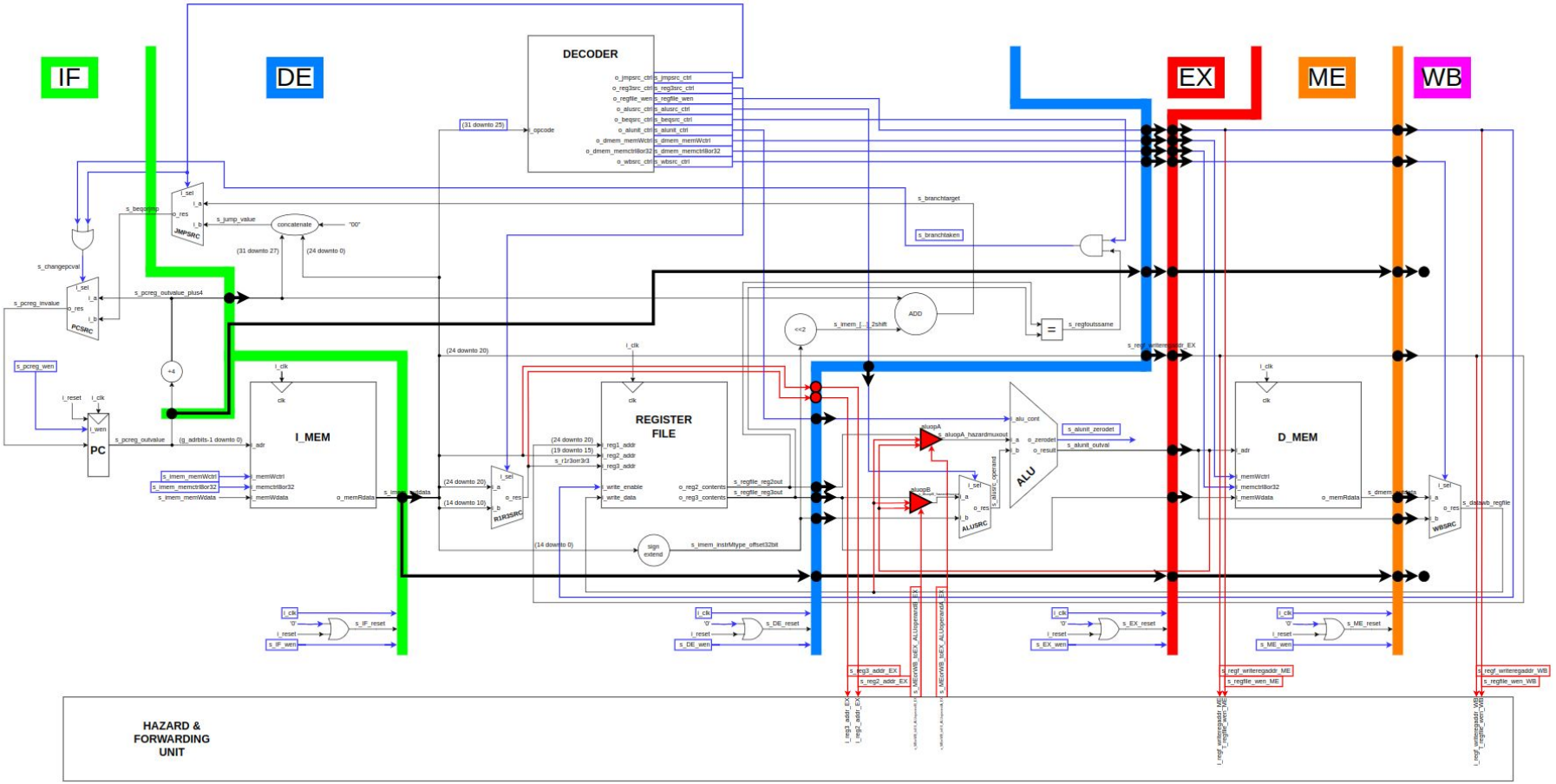
Write-back stage, corresponding update to regfile writing



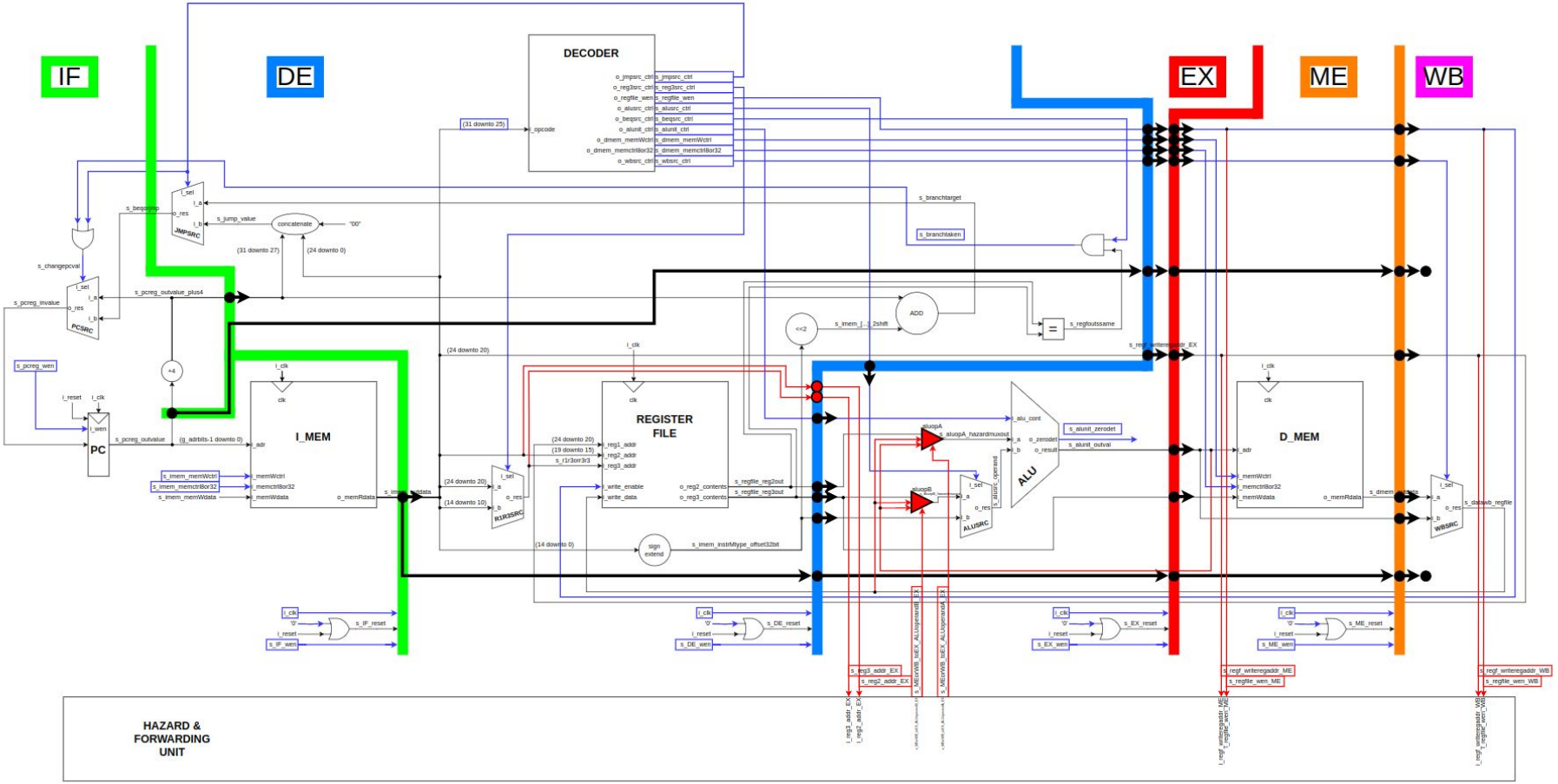
PC and imem-out flow through the pipeline for debugging purposes in waveforms…



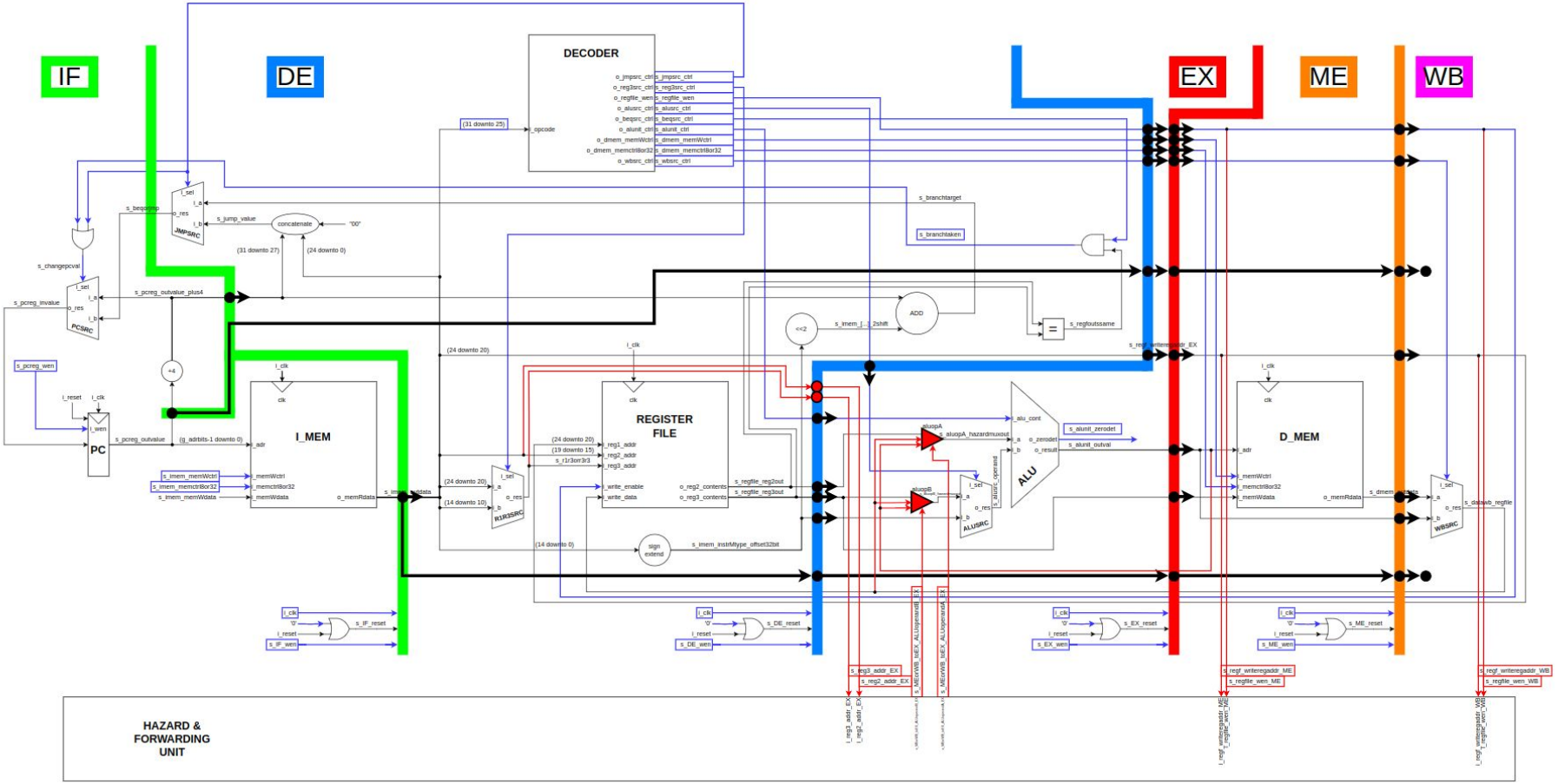
Enter bypass network, aka “Hazard & Forwarding Unit” (naming of signals starts getting out of hand…)



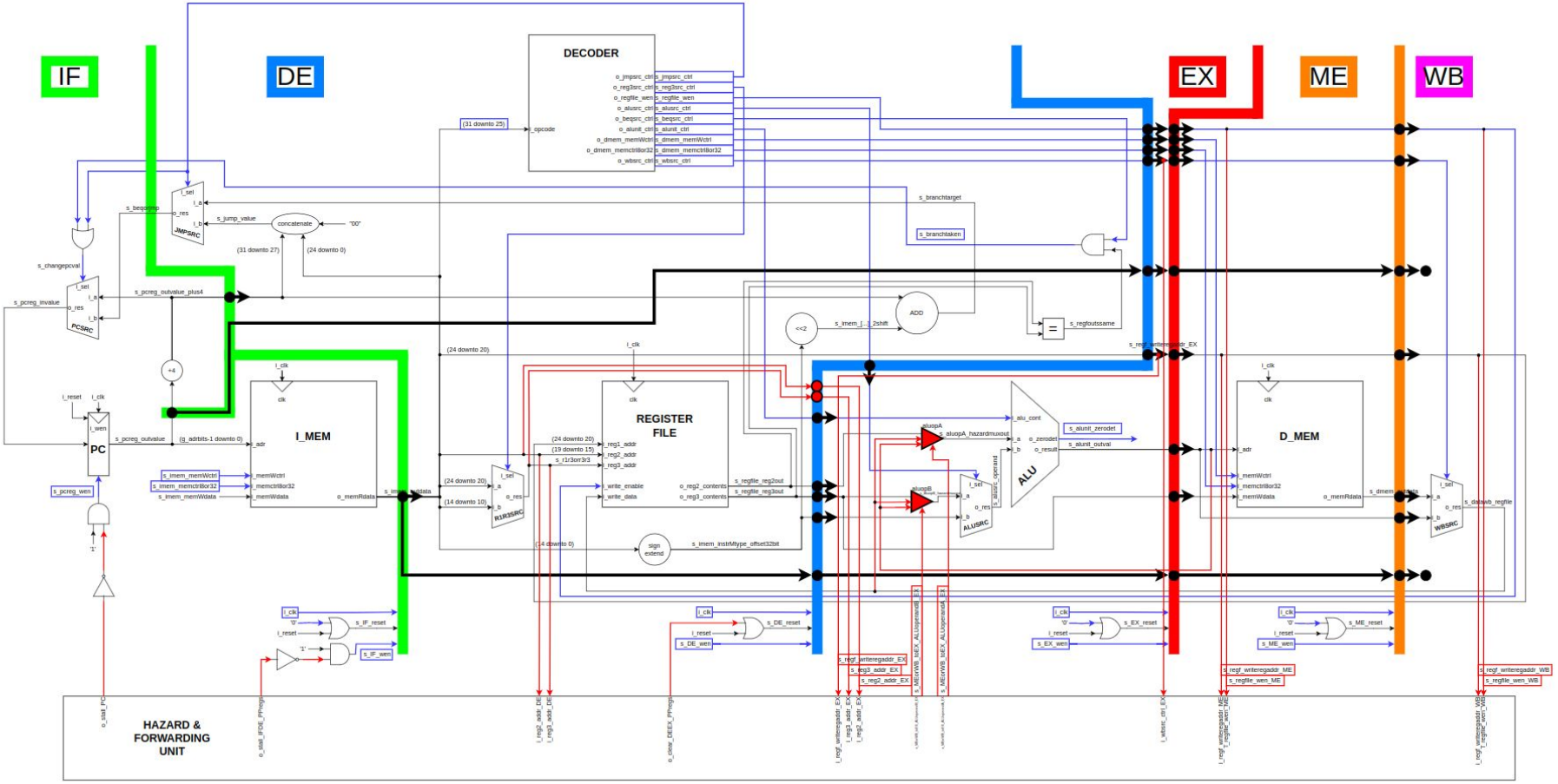
Red dots in pipeline-stage lines correspond to inter-stage registers necessary for bypassing/forwarding…



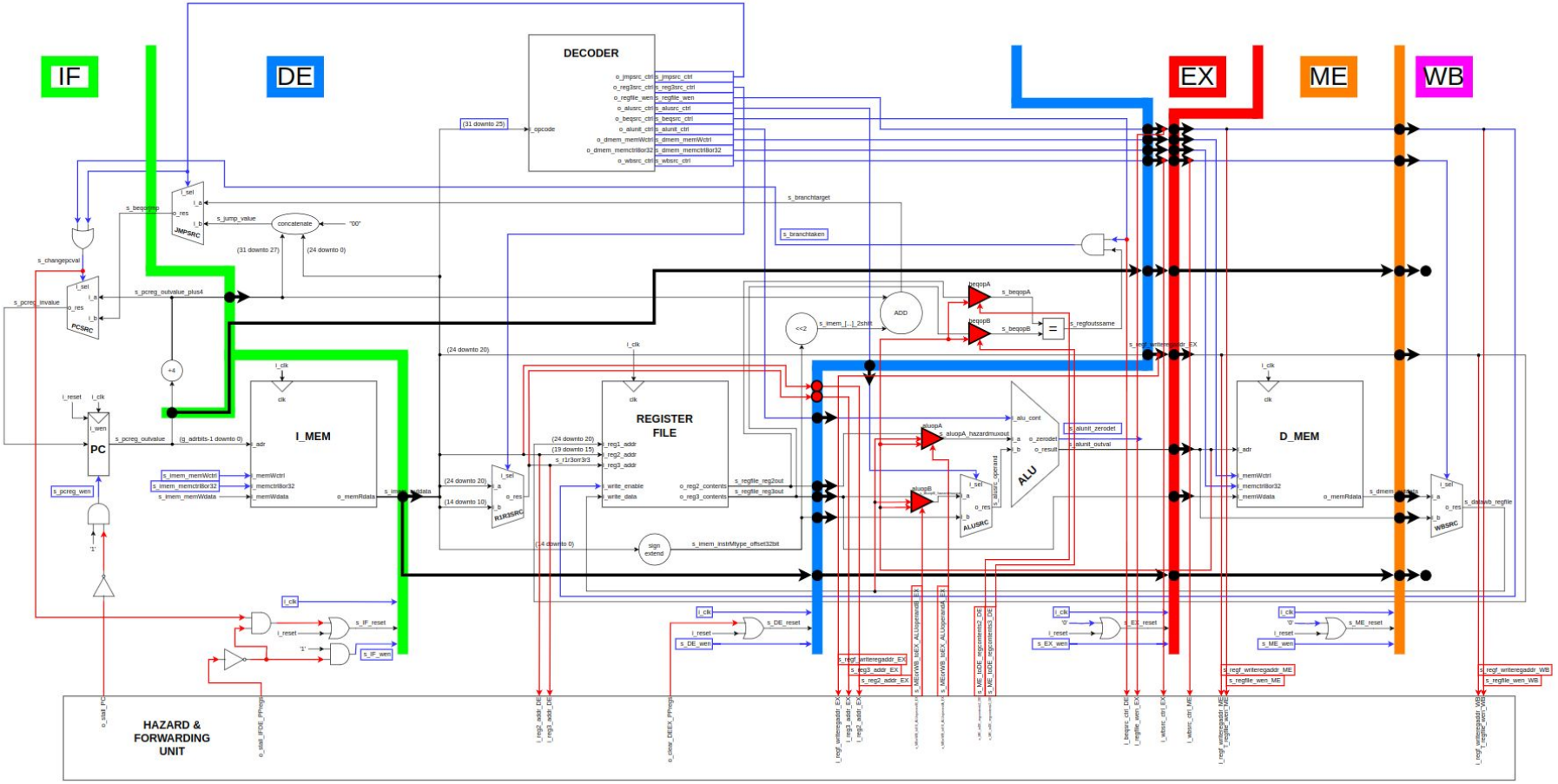
Red triangles correspond to muxes necessary for bypassing/forwarding…



Load-producer Arith-consumer delay logic



Arith-producer BEQ-consumer bypass and BEQ-induced stall at IF stage to avoid wrong branch path



Arith-producer Load-consumer bypass