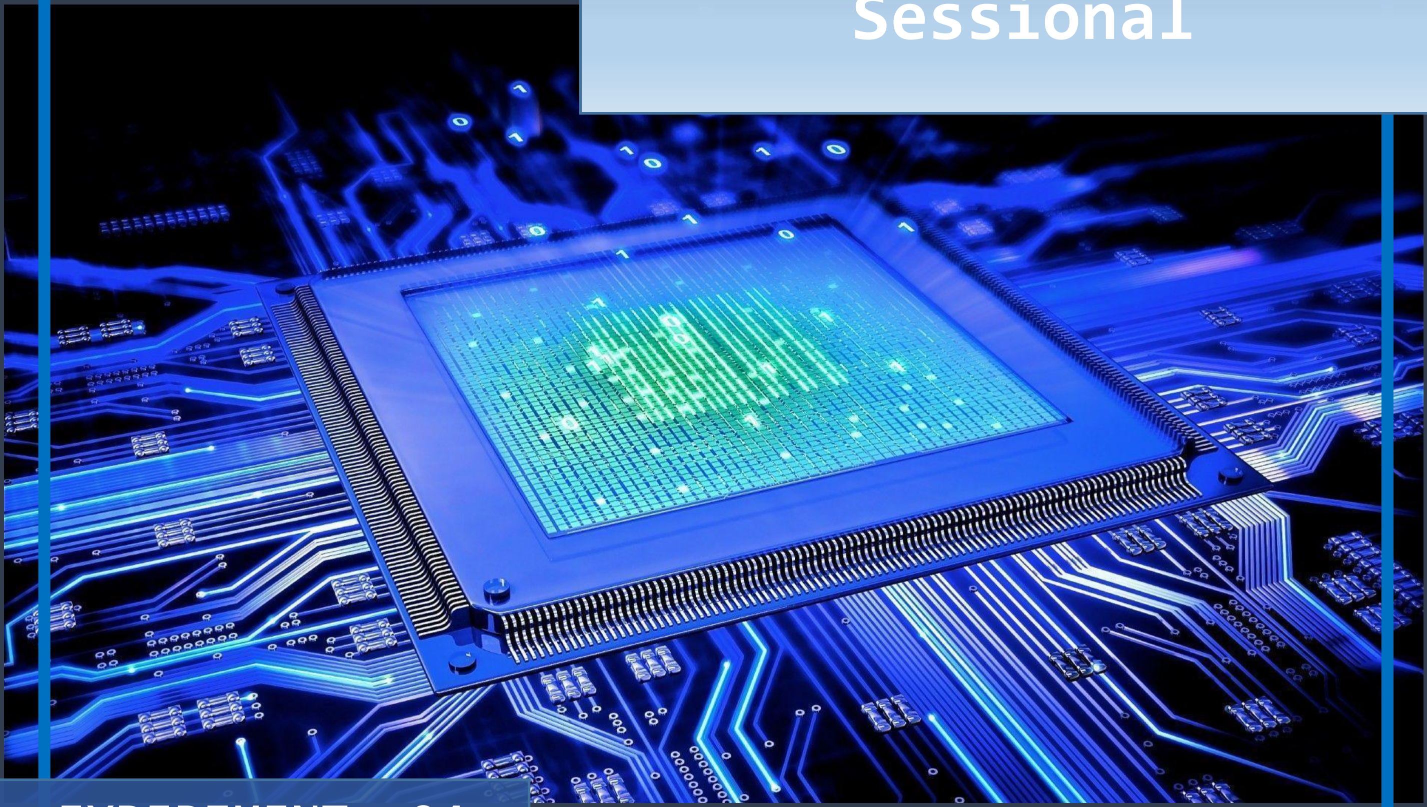
CSE 306

Computer Architecture Sessional



EXPERIMENT: 04

NAME OF EXPERIMENT:

8-BIT MIPS PIPELINED EXECUTION

GROUP NO:	**04**
Section:	A2
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Introduction:

A MIPS processor is one version of a reduced instruction set computer (RISC).Our design is an 8 bit MIPS processor that implements the MIPS instruction set with pipelined execution enabled. We focus to execute multiple operations of different instructions simultaneously and target to eliminate the relation between pulse duration and highest time for single instruction execution.

In the design, the instructions are divided into five stages:

1. Instruction Fetch (IF)
2. Instruction Decode (ID)
3. Execution and address calculation (EX)
4. Data Memory Access (MEM)
5. Write Back (WB)

The main components of the processor are inter-twined with these stages and robust control over the components and stages gives us the benefit of running segments of multiple instructions in our processor, which is in-turn pipelining.

Instruction Fetch (IF):

The codes for instructions are fetched from instruction memory and inserted into **IF/ID** registers. These are used in subsequent phases.

Instruction Decode (ID):

The instructions stored in **IF/ID** registers are decoded to opcode, rs, rt and rt in this phase and saved into **ID/EX** registers for future use.

Execution and address calculation (EX):

The execution of operations are done in this phase and ALU results, Rd of this phase and certain control bits are saved through **EX/MEM** registers.

Data memory Access (MEM):

The operations that includes data memory read/write are done in this phase. The memory locations and necessary control bits are taken from **EX/MEM** registers and the results of this phase are saved in **MEM/WB** register.

Write Back (WB):

MEM/WB register holds the data that is required to be written in registers. The registers are filled with necessary data(that was meant to be written) in this phase (in the first clock cycle) and marks the end of a complete tour of all phases for a certain instruction.

High Level Block Diagram:

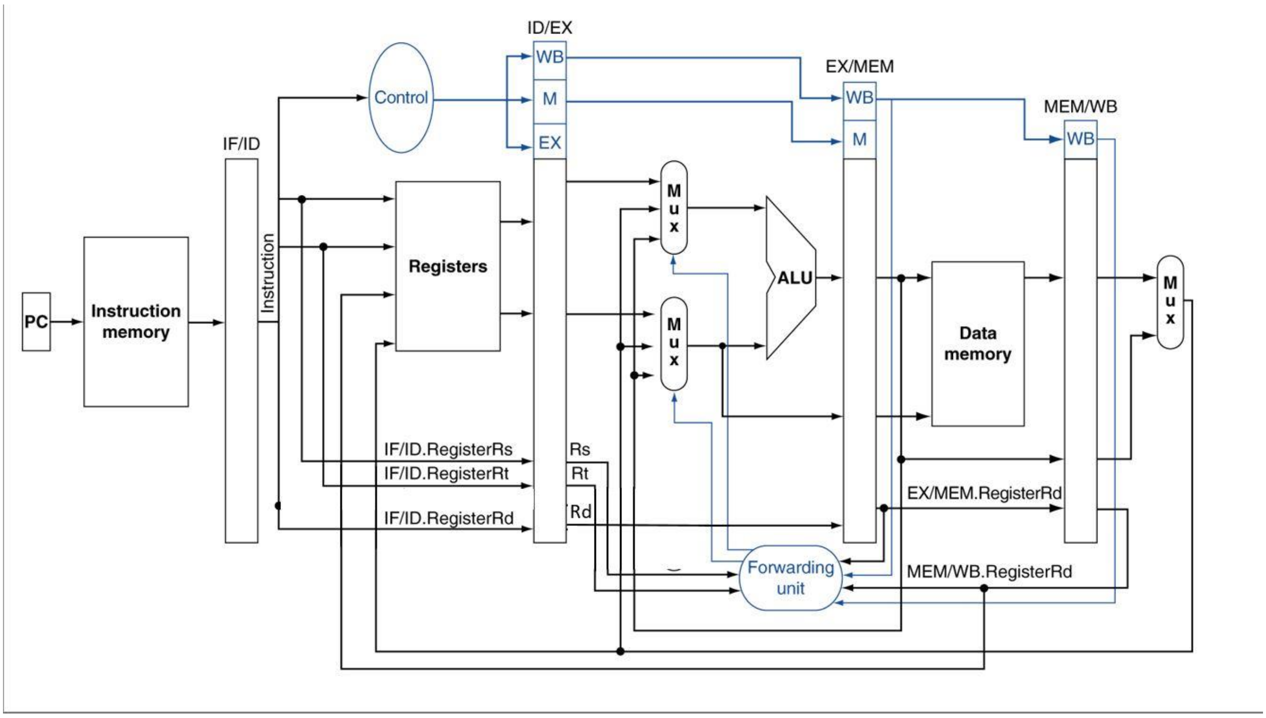

Fig-2: High Level Block Diagram of MIPS Pipeline

Block Diagrams and Size of Pipeline Registers:

Block Diagram of IF/ID Pipeline:

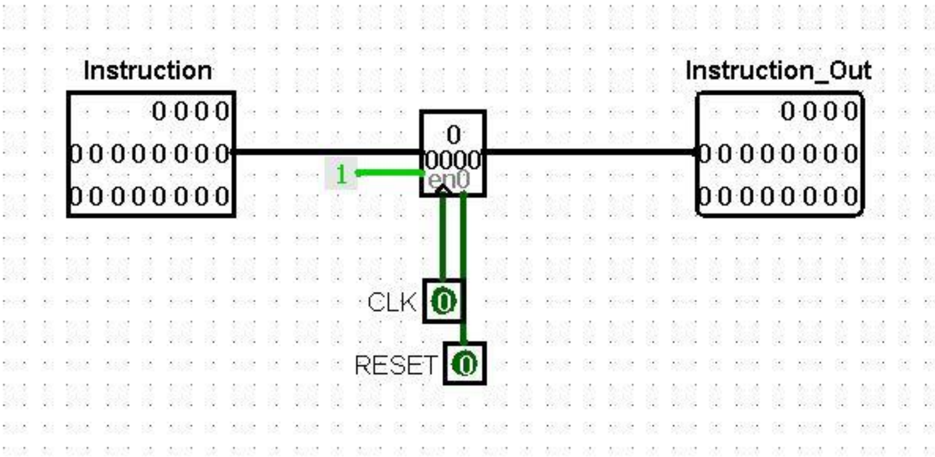

Fig-3.1: IF/ID Pipeline Circuit

Block Diagram of ID/EX Pipeline:

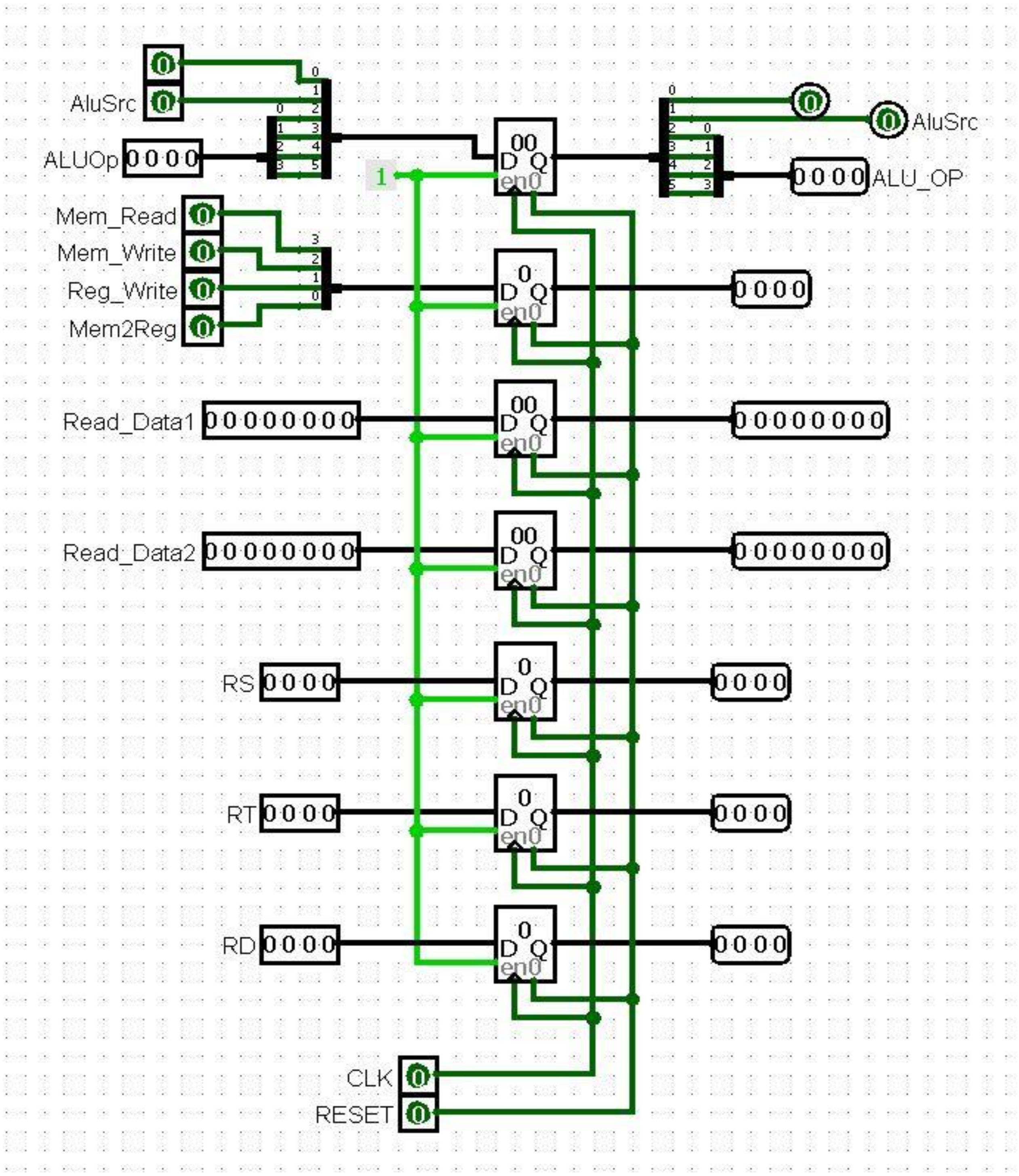

Fig-3.2: ID/EX Pipeline Circuit

Block Diagram of EX/MEM Pipeline:

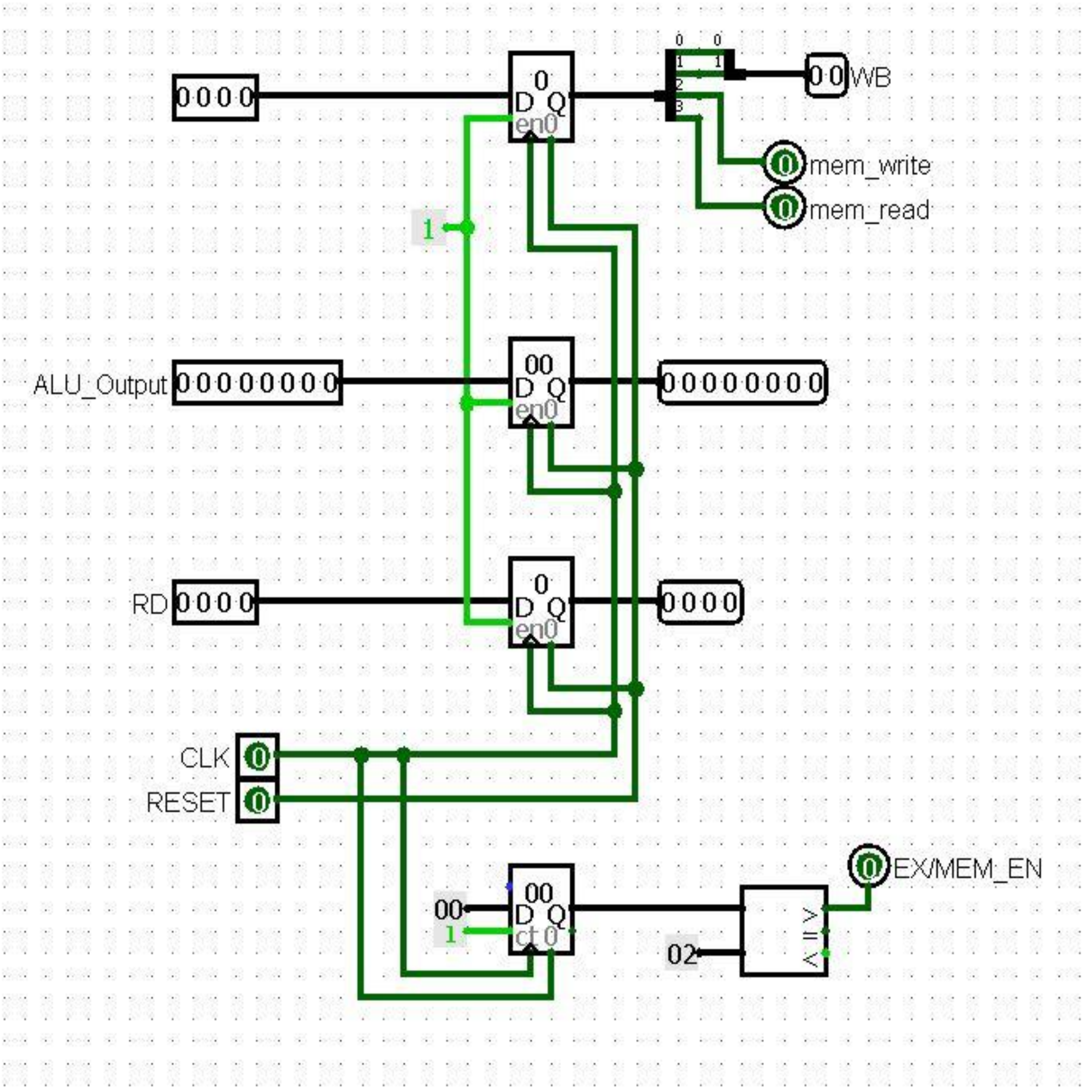

Fig-3.3: EX/MEM Pipeline Circuit

Block Diagram of MEM/WB Pipeline:

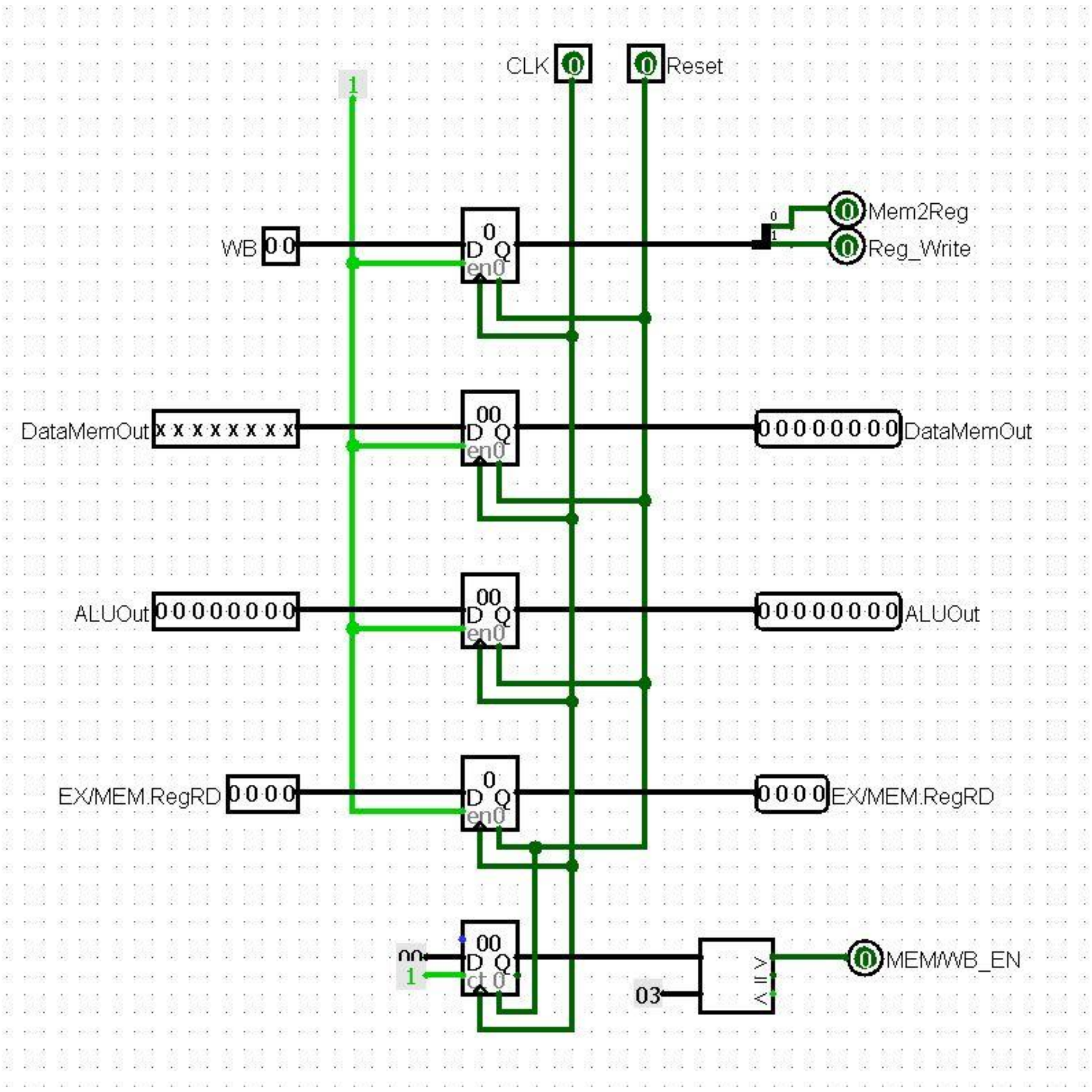

Fig-3.4: MEM/WB Pipeline Circuit

Size of Pipeline Registers:

Pipeline	Size (bits)
IF/ID	20
ID/EX	38
EX/MEM	16
MEM/WB	22

Mechanism and Block Diagram of Forwarding Unit:

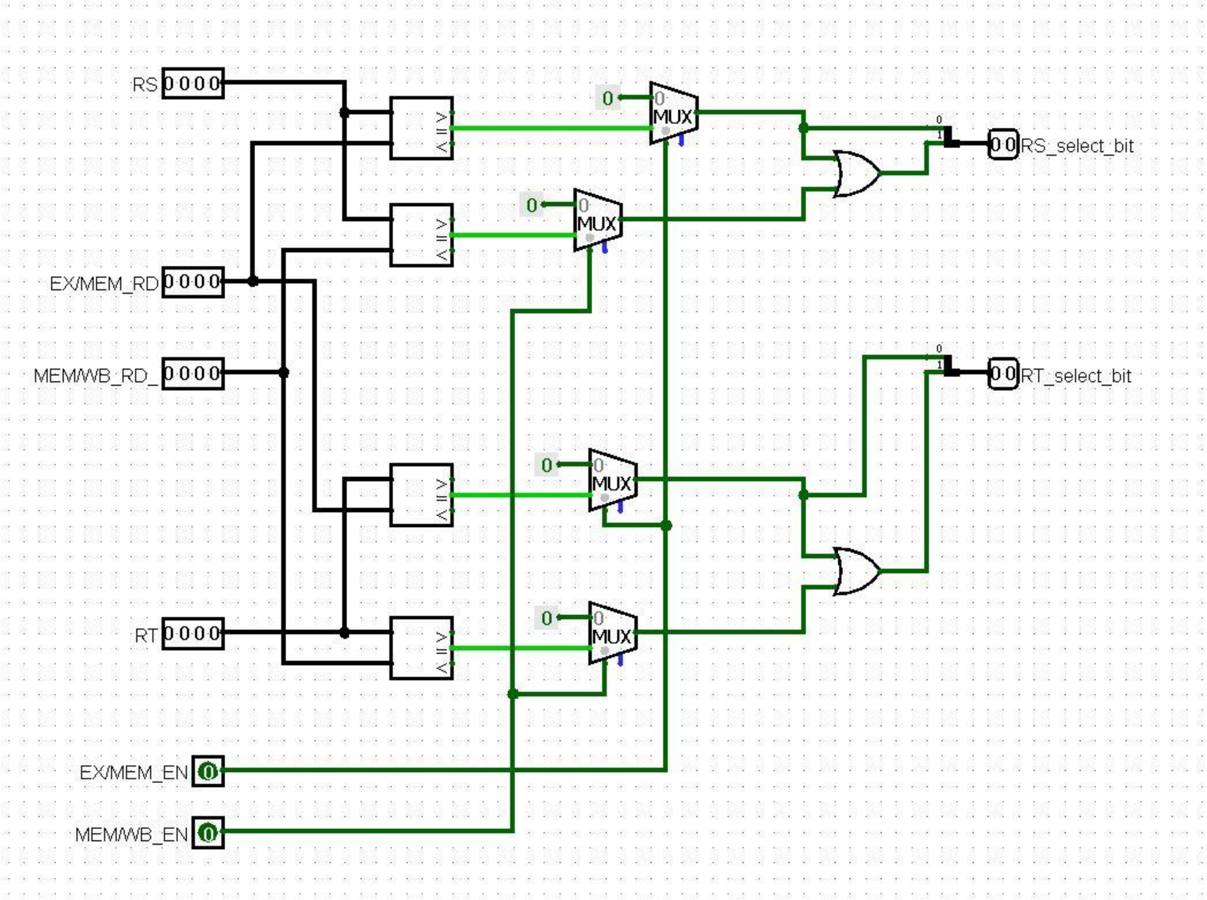

Fig-4: MEM/WB Pipeline Circuit

Mechanism:

1. Compare RS with EX/MEM_RD. If equals, then EX Hazard occurs. For this, RS_Select_bit is 11.
2. Compare RS with MEM/WB_RD. If equals, then MEM Hazard occurs. For this, RS_Select_bit is 10.
3. If both of them are not equal to RS, then no hazard occurs and RS_select_bit is 00.
4. Repeat this process for RT and RT_Select_bit.
5. Among RS_Select_bit and RT_Select_bit, if one of them indicates EX Hazard and another one indicates MEM Hazard, then Double Data Hazard Occurs.

Discussion:

The current MIPS processor is designed for the completion of instructions through pipelining. The main advantage here is that we can use small length signal(pulses) for any type of instruction and the length of pulses does not have to be dependent on the size of a instruction. In this experiment, we only implemented a subset of R-format instructions. For this we used 4 kinds of data registers. We also constructed a forward unit that helps us decide to use the particular value of a register at a certain stage in the past. The forward unit is designed to prevent EX hazard, MEM hazard and Double Data Hazard.

During the construction of forward unit we used logic gates, comparators and multiplexers to decide upon which value of Rd to take from which pipeline register. The control bits constructed in forwarding unit is used to select data paths into ALU.

The current implementation is a very limited version of powerful pipelined processors used in real life.