FLOYD

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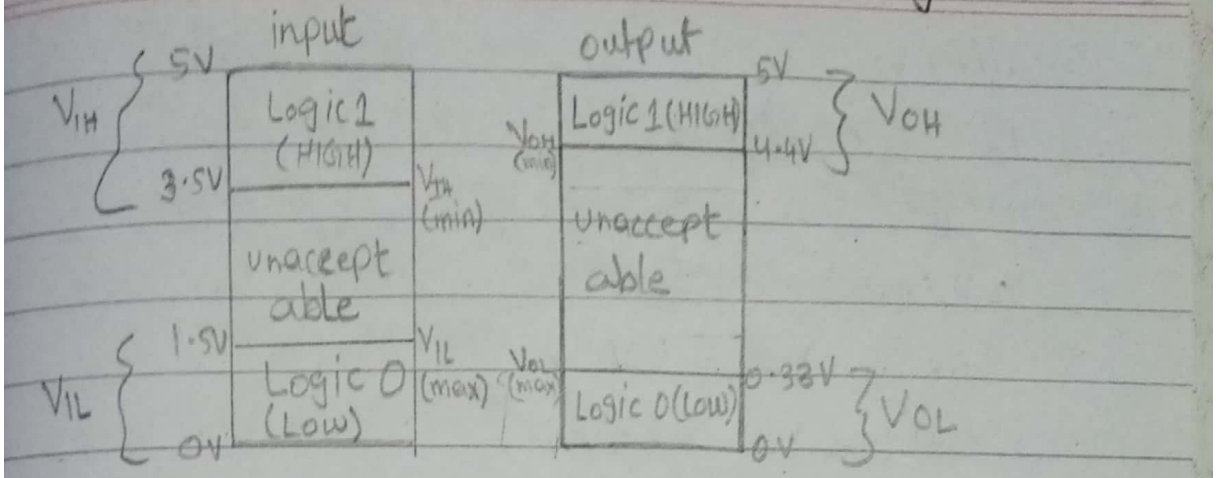
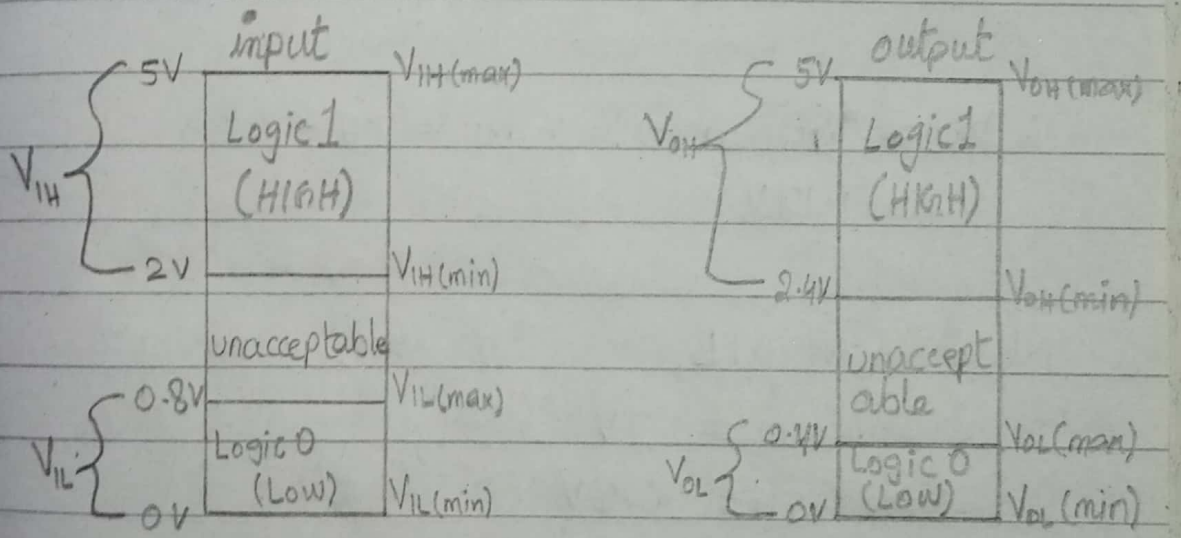


+5V CMOS



+5V TTL

Example 15-1

Q. Determine the high-level and low-level noise margins for CMOS and TTL by using the information in figures above.

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Solution:

For 5V CMOS,

$V_{IH(min)} = 3.5V$

$V_{IL(max)} = 1.5V$

$V_{OH(min)} = 4.4V$

$V_{OL(max)} = 0.33V$

$\therefore V_{NH} = V_{OH(min)} - V_{IH(min)} = 4.4 - 3.5$

$V_{NH} = 0.9V$

$\therefore V_{NL} = V_{IL(max)} - V_{OL(max)} = 1.5 - 0.33$

$V_{NL} = 1.17V$

Now, for TTL,

$V_{IH(min)} = 2V$

$V_{IL(max)} = 0.8V$

$V_{OH(min)} = 2.4V$

$V_{OL(max)} = 0.4V$

$\therefore V_{NH} = V_{OH(min)} - V_{IH(min)} = 2.4 - 2$

$V_{NH} = 0.4V$

$\therefore V_{NL} = V_{IL(max)} - V_{OL(max)} = 0.8 - 0.4$

$V_{NL} = 0.4V$

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Related Problem:

Q. Based on the preceeding noise margin calculations, which family of devices, 5V CMOS or TTL, should be used in a high-noise environment?

A. As we calculate the noise immune values of CMOS and TTL; CMOS can immune from more noises as compared to TTL.

Q. Example 15-2

Q. A certain get draws 2 μA when its output is HIGH and 3.6 μA when its output is Low. What is the avg. power dissipation if Vcc is 5V and gate operated on a 50% duty cycle?

Data:

$I_{CCH} = 2\mu A = 2 \times 10^{-6} A$

$I_{CCL} = 3.6\mu A = 3.6 \times 10^{-6} A$

duty cycle = 50%

$V_{CC} = 5V.$

$P_D = ?$

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$\therefore P_D = V_{cc} I_{cc}$

$\therefore I_{cc} = \frac{I_{CCH} + I_{CCL}}{2} = \frac{2 \times 10^{-6} + 3.6 \times 10^{-6}}{2}$

$I_{cc} = 2.8 \times 10^{-6} A$

$P_D = (5)(2.8 \times 10^{-6})$

$P_D = 14 \times 10^{-6} W$

Ans.

Related Problem:

Q. A certain IC gate has an $I_{CCH} = 1.5 \mu A$ and $I_{CCL} = 2.8 \mu A$. Determine the average power dissipation for 50% duty cycle operation if V_{cc} is 5V.

Data:

$I_{CCH} = 1.5 \mu A = 1.5 \times 10^{-6} A$

$I_{CCL} = 2.8 \mu A = 2.8 \times 10^{-6} A$

$V_{cc} = 5$

$P_D = ?$

Solution:

$P_D = V_{cc} \cdot I_{cc}$

$I_{cc} = \frac{I_{CCH} + I_{CCL}}{2} = \frac{1.5 \times 10^{-6} + 2.8 \times 10^{-6}}{2}$

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$I_{CC} = 2.15 \times 10^{-6}$ A

Now, $P_D = V_{CC} \cdot I_{CC} = (5)(2.15 \times 10^{-6})$

$P_D = 10.75 \times 10^{-6}$ W

Ans.

Section Checkup 15-1:

Q. Define V_{IH}, V_{IL}, V_{OH} and V_{OL}

A. V_{IH} = Input voltage when HIGH

V_{OH} = Output voltage when HIGH

V_{IL} = Input voltage when LOW

V_{OL} = Output voltage when LOW

Q2. Is it better to have a lower value of noise margin or a higher value?

A. A higher value of noise margin would better.

Q3. Gate A has a greater propagation delay time than gate B. Which gate can operate at high frequency

A. Gate B can operate at high frequency than gate A..

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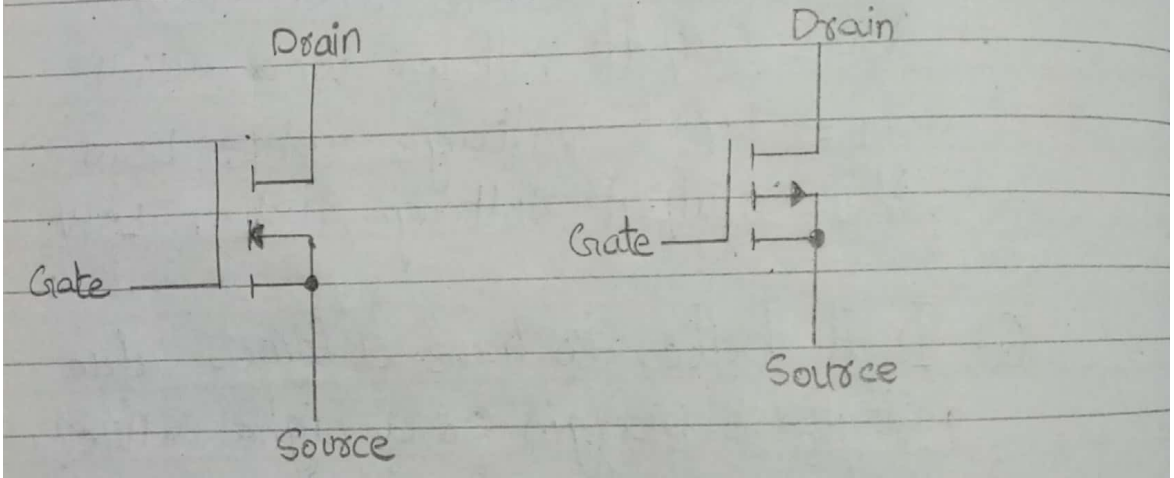
Q4. How does excessive loading affect the noise margin of a gate?

A. Excessive loading reduces the noise margin of a gate.

Section 15-2: CMOS

CMOS — Complementry Metal-Oxide Semi-conductor

MOSFET — Metal-Oxide Semiconductors Field effect transistors.



n-channel P-chanel.

MOSFET Symbols

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Section Checkups 15-2:

Q. What type of transistor is used in CMOS & logic?

A. MOSFETs

Q. What is meant by the term Complementry

A. Complementry is meant by theirs are two circuits n-type and p-type.

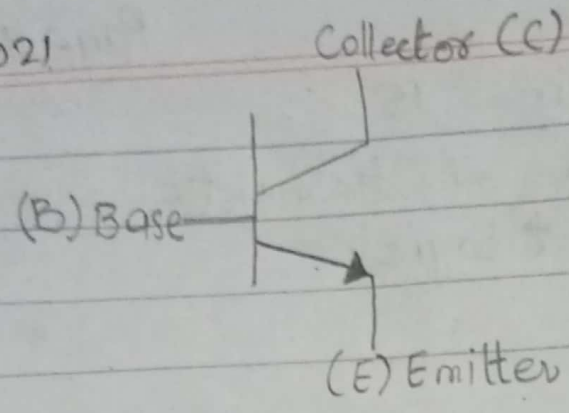
Q. Why must CMOS devices be handled with care?

A. Because electrostatic discharge can damage CMOS devices; electrostatic discharge is analog in nature so it can fuse both p-type and n-type circuits of CMOS/MOSFET.

Section 15-3: TTL (Bipolar) Circuits.

TTL has totem-pole circuits

BJT- Bipolar Junction Transister
BJT is an active switching element with npn and pnp terminals named: Base, emmiter and collector.



BJT (npn)

Section checkup 15-3:

Q. An npn BJT is on when the base is more negative than the emitter?

A. False, An npn BJT will be off.

Q. In terms of switching action, what do the on and off states of a BJT represent?

A. On is closed state and off is an open state.

Q. What are the two major types of output circuits in TTL?

A. Totem-pole and open-collector are types of TTL outputs.

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Q. Explain how tri-state logic differs from two-state logic?

A. Tri-state logic provides a high-impedance state, in which the output is disconnected from the rest of the circuit.

Section 15-4

Example 15-3:

Q. When a standard TTL NAND gate drives five TTL inputs, how much current does the driver output source, & much does it sink?

Total source current in HIGH output stat:

$I_{IH(max)} = 40\mu A$ / input

$I_{T(source)} = (5)(40\mu) = 200\mu A$

$I_{T(source)} = 200 \times 10^{-6} A$

Ans.

Total sink current in (low output state):

$I_{IL(max)} = -1.6$ mA / input

$I_{T(sink)} = (5)(-1.6m) = -8mA = -8 \times 10^{-3} A$

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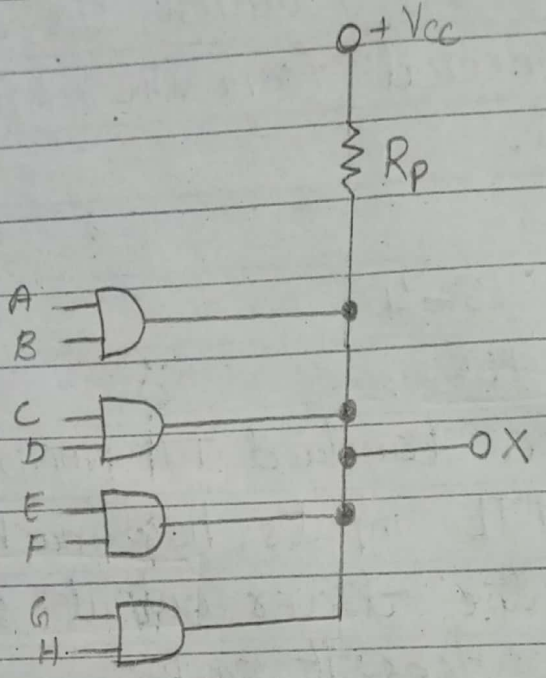
Example 15-5:

Q. Write the output expression for the wired-AND configuration of open-collector AND gates in figure below.



A. $X = ABCDEFGH$

4-wired 2-input AND gates creates an 8-input AND gate.

Related Problem:

Q. Determine the output expression if NAND gate is used.

A.

$X = \overline{AB} \cdot \overline{CD} \cdot \overline{EF} \cdot \overline{GH}$

4 wired 2-input NAND gates creates an AND gate with 4 2-input NAND gates

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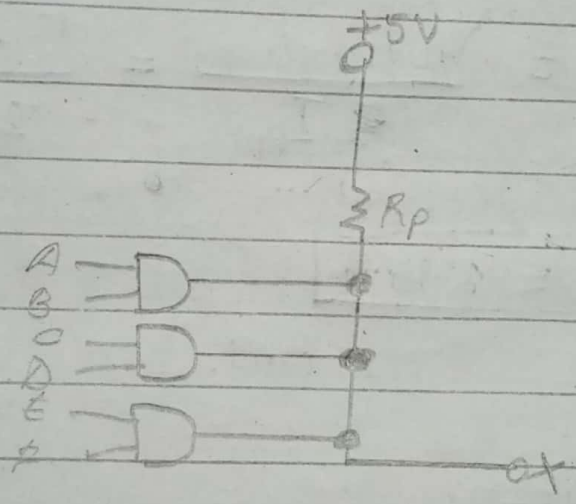
Example 15-6:

Q. Three open collector AND gates are connected in a wired-AND configuration. Assume that the wired AND ~~configurations as shown~~ circuit is driving four standard TTL inputs (-1.6mA each).



(a) Write its expression

(b) Determine the minimum value of Rp if $I_{OL(max)}$ for each gate is 30 mA and $V_{OL(max)} = 0.4\ V$

(a) $X = ABCDEF$

(b) $R_p = \frac{V_{CC} - V_{OL(max)}}{I_{R_p}}$; Ohm's Law

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$$\therefore I_{Rp} = I_{OL(max)} - I_T$$

$$I_T = 4 \times 1.6\,mA = 6.4\,mA = 6.4 \times 10^{-3}\,A$$

$$I_{Rp} = 30 \times 10^{-3} - 6.4 \times 10^{-3}$$

$$I_{Rp} = 23.6 \times 10^{-3}\,A$$

Now,

$$R_p = \frac{V_{cc} - V_{OL(max)}}{I_{Rp}} = \frac{5 - 0.4}{2.3 \times 10^{-3}}$$

$$\boxed{R_p = 295\,\Omega}$$

Ans.

Example 15-7:

Q. Determine the value of the limiting Resistor, R_L, in the open-collector circuit if the LED current is to be 20 mA. Assume a 1.5 V drop accross the LED when it is forward biased and a Low state output voltage of 0.1V at the output of the gate.

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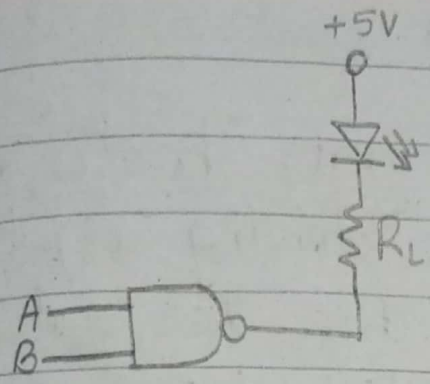

Solution:

We use ohm's Law,

$$V_{R_L} = I R_L \Rightarrow R_L = \frac{V_{R_L}}{I}$$

$$V_{R_L} = V_{CC} - V_{IL(max)} - V_{OH(max)}$$
$$= 5 - 1.5 - 0.1 = 3.4$$

$$\boxed{V_{R_L} = 3.4\ V}$$

$$R_L = \frac{V_{R_L}}{I} = \frac{3.4}{20 \times 10^{-3}} = 170\ \Omega \quad \text{Ans.}$$

Related Problem:

Q. Determine R_L if LED requires 35 mA.

A. $$R_L = \frac{V_{R_L}}{I} = \frac{3.4}{35 \times 10^{-3}} = 97.143\ \Omega$$

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PROBLEMS

Q1. A certain logic gate has a $V_{OH(min)}$ is 2.2V and it driving a gate with a $V_{IH(min)} = 2.5V$. Are these gates are compatible for HIGH-state operation? Why?

A. These gates are not compable for HIGH-state operations because $V_{OH(min)} < V_{IH(min)}$

Q2. A certain Logic gate has a $V_{OL(max)} = 0.45V$ and it is driving a gate with a $V_{IL(max)} = 0.75V$. Are these gates are compatible for Low-state operation? Why?

A. The two gates are compatible for LOW state operation because $V_{OL(max)}$ is less than $V_{IL(max)}$.

Q3. A TTL gate has the following actual voltage level values: $V_{IH(min)} = 2.25$ $V_{IL(max)} = 0.65V$. Assuming it is being drive by a gate with $V_{OH(min)} = 2.4V$ and $V_{OL(max)} = 0.4V$, What are the HIGH

and LOW level noise margins?

A.

$V_{NH} = V_{OH(min)} - V_{IH(min)}$

$= 2.4 - 2.25$

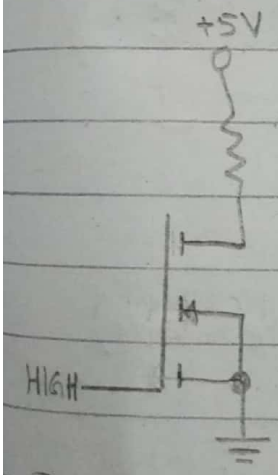
$\boxed{V_{NH} = 0.25}$

$V_{NL} = V_{IL(max)} - V_{OL(max)}$

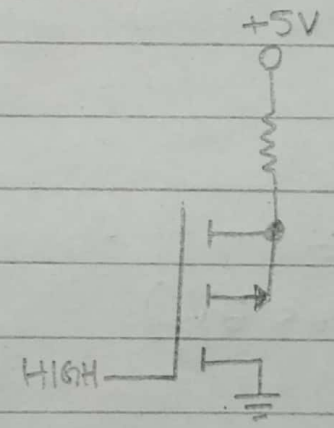
$= 0.65 - 0.4$

$\boxed{V_{NL} = 0.25}$

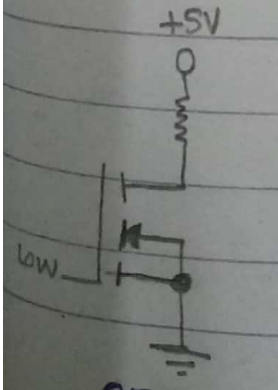
Q. Determine the state (on or off) of each MOSFET in Fig. 15-53.



ON



OFF



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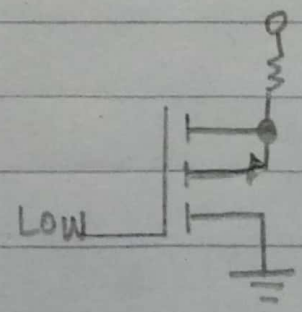

ON

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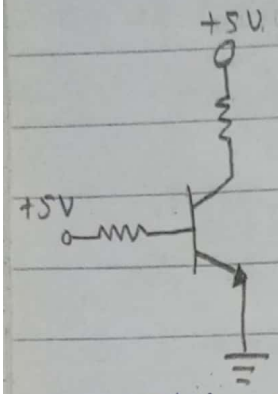
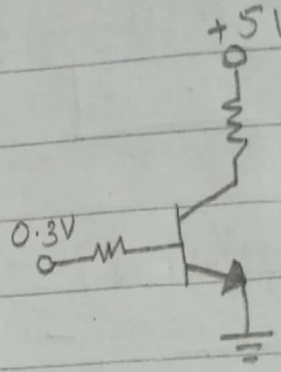
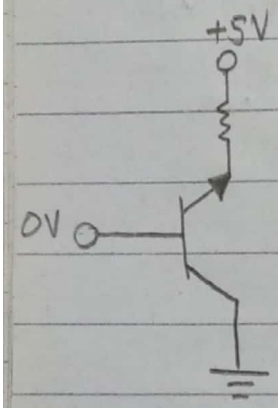
Q16. Determine the BJTs in Fig. 15-55 are off and which are off?



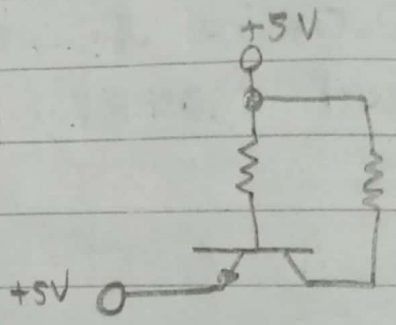
ON ($V_B > V_E$)



OFF ($V_B < V_E$)



OFF ($V_B < V_E$)



OFF ($V_B < V_E$)

Q23. Determine the minimum value for the pull up resistor in each circuit if $I_{OL(max)} = 40mA$ and $V_{OL(max)} = 0.25V$ for each gate assume that 10 standard TTL unit loads are being driven from output x and the supply voltage is 5V.

A. Data:

$V_{OL(max)} = 0.25V$

$I_{OL(max)} = 40mA = 40 \times 10^{-3} A$

$V_{CC} = 5V$

$\therefore R_p = \frac{V_{CC} - V_{OL(max)}}{I_{Rp}}$

$\therefore I_{Rp} = I_{OL(max)} - I_T = 40 \times 10^{-3} - 10$

$\boxed{I_{Rp} = -9.96\ A}$

$R_p = \frac{5 - 0.25}{-9.96} =$

$\boxed{R_p = -0.47692\ \Omega}$

Ans.

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Q25. Determine the IC family with the best speed-power product in Table 15-1.

A. ALVC

CHAPTER # 4 MAVINO
TTL CIRCUITS PROBLEMS

Q. A segment seven decoder is driving a LED display like. Which LEDs are on when digit 8 appears? Which LEDs are on when digit 4 appers?

A. For digit 8, all LEDs are on i.e a,b,c,d,e and f.
For digit 4, b, c, f and g are on.

Q. What is propagation delay?

A. Propagation delay is the length of time required for a signal to reach its destination.

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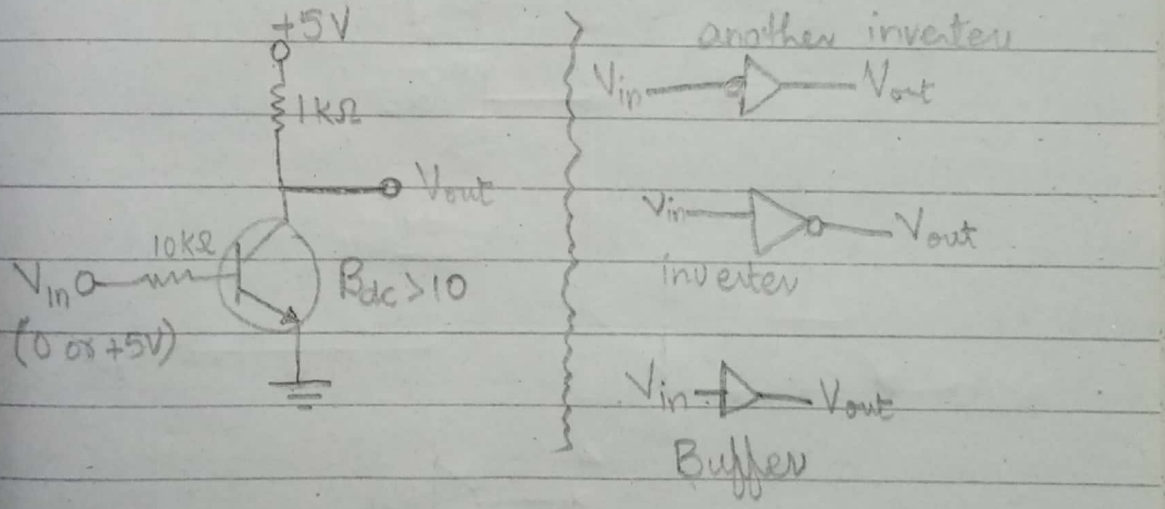
Q. What is the noise margin of TTL Devices?

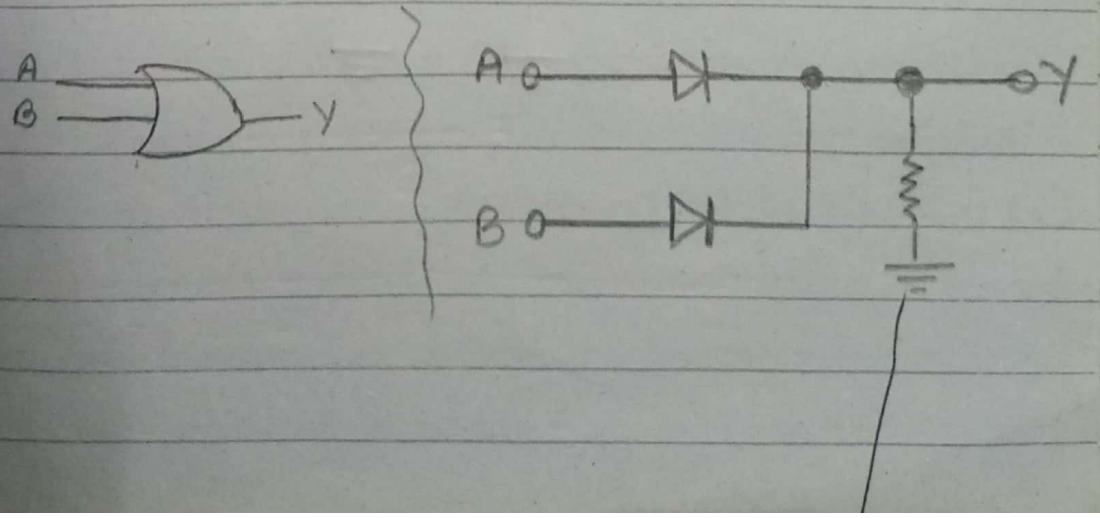
A. Standard TTL devices has noise margin of ~~0.7~~ 0.4V

2-6 (Vi): Solid State Circuit Transforming from Logic Map:

Transistor Inverter:



Diode OR Gate:



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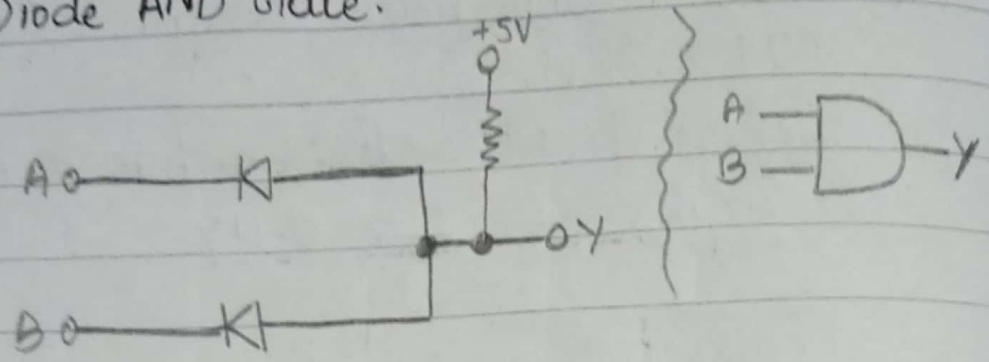
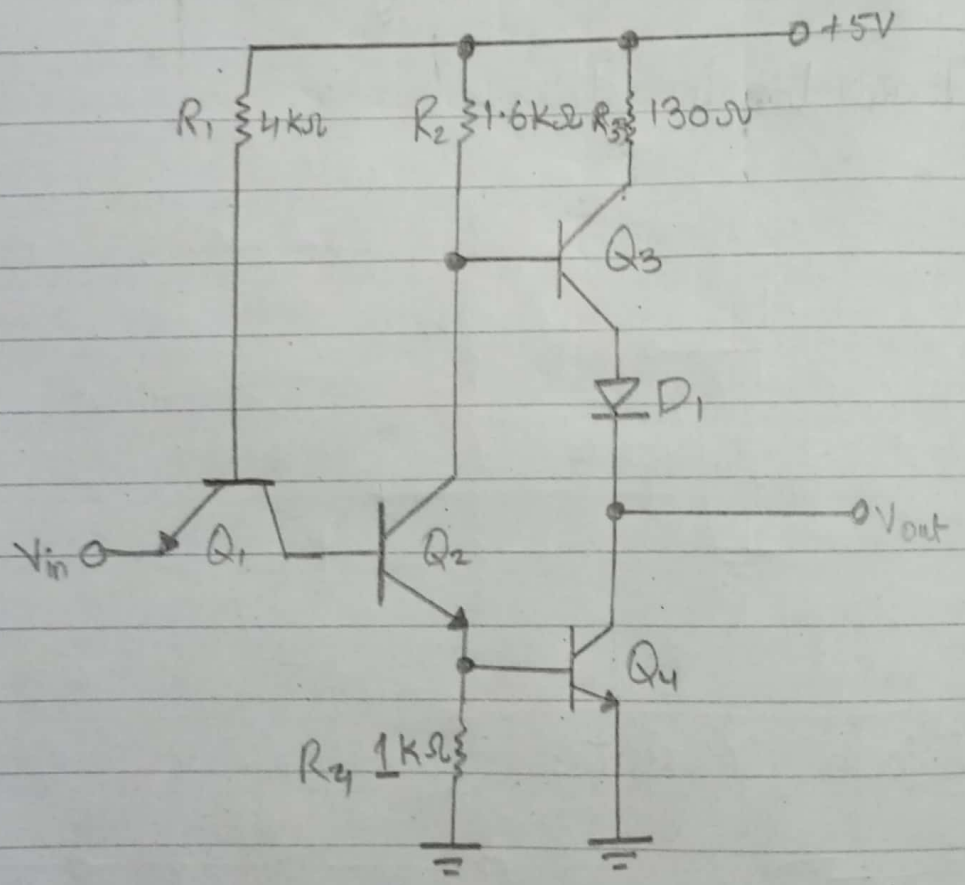
Diode AND Gate:



Standard TTL Inverter:



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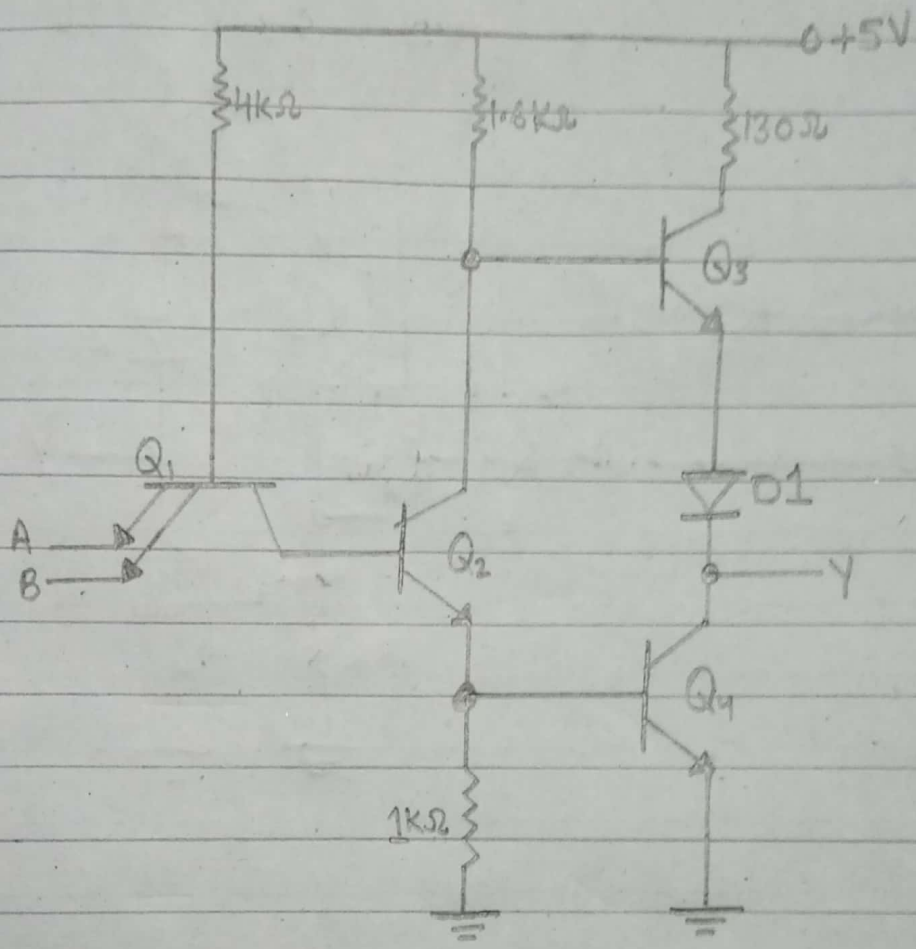
Standard TTL NAND gate:



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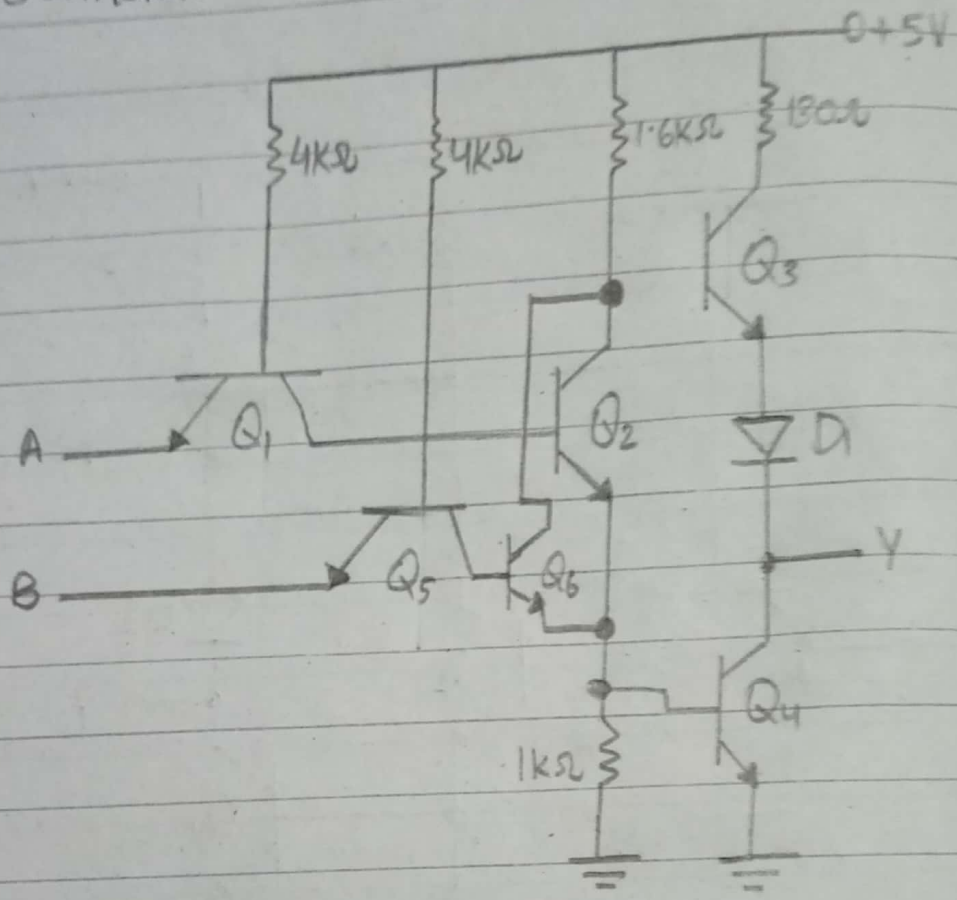
Standard TTL NOR Gate:



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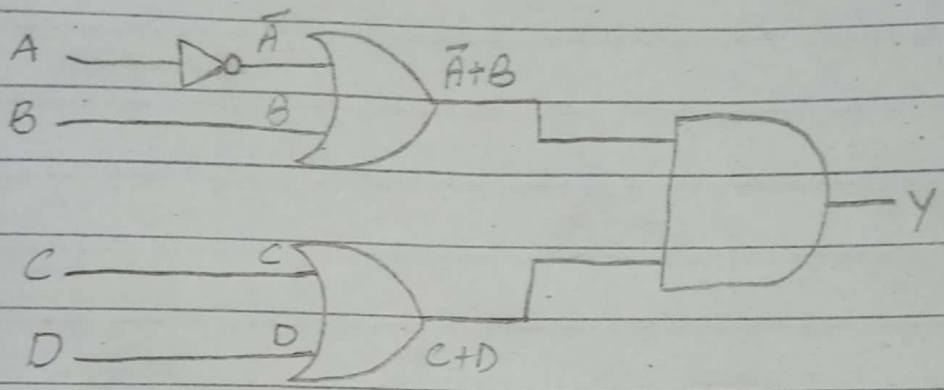
Q. Transform the given Logic Map to simple TTL/DDL Logic based solid-state circuit.



$$Y = (\bar{A}+B)\cdot(C+D)$$

Solution: