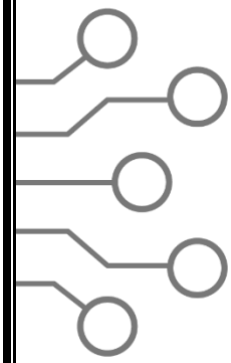


NORTH SOUTH UNIVERSITY

DEPARTMENT OF ELECTRICAL & COMPUTER ENGINEERING

CSE332L

Computer Organization and Architecture

Lab Report

Experiment No : 4
Experiment Name : Design of a 4-bit binary up-down counter

Date of Performance : 16th November 2022
Date of Submission : 23rd November 2022

Section : 9
Group No : **7**
Group Member Info and Remarks**:**

Name	*ID*	*Writer*	*Remarks*
1.		□	
2.		□	
3.		□	
4.		□	
5.		□	

Objective:

To design a 4-bit binary up-down counter

Theory:

A counter is a type of resister which goes through a predetermined sequence of states upon the application of input pulse. The input pulses, which are used for generating time signals for controlling the sequence, may be clock pulses or it may also originate from an external source. Input pulses can occur at uniform intervals of time or at a random.

A binary counter is a type of counter that follows the binary number sequence. A 4-bit binary counter contains 4 flip flops and associated gates that can show the sequence of states according to the binary count of 4 bits, that is from 0000 to 1111. We assume that the Least Significant Bit is always complemented on every state. The sequence works such a way that the next significant bit will be complemented only when a previous bit transforms from 1 to 0.

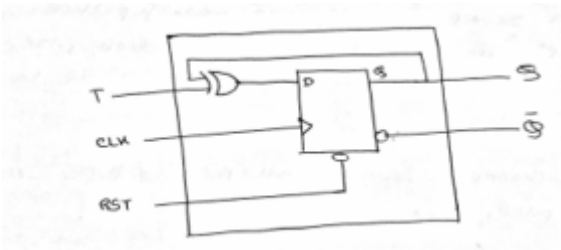
In a counter, the flip-flops are usually used for the complementing capabilities. T and JK flip flops have the capability of complementing. We will be using T flip flops, made using D flip flops and a XOR gate. The T flip flops will work as a toggle switch. When the input is 0, there will not be any output of the flip flops, that means the previous value will be retained. But when the input is 1, the output will be complemented.

For designing a 4 bit synchronous up-down counter, the flip flops will need a common clock pulse. For counting up, the next flip flop will change state when there is a transition from 0 to 1. Here the Q output has to be connected to the next flip-flop. For counting down, the next flip-flop will change state when there is a transition from 1 to 0. In this case, Q' output will be connected to the next flip flop.

Equipment List:

Equipment Name	Quantity
Trainer Board	1
IC 7404	1
IC 7408	2
IC 7432	1
IC 7486	1
IC 7474	2
Wires	A lot

Circuit Diagram:



Creating a T flip-flop using a D flip-flop

Truth Table:

Clock pulse	A	B	C	D
P0	0	0	0	0
P1	0	0	0	1
P2	0	0	1	0
P3	0	0	1	1
P4	0	1	0	0
P5	0	1	0	1
P6	0	1	1	0
P7	0	1	1	1
P8	1	0	0	0
P9	1	0	0	1
P10	1	0	1	0
P11	1	0	1	1
P12	1	1	0	0
P13	1	1	0	1
P14	1	1	1	0
P15	1	1	1	1

Discussion:

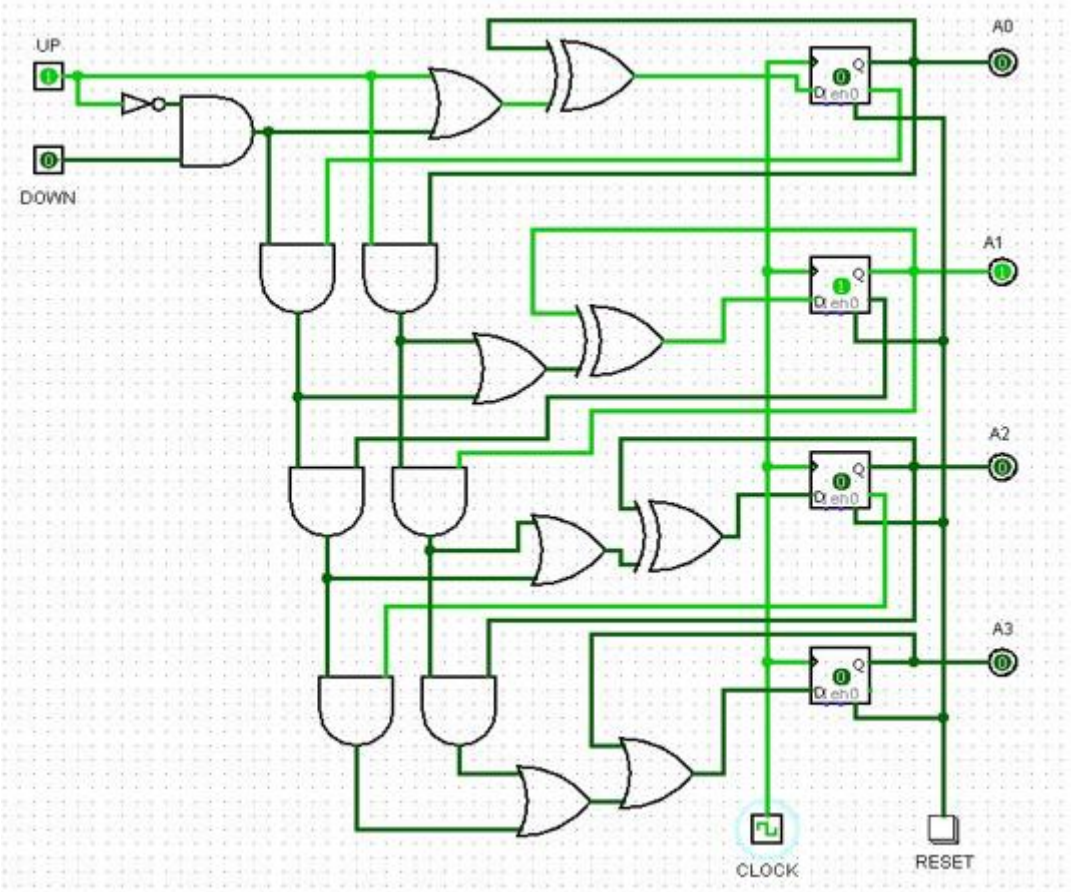
In today's lab, we designed a 4-bit binary up-down counter. A counter which has the capability of counting upward as well as downward is called up-down counter. It is also known as multimode counter. A 4-bit binary up-down counter can count from 1111 to 0000 while counting downward and 0000 to 1111 while counting upward.

The circuit can be explained like, when the external input labeled UP is equal to 1, the circuit will operate as and up counter. In this case, the value of DOWN input will not affect. The circuit will count sequence from 0000 to 1111.

When the external input DOWN is equal to 1 and UP is equal to 0, the circuit will operate as down counter. The circuit will count sequence from 1111 to 0000.

We designed the counter using T flip flops which are made of D flip flops. We applied the input combinations from the truth table for output results. However, out trainer board had some issues, as a result we did not get to see our expected results. This may also happen due to loose wire connections as the circuit and wire connections were a bit complicated.

Logisim:



References:

There is no reference.

I am the reference.