Energy-Efficient Neuron, Synapse and STDP Integrated Circuits

Jose M. Cruz-Albrecht, *Member, IEEE*, Michael W. Yung, and Narayan Srinivasa, *Member, IEEE*

***Abstract*—Ultra-low energy biologically-inspired neuron and synapse integrated circuits are presented. The synapse includes a spike timing dependent plasticity (STDP) learning rule circuit. These circuits have been designed, fabricated and tested using a 90 nm CMOS process. Experimental measurements demonstrate proper operation. The neuron and the synapse with STDP circuits have an energy consumption of around 0.4 pJ per spike and synaptic operation respectively.**

***Index Terms*—Brain, CMOS, energy, learning, low power electronics, neurons, spike timing dependent plasticity (STDP), synapses.**

I. Introduction

BIOLOGICAL systems are extremely energy efficient. The brain in particular, composed of billions of neural cells, consumes about 20 W of power [1]–[3]. These cells are noisy, imprecise and unreliable analog devices. When they are integrated into a brain architecture composed of assemblies of interacting neurons, they can solve complex tasks and exhibit complex behaviors in real-time and with high precision while consuming very low power [3].

To mimic this immensely useful capability of biological systems, electronics engineers have drawn inspiration from some key features found in biology. In particular, Prof. Carver Mead founded and pioneered such electronic system design and coined the term *neuromorphic electronics* [4]. The focus over the past several years has been to develop circuits that address various aspects of neuromorphic electronics including designing the basic elements of the neural architecture: neurons and synapses.

The human brain contains around 10^{11} neurons and 10^{15} synapses. To architect systems with such great computational power and remarkable energy efficiency in electronics is a daunting challenge. Evolution has provided some lessons on how the brain achieves such efficiency. The primary mode of communication between neurons in the brain is encoded in the form of impulses, action potentials or spikes. The brain generates these spikes at much slower speeds (order of 10–100 Hz) compared to electrical impulses that encode the zeros and ones in the modern computer (order of GHz). Thus, the brain has evolved to be a very power efficient machine by conserving energy via spike based operation while also operating at very slow speeds.

The neurons are also complex adaptive structures that make connections between each other via synapses. These synapses can change their function dramatically depending upon the spike encoded messages they receive. These changes are thought to provide energy efficiency during signal transmission as well as flexibility to direct the storage and recall of information in the brain [3], [5]. Thus, in this paper, we will focus on designing the neurons and synapses of the brain in electronics with the goal of energy efficient design.

Recent advances in electronics in CMOS integrated circuit design [6] have enabled the packing of billions of transistors within a square cm by reducing the size of the transistor. It is now conceivable to mimic brain like circuits with such advances. These electronic systems run on power supply voltages (~ 1 V typically) but the performance of traditional analog circuits can significantly degrade at such low power supply voltages. For ultra low power electronic systems, the transistor is instead operated in a regime below its threshold voltage (or the subthreshold regime) where the current decreases exponentially as the magnitude of the transistor's gate-to-source voltage is decreased. This combination of low currents with low operating voltage enables ultra low power designs to be realized [3]. Further reduction in power can be achieved by designing brain-like spike-type circuits that are mostly active only during spike events.

In this paper, we will present electronic implementations of ultra-low power neurons and synapses using the subthreshold regime principles. These circuits operate with spike-type signals. The synapse includes an adaptation circuit that adjusts the weight or gain of the synapse according to a biologically-inspired spike timing dependent plasticity (STDP) learning rule. The goal of our work in this paper is to optimize the circuits for energy consumption and thus the designs are phenomenological and does not focus on biological fidelity (e.g., does not explicitly model Na^+ or Ca^{2+} channel dynamics or receptor dynamics).

We will show (a) a neuron circuit based on the use of a hysteresis comparator and (b) a synapse with STDP circuit based on 5 transconductance amplifiers and three capacitors. The topologies are intended for low power and low energy per spike operation. We have implemented both circuits in a 90 nm CMOS technology. These circuits exhibit high energy efficiency while

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J. M. Cruz-Albrecht and M. W. Yung are with the Microelectronics Laboratory, HRL Laboratories LLC, Malibu, CA 90265 USA (e-mail: jcruz@hrl.com).

N. Srinivasa is with the Information and System Sciences Department, Center for Neural and Emergent Systems, HRL Laboratories LLC, Malibu, CA 90265 USA.

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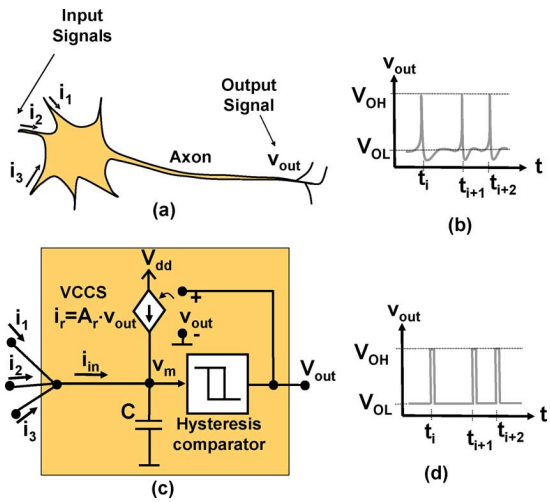

Fig. 1. (a) Simplified diagram of a biological Neuron. (b) Typical output signal of a biological neuron. (c) Top level diagram of the electronic neuron. (d) Output signal of the electronic neuron.

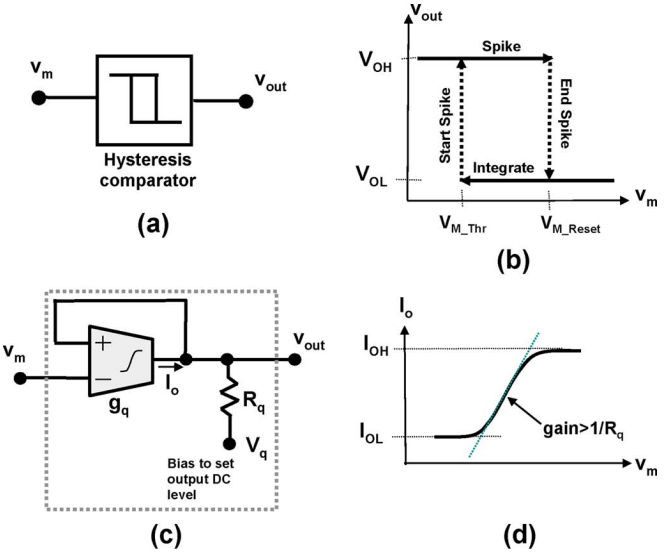

Fig. 2. (a) Hysteresis comparator. (b) Input-output characteristic of comparator. (c) Implementation of comparator. (d) Input-output characteristic of transconductance amplifier g_q.

reproducing key functional operating characteristics of the biological neuron and synapse. To our knowledge, both these circuits consume the lowest power and energy per spike operation reported to date.

II. Circuit Architecture of Neuron and Synapse

A. Neuron

The neuron is a very complex entity with sophisticated interplay between various ion channels as discovered by Hodgkin and Huxley [7]. There have been several circuit implementations that address this complexity using neurmorphic electronics (for e.g., in [8], [37]). There have several other models that model the neuron dynamics in a phenomenological fashion such as the Izhikevich model [9], Fitz–Nagumo neuron [10] and the adaptive exponential integrate and fire model [11]. In this paper, we will implement the most basic type of phenomenological neuron model commonly known as the leaky integrate and fire neuron model [12]–[14]. The membrane potential, v_m, of the leaky integrate and fire model [Fig. 1(a)] can be determined by

$$\tau_m \frac{dv_m}{dt} = -\alpha v_m + \sum_i I_i - \sum_j I_j$$
$$\text{where } I_i = w_i^{ex} \cdot v_{mi} \text{ and } I_j = w_j^{in} \cdot v_{mj}. \quad (1)$$

The constant α is the decay rate, τ_m is the membrane time constant, I_i is the total excitatory input current, I_j is the total inhibitory input current, w_i^{ex} is the synaptic conductance for the i^{th} excitatory input synapse and w_j^{in} is the synaptic conductance for the j^{th} inhibitory input synapse. In our circuit implementations, for simplicity, we will only consider the case with excitatory input currents and the neurons will also not exhibit any refractory period.

Fig. 1(a) shows a simplified diagram of a biological neuron. The neuron receives multiple excitatory input current signals $(i_1, i_2, i_3 \ldots)$ and produces a single output signal, v_{out}. Fig. 1(b) shows an example of a typical output signal. It consists of a stream of spikes (pulses of short duration). The output information is encoded into the timing of these spikes $(t_1, t_2 \ldots)$. A high level circuit model of our implementation of the neuron is shown in Fig. 1(c). It consists of a capacitor, a hysteresis comparator, and a voltage controlled current source (VCCS). Fig. 1(d) shows the typical output signal of the electronic neuron. The output information is encoded into the timing of these spikes $(t_1, t_2 \ldots)$. The spikes are asynchronous; they are not aligned to any clock. The voltage amplitude of the output can have only two possible values: a low value denoted by $\mathrm{V_{OL}}$ and a high value denoted by $\mathrm{V_{OH}}$. This type of time-asynchronous binary-amplitude signals can encode analog information [15]–[17]. The use of binary amplitude signals has the advantage that it simplifies the implementation of internal circuitry and reduces the power consumption. Two examples of related neuron circuits are show in [4], [31]. The neuron of [4] a comparator, two capacitors, and uses a switched current. In our circuit we use only one capacitor. The neuron of [31] uses a hysteresis comparator, a capacitor and nonlinear analog resistor based on CMOS circuit. In our implementation we do not use a nonlinear resistor.

During a time interval at which neuron output is at the low value $\mathrm{V_{OL}}$ the VCCS does not produce any current output. The capacitor is used to integrate all the incoming currents. The voltage variable v_m contains that integral value. When v_m reach a certain threshold the output of the neuron goes to a high value $\mathrm{V_{OH}}$ (spike event). This in turn causes the VCCS to produce a current that forces v_m to revert to a reset voltage and also ends the spike.

The detailed implementation of the hysteresis comparator of the neuron is shown in Fig. 2. Fig. 2(a) show a block diagram of the comparator. The input is v_m and the output is v_{out}. Fig. 2(b) shows the output-input transfer characteristic of the comparator. The output is high during the spike interval of the neuron and low during the integration (no spike) interval.

We use an inverting-type comparator as it can be implemented more efficiently (less components) than a non-inverting comparator. This has no effect in the functionality of the neuron or

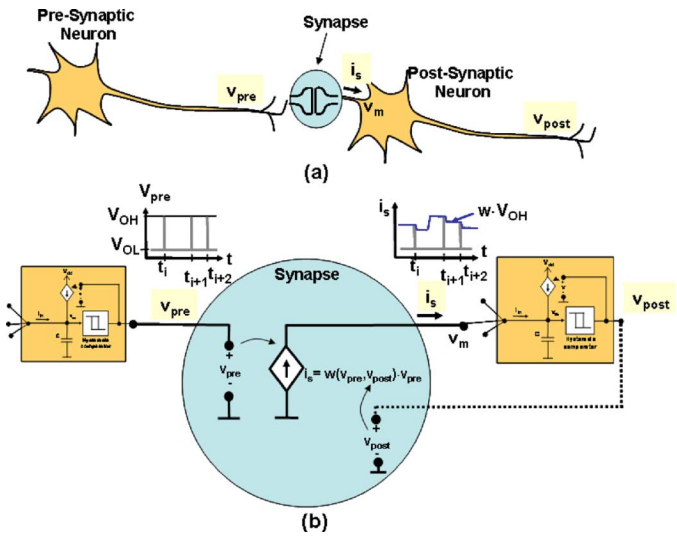

Fig. 3. (a) Simplified diagram of biological synapse interconnecting two neurons. (b) Top level diagram of Synapse circuit with example of typical waveforms of input voltage and output current.

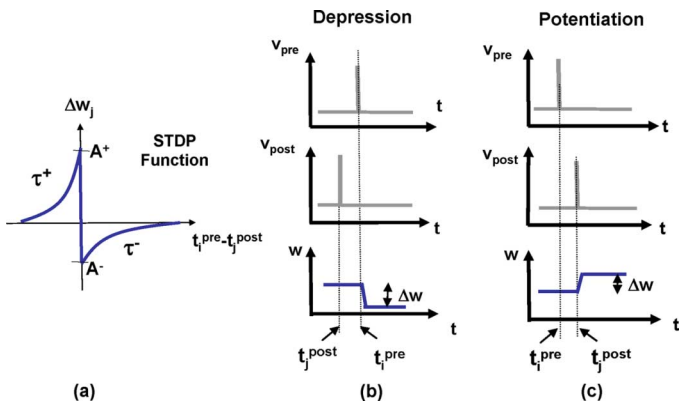

Fig. 4. (a) The STDP function to modulate w is defined by four parameters (A^+, A^-, τ^+, τ^-). The change Δw (b) for the case of depression and (c) for the case of potentiation is dependent on $(t_i^{pre} - t_j^{post})$ (see text for details).

in the output waveform, except in the sign of some circuit signals as compared to traditional integrate and fire neurons [13], [14]. In our neuron, excitatory inputs are represented by negative currents (that discharge the capacitor C). Also, in our neuron the internal voltage v_m decreases during the integration interval.

Fig. 2(c) shows the implementation of the hysteresis comparator. It consists of a nonlinear transconductance amplifier, g_q, and a resistor, R_q. A feedback wire connects the output of the amplifier to its positive input terminal. Fig. 2(d) shows the input-output characteristic of the amplifier. The output current saturates at two values. This type of nonlinear transfer characteristic can be implemented with very simple transconductance amplifiers normally used in transistor differential pairs and current mirrors. For proper operation the small signal gain of the transconductance amplifier is set to a higher value than $1/R_q$. This ensures that the circuit of Fig. 2(c) has enough positive feedback to force its output to have only two possible stable values. This positive feedback within the comparator also enables to achieve sharp spikes.

B. Synapse With STDP

The synapse is the junction between two interconnected neurons. The synapse has two terminals. One terminal is associated with the neuron providing information (this neuron is referred as the pre-synaptic neuron). The other terminal is associated with the neuron receiving information (this is referred as the post-synaptic neuron). Fig. 3(a) shows a diagram of a biological synapse which is chemical in nature. In neuromorphic circuits, this chemical synaptic dynamics is abstracted as an electronic circuit.

Fig. 3(b) shows a simplified model of the synapse circuit. The input terminal of the synapse is designated to receive the output voltage signal of a presynaptic neuron. This voltage is called the presynaptic input voltage and is denoted as v_{pre}. The output terminal of the synapse is designated to provide a current into the input node of the postsynaptic neuron. This output current of the synapse is denoted as i_s. This current is determined by v_{pre} and by an internal weight variable w commonly referred to as the synaptic conductance. The current i_s is independent of the voltage at the output terminal (v_m). The voltage v_{post} is provided to the synapse via a feedback path from output of the postsynaptic neuron. This path is shown as a dotted line at the bottom of Fig. 3(b).

For a synapse with fixed synaptic conductance, w, only the input and the output terminals would be required. However, in our synapse the weight is not fixed but is internally adjusted according to a learning rule called the spike-timing dependent plasticity or STDP [Fig. 4(a)] discovered in the brain [18]–[20]. The STDP function modulates the synaptic conductance w based on the timing difference $(t_i^{pre} - t_j^{post})$ between the action potentials of pre-synaptic neuron i and post-synaptic neuron j. There are two possibilities for the modulation of synaptic conductance. If the timing difference $(t_i^{pre} - t_j^{post})$ is positive, then synapse undergoes *depression* [Fig. 4(b)] according to the exponential decay curve on the right half of the STDP function. The synaptic conductance w is modified by Δw at that timing difference. If the timing difference $(t_i^{pre} - t_j^{post})$ is negative, then synapse undergoes *potentiation* [Fig. 4(c)] according to the exponential decay curve on the left half of the STDP function. The synaptic conductance w is modified by Δw at that timing difference. If the timing difference is too large in either direction, there is no change in the synaptic conductance. The STDP function has four parameters (A^+, A^-, τ^+, τ^-) that control the shape of the function. The A^+ and A^- correspond to the maximum change in synaptic conductance for potentiation and depression respectively. The time constants τ^+ and τ^- control the rate of decay for potentiation and depression portions of the curve as shown in Fig. 4(a).

If there are more than one pre or post-synaptic spikes within the time windows for potentiation or depression, then a way to account for these multiple spikes is a subject of active research [21]. In our implementation, we follow the model described in [22] called the additive STDP where the dynamics of potentiation $P(t)$ and depression $D(t)$ at a synapse are governed by the exponential decays which can be modeled by

$$\tau^- \frac{dD(t)}{dt} = -D(t) \tag{2}$$

$$\tau^+ \frac{dP(t)}{dt} = -P(t). \tag{3}$$

Whenever a post-synaptic neuron fires a spike, $D(t)$ is decremented by an amount A^- relative to the value governed by (2). Similarly, every time a synapse receives a spike from a pre-synaptic neuron, $P(t)$ is incremented by an amount A^+ relative to value governed by (3). These changes can be summarized as

$$D(t) \leftarrow D(t) + A^- \tag{4}$$
$$P(t) \leftarrow P(t) + A^+. \tag{5}$$

These changes to $P(t)$ and $D(t)$ affect the change in synaptic conductance as follows. If the post-synaptic neuron fires a spike, then the value of $P(t)$ at that time, $P^*(t)$, is used to increment Δw for the duration of that spike. Similarly, if the pre-synaptic neuron fires a spike that is transmitted by the synapse, then the value of $D(t)$ at that time, $D^*(t)$, is used to decrement Δw for the duration of that spike. Thus, the net change Δw is given by combining these two values as

$$\Delta w = P^*(t) - D^*(t). \tag{6}$$

The final effective change to the synaptic weight w due to STDP is thus expressed as

$$w(t) \leftarrow w(t) + \Delta w. \tag{7}$$

The key advantage of this approach is that it can be readily implemented in hardware without the need for storing the timing difference values.

Fig. 5(a) shows a diagram of the electronic synapse. It has two components: a synapse core and a STDP circuit. The synapse produces the final output in the form of a current that is scaled by the synaptic conductance w while the dynamics of changes in w is dictated by the STDP circuit. These computations are performed by the circuit shown in Fig. 5(b). The circuit has two voltage inputs (v_{pre} and v_{post}) and one current output i_s. The circuit is composed of five transconductance amplifiers and three integrators (two of the integrators are leaky). Two of the transconductance amplifiers (g_1 and g_2) have an analog voltage input and analog current output. The other three amplifiers have in addition an extra voltage control input that is used to enable/disable its operation depending on presence/absence of a spike.

Examples of previous STDP circuits are described in [29], [30], [25]. The circuit of [29] implements similar exponential-type STDP function as this paper [shown in Fig. 4(a)]. The circuit of [29] is based on analog blocks and flip-flop digital blocks. Our circuit is based in analog blocks and digital inverters. The circuit of [30] also implements similar exponential STDP functions as this paper and uses only analog blocks and switches. But all analog blocks remain operating all the time. The circuit presented in our paper can reduce power by shutting down analog components when a spike is not present. This aspect helps in achieving good energy consumption figures. The circuit of [25] implements a related STDP function using analog blocks. However the shape STDP of [25] is not strictly of an exponential-type. Our circuit is intended to implement exponential-type STDP.

The synapse core is implemented by a transconductance amplifier with enabling control. The v_{pre} signal is connected to the enable control terminal of the amplifier. The weight analog voltage signal, $w(t)$, is connected to the analog input of the amplifier. Every time that there is a voltage spike at v_{pre}, the amplifier is enabled and it produces a current spike at its output. The amplitude of the current spike i_s depends on the analog weight $w(t)$.

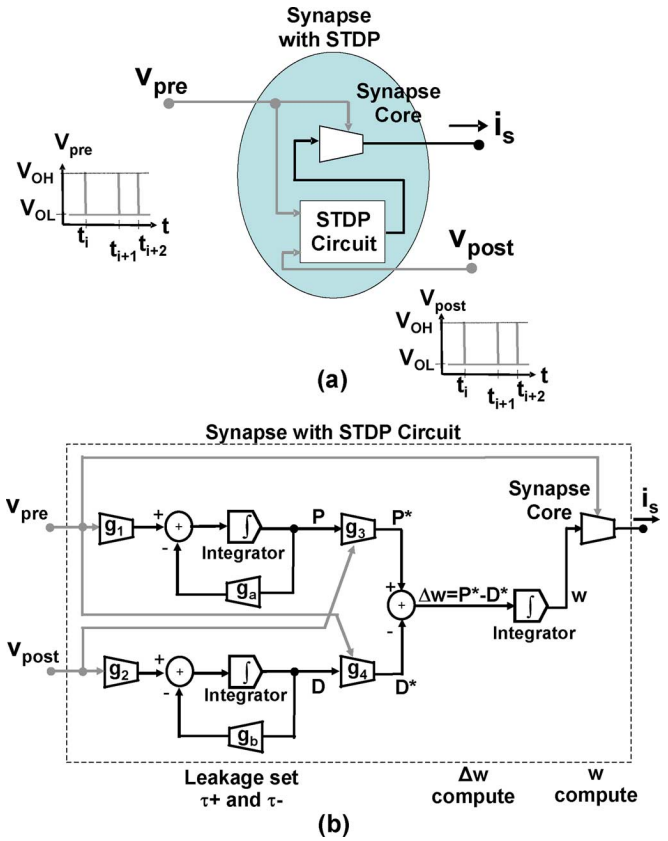

Fig. 5. The synapse with STDP circuit. (a) Overall circuit. (b) Details of the circuit.

The STDP circuit determines the value of $w(t)$ and is composed of four transconductance amplifiers (g_1, g_2, g_3 and g_4) and three integrators (two of them leaky) as shown in Fig. 5(b). The front-end of the STDP circuit (four amplifiers and two leaky integrators) is used produce a correction signal Δw according to the STDP function (described by (2) through (7)).

The top half of the STDP circuit [in Fig. 5(b)] scales the signal v_{pre} and transforms (by leaky integration) the incoming spikes time-domain step functions with exponential decay with time constant of τ^+. The amplitude of this exponential time domain function, $P(t)$ [equation (3)], is sensed by amplifier g_3 when a subsequent spike at v_{post} occurs. Every time that a spike at v_{post} follows one at v_{pre}, the amplifier g_3 produces a current pulse that encodes the positive correction signals $P^*(t)$ of Δw.

The bottom half of the STDP circuit [in Fig. 5(b)] scales the signal v_{post} and transforms (by leaky integration) the incoming spikes time-domain step functions with exponential decay with time constant of τ^-. The amplitude of this exponential time domain function, $D(t)$ [equation (2)], is sensed by amplifier g_4 when a subsequent spike at v_{pre} occurs. Every time that a spike at v_{pre} follows one at v_{post}, the amplifier g_4 produces a current pulse that encodes the negative correction signals $D^*(t)$ of Δw.

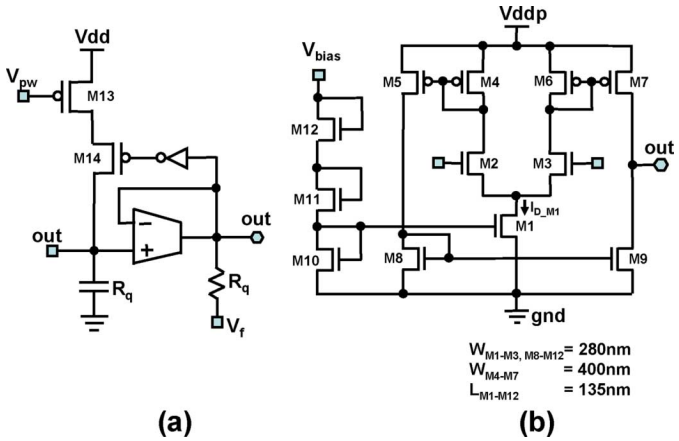

Fig. 6. (a) Transistor-level diagram of the neuron. (b) Detail of transconductance amplifier.

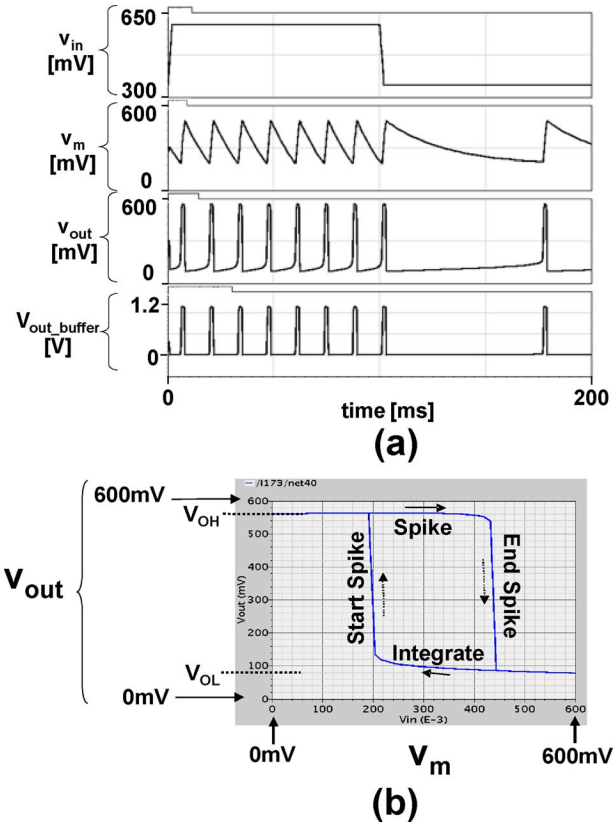

Fig. 7. (a) Transistor-level simulation of the neuron (see text for details). (b) Hysteresis curve for the neuron during current integration and spike firing.

The final integrator of the STDP circuit is used to convert Δw into $w(t)$ as shown in Fig. 5(b).

It should be noted that the control of amplifiers with enable/disable capability is done using binary-amplitude signals (v_{pre} or v_{post}): a low voltage at the control disables the amplifier (in that situation the amplifier will have no output current and also will not dissipate any power) and a high control voltage enables the normal operation of the transconductance amplifier. The extra control input enables these amplifiers to be used as compact multipliers of an analog signal with binary amplitude spike signals. The circuit also is power efficient as it consumes no power in the disabled mode (which occurs most of the time for circuits with spiking dynamics).

III. Transistor Level Implementation

A. Neuron: Transistor-Level Design and Simulation

The neuron circuit is composed of a capacitor, a transconductance amplifier, an output resistor, an inverter, and two transistors. Fig. 6(a) shows a top-level transistor-level diagram of the neuron. The two transistors are used to implement a current source and a switch. The current source is enabled while there is a spike. Fig. 6(b) shows a detail of the transconductance amplifier. It is composed of a differential pair (transistors M2 and M3) and three current mirrors (transistors M4–M9). It also contains a bias circuitry (M10–M12). The circuit power supply is 0.6 V. All the transistors are super high $\mathrm{V_T}$ type ($\mathrm{V_T} = 0.66\,\mathrm{V}$). They operate in the deep subthreshold regime. The differential pair tail transistor (M1) is biased at a gate to source voltage of $\mathrm{V_{GS}} = 171\ \mathrm{mV}$ and produces a simulated drain current of $\mathrm{I_D} = 13\ \mathrm{pA}$.

The circuit has two feedback loops. The inner feedback loop is from the output of the gm cell to its positive input. Even though this is a positive feedback loop, this loop does not produce unstable oscillations if the amplifier has a nonlinear saturating characteristic as shown in Fig. 2(d). We design the amplifier to saturate (not increase its output current) once the difference $|\mathrm{inn\text{-}inp}|$ is large. This loop forces the output to one of two possible states (high or low).

A computer simulation of the transistor level circuit was performed as shown in Fig. 7. The top trace in Fig. 7(a) is an external input voltage that controls an internal VCCS to generate a current input for the neuron. The second trace of Fig. 7(a) shows the internal capacitor voltage v_m while the third trace shows the neuron output. The fourth trace shows the neuron output after being amplified by a buffer. These buffers operate at 1.2 V and amplify the neuron spikes from 0.6 V to 1.2 V. This buffer is not part of the neuron, but is included to drive external instrumentation. The hysteresis curve between v_m and v_{out} for a single integrate and fire neuron is simulated in Fig. 7(b).

This simulation shows the response of the neuron circuit. For the first 100 ms a current of $\sim 5\ \mathrm{pA}$ is injected into the neuron. That causes the neuron to spike with a frequency of about 80 Hz. In the next 100 ms the injected current is about 1 pA which causes the neuron to spike at a frequency of about 13.3 Hz. It should be noted that the simulated frequencies in this example have the same order of magnitude as biological neurons and has similar phenomenological behavior.

B. Synapse With STDP: Transistor-Level Design and Simulation

Fig. 8(a) shows a top level transistor level diagram of the synapse with STDP. The circuit also operates at 0.6 V. The circuit has five transconductance amplifiers (two without enable control and three with enable control), three capacitances (implemented by two capacitors at the left, and a set of two parallel

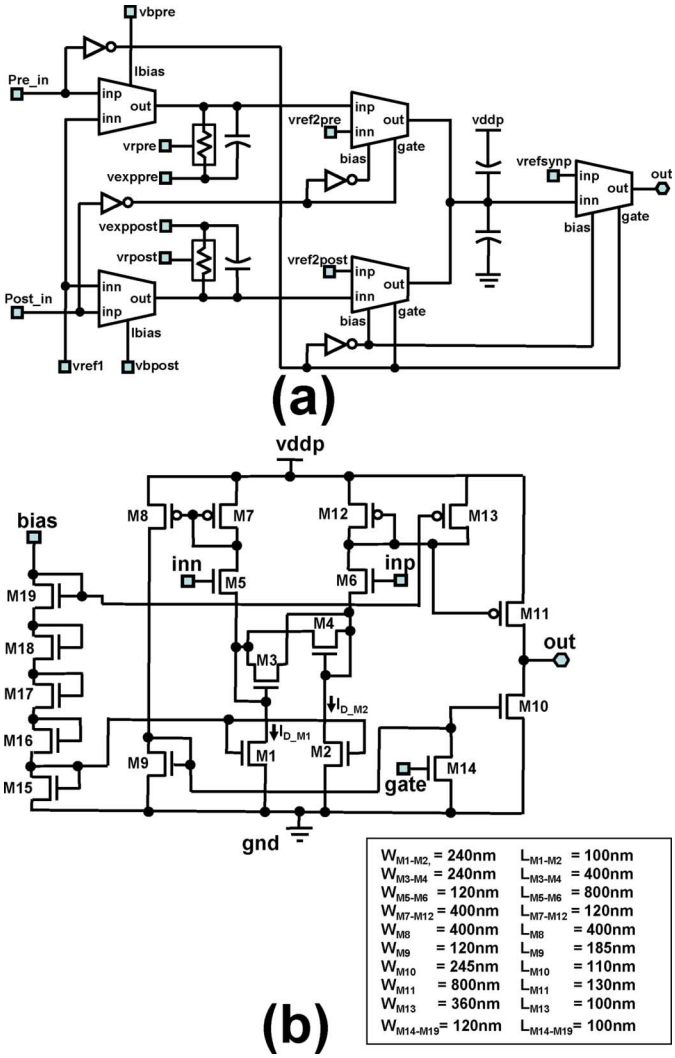

Fig. 8. (a) Top-level diagram of synapse with STDP. (b) Detail of transconductance amplifier with enable/disable capability.

connected capacitors at the right), two resistors (each one implemented by a pass transistor) and four inverters. The inverters (each one implemented by 2 transistors) are part of the control circuitry of the transconductance amplifiers with enable/disable capability.

The capacitance of each one of the two capacitors at the left in Fig. 8(a) is 200 fF. This capacitance and the resistance of the two active resistors sets the time constants τ^+ and τ^-. Smaller capacitances and larger resistors can be used to reduce area but very small capacitances can lead to higher mismatch. The capacitance of two combined capacitors on the right in Fig. 8(a) is 4 pF. This larger capacitance is selected to hold an approximately constant weight value between consecutive synaptic operations, even in the presence of leakage currents of the order of 0.1 pA.

The two amplifiers on the left half of Fig. 8(a) have the same topology as shown in Fig. 6(b). The three amplifiers on the right portion of Fig. 8(a) have enable/disable capability. Fig. 8(b) shows a detail of the transconductance amplifier with enable/disable capability used for the synapse. The analog input is provided via the terminal marked as "inn". The terminals marked as "bias" and "gate" are used for enabling/disabling control. In the disabled mode all the transistors are OFF. In that mode the amplifier ideally would produces no output current (in our subthreshold transistor level implementation about one order of magnitude lower than in enabled mode) and also consumes significantly less power. During normal operation the transconductance amplifiers are most of the time in the disabled mode. In our STDP circuit the enabling/disabling control in the three amplifiers the right of Fig. 8(a) are used to get proper functionality and to reduce power. The enabling/disabling control is not needed for proper functionality of the two amplifiers at the left of Fig. 8(a). We do not use enabling/disabling control for these two amplifiers. However, the use of enabling/disabling control could be possible in these amplifiers if it would be desired to further reduce power.

The transconductance amplifier of Fig. 8(b) is composed of a differential pair (implemented by transistors M5 and M6) and three current mirrors (implemented by M7–M8, M9–M10, and M12–M11). The differential pair is source-degenerated to increase the linearity (transistors M3-M4 are used to implement a resistance between the sources of the two transistors of the differential pair). The differential pair is biased by tail currents (implemented respectively by M1 and M2). A bias circuitry is implemented using (M15–M19). The bias circuitry sets the bias current on the tail transistors. This bias current is adjusted by the control signal "bias". The signal "bias" is high in the enable mode (current flowing through M15–M19) and low in the disabled mode (no current flowing through M15–M19, which also sets all other currents in the circuit to approximately zero). Two additional control transistors (M13 and M14) are included. They are used to further force all the output transistors (M10 and M11) in the OFF position when the amplifier is in the disabled mode. The circuit voltage supply is 0.6 V. All the transistors are super high $\mathrm{V_T}$ type ($\mathrm{V_T} = 0.66$ V). They operate in the deep subthreshold regime. When the transconductance amplifier is in the enable mode each one of the tail transistors (M1 and M2) is biased at a gate to source voltage of $\mathrm{V_{GS}} = 95$ mV and produces a drain current of $\mathrm{I_D} = 5$ pA.

The transconductance amplifier used to implement $\mathrm{g_3}$ (see Fig. 5) is identical to the one shown in Fig. 8(b). The transconductance amplifiers used to implement $\mathrm{g_4}$ (see Fig. 5) is identical to the one shown in Fig. 8(b) except that transistors M10 and M11 have half the width. This reduces its nominal gain by factor of 2. This allows to have a nominal ratio of $\mathrm{A^+/A^-} = 2$, where $\mathrm{A^+}$ and $\mathrm{A^-}$ are coefficients of the STDP curve.

The transconductance amplifiers used to implement $\mathrm{g_1}$ and $\mathrm{g_2}$ (see Fig. 5) have the same topology as that shown in Fig. 6(b), but with tail currents of 1.64 pA. Fig. 9 shows an example of transistor-level simulation of the STDP circuit. The two bottom traces show an example of waveforms of v_{pre} and v_{post} that are received by the synapse with STDP. The two top traces show the waveforms $P(t)$ and $D(t)$ that are generated by the STDP circuit (see Fig. 5). The time evolution of these two traces (as shown in Fig. 9) has the dynamics given by (2) through (5).

The implemented circuits include auxiliary circuitry for bypassing capacitors and an output buffer. We have implemented two versions of the low power circuits. In one version the buffer monitors the weight produced at the output of the STDP circuit.

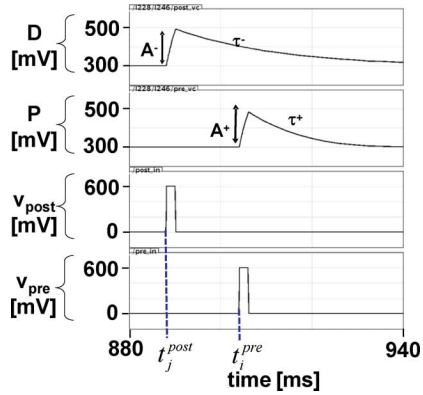

Fig. 9. Transistor-level simulation of a synapse with STDP.

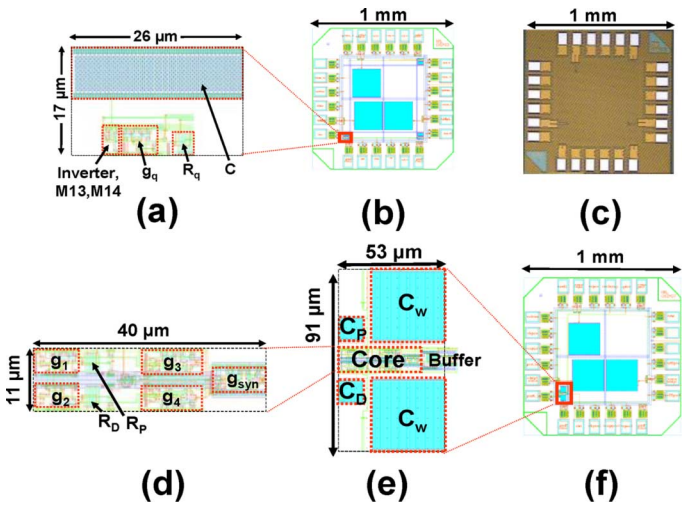

Fig. 10. (a) Layout of neuron circuit. (b) Layout of chip with neuron circuit. (c) Example of micrograph of a chip with neuron. (d) Layout of synapse with STDP core circuit without capacitors. (e) Layout of a synapse with STDP circuit including capacitors. (f) Layout of a chip with synapse and STDP circuit.

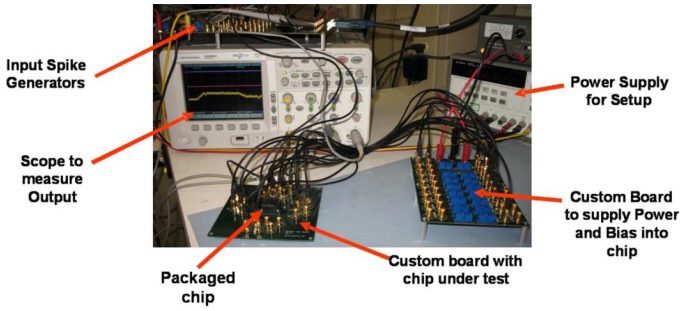

Fig. 11. Photograph of test set up.

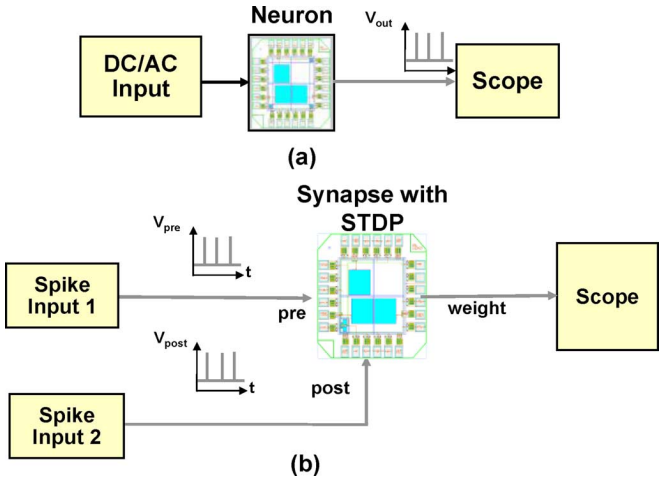

Fig. 12. Diagram of test set up to test the (a) neuron and (b) synapse with STDP circuit.

In another version the monitored signal is the output current of the synapse, i_s. The current is fed into an on-chip resistor (active resistor) to produce a voltage. That voltage is connected to the input terminal of the output buffer.

C. Layout of Neuron and Synapse With STDP Circuits

Fig. 10(a) shows the layout of the 90 nm CMOS neuron circuit. The circuit area of a neuron, including integrating capacitor, is 26 μm$\times$ 17 μm. Fig. 10(b) shows the layout of the neuron chip. The neuron chip has three copies of neuron circuits as well as bypassing circuitry, and output buffers. The output buffers are designed to be able to drive external equipment (oscilloscopes). Fig. 10(c) shows a photo of a neuron chip. Each chip is 1 mm on the side.

Fig. 10(d)–(e) show the layout of synapse with STDP. The core active area, not including capacitors, is 40 μm$\times$ 11 μm. The circuit area of the synapse with STDP (including circuit capacitors), is 53 μm$\times$ 91 μm. The synapse chip has one copy of the synapse with STDP circuit as well as bypassing circuitry, and output buffers. The output buffers are included to facilitate testing. The output buffers are designed to be able to drive external equipment. The fabricated chip has the same size and pad frame as the neuron chip of Fig. 10(c). The chips use 24 pads to access inputs, outputs and to provide bias and power.

IV. Experimental Testing and Data

A. Test Setup

For testing the neuron we used a DC and an AC source. To test the synapse with STDP we used two spike sources. We controlled the delay between spikes produced by the two sources.

The experimental setup to test the neuron and the synapse with STDP is shown in Fig. 11. We built a custom main board (see Fig. 11 that interfaces the chip to SMA connectors while other boards supply input signals and bias signals. We used a scope to monitor the outputs. Fig. 12 shows a diagram of the setup to test the neuron and the synapse with STDP. In the setup for the synapse for each pair of pre and post synaptic spikes, we monitored the change in the synapse weight $w(t)$.

The experimental data for the neuron is shown in Fig. 13. Fig. 13(a) shows an example of neuron operation for a DC input. The output signal in this example is a periodic stream of spikes at $\sim$ 47 Hz. Fig. 13(b) shows the operation of the neuron for an AC voltage. The top trace shows a sinusoidal voltage that is applied to the chip. This is converted into an analog current by an internal interface VCCS (voltage controlled current source). The current is then converted by the neuron into stream of spikes with variable rate in the range of 0–260 Hz. It should be noted

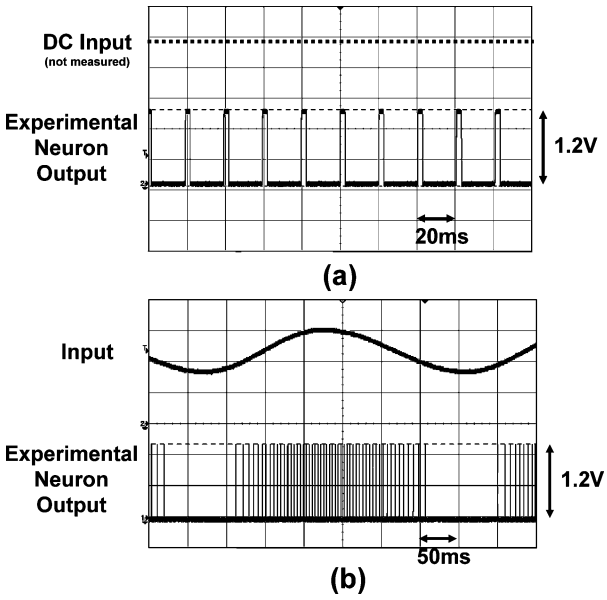

Fig. 13. Experimental data for the spiking neuron. (a) DC input. (b) AC input.

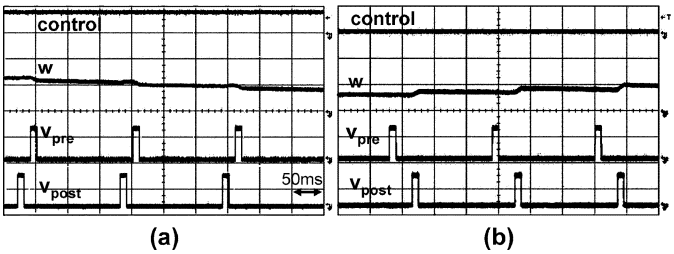

Fig. 14. The experimental measurement for the synapse with STDP for the cases of (a) depression and (b) potentiation. Vertical scale for control is 1 V/div. Vertical scale for w is 2 V/div. Vertical scale for v_{pre} and v_{post} is 500 mV/Div.

these spike rates occur within the same order of magnitude as in biological neurons.

B. Synapse With STDP

Fig. 14 shows an example of operation of STDP of a synapse. The two bottom traces shows the two signals applied into the chip, one with v_{pre} and another with v_{post}. The second trace from the top shows the measured weight produced by the STDP circuitry. The top trace shows a signal that we used to control the relative timing of our spike generator sources. Fig. 14(a) shows the case of spikes at v_{pre} happen soon after spikes at v_{post}. A weight decrease, or depression, was observed every time a spike at v_{pre} follows a spike at v_{post}. Fig. 14(b) shows the case of spikes at v_{post} happen soon after spikes at v_{pre}. A weight increase, or potentiation, was observed every time a spike at v_{post} follows a spike at v_{pre}. This measured weight change (decrease or increase) according to the order of spikes is consistent with biological synapses.

Fig. 15 shows a diagram of the experimental STDP data and a least square exponential fit for the chip under nominal bias conditions. The experimental curve of Fig. 15 follows the desired shape as shown in Fig. 4(a). This curve of Fig. 15 also matches biological experimental STDP curve shape [19], [20].

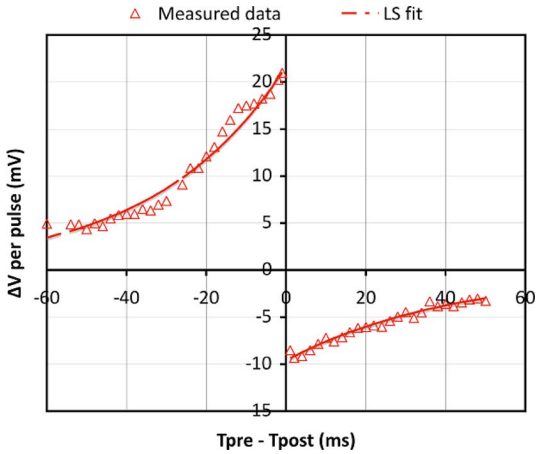

Fig. 15. STDP data measured for the pico power version of the 90 nm CMOS chip.

TABLE I
COMPARISON OF POWER, SPIKE RATE AND ENERGY PER SPIKE BETWEEN OUR NEURON CIRCUIT AND OTHER CIRCUIT DESIGNS

Reference	Power [pW]	Rate [Spikes/s]	Energy per Spike [pJ]
Indiveri[14]	~570,000	200	2,850
Lee [26]	163,400	~15,000	10.9
Wijekoon [24]	100,000-600,000,000	-	8.5-9
This work	40.2	100	0.4

The experimental data follow an exponential decay curve as desired. The A^+ is larger than A^-, as typically desired. The τ^- is larger than τ^+, as typically desired. In this example the time constants of the exponentials fitted to the experimental data are in the order of 30 ms to 45 ms. These values of A^+, A^- , τ^+ and τ^- (and the total area under each one of the two exponential curves) can be adjusted by tuning the chip level bias and are typical of biologically measured data [19], [20].

V. SUMMARY OF PERFORMANCE

We have shown the circuit of a neuron and a synapse with STDP. Table I shows a comparison of the power, spike rate, and energy per spike from hardware neuron in comparison to other neuron designs. Our hardware neuron consumes around 40 pW of power and 0.4 pJ of energy per axonal spike for a spike rate of 100 Hz. This compares very favorably in terms of both power and energy efficiency with other designs [14], [23]–[27].

We have also fabricated and tested a higher speed version of the neuron described in the paper. For that version the power is 7,800 pW, the rate is 6,000 spikes/s and the energy per spike is 1.3 pJ. For this neuron we use a different design where a similar capacitance is driven by a synapse with higher input currents (this reduces the time to fire). This neuron has similar gm cell topology and switches. But all the circuitry is biased at higher current to produce spikes with shorter rise and fall times and shorter pulse duration.

Table II shows a comparison of the power, spike rate, and energy per spike from hardware synapse with STDP in comparison to other designs. Our synapse with STDP consumes around 37

TABLE II
COMPARISON OF POWER, SPIKE RATE AND ENERGY PER SPIKE BETWEEN OUR SYNAPSE WITH STDP CIRCUIT AND OTHER CIRCUIT DESIGNS

Reference	Power [pW]	Rate [Spikes/s]	Energy per Spike [pJ]
Zhang [32]	-	-	480
Tanaka [28]	~(1.25-2.5)x10^8	~3x10^6	~42-83
This work	37	100	0.37

pW of power and energy of 0.37 pJ per spike (either presynaptic or postsynaptic) for a spike rate of 100 Hz (100 total spikes into the STDP either presynaptic or postsynaptic). This also compares very favorably in terms of both power and energy efficiency with other designs [28].

The work of [32] implements a STDP function by using a modified transistor technology combined with CMOS. This STDP function uses 480 pJ per pulse (spike), as listed in [32]. The power and spike rate are not stated in [32] and are not listed in our table.

The work of [28] implements STDP circuits in CMOS. The energy per spike is not provided in [28]. The data stated in the table is derived approximately as follows. The [28] shows a power of 250 μW for a block containing one STDP circuit with two synapses. The power with a circuit with one STDP with one synapse is assumed in our table to be in the range of 125 μW to 250 μW. It should be noted that [28] lists two types STDP characteristics (symmetric and asymmetric). We are using the data for the symmetric STDP characteristic because the power is stated explicitly. In our work the goal was to implement an asymmetric characteristic, but we believe that the type characteristic (symmetric/asymmetric) does not have a significant impact on power. The [28] does not list the rate but provides a plot with spike rates in STDP input channels of ~ 3 MHz. With this data we estimate that the approximate energy per spike for the circuit of [28] could be in the range of 42–83 pJ per spike.

The STDP circuits described in [29], [30] implement STDP in CMOS. The power energy per spike for an individual synapse with STDP block is not explicitly provided, in [29], [30]. However, the work of [29] indicates that one of the internal current of the STDP is in the order of μA. This is about 6 orders of magnitude higher than any of our internal currents, which are in the order of pA. The internal current of μAs (and supplies over 1 V) would limit the minimum power of the STDP circuit of [29] to at least the order of μWatts, which is about 5 orders of magnitude higher than our power. A comparison table in [32] estimates that the energy per spike of the STDP circuits of [29] and [30] are $\sim 4{,}500{,}000$ pJ and 900 pJ respectively. This is higher than the other data listed in our table. We have not included this data in our table.

Other work in STDP circuits has been done by using memristors [33] and floating gate technology [34], [35]. The STDP power and energy per spike figures are not listed in [33]–[35]. The work of [33] achieves a STDP function by using a memristor combined with peripheral control circuitry that generates memristor programming signals from neuron spikes. The current across the memristor in [33] is in the order of tens of nA, and the programming voltages are ($+3.2$ V, -2.8 V). In our low-power STDP circuit we use currents several order of magnitude lower (in the pA range) and all voltages are also lower. The work of [34], [35] shows how to achieve a STDP function by combining a core floating-gate transistor with peripheral control circuitry that generate programming signals. The work of [34] include an example of operation of a core floating gate transistor implemented in 0.35 μm CMOS and driven with programming control signals. The work of [35] shows transistor-level circuits and simulation of STDP functions, in 60 nm CMOS, for floating-gate transistors and control programming circuits. The programming voltages are of up to 15 V in [34] and a few volts in [35]. In our work, the synapse with STDP circuit does not need any peripheral control circuits to convert neuron spikes into programming signals and can directly accept spike signals from a neuron.

We have also fabricated and tested a higher speed version of the STDP circuit. For that version the power is 3,000 pW, the rate is 12,500 spikes/s and the energy per spike is 0.24 pJ. We believe that our neuron and the synapse with STDP have the lowest power and energy per operation (spike) reported to date.

VI. EXTENSIONS OF THIS WORK

In this paper we have focused on the design, fabrication and test results of elementary neuron, synapse and STDP circuits. These circuits can be used as the main building blocks to implement large, very low-power neural chips.

The size of each neuron is about 26 μm$\times$ 17 μm and each synapse with STDP about 53 μm$\times$ 91 μm. These elements can be combined using CMOS wire interconnect. Assuming a typical fixed mainly-local wire interconnect and reserving approximately 33% of a chip area for interconnect we estimate that over 10,000 elements (neurons elements or synapse with STDP elements) could fit in a 1 cm $\times$ 1 cm chip. The 33% of chip area can provide a total length of $\sim 100{,}000$ mm of wires (140 nm width and 280 nm pitch) per metal layer, or about 10 mm of wire per element.

The communication between elements can be done using spikes of amplitude 0.6 V. A core neuron by itself consumes 0.40 pJ per spike. Assuming a typical fixed mainly-local interconnect with CMOS axon wire segments up to 1 mm long the energy needed to transmit a spike in that wire is about 0.07 pJ. The total energy per spike in a neuron with a 1 mm axon wire is about 0.47 pJ. This includes spike generation and driving the axon. When multiple synapses are connected to a neuron axon, the signaling neuron needs also to drive the input capacitance of each connected synapse with STDP. In our case that input capacitance of each synapse with STDP is 0.8 fF and could be driven by using an energy of ~ 0.3 fJ per input spike. The total energy per spike for a neuron with a 1 mm axon wire and driving k synapses with STDP would be $(0.44 + k * 0.0003)$ pJ. For example, one neuron with a 1 mm axon and driving the input capacitances of 100 synapses with STDP would consume about 0.50 pJ per spike. This includes the spike generation and transmission. The power in a neuron with a 1 mm axon wire, driving the input stages of 100 synapses, and operating at a typical spike rate of approximately 100 Hz would be 50 pW. Each synapse with STDP circuit consumes energy of about

0.37 pJ per spike as described in the previous section. When operating at 100 Hz it consumes about 37 pW. The synapse with STDP presented does not regenerate the input spikes. However, in a network the synapse with STDP circuit could include a front-stage that regenerates the pulse width. This would make STDP insensitive to variations associated with pulse width changes. That front stage could operate with the same range of currents that we have used for the rest of the STDP. We estimate that this front stage would require less power than the STDP circuit. The total power in a network with 20,000 elements (each element being a neuron with axon or a synapse with STDP) could be in the order of 1 μW.

We have recently designed, fabricated and tested a variety of neural circuits based on the elementary neuron, synapse and STDP circuitry described in this paper. These neural circuits require multiplexing techniques to output the data via a limited number of chip pads. The circuit details and test results of those neural circuits are out of scope of this paper but will be described in a separate paper.

VII. Conclusion

We have presented neuron and a synapse with STDP integrated circuits. The neuron is based on a new circuit based on hysteresis comparator and a current reset. The hysteresis comparator is implemented by a nonlinear transconductance amplifier and a resistor. The synapse with STDP is based on a new circuit based on five transconductance amplifiers (three with enable control) and three capacitors. The circuits designed in 90 nm CMOS have the lowest energy per spike reported to date. Experimental data shows that the fabricated circuits perform the desired neuron and synapse operations, including STDP, comparable to biological neurons and synapses.

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Jose M. Cruz-Albrecht (S'88–M'97) received the B.S. and M.S. degrees in physics from the University of Seville, Seville, Spain, in 1987 and 1989, the M.Eng. degree (with high distinction) from the University of Leuven, Leuven, Belgium, in 1990, and the M.S. and Ph.D. degrees in electrical engineering and computer sciences from the University of California, Berkeley, in 1992 and 1996, respectively.

He has worked for the National Center of Microelectronics, Seville, Spain, the E.S.A.T-M.I.C.A.S. Laboratory of the K.U. Leuven, Heverlee, Belgium, the Electronics Research Laboratory, University of California, Berkeley, and with industry research laboratories. Since 2002, he has been with HRL Laboratories, Malibu, CA, where he is currently a Senior Research Staff Engineer. He has been involved in the architecture, design, modeling, and testing of analog chips, including cellular neural networks, chaotic circuits, high-speed ADC and DAC converters, time encoding circuits, amplifier circuits and biologically-inspired neural circuits, in CMOS, HBT, and GaN technologies. His research interests include the integrated circuit implementation of neural circuits and the design and analysis of nonlinear analog circuits.

Dr. Cruz has been on the program committee of the IEEE Custom Integrated Circuit Conference (CICC) and the Biologically Inspired Cognitive Architectures (BICA) conference. He has coauthored articles in two edited technical books and has coauthored 16 papers in journals and conference proceedings. He has over 30 issued patents.

Michael W. Yung received the B.S. degree from the California Institute of Technology, Pasadena, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Los Angeles, 1984 and 1977, respectively.

In 1985, he joined HRL Laboratories, Malibu, CA, where he is currently Research Project Manager. He has worked on high speed mixed signal, optoelectronic and RF circuits in InP, GaN, SiGe, and CMOS technologies. His latest research interest was in extremely low power neural circuits. He has contributed to over 20 technical publications and had more than 10 issued or pending patents.

Narayan Srinivasa (M'00) received the Ph.D. degree in mechanical engineering with specialization in bio-inspired control systems from the University of Florida, Gainesville, FL, in 1994.

He is a Principal Research Scientist and Manager for the Center for Neural and Emergent Systems in the Information and System Sciences Department, HRL Laboratories LLC , Malibu, CA. His primary research interests are in the areas of learning, perception, adaptive control and evolutionary dynamics. He is currently the Program Manager and Principal Investigator for two DARPA projects, SyNAPSE and Physical Intelligence, which attempt to develop a theoretical foundation inspired by brain science and physics to engineer electronic systems that exhibit intelligence. In his 12 years at HRL, he has designed and managed several projects for GM and Boeing, solving real-world problems in the areas of sensing and control, winning numerous awards, including the HRL Distinguished Inventor Award, GM Most Valuable Colleague Award, and HRL Outstanding Team Award. He was an invitee to the Frontiers of Engineering Symposium conducted by the National Academy of Engineering in 2008. He was also an invitee to the National Academy of Sciences Keck Futures Initiative on Synthetic Biology in 2009. He was a Beckman Fellow at the Beckman Institute, University of Illinois at Urbana-Champaign, from 1994–1997. At Beckman Institute, he was a member of Human Computer Intelligent Interaction Group and worked in the areas of learning algorithms for robotics, manufacturing, and computer vision. He has authored 80 technical papers and holds 25 U.S. patents. He is a member of INNS and AAAS.