5152

B.Sc (Hons.) IN CSE, PART-I, 2ND SEMESTER EXAMINATION, 2018
DIGITAL SYSTEMS LAB
Subject Code: 510209

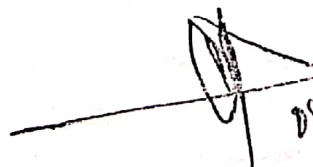Time- 3 hours   Full Marks -- 40

[N.B. - Answer any two questions.]

1. Verify the operations of Basic gates.
2. Verify the operations of NAND gate as universal gate.
3. Implementation of NOR Gate using basic gates.
4. Verify the operation of XOR gate using basic gates.
5. Design and implementation of a Half Adder Circuit and verify its operation.
6. Design and implementation of a Full Adder Circuit and verify its operation.
7. Verify the operation of J – K Flip Flop.
8. Design and implementation of a 3 to 8 line decoder circuit using 74LS138 and verify its operation.
9. Design and implementation of a Half Subtractor circuit and verify its operations.
10. Design and implementation of an Asynchronous Counter.
11. Implementation of a Demultiplexer circuit.
12. Verify the operations of D/A Converter.

Marks Distribution:

Algorithm/Circuit Design	: 10
Coding/Circuit Construction	: 10
Result	: 10
Viva	: 10
Total	= 40

09.4.19

09.07.19