A Novel Power Efficient 8T SRAM Cell

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***Abstract*—As the technology is being scaled down leakage power is becoming an important contributing factor in total power dissipation of the circuit. So in the portable devices such as cell phones, laptops emphasis has to be given to reduce power consumption during active as well as standby mode. This paper presents certain leakage reduction techniques in 8T SRAM cell. The technology used is 90 nm. The results have been obtained using Cadence Virtuoso Tool. The results show significant reduction in power as compared to conventional cells without degrading the stability of the cell.**

Keywords: Leakage Current; Threshold Voltage; Stacking;

I. INTRODUCTION

Memory arrays are an integral part of the processors and other devices being used. The memory arrays constitute of several SRAM cells. Each cell store a single bit of data. So to store considerable amount of data an array of cells is used. These SRAM cells are available in various configurations depending upon number of transistors being used. In order to increase the density of the manufactured chips the channel length of the devices is being decreased. This in turn leads to reduction in power dissipation. Total power dissipation includes static as well as dynamic power dissipation. Dynamic power dissipation occurs during certain activity in the circuit and static power corresponds to leakage power that is the power consumed when circuit is in idle state. In long channels leakage power is negligible hence total power remains equal to dynamic. Before the CMOS is scaled down into deep sub process, dynamic power has been dominated, while leakage power is less in comparison [1].

The aggressive scaling of CMOS device achieves higher density, improved performance and lower power consumption. Transistor delay time decreased per technology results doubling of microprocessor performance in every two years. To keep the power consumption under control the supply voltage has been scaled down since the threshold voltage and the transistor has to be scaled to achieve high performance. When the threshold voltage scaling results increasing of the sub threshold Leakage Current [1].

There are four prominent sources of leakage current in a MOS transistor [1]. Fig.1. shows the different Leakages in MOSFET device.

- Reverse-biased junction leakage current
- Gate induced drain leakage
- Gate direct-tunneling leakage
- Sub threshold (Weak Inversion) Leakage

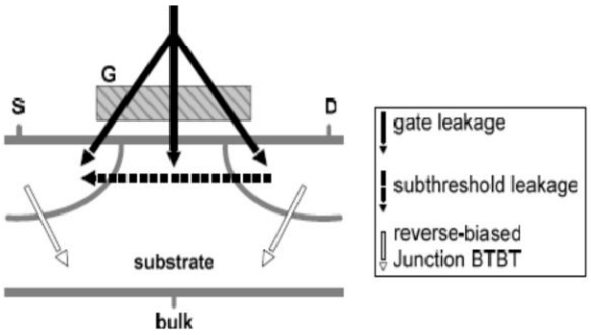

Fig.1. Different Leakage in MOSFET Device

A. Junction Leakage

The P-N Junction leakage current is due to the reverse biasing of the drain and source to well junctions. The two main components of a reverse-bias P-N junction leakage are minority carrier diffusion near the edge of depletion region and the other one is due to the electron-hole pair generation in the depletion region of the reverse-biased junction. Former is a function of doping and junction area concentration [3].

B. Gate Induced Drain Leakage

High field effect in the drain junction of MOS Transistors is the main cause for the Gate Induced Drain leakage. In the case of NMOS transistor important band bending in the drain makes generation of electron-hole pair, through avalanche multiplication and band to band tunneling, when gate is grounded and drain potential is connected to VDD. Due to the reason of holes rapidly swept out, to the substrate, a deep depletion condition is developed. Meanwhile due to the collection of the electrons in the drain, produces GIDL current

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IGIDL). Increase in drain to gate voltage and in drain to body voltage will make this leakage mechanism very worse.

C. *Gate Direct Tunneling Leakage*

As supply voltage and transistor length are scaled down, gate oxide thickness should also be reduced to maintain efficient gate control over the channel region. But this results in an exponential increase in the gate leakage due direct tunneling of electrons through the gate oxide.

D. *Sub-threshold Leakage Current*

To make dynamic power consumption under control, voltage supplied has to been scaled down. The threshold voltage (V_{th}) has to be scaled too, to maintain a high drive current capability. However, the V_{th} scaling results in increasing sub threshold leakage currents. Sub-threshold current exists between source and drain when transistor is operating in the weak inversion region (gate voltage is lower than the V_{th}).The drift current is the prominent mechanism in strong inversion device, when the gate-to-source voltage exceeds the V_{th}. When there is weak inversion then the minority carrier concentration is almost zero, and the channel has, a small longitudinal electric field but no horizontal electric field appears due the drain-to-source voltage. At this state, the carriers move by diffusion between the source and the drain of CMOS transistor. Therefore, the sub-threshold current is goverened [4] by diffusion current and it depends exponentially on both gate-to-source and threshold voltage.

The whole paper is divided into 5 sections. Section 1 gives the basic introduction regarding Leakage components, Section 2 explains Operation of memory cells, Section 3 explains performance comparison of 6T with 8T SRAM Cell, Section 4 describes the leakage reduction schemes, Section 5 shows the Technology Effects Estimated, Section 6 describes Simulation Results Section 7 describes area and power comparison, the paper has been concluded in Section 8.

II. Operation of Memory Cells

A. *6T SRAM Cell* [2]

6T SRAM cell refers to memory cell which uses 6 transistors to store single bit of information. The figure 1 below shows basic 6T cell.

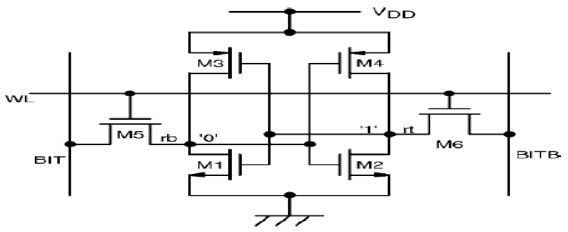

Fig. 2.6T SRAM Cell [2]

The data to be stored is supplied to Bit Line and its complement to BITB. ‘rb’ and ‘rt’ are two storage nodes. M5 and M6 are two access transistors. M3 and M4 are two pull up PMOS transistors and M1 and M2 are two pull down NMOS transistors. M3, M1 and M4, M2 are two pairs of cross coupled inverter. The Word line WL is responsible for keeping the cell in active or standby mode. Its value will make access transistors on or off [5]. During read operation the data stored is received from two complementary Bit lines. Word line is deactivated in the hold state and no activity is performed in the cell. The data would remain as it is. VDD is the supply voltage. Scaling of devices leads to reduction in the supply voltage and hence power reduces but stability of the cell decreases.

B. *8T SRAM Cell*

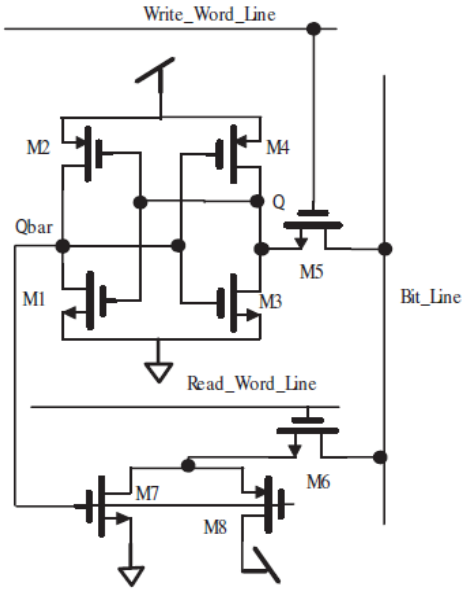

Fig. 3.8T SRAM Cell [7]

The main idea of this topology is to separate the read operation from internal node of latch. In this cell, single Bit Line is used for write operation which reduces write power consumption.

Write Operation During write ‘1’ operation, Transistor M5 (Fig. 3) turns-on by enabling the ‘write word line signal’. When the ‘Bit Line’ is imposed to logic ‘1’, then ‘Q’ node starts charging and turns on Transistor M1 which cause to flip ‘Qbar’ node to logic ‘0’ . Now ‘Qbar’ node helps enabling the Transistor M4 which facilitates writing good logic ‘1’ at ‘Q’ node. On the other hand, during write ‘0’ operation, the ‘Bit Line’ is imposed to logic ‘0’ and Transistor M5 turns-on by enabling ‘write word line’ signal. The ‘Q’ node starts discharging and turns on TransisitorM2 which in turn flipped ‘Qbar’ node to logic ‘1’. Now ‘Qbar’ node helps turning Transistor M3 on, which facilitates discharging ‘Q’ node properly and consequently logic ‘0’ is obtained at ‘Q’ node.

Read Operation: Read operation is performed by using MOSFETs M6, M7 and M8. Node ‘Qbar’ is connected to the gates of M7 and M8. In this case, a current flows in and out of the read circuit by turning on transistor M6 using Read Word Line. During read ‘1’ operation, Transistor M5 and M6 are

turned off and on respectively. As 'Qbar' node stores '0' logic, it enables the Transistor M8 (PMOS) transistor which in turn imposes the Bit Line through Transistor M8 and M6. The sense amplifier detects the bit swing and output '1' is obtained. During read '0' operation, Read Word Line signal enables the Transistor M6 and as 'Qbar' node stores logic '1', so it turns on Transistor M7 (NMOS) which discharges the Bit-Line through Transistor M7 and M6. This effect builds a voltage difference between the Bit Line and the local reference line which is sensed by the differential amplifier, and logic '0' is obtained at the output.

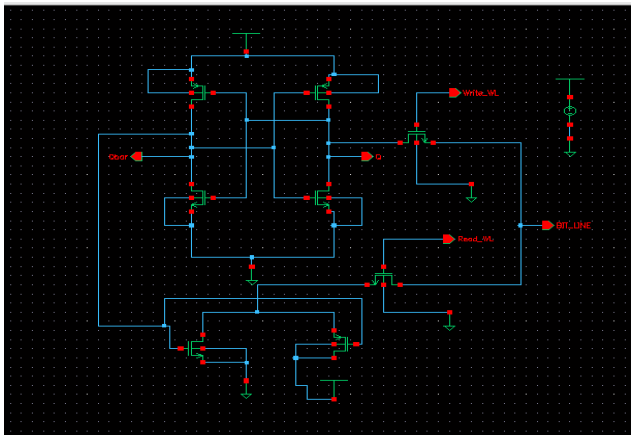

Fig.4. Simulation of 8T SRAM Cell

III. PERFORMANCE COMPARISON OF 8T WITH CONVENTIONAL 6T SRAM CELL

Table I shows comparison of various parameter between 6T and 8T [7] SRAM Cell The write time of the proposed cell is higher than conventional cell due to its single bit-line structure. Here write time is considered as the time gap between word line active and data stored in 'Q' or 'Qbar' node whichever occurs later. [7] Read Time for 8T Cell is less as compared to 6T SRAM Cell. Single Bit Line is used in 8T SRAM Cell for write operation which reduces write power consumption. But overall cell power required for 8T cell is more.

TABLE I. PERFORMANCE COMPARISON OF 8T & 6T SRAM CELL AT 90 nm & VDD=1V

Parameter Name	**Conventional 6T**	**8T[7]**
Cell power (microwatts)	0.19	0.23
Read time (picoseconds)	544	531
Write time (picoseconds)	409	593

IV. LEAKAGE REDUCTION SCHEME

When gate to source voltage of MOSFET drops below threshold voltage Vth, device is in off state and no current should flow. But even in the off state, certain current continues to flow which is referred to as the Sub-threshold leakage current. The Sub-threshold drain current has a certain finite value but depends exponentially on gate to source voltage of the transistor [6,7]. The threshold voltage Vth and Sub-threshold leakage current has inverse relationship with each other. So to reduce this leakage current Vth needs to be increased. Apart from Sub-threshold current, gate leakage current, tunneling current and others do constitute the total leakage current [1].

Reduction in the channel length reduces Vth and further aggravates the problem of leakage power. Due to short channel effects, the contribution of these currents towards total power is increasing. These leakage currents can be reduced both at process level as well as at circuit levels. Various circuit level techniques have been proposed in [1] to increase threshold voltage. It involves the use of stacking effect [1] which states that leakage power reduces if more than one transistor in series is in off state.

When both the transistors are off, a certain positive potential is present at the common terminals thereby increasing the body effect and hence reducing the leakage current. Secondly reverse biasing the body of the transistor leads to increase in threshold voltage according to the equation (1) below

$$Vth = Vth0 + \sqrt{\{ (|2\varphi_f + Vsb|) - |2\varphi_f| \}} \qquad (1)$$

Here Vth0 is the threshold voltage when source and body are at same potential Vsb=0. γ represents the body effect co-efficient and φ_f represents the work function of silicon substrate [8]. In case when Vsb is equal to zero, Vth = Vth0. On connecting body to negative terminal Vsb increases as bulk potential becomes negative. So source potential and bulk potential add up which in turn leads to the increase in threshold voltage. Even in the active mode one or more transistors in the cell remain off. Hence leakage current occurs both in active as well as in hold state

V. TECHNOLOGY EFFECT ESTIMATED

The circuits have been simulated using Cadence Virtuoso Tool and Trans-Trans are used for checking power and viewing waveforms. Since the technology used is 90 nm. Hence the DC supply voltage is 1.0 volts. The schematic and results are shown below.

VI. SIMULATION RESULTS

The threshold voltage of pull down transistor has been reduced by connecting the body of the transistor to negative terminal. Threshold voltage of only NMOS transistor is increased because increase in Vth results in increase in delay. That is speed of the system reduces. In first proposed work the pull up PMOS transistors are stacked and threshold voltage of pull down transistors is increased by reverse biasing its body. In second proposed circuit pull down transistor is body reverse biased and read Bit line path NMOS and PMOS are stacked. In third proposed circuit both pull up transistor and read line

transistors are stacked and pull down transistors are reverse biased.

A. Increasing Vth of Pull down transistors

In NMOS transistor the body or the substrate is of P type material so if the substrate is connected to negative terminal, extra supply voltage is required to switch the transistor from OFF state to ON state. Hence Vth increases and Sub-threshold leakage current reduces. Figure 5 shows the circuit diagram of 8T cell with increased Vth. For increasing the threshold voltage of the pull down transistors a supply voltage of 0.5 in negative direction is applied. Increasing the value beyond this potential leads to increase in the power consumption. In the circuit, wl represent the word line, bl represents the Bit line and blb represents the complement of bit line, q and qbar are two storage nodes.

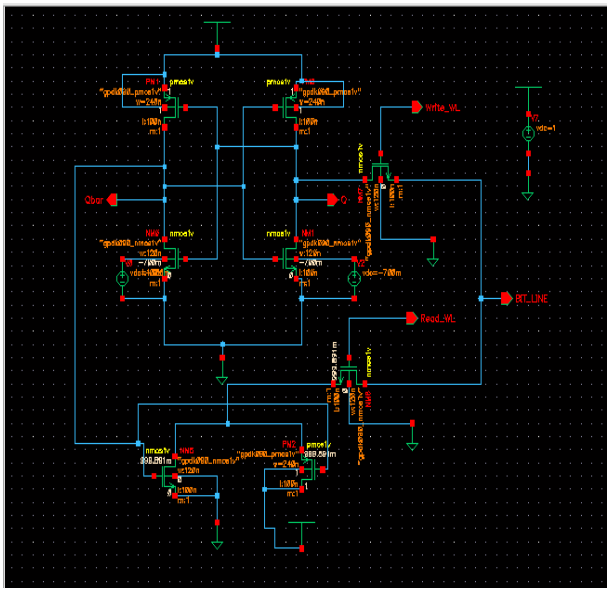

Fig.5. Increased Vth 8T SRAM Cell

Table II Vth COMPARISON

Transistor	Conventional	New Scheme
MN1	237 mV	299 mV
MN2	122 mV	146 mV

B. Stacking in PMOS and Vth increase in NMOS

Another scheme employing stacking of Pull up PMOS transistors and increasing Vth of lower NMOS transistors has also been proposed. The power dissipation of memory cells is further reduced. Since the PMOS transistors in the Figure 6 are stacked, their sizes are also reduced by half. Transistor size here means W/L ratio.

Table III represents the power dissipation of conventional, increased Vth and proposed schemes. Table III also illustrate area comparison of various schemes.

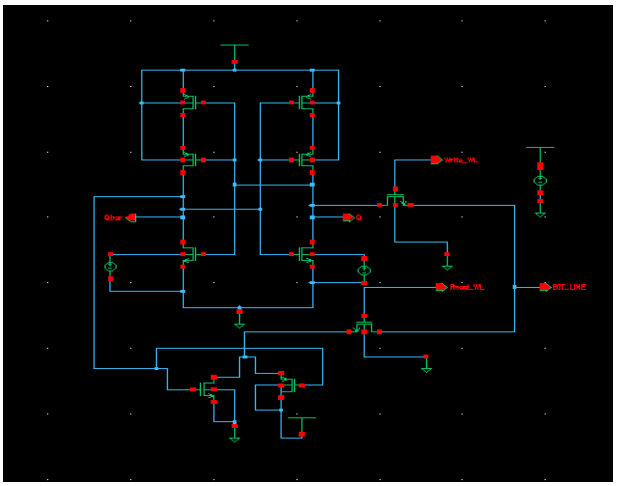

Fig 6.Proposed Scheme 1 in 8T SRAM

C. Stacking in Read Line Transisitors and Vth increase in Pull down Transistor

Another scheme employing stacking of Read transistors and increasing Vth of lower NMOS PDN transistors is also been proposed This techniques further improves on power consumption as shown in figure 7.

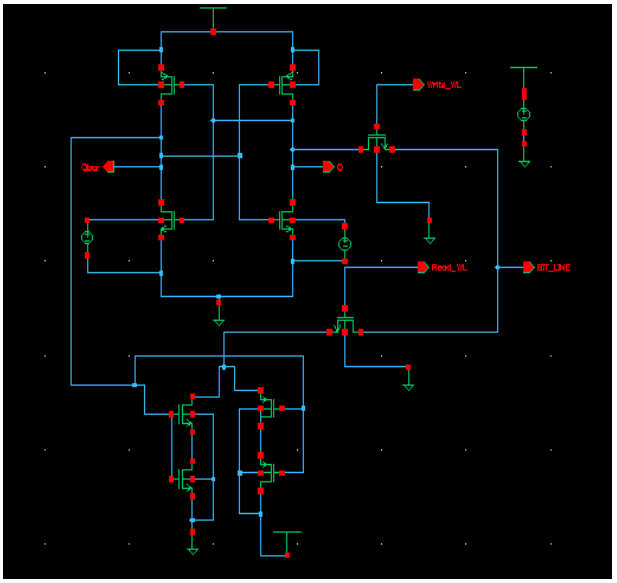

Fig.7. Proposed Scheme 2 in 8T SRAM

D. Stacking in Read line Transistors and PUP Transistor and Vth increase in Pull down Transistor

Another scheme employing stacking of Read transistors

And PUP Transistors and increasing Vth of lower NMOS PDN transistors is also proposed this technique further improves on power consumption as shown in Table 2. Circuit for this technology is shown in Figure 8.

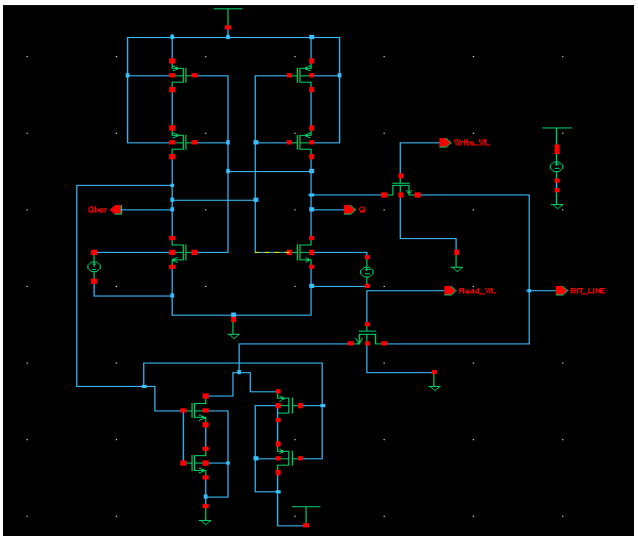

Fig.8. Proposed Scheme 3 in 8T SRAM

E. Read and write waveforms

The read and write waveform of 8T SRAM cell are shown in Figure 9 below. During the read the output is taken from read path and word line remains active high during write operation the input is applied at Bit Lines and WL is asserted. During hold the WL remains off and cell is in idle state.

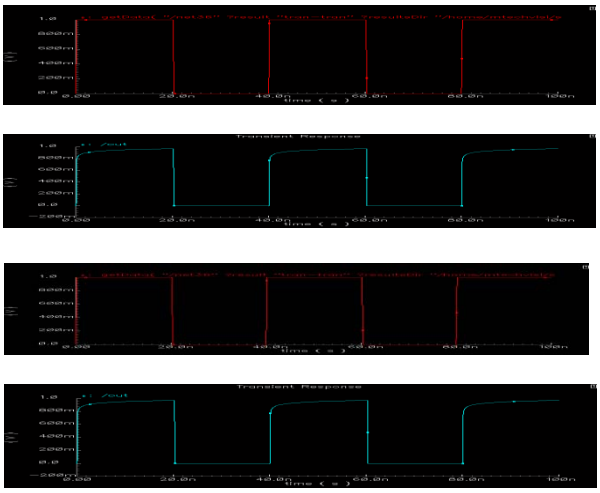

Fig.9. Read Write Waveform of 8T SRAM

VII. AREA AND POWER COMPARISON

Table III shows the comparison of different structures. Total power consumption of the proposed structure shows 40% reduction in comparison to the conventional 8T and this reduction in total power is due to substrate biasing either due to direct substrate biasing or transistor stacking. Table also shows the area comparison of various structures. A notable decrease in power is achieved both for read and write operations.

Table III. Area &Power Comparison

Operation	**Power Read(Watts)**	**Power Write(Watts)**	**Area Comparison**
Conventional	$2.377 * 10^{-7}$	$2.70 * 10^{-7}$	A
Vth and Pull up Transistor Stack	$2.125* 10^{-7}$	$2.16 *10^{-7}$	1.25A
Vth and Read Line Stack	$1.863 *10^{-7}$	$1.90 *10^{-7}$	1.25A
Vth With Read and Pull up Transistor Stack	$1.5885 *10^{-7}$	$1.64*10^{-7}$	1.5A

VIII. CONCLUSION

Memory cell are part and parcel of almost all the devices used nowadays. Low power VLSI Design strives to reduce the power consumption in these devices so as to increase the battery life. In this paper, four different techniques is proposed to reduce the power dissipation. Results show that power dissipation gets reduced by almost 40% when Vth of transistor is increased. To further reduce the power consumption concept of stacking was used. These techniques can further be applied on various other configurations of SRAM cells to achieve optimum results.

REFERENCES

[1] Kaushik Roy, Saibal Mukhopadhyay,And Hamid Mahmoodi-Meimand "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits" Proceedings Of The IEEE, Vol. 91, No. 2, February 2003

[2] A. Goel, R.K. Sharma, A.K. Gupta "Process variations aware area efficient negative bit-line voltage scheme for improving write ability of SRAM in nanometer technologies" IET Circuits Devices Syst., 2012, Vol. 6, Iss. 1, pp. 45–51.

[3] A. pierret, "semiconductor device fundamentals", reading, MA: Addison-Wesley, 1996, ch.6, pp235-300

[4] A. Keshavarzi, C. F. Hawkins, K. Roy, and V. De. Effectiveness of Reverse Body Bias for Low Power CMOS Circuits. In Proc. of the 8th NASA Symp. on VLSI Design, pages 231–239, 1999

[5] Sunil Jadav, Vikrant, Munish Vashisath "design and performance analysis of ultra low power 6T SRAM using adiabatic technique" International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, June 2012.

[6] Y.Tsividis, Operation and Modelling of the MOS transistor,Second Ed, Boston :Mc –Graw Hill 1999.

[7] Y.Taur and T.H. Ning, Fundamentals of Modern VLSI Devices, New York ,Cambridge University Press,1998.

[8] R.S Muller and T.I Kamins ,Device Electronics for Integrated Circuits, Second Ed, New York ,Wiley 1986