# Optimizing Power Efficiency in SRAM for High Performance Computing

A project report submitted in partial fulfillment

of the requirements for the degree of

Bachelor of Technology

in

Electronics & Communication Engineering

by

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November 2024

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We hereby declare that the report titled ***Optimizing Power Efficiency In SRAM For High Performance Computing*** submitted by me to the School of Electronics Engineering, Vellore Institute of Technology, Chennai in partial fulfillment of the requirements for the award of **Bachelor of Technology** in **Electronics and Communication Engineering** is a bona-fide record of the work carried out by me under the supervision of ***Dr. Sridhar C***.
We further declare that the work reported in this report, has not been submitted and will not be submitted, either in part or in full, for the award of any other degree or diploma of this institute or of any other institute or University.

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# *Abstract*

SRAM elements find their place in many applications, such as processor caches, embedded systems, and networking devices, in the integrated element of modern high-speed digital architectures. However, the very challenging requirement to design SRAM for both high-speed performance and low power arises because of increased power dissipation and stability issues at high frequencies.

This work discusses the enhancement of power efficiency in SRAM within high-performance computing by moving from traditional 6T SRAM to the new 8T SRAM configuration. The scheme under discussion utilizes transmission gates and 8T models, which would contribute toward reducing both static as well as dynamic power consumption. Such changes could control memory cells efficiently, lessen leakage currents, and diminish read-disturb effects while the data is processed at higher frequencies.

Simulations were done using Cadence Virtuoso tool over CMOS technologies 180nm, 90nm and 45nm. Power dissipation, stability and performance are compared across the frequency ranges of 500 MHz, 1 GHz and 2 GHz. The results indicate that SRAM 8T has better performance compared to standard 6T architecture in terms of power efficiency and operational stability with remarkable reductions in dynamic power consumption due to a higher operating speed. This work shows that the proposed 8T SRAM design has a viable path to solving power consumption and stability problems in high-speed digital systems. The development of more efficient and reliable SRAM designs will hence be achievable in future computing systems. The future work will help in minimizing the area overhead of additional transistors. The emphasis will be in improving PDP metrics.

# *Acknowledgements*

We wish to express our sincere thanks and deep sense of gratitude to our project guide, Dr. Sridhar C, Assistant Professor senior grade 2, School of Electronics Engineering, for his consistent encouragement and valuable guidance offered to us in a pleasant manner throughout the course of the project work.

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# Chapter 1

# Introduction

Static Random Access Memory is one of the most important current digital positions, which acts as a core component in processor caches, networking architectures, embedded systems, and even Field-Programmable Gate Arrays. Being a volatile kind of memory, SRAM retains information only during the period of power supply, using latching circuitry to retain each separate bit, whereas dynamic RAM requires constant refreshing intervals. This intrinsic architecture of SRAM provides advantages such as accelerated access times and reduced latency, making it critical for applications in high-performance computing. Most significantly, it has meant that improvements in CMOS technology have advanced at a very rapid rate with increasing demands for greater computational speeds.
The rapid scaling of CMOS technology and the demand for higher computational speeds have introduced significant challenges in SRAM design:

**1. Power Loss**:
- Static Power Dissipation: Due to the leakage currents through transistors, even while idle.

- It mainly consists of dynamic power dissipation during read/write operations, forced by the rapid charging and discharging of capacitances at high speeds.

**2. Stability Problems**:
- SRAM cells operating at lower supply voltages become more sensitive to downward shifts in static noise margin; failures could occur on read or write.

- The operation of high frequencies intensifies both power consumption and stability challenges, thereby complicating the design process of dependable SRAM cells.

There have also been researchers and engineers in developing the advanced SRAM architectures intending to improve power and stability. Although simple and widely used,

traditional 6T SRAM cells cannot effectively maintain the efficiency under strict power and performance conditions. With such improved configurations as 8T SRAM that features splitting between read and write functions and including additional transistors with complementary functions, it has shown promise for lower power consumption and increased stability at higher frequency levels. This paper attempts to present an 8T SRAM architecture design for highspeed and low-power applications. The most important objectives include: - Architectural Changes such as transmission gates prevent power dissipation. It improves stability by overcoming the read-disturb effects and enhancing static noise margins.

Therefore, a detailed analysis of the presented design under 90 nm technology and different operating frequencies (500MHz, 1GHz and 2GHz) has to be presented. The results of this study are pertinent to future digital systems where power efficiency and stability are critical for making sustainable high-performance computation. In that perspective, the advancement and improvement of SRAM design bring more value both to the broader discipline of VLSI technology and to progress in electronic energy-efficient systems.

# Chapter 2

# Literature Survey

## 2.1 Overview of SRAM technology

SRAM is a basic component in digital electronics, with the characteristic of fast access and low latency. Unlike DRAM that requires periodic refreshes, latching circuitry such as inverters is used to memorize every bit that implies lower complexity operationally and high performance. At any rate, advancement in CMOS technology and an increasing demand for low power systems have presented significant difficulties in SRAM design, especially with regard to power dissipation and stability.

## 2.2 SRAM Architecture

The 6T SRAM cell has been the most dominant structure for Static Random Access Memory due to a graceful balance of simplicity, operational velocity, and energy efficiency. In this topology, six transistors are used, of which four form two cross-coupled inverters and are the access transistors, controlling communication between the memory cell and the external circuitry.

Components of 6T SRAM

**Two NMOS Transistors (Pull-Down)**: Provide high drive capability for storing a logic '0'.

**Two PMOS Transistors**: Retain the stored logic '1' and have complementary operation with NMOS.

**Two NMOS access transistors**: Facilitate the connection of the internal storage nodes to the bit lines throughout both read and write processes.

Architectural Diagram

**Cross-coupled Inverters**: Two inverters are placed back-to-back to form a bistable latch. This latch retains a single binary value, which may be a logic '0' or a logic '1'.

**Access Transistors**: Regulated by the Word Line (WL). Connect the storage nodes to the complementary Bit Lines (BL and BLB) during a read or write operation.

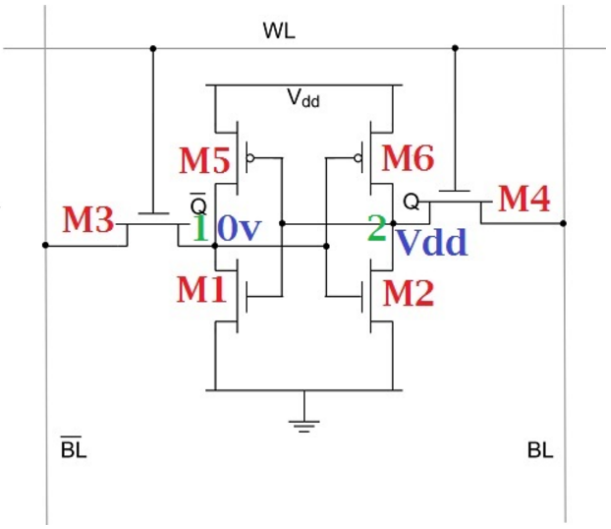


FIGURE 2.1: 6T SRAM

## 2.3 SRAM Operations

SRAM operates in three primary states: Write, Read, and Hold. Each state involves specific interactions among the memory cell components, primarily transistors and bit lines:

**Read Operation**: Assume that node 1 has logic 0v. So M1 and M6 are ON while M5 and M2 are OFF. Because of this, Node1 = 0V and V2 = VDD. Data lines are pre-changed from 0 to VDD and the word line is activated. So M3 and M4 are switched ON. Since the drain and source for M4 are at the same potential, no current flows in this area. However, the drain and source at M3 in LHS have a high differential potential, therefore M3 experiences non-zero current flow. Path: M3, M1, and GND The voltage at BL starts to decline, which causes the capacitor to discharge and raise V1. Since V1 is increasing from 0V and it may turn on M2 if M1 size is small, So for reading operation, M1 should be greater than M3

**Write Operation**: Consider that Node 1 stores Assume 1. So M2 and M5 are ON while M1 and M6 are OFF. Prior to the ON state of M2 and M4, V1 = VDD and V2 = 0V. As Wordline goes high, M3 and M4 are turned ON. Since Node2 is less than VT1,

Node2 cannot be used to turn ON M1. We need to turn ON M1 so that path is created from Node1 to GND and the voltage at Node1 will decrease to zero since the path is pulled down to GND. Therefore we turn OFF M2. Node1 is less than VT2 to turn OFF M2. When Node1 = Vin; M3 goes in the linear region and M5 in the saturation region. For a successful Write operation, we should have M4¿ M6

## 2.4 Power Dissipation in SRAM

Power dissipation in SRAM can be broadly categorized into:

**Static Power Dissipation**: Caused by leakage currents in transistors when the SRAM cell is idle. This issue is exacerbated by advanced CMOS scaling, where leakage becomes more significant due to reduced transistor sizes.

**Dynamic Power Dissipation**: Occurs during switching activities, such as read and write operations. The charging and discharging of bit and word line capacitances contribute significantly to dynamic power consumption, particularly at high frequencies

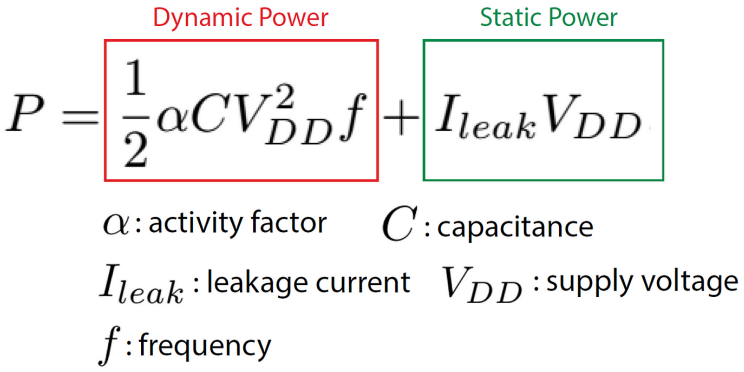


FIGURE 2.2: Total Power

In high-speed applications where SRAM operates at elevated frequencies, power consumption rises significantly due to increased switching activity. This includes faster read and write cycles, higher rates of charging and discharging capacitances, and greater leakage currents. For instance, in processor caches, SRAM runs at the processor's clock speed. Modern CPUs operating in the GHz range frequently access cache memory, which amplifies both dynamic and static power consumption. As clock speed increases, dynamic power scales linearly with frequency and quadratically with supply voltage.

## 2.5 Static Noise Margin

Static Noise Margin measures the immunity of the SRAM cell to noise while the stored information remains unchanged. It represents the largest voltage variation that can be tolerated by the cell without any state change. SNM is critically important in the evaluation of an SRAM's stability to noise, particularly in low-voltage or high-speed operating conditions.

The **Butterfly diagram** is a critical analytical tool used in the stability analysis of SRAM cells, particularly concerning SNM. SNM of an SRAM is essentially about designing it to measure the ability of a cell to maintain its information in the presence of electrical noise. SNM should be sufficient to guarantee reliable operation while in hold mode, read mode, and write mode for the SRAM cell.

The butterfly diagram is derived by plotting the voltage transfer characteristics (VTC) of the two cross-coupled inverters in an SRAM cell. By superimposing the curves of the two inverters, a visual representation resembling a butterfly is created.

X-axis: Represents the voltage at one of the storage nodes (Q).

Y-axis: Represents the voltage at the complementary node (Q'). Lobes of the Butterfly: Represent the stability regions where the cell can retain its state (logic '0' or '1'). Significance in Design

Static Noise Margin (SNM): The largest square that can be inscribed within the lobes of the butterfly diagram represents the SNM. Larger squares indicate higher stability.

Cell Stability: The butterfly diagram helps determine the cell's robustness against noise during:

Hold: Stability when the cell is idle and maintaining its state.

Read: Stability when the cell is being accessed for data.

Write: Ability to overwrite existing data without errors.

**Impact on SRAM Design** A well-balanced butterfly diagram ensures the SRAM cell can operate reliably across various operating conditions, such as low supply voltages or high temperatures. Design modifications, such as sizing transistors or adjusting supply voltage, can be validated by observing changes in the butterfly diagram.

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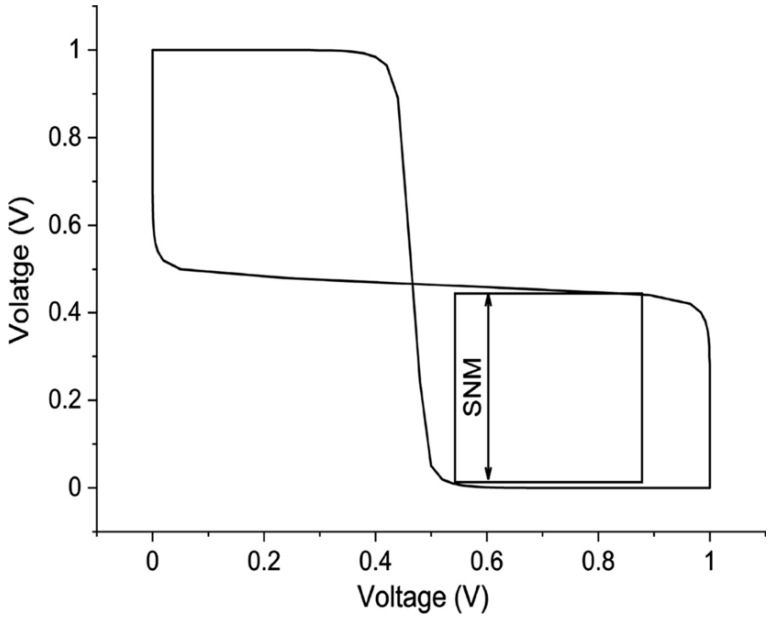


FIGURE 2.3: Butterfly Diagram to find SNM of SRAM Cell

high temperatures. Design modifications, such as sizing transistors or adjusting supply voltage, can be validated by observing changes in the butterfly diagram.

## 2.6 Challenges Encountered

However, these high-speed operations introduce significant challenges, including stability degradation, reduced Static Noise Margins (SNM), and increased susceptibility to read and write failures at lower supply voltages. To maintain reliability at higher speeds, SRAM typically uses elevated supply voltages, which further intensify power dissipation and heat generation. As the temperature rises, leakage currents grow exponentially, compounding overall power consumption. This combination of power and stability challenges necessitates advanced design methodologies to optimize performance without sacrificing energy efficiency.

## 2.7 Architectures implementations

The challenges have given way to a variety of SRAM architectures:

**Conventional 6T SRAM**: It is greatly used because of the simplicity and efficiency of the circuit. However, it suffers from read-disturb issues and increased leakage currents at scaled voltages.

**8T SRAM**: There are two extra transistors that decouple read and write, improving

stability and reducing power consumption as such. This is particularly effective in a high frequency-low power scenario.

**Transmission Gate-Based SRAM**: Use of transmission gates to improve the stability of read operations while minimizing area and power. It is efficient in biomedical and portable devices where both power and area are crucial..

## 2.8 Simulation and technology

Advancements in simulation tools and CMOS scaling have enabled detailed analysis and optimization of SRAM designs:

**Simulation Tools**: Cadence Virtuoso is widely used for evaluating power, stability, and performance metrics.

**CMOS Scaling**: Transitioning from 180nm to 45nm technology has introduced new opportunities for reducing power dissipation and improving performance, albeit with increased challenges in leakage and variability

# Chapter 3

# Methodology

## 3.1 Overview

This section describes the details of the design and optimization procedure of an 8T SRAM cell targeted for high-speed and low-power applications. Architectural enhancements and power reduction techniques are combined into a single methodology that utilizes advanced simulation tools to analyze the performance aspects.

## 3.2 Design Architecture

The proposed methodology takes forward the traditional 6T SRAM architecture by incorporating two supporting transistors that make up to an 8T SRAM setup. The decoupling architecture segregates both read and write operations while many advantages are also obtained:

Improved Stability: The design decouples read operations, thereby avoiding read-disturb issues and preserving data integrity. Reduced Power Consumption: Separate paths for the reading and writing operations reduce voltage ripples and so result in less dynamic power consumption.

It further uses trans gate transistors, which keep stability maximized with reduced leakage currents during idle states.

## 3.3 Power Reduction Techniques

There are various power reduction techniques deployed in order to overcome challenges with the high-speed operation.

1. The addition of two transistors to the conventional 6T SRAM creates a decoupled read and write path, which eliminates read-disturb issues and reduces dynamic power dissipation. This architecture ensures stability during high-speed operations by isolating read operations from the stored data, improving reliability and lowering power usage.
2. The integration of transmission gates in the SRAM cell enhances stability by providing stronger control over the storage nodes. Transmission gates reduce leakage currents and enable smoother transitions between read and write operations, particularly at lower supply voltages. This design is highly effective for applications requiring low power and high stability.

## 3.4 Simulation Setup

To evaluate the proposed design, simulations are conducted using the following tools and parameters:

1. **Simulation Tools**: Cadence Virtuoso
2. **Technology Nodes**: 90nm CMOS technology.
3. **Voltage Levels**: Supply voltages ranging from 0.5V to 1.8V.
4. **Frequencies**: Performance is tested at 500 MHz, 1 GHz, and 2 GHz.

## 3.5 Analytical Focus

The analysis of SRAM design involves a detailed evaluation of several key parameters that impact performance, power efficiency, and stability. These metrics are crucial in understanding how the proposed modifications, such as 8T architecture and transmission gates, influence the overall behavior of the memory cell.

1. **Static Noise Margins**: Butterfly diagrams are used to examine the stability of SRAM in hold, read, and write conditions.

2. **Power Dissipation**:
   (a) **Static Power**: It is measured in idle modes to measure leakage currents.
   (b) **Dynamic Power**: Measured on read and write operations, which basically measures the energy efficiency.

## 3.6 Design Flow

1. **Circuit Design**
   (a) Models and optimizes the 6T SRAM and 8T SRAM circuits.
   (b) Transmission gates, along with gated clocks, are incorporated to improve overall performance.
2. **Simulation**
   (a) The functionality will be tested through DC response and transient analysis.
   (b) Butterfly diagrams are made to detect SNM.
3. **Comparison**
   (a) The comparative analysis of the proposed 8T SRAM design with conventional 6T SRAM for power, stability, and performance metrics is established.
4. **Optimization**
   (a) Transistor sizes and supply voltages are iteratively tuned to achieve an optimal balance of power and performance.

# Chapter 4

# Implementations

## Objective

The objective of the implementation phase is to design, simulate, and validate an advanced SRAM architecture that addresses the limitations of conventional 6T SRAM by integrating an 8T design with transmission gates.

## 4.1 Validation of 6T SRAM Functionality

The circuit layout of the 6T SRAM shows a proper connection of the six transistors:

1. Two cross-coupled inverters form the bistable latch.
2. Two access transistors connect the storage nodes to the bit lines during read and write operations.

The layout is designed with optimal transistor sizing to balance stability, power efficiency, and performance.

DC and transient analysis are used to verify that the 6T SRAM cell would operate properly through both functionally during hold, read, and write operations. Simulations are run to show that the design of the 6T SRAM is stable and correct.

The DC response of the 6T SRAM cell is shown in the butterfly diagram, which represents the voltage transfer characteristics (VTC) of the cross-coupled inverters.

The transient response provides a detailed view of the SRAM's dynamic behavior during read, write, and hold operations. This analysis ensures that the cell responds correctly to input signals and transitions between states seamlessly.

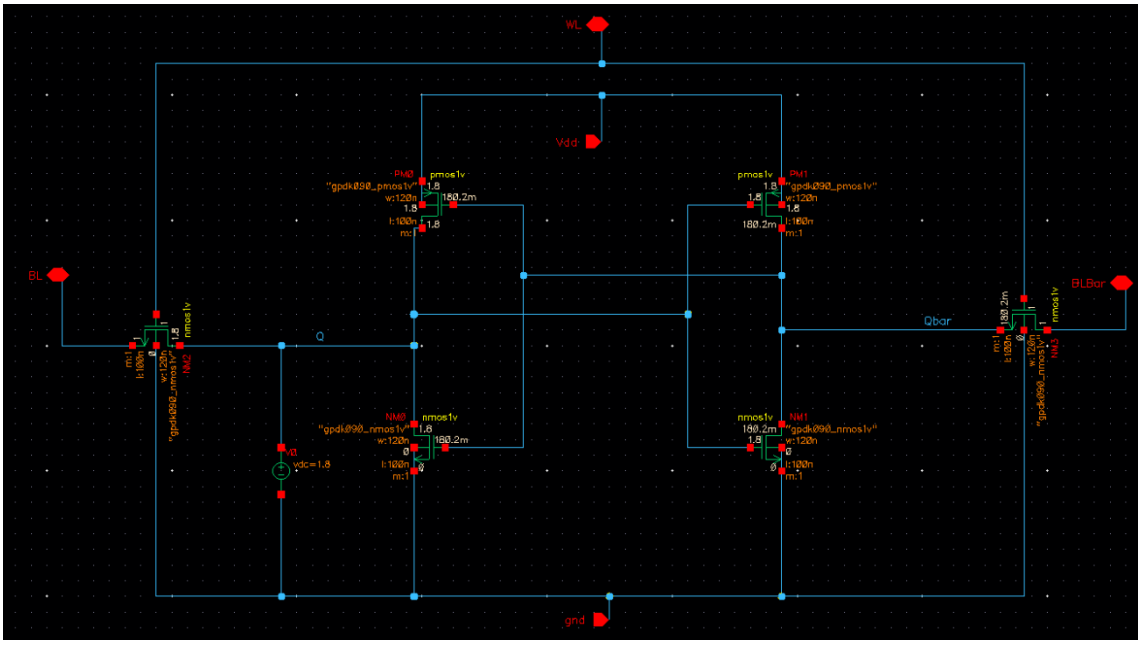


FIGURE 4.1: Schematic of 6T SRAM

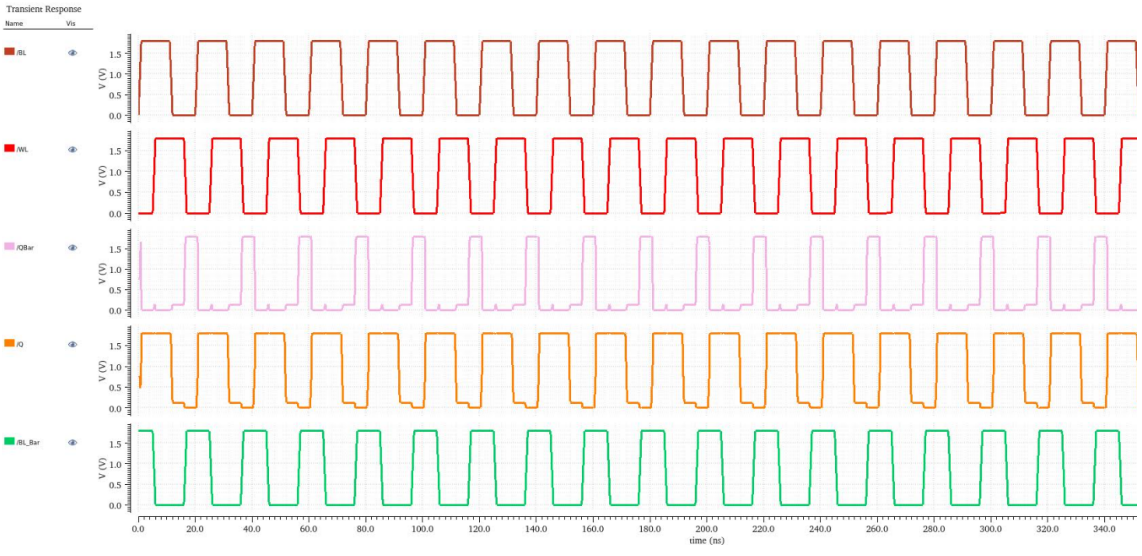


FIGURE 4.2: Transient Response of 6T SRAM

### 4.1.1 Analysis

This section examines the impact of increasing supply voltage on the stability and power efficiency of the 6T SRAM cell. The results demonstrate that as the supply voltage increases:

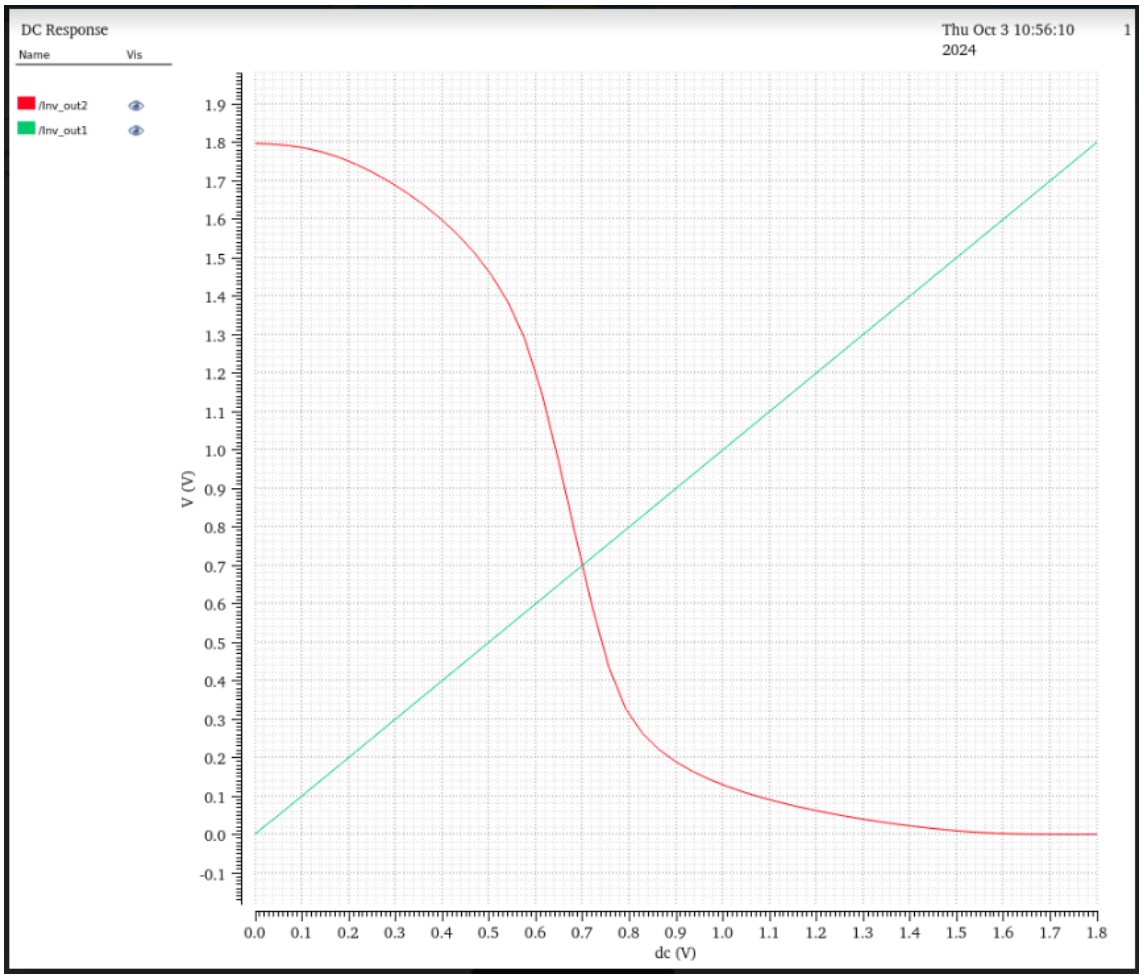


FIGURE 4.3: DC Analysis of 6T SRAM

1. Stability deteriorates, as observed from the shrinking and distorted lobes in the butterfly diagram.
2. Power consumption escalates, particularly the dynamic power due to increased switching activity and higher leakage currents.

The butterfly diagram of the 6T SRAM cell sheds light on the stability regions with the stored states, or the logic '0' and '1'.

**Observations**: At low voltage conditions, the butterfly diagram is symmetric and well-defined. SNM is very high while a sense of stability. As the supply voltage increases, the lobes shrink and distort, and SNM becomes decreased. Degradation in SNM indicates higher susceptibility to noise and state flipping chances increase during read or write operations.

**Conclusion**: - The analysis did indeed verify that increasing supply voltage degrades the stability of SRAM, by the degradation of the butterfly diagram and its decreasing SNM.

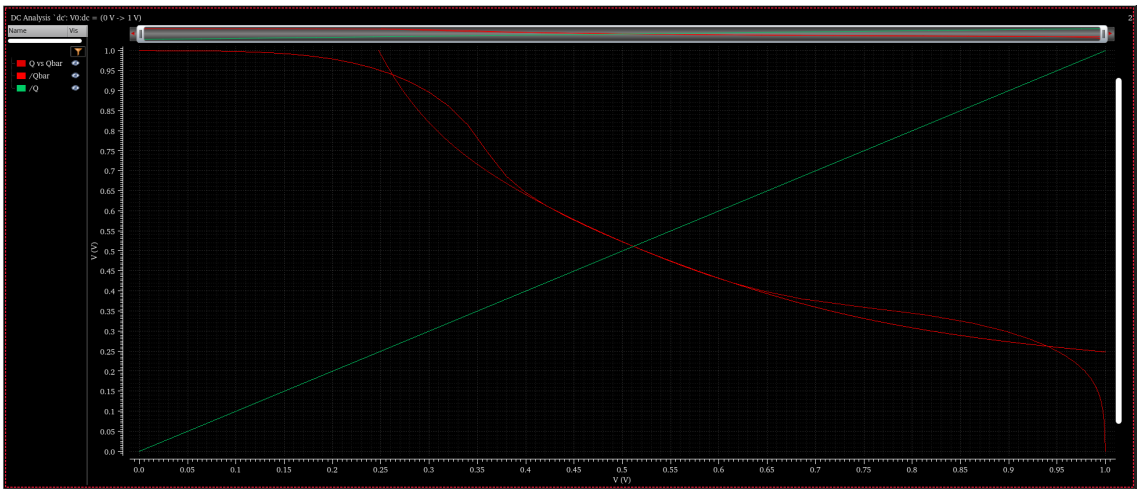


FIGURE 4.4: Butterfly Diagram for 6T SRAM

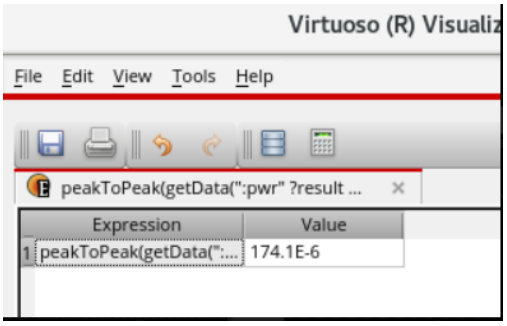


FIGURE 4.5: Power obtained for 1.8 V

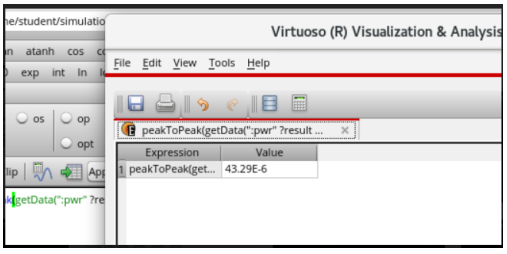


FIGURE 4.6: Power obtained for 2.5 V

- Power trends analyses also reinforce this indeed, running SRAM at higher voltages and speeds is highly inefficient from an energy consumption point of view.

- These results unveil the significance of high-performance optimized designs, namely 8T SRAM architectures, which help overcome stability problems and reduce power dissipation for high operating speeds.

## 4.2 Proposed 8T SRAM

The 8T SRAM cell is an advanced modification of the traditional 6T design, introduced to address the limitations of stability and power inefficiency in high-speed and low-voltage operations. This design incorporates two additional transistors to decouple the read and write operations, improving stability and reducing power dissipation

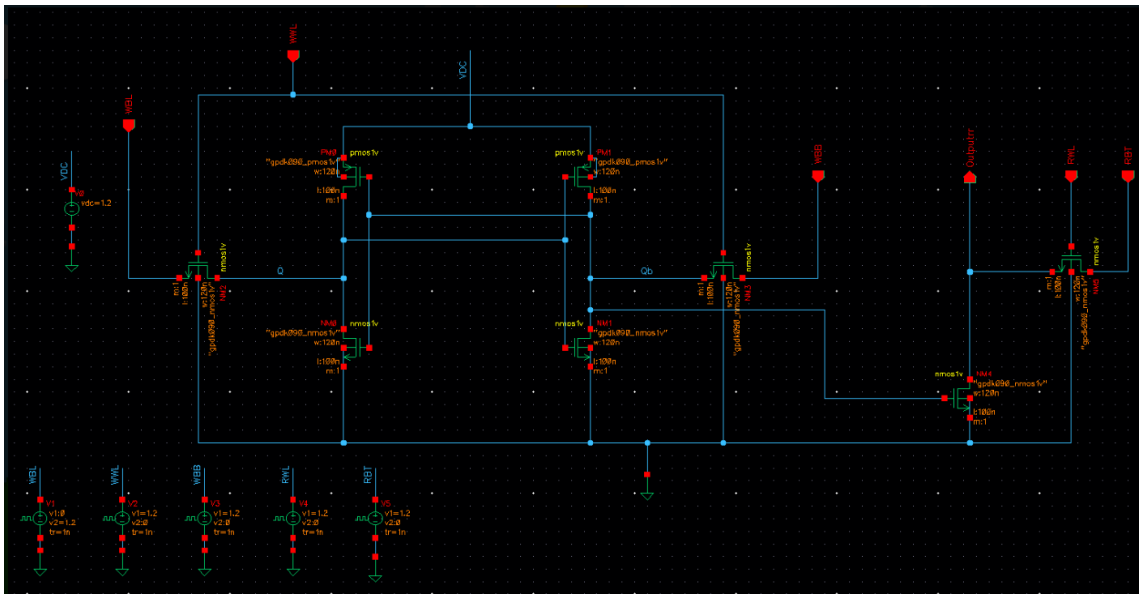


FIGURE 4.7: Schematic of proposed 8T SRAM

### 4.2.1 Key Features of Proposed 8T SRAM

1. **Decoupled Read and Write Paths:** It brings in additional two transistors that are distancing the read operation from the storage nodes, namely Q and QBar.

   It decouples the read operation. As a result, read-disturb issues won't come in between the stored states getting flipped accidentally while reading out data.

2. **Better Stability:** Decoupling here enhances SNM particularly while reading out, which is a common weak point in 6T designs.

   The stability of operation is retained even at low supply voltages, thus making the design more robust for modern low-power applications.

3. **Lower Power Dissipation**: By isolating the read and write paths, power consumption in terms of dynamic power is minimized during high-frequency operations.

   In idle states, better control over the transistors curtails leakage currents.

## 4.3 Proposed 8T SRAM with Transmission Gate

The 8T SRAM with transmission gates is an enhancement over the conventional 8T SRAM architecture, designed to further optimize power efficiency and stability. Transmission gates (TG), comprising parallel-connected PMOS and NMOS transistors, are

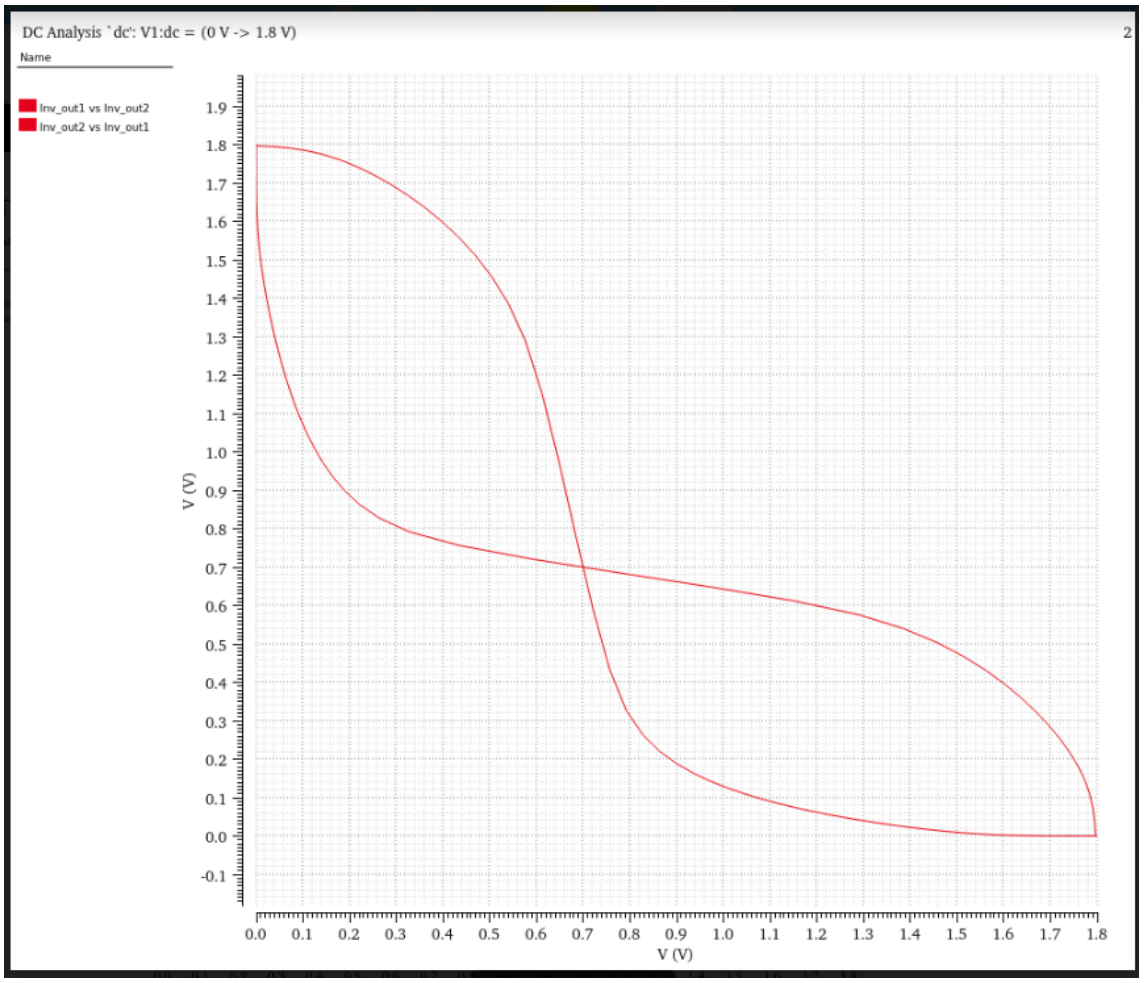


FIGURE 4.8: DC Analysis of proposed 8T SRAM

used in place of traditional pass transistors for improved signal integrity and noise immunity. This design is particularly advantageous for applications requiring high reliability, low power, and minimal area overhead.

### 4.3.1 Additional Advantages of Using Transmission Gates in 8T SRAM

The incorporation of transmission gates (TG) in the proposed 8T SRAM design offers several notable improvements over conventional pass-transistor-based SRAM cells:

1. **Enhanced Signal Integrity:** Transmission gates provide *bidirectional conductivity*, ensuring stronger signal transmission with minimal degradation. This feature is especially useful for read/write operations at lower supply voltages, where traditional pass transistors may suffer from weak signal levels.

2. **Improved Noise Immunity:** By using both PMOS and NMOS transistors in parallel, transmission gates significantly reduce the impact of *threshold voltage*

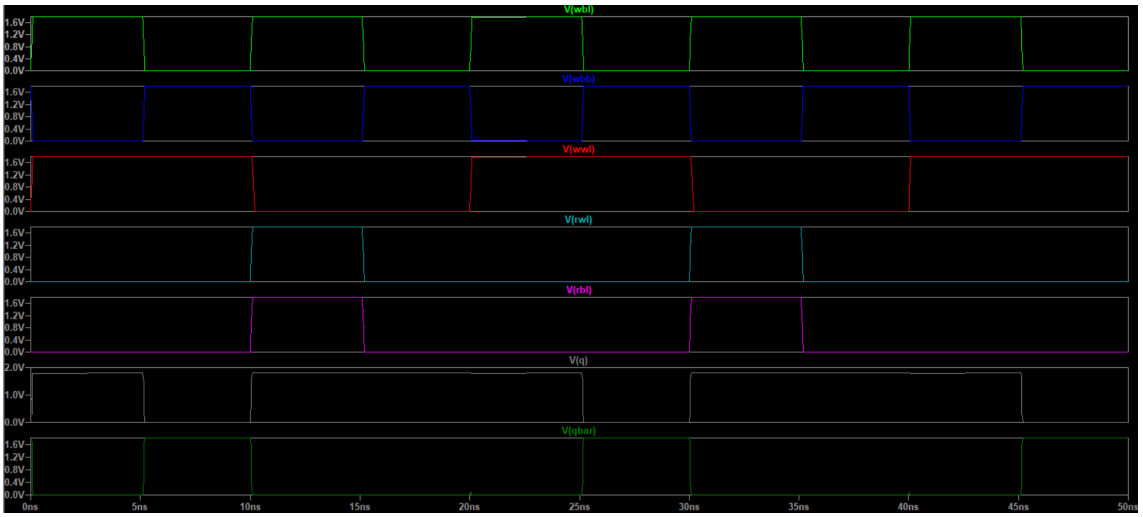


FIGURE 4.9: Transient Analysis of proposed 8T SRAM

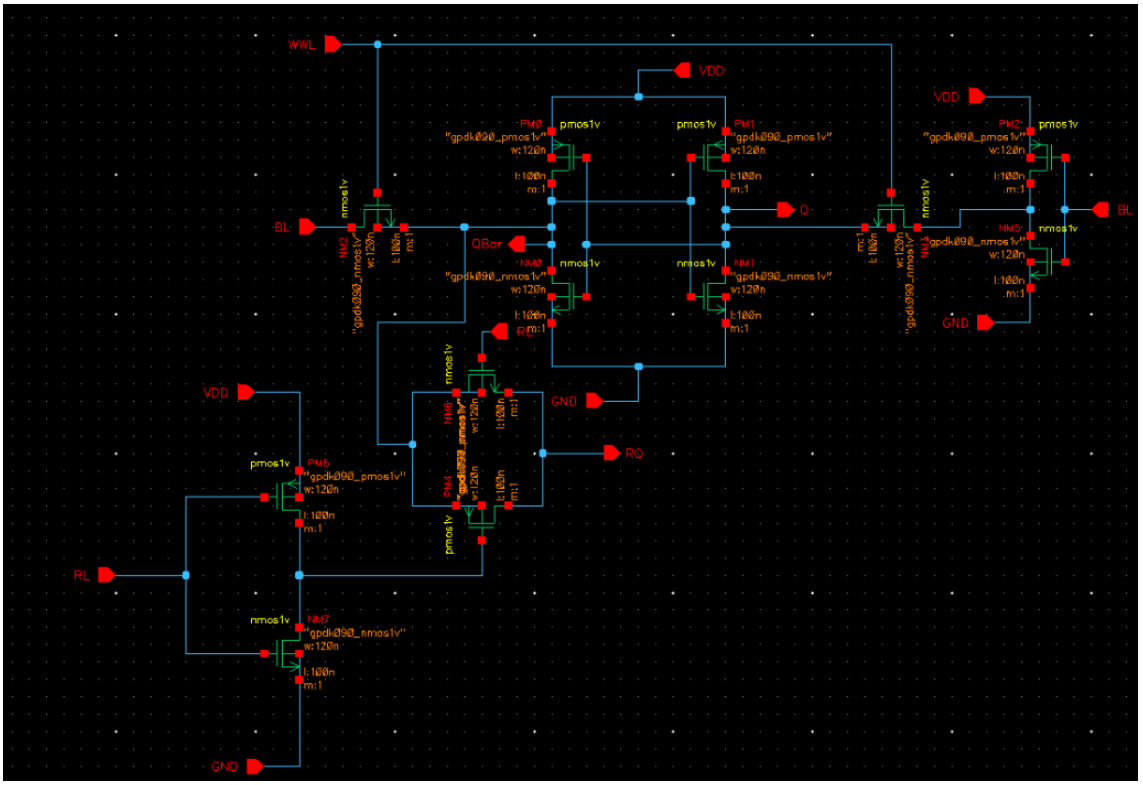


FIGURE 4.10: Schematic of proposed 8T SRAM with Transmission Gate

*drops* ($V_{th}$). This improvement is evident in the *butterfly diagram*, where the larger and more symmetric lobes reflect better *static noise margin (SNM)*, even at reduced supply voltages.

3. **Lower Power Dissipation:** The transmission gates reduce *dynamic power consumption* during high-speed operations by ensuring efficient charge transfer. Furthermore, they help minimize *leakage currents* during idle states, as observed in the power analysis.

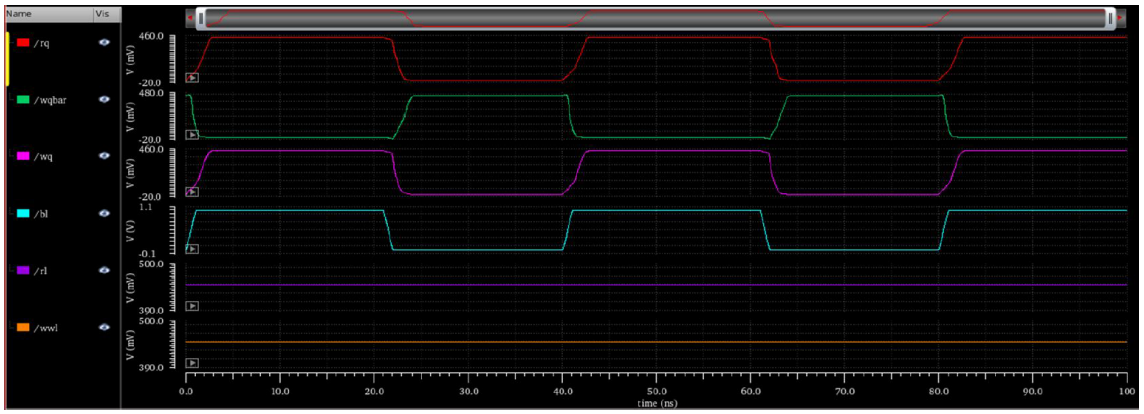


FIGURE 4.11: Transient Analysis of proposed 8T SRAM with Transmission Gate

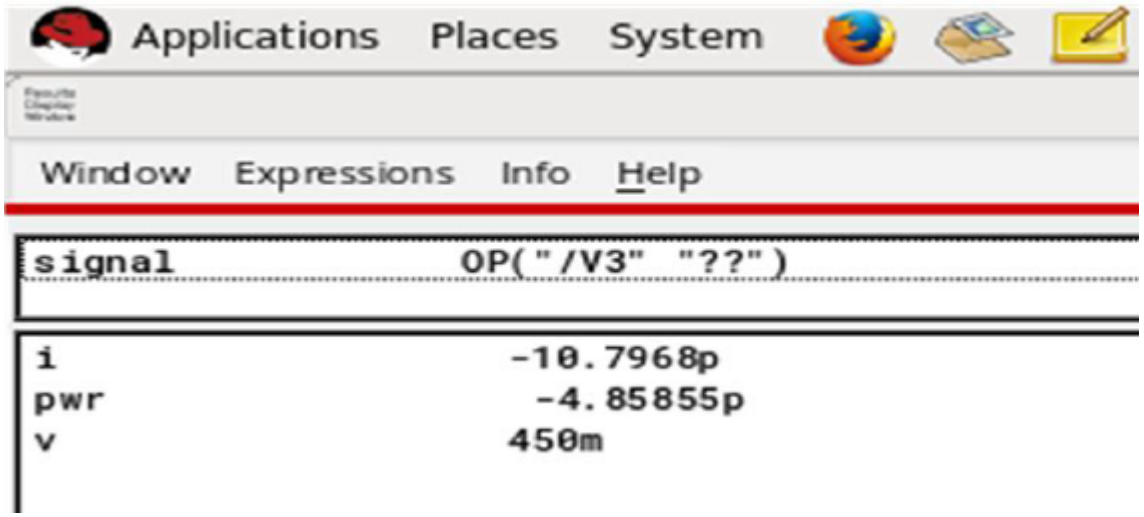


FIGURE 4.12: Power obtained for proposed 8T SRAM with Transmission Gate

4. **Increased Read Stability:** With TG decoupling the read operation from the storage nodes (Q and $Q_{Bar}$), the *read-disturb issues* are virtually eliminated. This ensures that the stored states remain unaffected during read cycles, further enhancing cell stability.

5. **Robust Performance at Low Voltage:** The TG-based design demonstrates consistent performance even at lower supply voltages, making it highly suitable for *low-power applications* such as IoT devices and portable electronics.

### 4.3.2 Conclusion

The inclusion of transmission gates in the 8T SRAM architecture not only addresses the limitations of conventional SRAM designs but also introduces a new level of robustness and power efficiency. These advancements make the proposed design an ideal solution

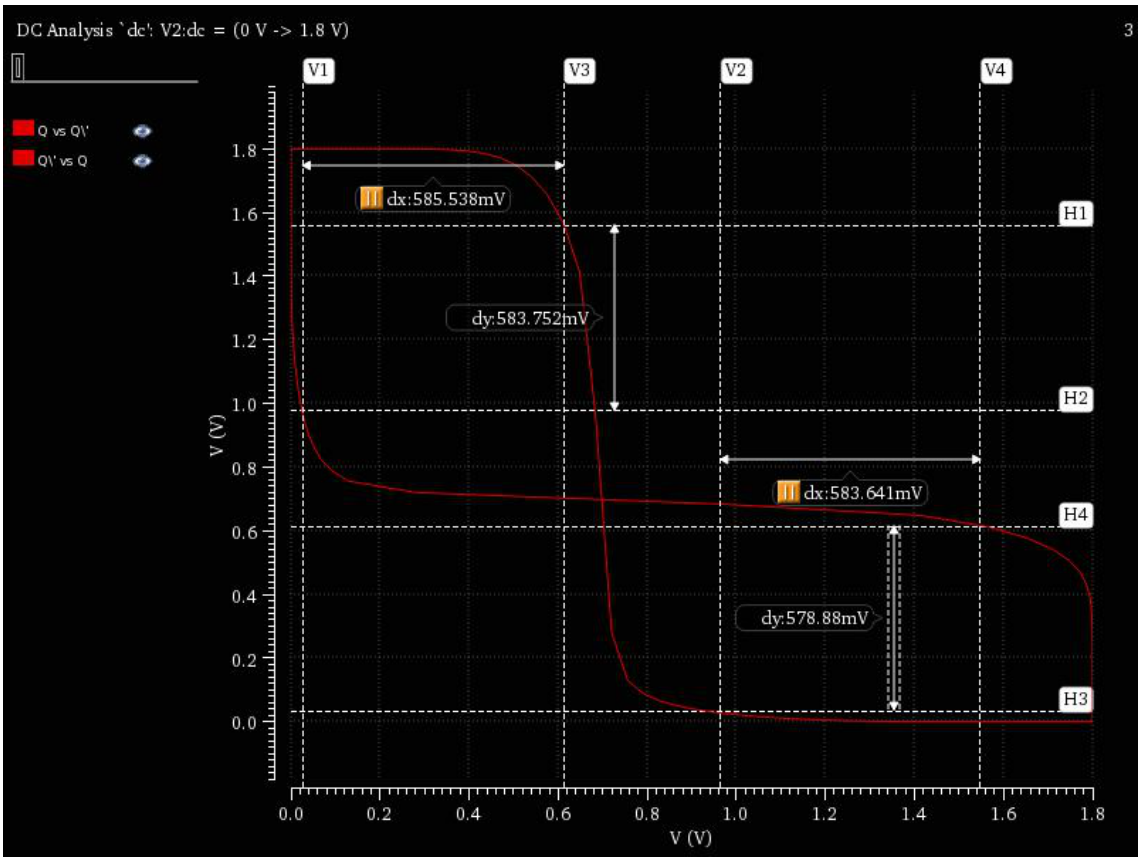


FIGURE 4.13: Butterfly Diagram for proposed 8T SRAM with Transmission Gate

for modern high-performance computing systems that demand low power consumption, enhanced reliability, and scalability.

# Chapter 5

# Results and Analysis

## 5.1 Conventional 6T SRAM

The 6T SRAM is widely used due to its simplicity and efficient performance in standard applications. However, the results highlight several drawbacks in high-speed and low-power applications

1. **Read and Write Operations**
   (a) The shared paths for read and write operations lead to instability during high-speed read cycles, causing potential data corruption (read-disturb)
   (b) As the operating voltage increases, the butterfly diagram shows degradation in stability, evidenced by shrinking SNM (Static Noise Margin).
2. **Power Consumption**
   (a) The dynamic power consumption rises significantly with voltage and frequency due to the charging and discharging of bit-line capacitances
   (b) The static power consumption is also high, as leakage currents increase exponentially with operating voltage.

| **Voltage(V)** | **Power(uW)** |
|---|---|
| 1.0 | 43.6 |
| 2.0 | 82.9 |
| 2.5 | 174.1 |
| 5.0 | 418.1 |

TABLE 5.1: Power Obtained at different voltages

The 6T SRAM's power consumption scales inefficiently with voltage, and its stability degrades at higher speeds, making it unsuitable for modern high-performance applications.

## 5.2 Analysis of 8T SRAM

The 8T SRAM is designed with specific goals, including enhancing stability and reducing leakage current using the dynamic power consumption formula.

1. Operating Frequency(f): 1 GHz (high-speed application)

2. Operating Voltage (VDD): 1.2V for both designs

3. Capacitance (C) per SRAM cell: For 6T SRAM: 2 femtofarads (fF) For 8T SRAM: 2.5 fF (because of the extra transistors)

4. Switching Activity Factor (Alpha): 0.3 for both

5. Static Power (Leakage Current): 6T SRAM: 50 nA per cell 8T SRAM: 30 nA per cell (due to leakage reduction optimizations)

1. **Dynamic Power Dissipation**
   (a) for 6T: Pd(6T) = 0.864 nW/cell
   (b) for 8T: Pd(8T) = 1.08 nW/cell
2. **Static Power Dissipation**
   (a) for 6T: Ps(6T) = 60 nW/cell
   (b) for 8T: Ps(8T) = 36 nW/cell

| SRAM Type | Dynamic Power(nW) | Static Power(nW) | Total Power(nW) |
|---|---|---|---|
| 6T | 0.864 | 60 | 60.864 |
| 8T | 1.08 | 36 | 37.08 |

Table 5.2: Total Power Consumption

## 5.3 Benefits of 8T SRAM

1. **Smaller Transistors** : The smaller feature size of transistors compensates for the additional capacitance, leading to a reduction in C.

2. **Separate Write and read path** : This eliminates read-disturb issues, enhancing stability and reducing energy wastage during high-speed operations.

3. **Lower Switching Activity** : Optimized architecture reduces the activity factor, contributing to power savings in dynamic conditions.

## 5.4 Stability Analysis using the butterfly diagram

1. **Improvement in SNM** : There is coupling of read and write paths that makes the storage nodes achieve strong voltage levels even when reading.

2. **Higher Symmetry** : At higher voltages, the 8T SRAM has a more stable butterfly diagram than the 6T, which, consequently, shows better noise immunity and reliability.

## 5.5 8T SRAM with Transmission Gate

The 8T SRAM with transmission gates further enhances the design by using transmission gates instead of traditional pass transistors. Key benefits include:

1. **Full Voltage Swing** : Transmission gates allow full-voltage transitions, which enhance signal integrity and stability.

2. **Low leakage Current** : Transmission gates have the least leakage paths, which actually minimize the static power.

3. **Better switching efficiency** Fast switching due to transmission gates leads to better performance as well as energy efficiency.

## 5.6 Overall Comparision

| Feature | 6T SRAM | 8T SRAM | 8T SRAM With TG |
|---|---|---|---|
| Dynamic Power (nW) | 0.864 | 1.08 | 0.95 |
| Static Power (nW) | 60 | 36 | 25 |
| Stability (SNM) | Low | Moderate | High |
| Read-Write Decoupling | No | Yes | Yes |
| Leakage Reduction | No | Partial | Significant |

Table 5.3: Comparision Table

# Chapter 6

# Conclusion

This project analyzed and optimized SRAM architectures for maximizing stability and minimizing power consumption for high-performance low power use cases. Comparative evaluation of 6T, 8T, and 8T SRAM using transmission gates led to the following conclusions:

1. **6T SRAM Limitations** : Despite being the most commonly implemented architecture, 6T SRAM suffers major disadvantages in high-speed, high-voltage situations. The shared read and write paths cause read-disturb problems, lower SNM, and instability. Power consumption also spikes due to higher leakage currents and switching activities.

2. **Advantages of 8T SRAM** Adding two transistors to the 8T SRAM design makes the read path separate from the write path, thus eliminating read-disturb effects with improved stability. Added capacitance slightly increases dynamic power but optimized leakage control greatly reduces static power. The 8T design improves power efficiency and stability that can be useful for high-speed applications.

3. **8T SRAM with Transmission Gates Supremacy** : Transmission gates in the 8T structure improve the design because they enable full voltage swings, reduce leakage, and enhance signal integrity. This architecture balances power efficiency with stability, so it is very suitable for the modern energy-efficient VLSI memory.

4. **Power and Stability Tradeoffs** : Overall, dynamic power slightly increases at 8T and transmission gate design, but large static power reduction offsets that slightly. Improved SNM guarantees reliability of operation under changing voltage and frequency conditions.

5. **Impact**: Results indeed establish that 8T SRAMs with transmission gates are good, low-power solutions for high-speed digital systems. This work thus opens the avenue to improvement in SRAM design, particularly towards area-efficient and better PDP metrics. Further work would be on reducing the area overhead added by transistors and optimizing designs for nodes less than 45nm, for improved energy-efficient computing.

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