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Analysis of Power, Delay and SNM of 6T & 8T SRAM Cells

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Abstract— **6T and 8T SRAM cells have been compared on 180nm technology using an industry-standard Cadence Virtuoso Tool. It's challenging to make an SRAM cell with low power consumption and stay in a small space. The consumption of power on both the SRAM cells are compared. The parameters of SRAM Static Noise Margin (SNM), Write Delay, Read Delay and average power consumption are examined and discussed thoroughly. Results illustrate that Read delay and Write delay will decrease of 8T as differentiate to 6T SRAM. Effect of V_{dd} on average power consumption and delay is further highlighted in the present paper. These comparisons then can provide a vision to designers for finding an optimal supply voltage for a particular design while minimizing the design to process variation.**

Keywords— SRAM cell, Cadence Virtuoso, SNM, Read Delay, Write Delay.

I. INTRODUCTION

SRAM is a memory unit that demands no periodic refresh, and each bit can be accessed (read/write) independently. SRAM has a prominent role in the circuit used for low power VLSI systems [1]. It is complicated to design chips of high efficiency with low power consumption at the same time. SRAM has offered a widely used application for chips cache/memory in microprocessors, gaming hardware, operating systems, portable electronic devices as it provides qualities like high speed of data transfer, low power supply and no periodic refresh requirement [2][3].

It has the capability to store value in its memory until power is given. The only difference in the circuit designing of 6T and 8T SRAM is of the addition of two transistors in 8T which is used as a buffer in the circuit as read operation most vulnerable in 6T SRAM [4]. 6T SRAM is broadly used as it is compact and has a symmetrical shape and needs less area [5]. The relevance of SNM is that it should be highly reliable memory of SRAM. In the sub-threshold region, standard 6T SRAM cell is characterized by poor reading and writing ability, and a decrease in SNM in various threshold voltage fluctuations [6].

8T SRAM has a more steady and credible memory cell form as compared to 6T SRAM [7]. This is a vulnerable decision when memory is produced for low power consumption as memory configurations are inclined to consume a lot of space in System on Chip (SoC), a small 6T SRAM cell would be one more fascinate option [8][9]. Therefore, this is the major reason for drawing a comparison of 6T and 8T SRAM have been expedient based on its parameters.

II. CIRCUITS

The name of components, control signals and nodes of 6T SRAM is exhibited in Fig.1. In this figure, two CMOS inverters are connected that act as NOT gate and are called their memory part. The memory part is linked to two-bit lines BL & BLB which is used as read & write lines. M5 & M6 transistors are the access transistors [10][11]. To access these two lines, access transistors are used when the word line (WL) is enabled (1) otherwise memory part will be in a hold state if WL is disabled (0). BL & BLB will play a part of I/P lines when something is write in memory, and they will play a part of O/P lines when there must read from memory [12-15]. Additionally, a precharge circuit will be utilized for read & write operations so that bit lines are precharged to V_{dd}. Value of bit lines will send to a sense amplifier which acts as a comparator and like if bit line value decreases, then the output should be 1 and vice-versa [16].

The performance failure of the readings is sometimes detected, caused by an increase in power of the nodes Q or QB of inverter resulting in the output of another inverter means that the voltage at one of the nodes QB or Q begins to drop data loss [17][18].

When the read operation is performed, this means the memory part should hold some values, let's say Q=1 and QB=0 and vice-versa. To read in memory, bit lines BL & BLB are used. To use these bit lines Word Line (WL) is enabled. So if WL is 1 the access transistors will be ON. If these are ON these lines can be used. To read some value, bit lines will act as output lines. The Bit Lines are precharged to the voltage V_{dd}. The storage node (Q or QB) which is having 0 will be discharged due to voltage difference. This discharge will then be sensed by a sense amplifier to register a read operation. Let's say if value of bit decreases then output should be 1 and vice-versa. If this happen then data is successfully read from the memory [19].

Similarly, for write operation, some values are given to Q and QB. Then W_L is enabled to access BL and BLB which acts as input lines. As bit lines are the input lines to control over these lines is necessary, so one bit line is connected to ground. Now there will be voltage difference where bit line is grounded. Let's say QB is grounded then voltage decreases this means M1 and M2 will get affected. If voltage is less than threshold voltage of M2, this means M2 is off then M1 is on and hence output is obtained. By this way write operation is performed in the memory [19][20].

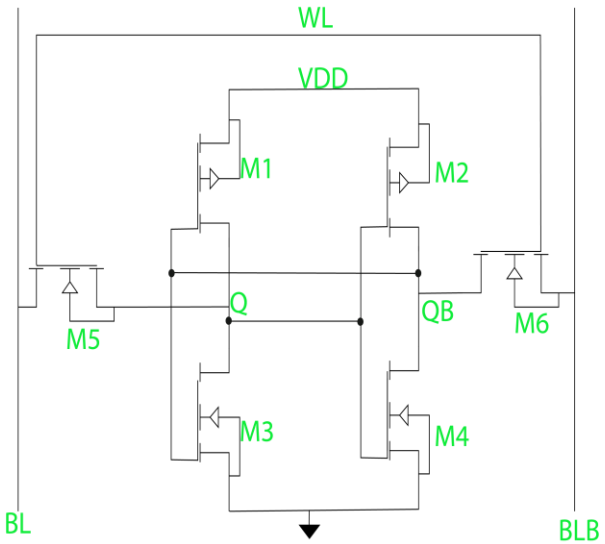


Fig.1 Diagrammatical view of 6T SRAM Cell

Name of components, control signals and nodes of 8T SRAM cell used in comprehensive comparative work is illustrated in Fig.2. In this 8T SRAM cell, two back-to-back inverters are connected with M5 & M6 access transistors, for read buffer M7 and M8 transistors are utilized [21][22]. For the write operation word line WWL is used and RWL is used for the read operation.

The addition of the extra two transistors in 8T SRAM makes the size of the circuit bigger in comparison to 6T SRAM, as a result it consumes a lot of space on SoC. Both the SRAM cells are connected to the precharge, write driver, and sense amplifier which makes them a complete circuit [23].

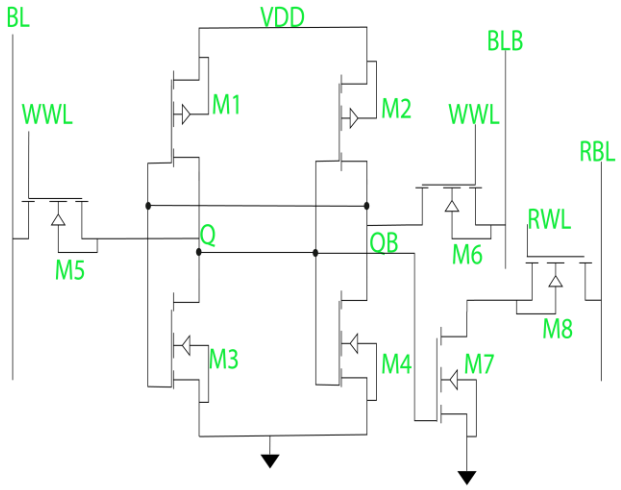


Fig.2 Diagrammatical view of 8T SRAM Cell

III. SRAM PARAMETERS

Hold Margin (SNM_H), Read margin (SNM_R) and write margin (SNM_W), average power dissipation, write delay, and read delay are key parameters. SNM is an essential parameter to determine SRAM stability. The minimum noise voltage required to switch the state of cell is defined as SNM [24]. Noise margin explains, up to what extent, IC allows noise in transmission of logic '0' and logic '1'. If we receive a range of voltages then we identify logic '0' or '1' based on it. The received voltage range widens, based on noise in the circuit. So, for errorless transmission, a noise margin is required [24][25].

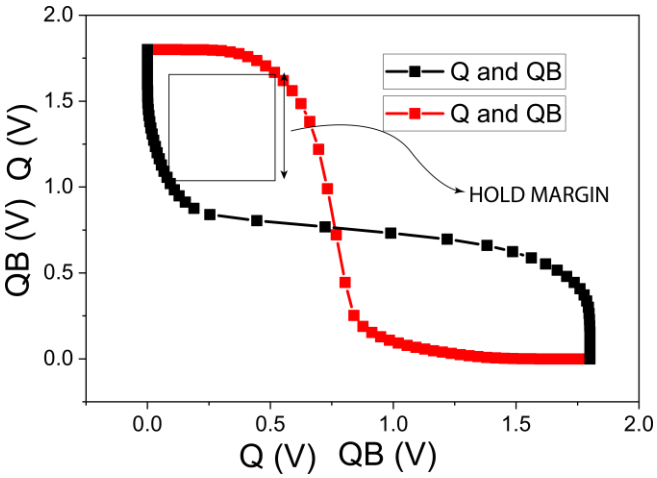


Fig.3 SNM_H of 6T SRAM

A. SNM_H

The noise to be accompanied when the hold period to spin saved data in cell is defined as SNM_H. During the hold mode access transistors M5 & M6 are OFF and bit lines will also disconnect, only two cross-coupled inverters are used that is M2 and M4. All the operation controlled by WL which is kept 0 for the Hold state. The noise margin can be determined for hold mode by considering different values for Q and QB & vice-versa. Fig.3 exhibits hold margin of 6T SRAM and Fig.4 exhibits a hold margin for 8T SRAM where Q and QB are data storage of cells. By comparing these two graphs we observe there is no significant deviation take place in SNM_H [25][26].

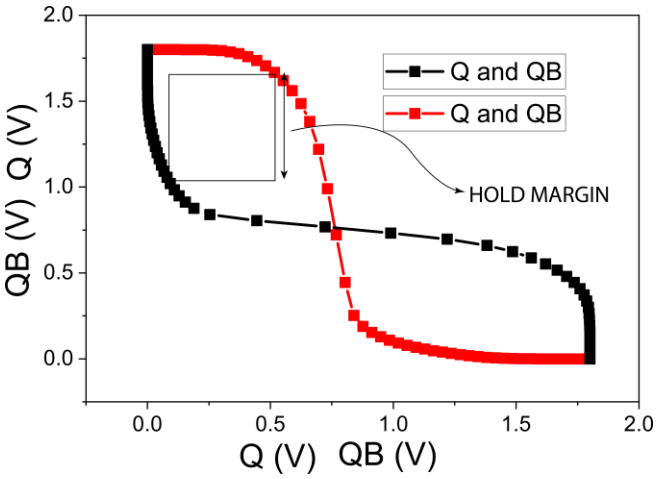


Fig.4 SNM_H of 8T SRAM

B. *SNM_R*

SNM_R is determined by the largest square formed inside the butterfly curve. Differential voltage should not be large as it flips the state of invertors [27]. Meanwhile, in read operation M5 & M6 are ON and both bit lines are at potential V_{dd}, that is logic '1'. Then there is supply of source to Q and change voltage to Q and analyse the data of QB and then performed opposite with the QB variantion in values and note the Q value [27][28]. Fig.5 exhibits the read margin of 6T SRAM and Fig.6 exhibits read margin of 8T SRAM. By comparing these two graphs we observe SNM_R of 8T is higher than 6T as the square inscribed in the curve of 8T is slightly larger.

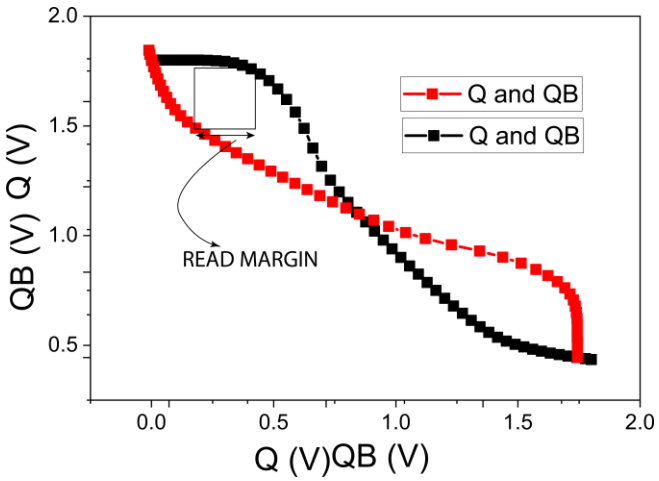


Fig.5 SNM_R of 6T SRAM

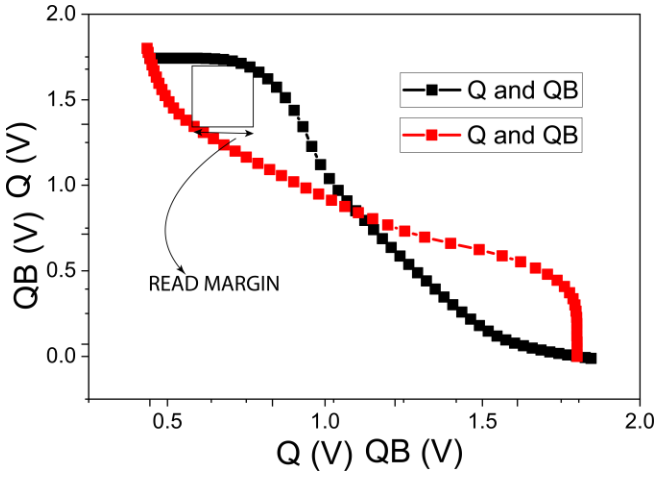


Fig.6 SNM_R of 8T SRAM

C. *SNM_W*

SNM_W is a framework required compute SRAM cell write stability as it is the minimum bit line voltage essential to spin the state of SRAM. For a write operation, Word Line (WL) is put to logic '1' which allow access transistors M5 & M6 to connect cell to bit lines, after that content from bit lines is shifted to [29][30]. SNM_W is determined by forming the largest square inside the curve. Fig.7 shows write margin of 6T SRAM and Fig.8 shows write margin of 8T SRAM. By comparing these two graphs we observe SNM_W of 8T is higher than 6T as square inscribed in 8T is slightest larger [31].

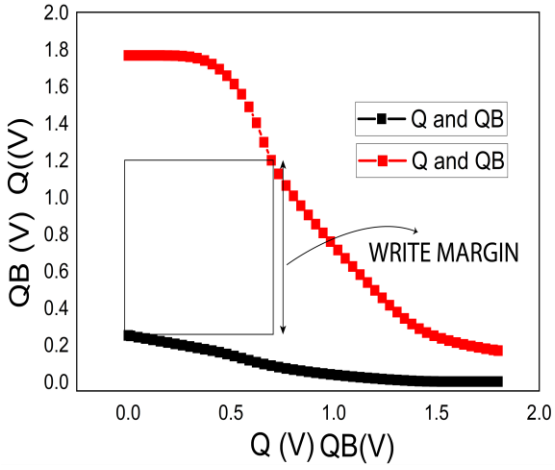


Fig.7 SNM_W of 6T SRAM

IV. ANALYSES AND RESULTS

This section we have examined results, and analysed the parameters completely performed on 6T and 8T SRAM. A thoroughly discussion have been made on write delay, read delay, and average power consumption.

A. *Read Delay*

At the time we increase voltage read delay decreases. Delay is a distinction between time when the WL exceeds half of value when subtracts a fraction of its value when we read data with WL and read enable is higher [32]. Fig.9 exhibits the plotting of Read Delay appearing in various V_{dd}. From the figure, it is concluded that read delay decreases more of 8T with an increase in voltage in comparison to 6T SRAM.

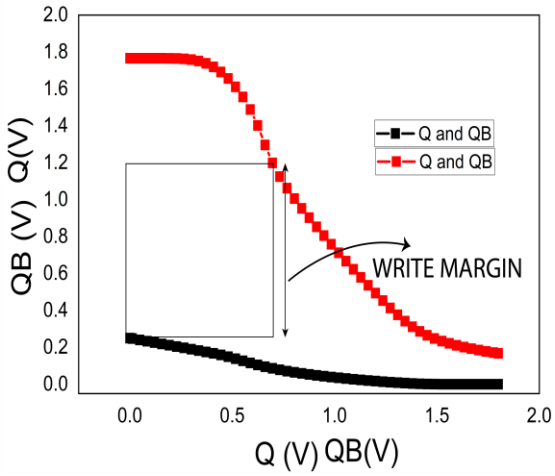


Fig.8 SNM_W of 8T SRAM

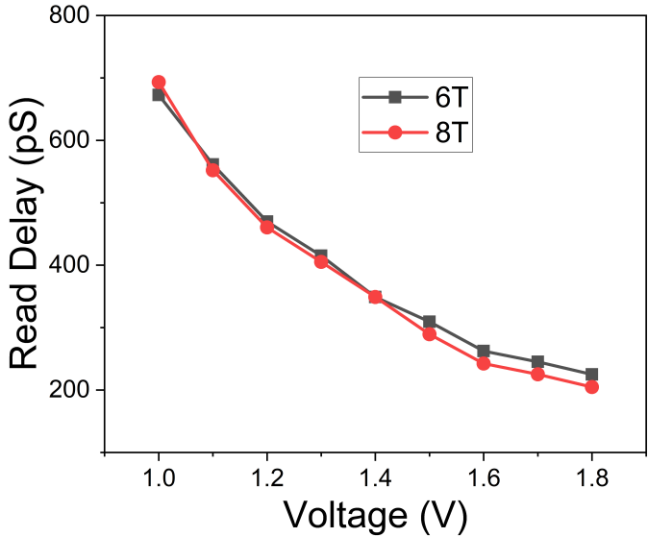


Fig.9 Read Delay v/s V_{dd}

Fig.10 Write Delay v/s V_{dd}

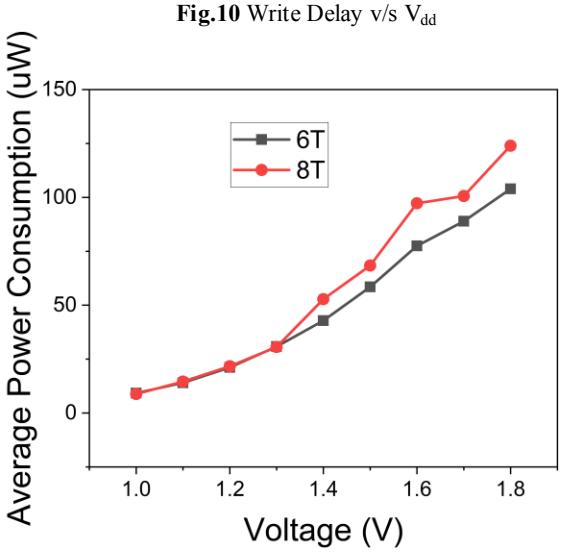


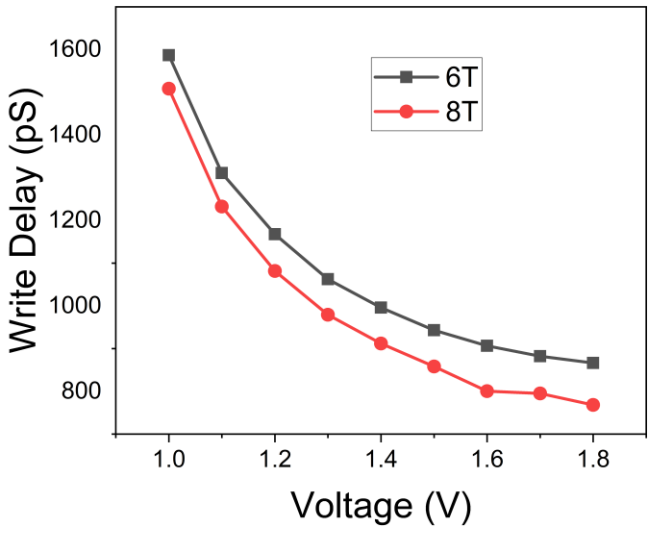
Fig.11 Average Power Consumption v/s V_{dd}

B. Write Delay

At the time we increase V_{dd} write delay decreases. We calculated write delay as a distinction between time when WL exceeds half of its value during Q exceeds half of its value when we write in cell and WL is higher [33]. Fig.10 exhibits the plot of Write Delay at various V_{dd}. From the figure, it is concluded that write delay decreases more of 8T as we rise voltage by comparing to 6T SRAM.

C. Average Power Dissipation

As we increase V_{dd} , average power dissipation also increases [34]. We calculate the Read Delay as a distinction between time when WL exceeds half its value during result subtracts a fraction of its value when we read data with WL and the read enable is higher [34][35]. Fig.11 depict the plot of average power consumption at various V_{dd} . From the figure, we can conclude that comparatively, 8T SRAM got more power consumption compared to 6T SRAM as the voltage is incresed.



V. CONCLUSION

In this paper, it is concluded that on the various parameters such as in SNM_H there is no such change in both the cells and SNM_R and SNM_W is more for 8T than 6T SRAM. Write delay, read delay, and average power consumption was also discussed and the variation of average power consumption and delay has been observed as an operation of the supply voltage. It is concluded that for better efficiency 8T SRAM cell consume more power than 6T SRAM.

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