

Diagram illustrating a 11-stage current mirror array. The array is connected between a +3.3V supply and GND. The stages are labeled C1 through C11, with values: C1=100n, C2=100n, C3=100n, C4=100n, C5=100n, C6=100n, C7=100n, C8=100n, C9=1u, C10=1u, and C11=4.7u. The output is taken from the node between the PMOS transistors and the current sources.

Equations for the output voltages:

$$V_{DD} : 6 \times 100n + 1 \times 4.7u$$

$$V_{REF}, V_{DDA} : 1 \times 100n + 1 \times 1u$$

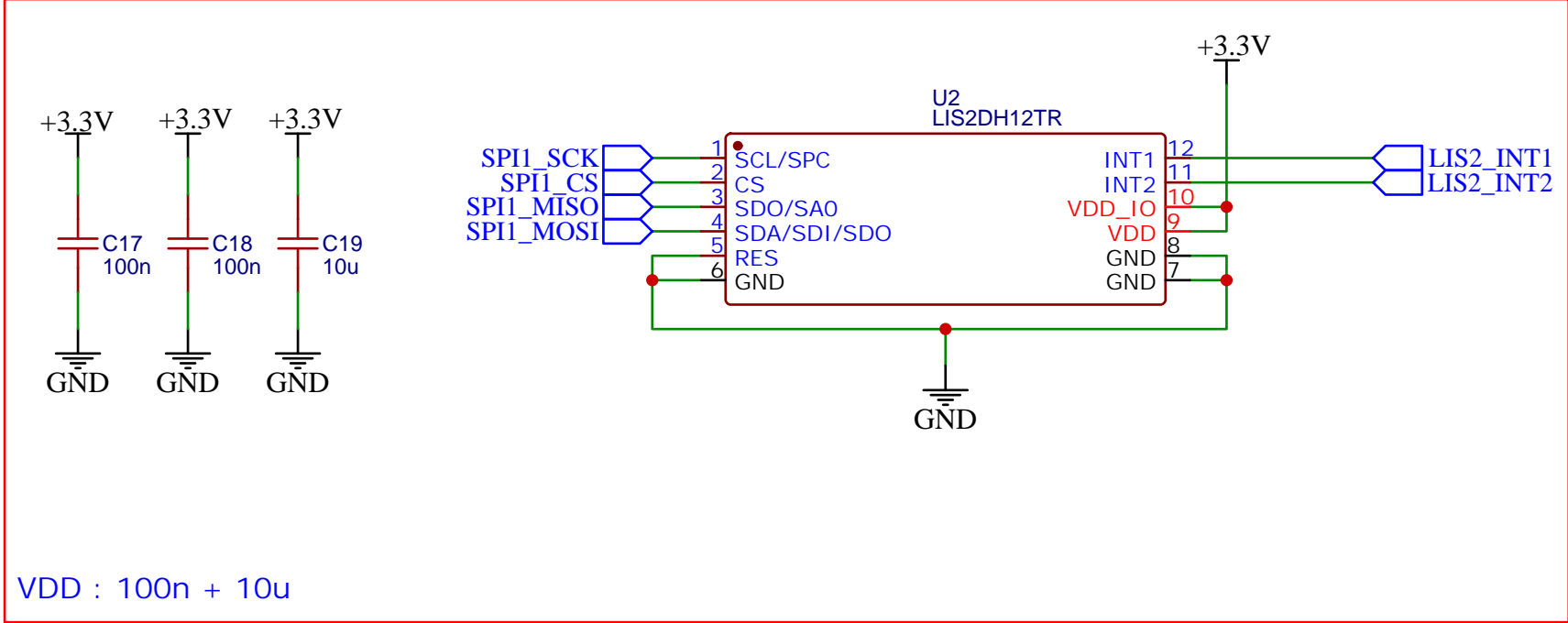
The schematic diagram illustrates the SWD interface for the STM32F103C8T6 microcontroller. The microcontroller is represented by a box labeled "KEY1 K4-6 x 6_TH". The SWD pins are connected to the J2 header (HDR-M-2.54_1x5) as follows:

- SWCLK is connected to pin 2 of J2.
- SWDIO is connected to pin 3 of J2.
- NRST is connected to pin 4 of J2.

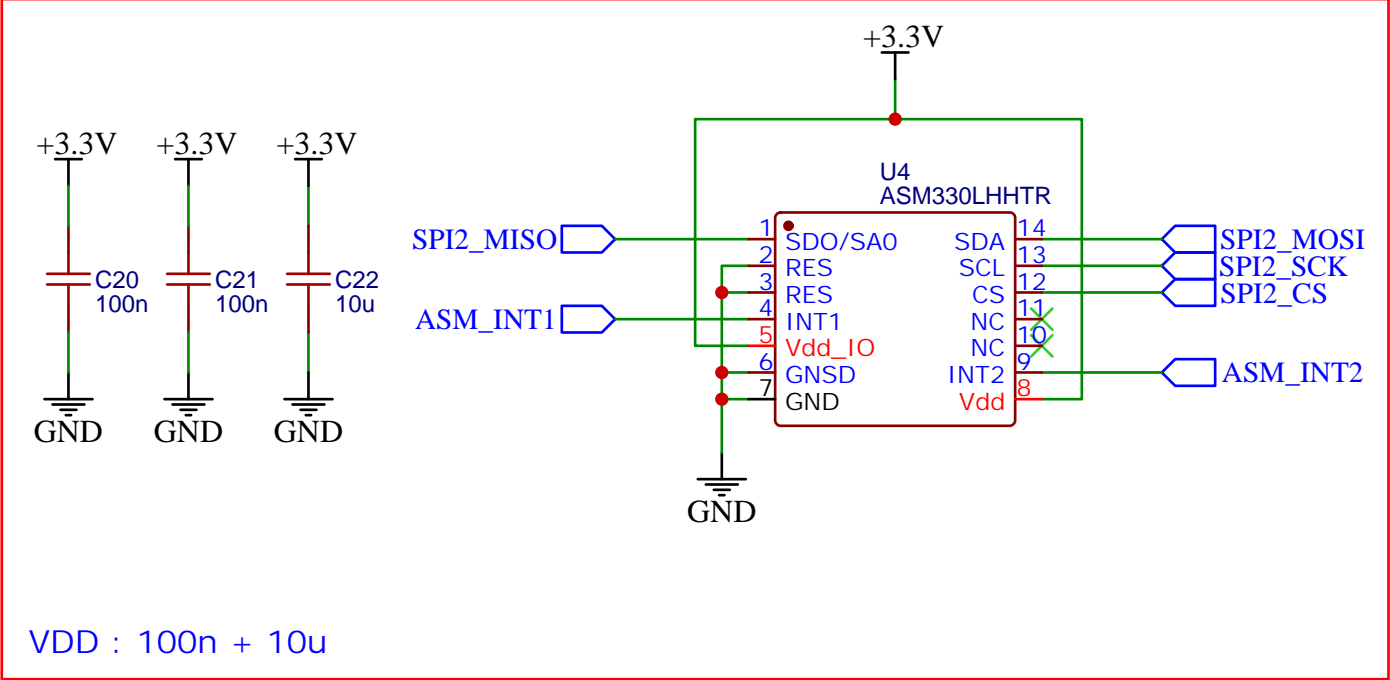
The NRST pin is also connected to a 10k pull-up resistor (R8) to +3.3V and a 100nF capacitor (C13) to GND. The J2 header is labeled HDR-M-2.54_1x5. The microcontroller is labeled KEY1 K4-6 x 6_TH.

C: min 10V

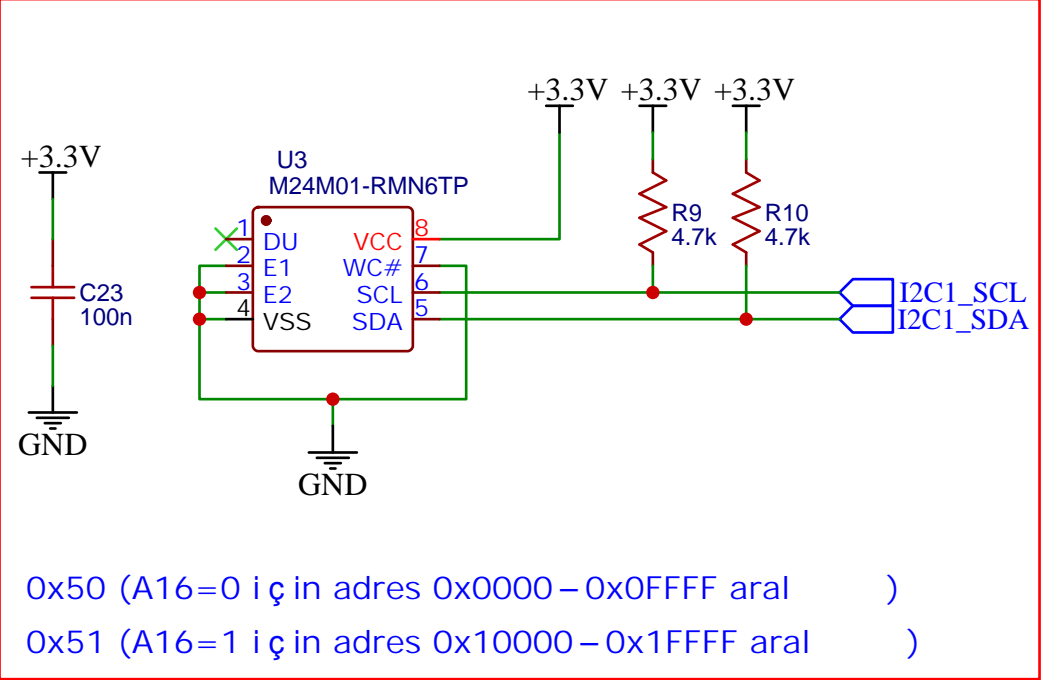
LIS2DH12 ACCELEROMETER



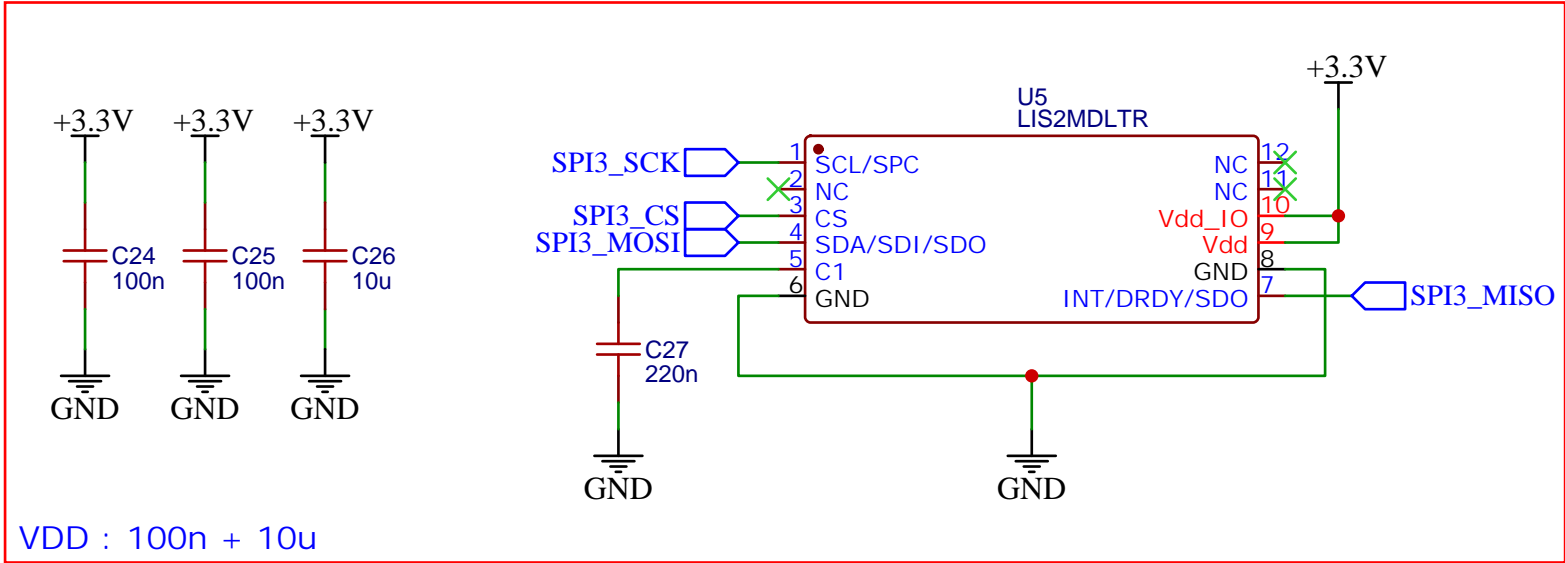
ASM330LHH GYROSCOPE



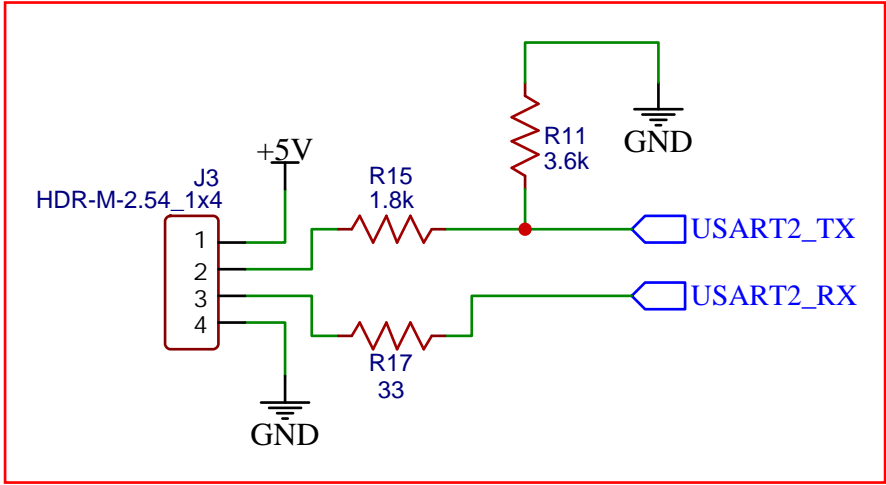
EEPROM



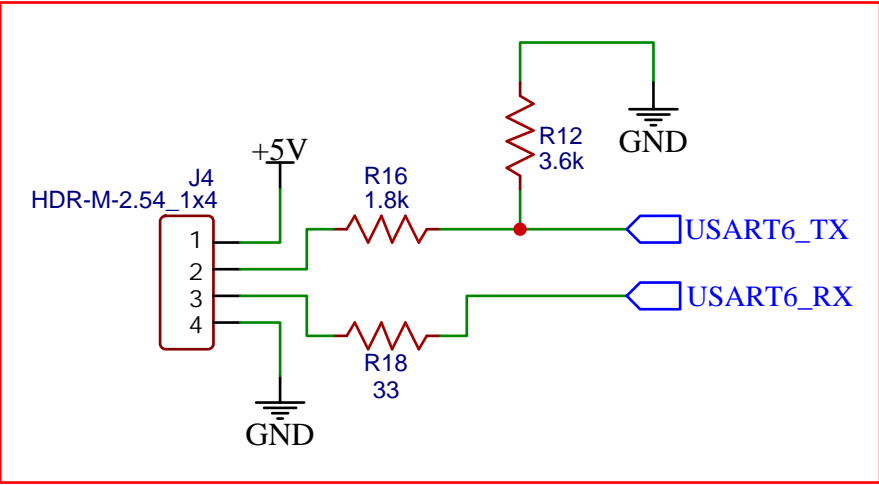
LIS2MDL MAGNETOMETER



UART CONNECTOR 1 (5V)



UART CONNECTOR 2 (5V)



I2C2 CONNECTOR

