

# Intro to ASIC Tapeout & Project

98-154: Intro to Open-Source Chip Design

# Why open-source chips?

- Freedom & Control
- Reproducibility
- Lower barrier-to-entry
- Lower cost = better competitiveness
- Security & Auditability

# Security

- Significant risk of backdoors or untrusted logic in chips
  - Inserted by manufacturer, compelled by governments, or maliciously inserted at factory
- Open-source can make it easier to trace the correctness of a design through the design and tapeout process
- Full lecture on security later this semester

# Self-Hosting, Trustworthy Computing

Great talk by Gabe Somlo on the importance of trustworthy, open-source machines: [Bootstrapping a Libre, Self-Hosting RISC-V Computer \(2021\)](#)

Based on the classic: [Reflections on Trusting Trust \(1984\)](#)

# **History of open-source ASICs**

# 1981: MOSIS

- One of the earliest multi-project-wafer (MPW) tapeout services
- Provided significant support to tapeout programs at universities
- Not quite open-source but worth noting

# 2019: Raven

- RISC-V SoC using only open-source tools
- Relying on abstracted layout; not truly open-source because the process node wasn't open
- First-time silicon success with X-Fab tapeout
- [https://wiki.f-si.org/images/c/c4/Qflow\\_Raven\\_FSiC2019.pdf](https://wiki.f-si.org/images/c/c4/Qflow_Raven_FSiC2019.pdf)

# Jun 2020: SKY130 PDK Released

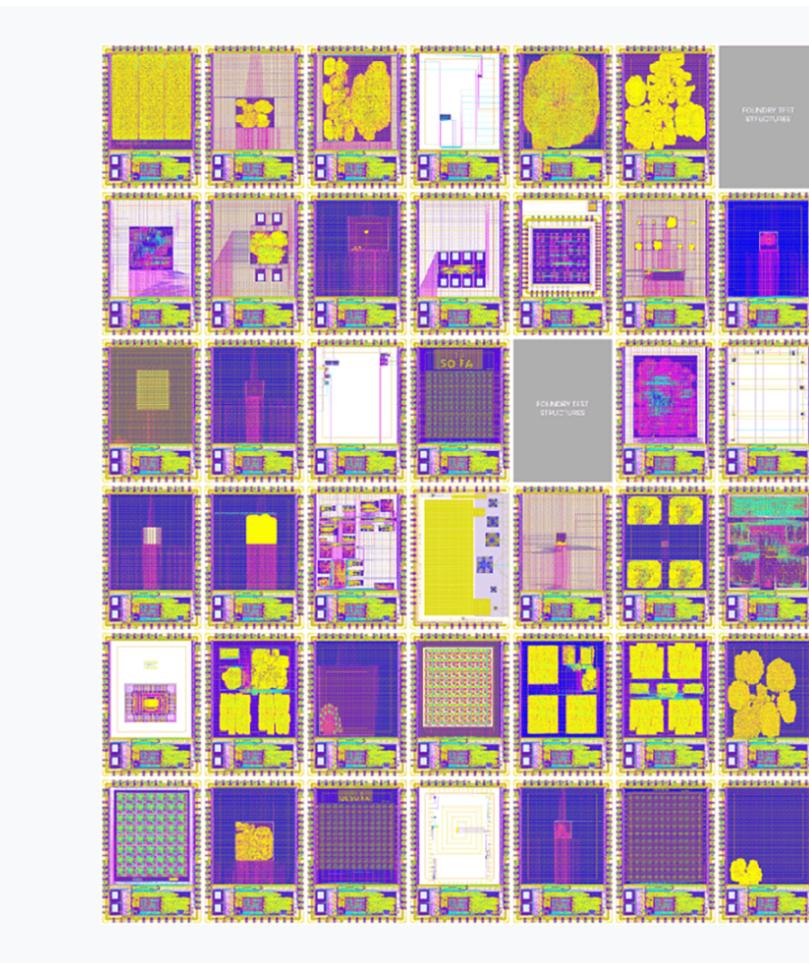
- Previously thought to be impossible, Google and Skywater released a 130nm process node, 100% open-source down to all the manufacturability details.
- <https://skywater-pdk.readthedocs.io/en/main/>
- [https://diychip.org/sky130/sky130\\_fd\\_sc\\_hvl/cells/](https://diychip.org/sky130/sky130_fd_sc_hvl/cells/)

# Jun 2020: Open MPW Tapeout Program

- Shuttle runs sponsored by Google and Efabless (40 designs per tapeout)
- Designs required to be fully open-source, minimal other requirements
- [https://efabless.com/open\\_shuttle\\_program](https://efabless.com/open_shuttle_program)

# Dec 2020: MPW-1 Tapeout

First Open MPW tapeout, ~45 submissions, selected 40 designs as a lottery



**MPW-1**  
45 designs submitted in 30 days!

- > 9 x Open processor cores
- > 9 x SoC's
- > Crypto-currency Miner
- > Robotic App Processor
- > Amateur Satellite Radio Transceiver
- > 7 x Analog/RF
- > 5 eFPGA's

# May 2021: ChipIgnite Launched

- Commercial version of MPW program
- Relatively low cost (\$10K), guaranteed silicon
- Supports open-source or proprietary tools
- <https://efabless.com/>

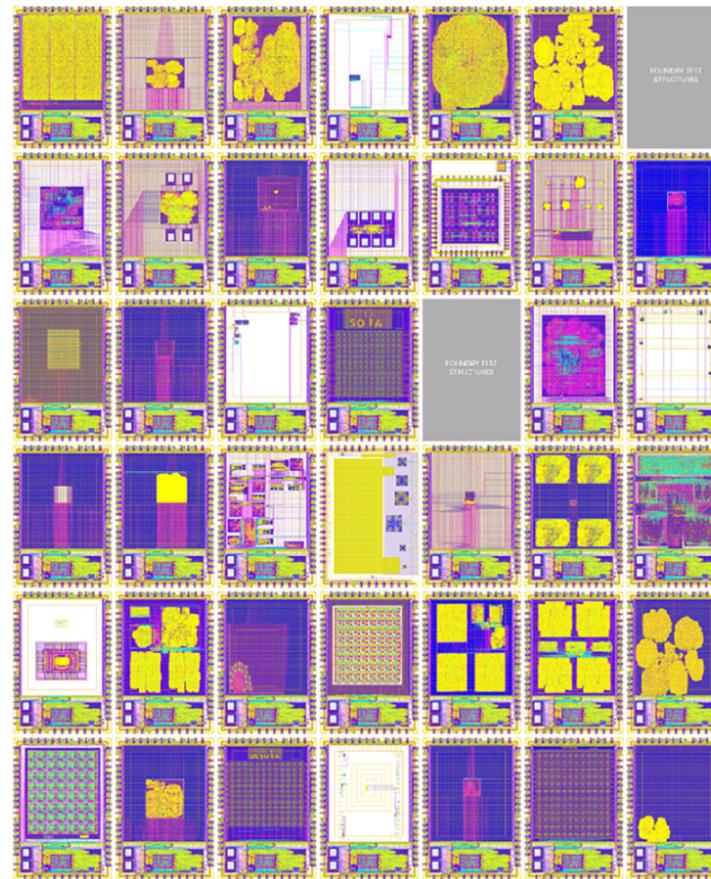
# Jul 2021: MPW-2 Tapeout

Second Open MPW tapeout, ~56 submissions, selected 40 designs to be manufactured

## MPW-2

56 designs submitted in 30 days!

- > 11 x Open processor cores
- > 11 x SoC's
- > Crypto-router
- > Time to Digital Converter - LIDAR
- > Multi-project harness for Caravel
- > 17 x Analog/RF
- > 3 eFPGA's



# Sep 2021: MPW-1 Chips Back From Fab

- Found significant clock-tree issues as a cascading failure
  - Clock tree was not synthesized correctly, high clock skew
  - STA tools did not calculate parasitics correctly
  - Led to severe hold-time path violations
  - No top-level timing analysis & no testing using proprietary tools

# Nov 2021: First WOSET

Workshop on Open-Source EDA Technology (at IEEE ICCAD conference)

<https://woset-workshop.github.io/WOSET2021.html>

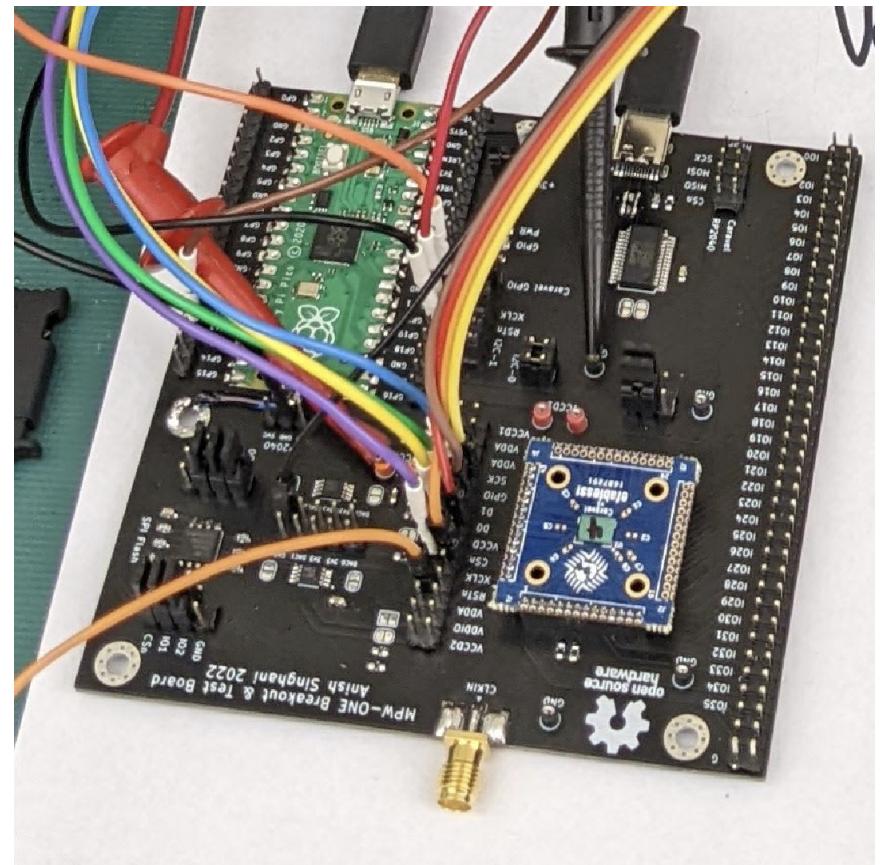
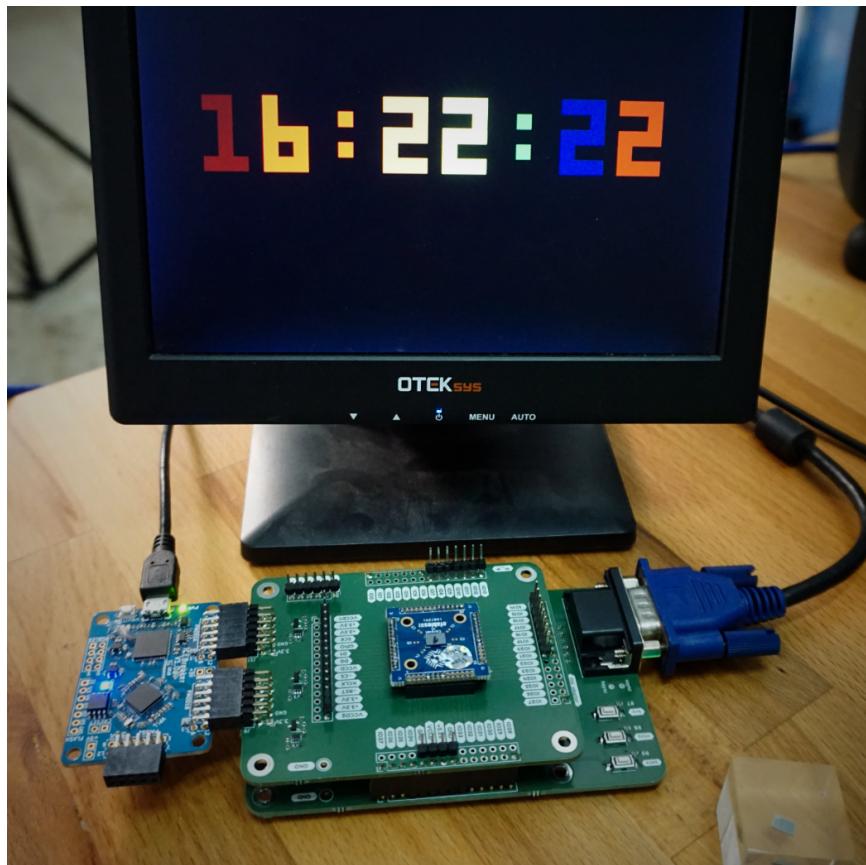
# Late 2021: MPW-3

- Many bugs fixed (parasitic extraction, etc.)
- Still did not fix top-level hold violations so I/O is still questionable
- Chips not back from fab yet

# Jan 2022: MPW-1 Bringup Success

Able to get some amount of success via voltage manipulation

[asinghani/mpw1-bringup](https://github.com/asinghani/mpw1-bringup)



# Other MPW Tapeouts

- MPW-4 (December 2021)
- MPW-5 (March 2022)
- MPW-6 (June 2022)
- MPW-7 (November 2022)
- MPW-8 (December 2022)

# Jul 2022: SKY90FD Released

- Second open-source process, Skywater 90nm released
- Still working on building infrastructure for taping it out

# Sep 2022: TinyTapeout

- Open MPW shuttles work great, but 40 designs was limiting, especially for learning purposes
- Despite evolution in tools, still not easily approachable to a beginner
- TinyTapeout gives designer a tiny area (~hundreds of gates) to learn how to build a design; a few hundred designs get combined onto one chip submitted to ChipIgnite
- <\$100 per-design cost

# Dec 2022: GF180MCU MPW-0

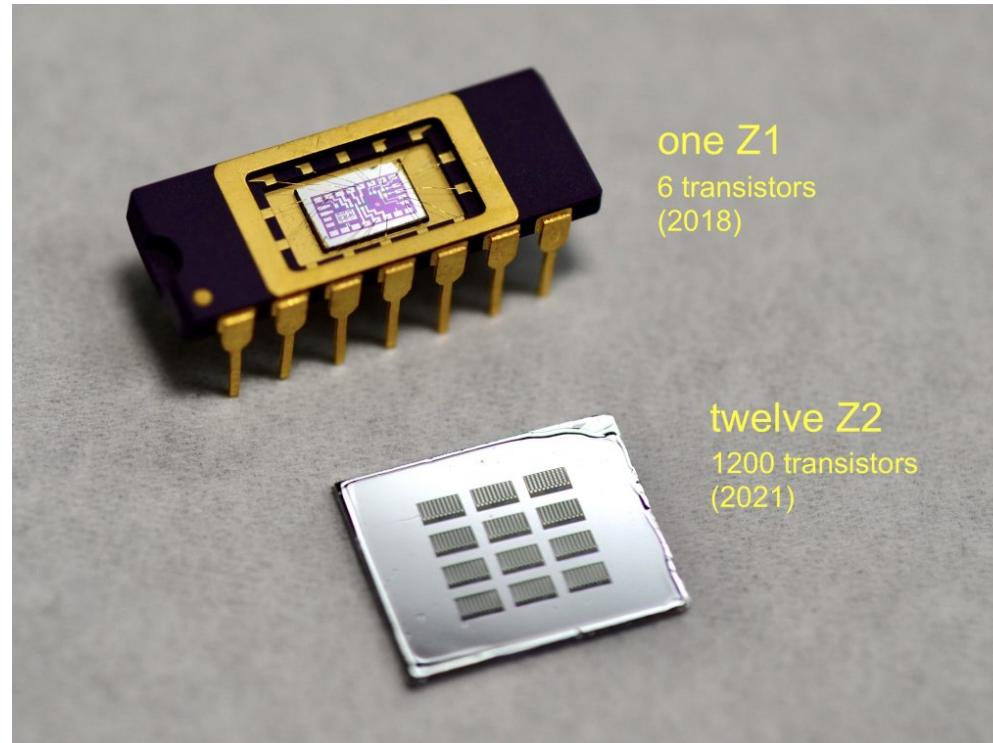
- GlobalFoundries 180nm process released as open-source
  - This is a different fab from SKY130/SKY90FD
- First tapeout at the end of 2022, same lottery system
- Tiny\_User\_Project as a way to build up from TinyTapeout to full shuttles
- <https://platform.efabless.com/shuttles/GFMPW-0>

# Feb 2023: SiliWiz

- Aiming to bring TinyTapeout-level simplicity to analog design
- Not manufacturable, but incredible as a teaching tool
- <https://app.siliwiz.com/>

# Open Chip Fab

- Sam Zeloof home chip fab (mostly single-gates and analog components)
- CMU Hacker Fab



# TinyTapeout: Economy of Scale

- \$10K to tape out 3000um x 3000um chip with I/O
  - Split up into a few hundred designs, sell slots for \$25 each
  - Chips on boards for \$100 each
- Can fit a few hundred gates onto a slot, for simple teaching-level design
- Targeted at schools and hobbyists

# TinyTapeout: How It Works?

- How can we build up a way to combine several small logic designs into a chip?
- Even with automated tools, synthesizing a large design is much slower than synthesizing many small designs and interconnecting them together
- However, there are limits on how much density we get with interconnecting many designs

# TinyTapeout: How It Works?

- Scan Chain
- Example Designs from TT02
- TinyTapeout Template

# Course Final Project

- Our final project will be similar to TinyTapeout but entirely for this class
- Aim is to tape out using ChipIgnite in June
- 250um x 250um design area (roughly up to 2K gates)
- 12 inputs, 12 outputs, 1MHz target clock speed

# I/O Interface

- 12 inputs, 12 outputs + clock + reset
- For outputs, consider:
  - Multiplexing
  - External Shift Reg
- Can use FPGAs for testing your design
- We can likely get other hardware peripherals if you need them as part of your design + use TechSpark to prototype

# Input Peripheral Options

- 12 input pins (plus dedicated clock & reset)
  - Buttons
  - Switches
  - USB-UART
  - Simple digital sensors
  - Bit-Banging from microcontroller
  - ???

# Output Peripheral Options

- 12 output pins
  - LEDs (can multiplex up to 36 LEDs on 12 pins)
  - 7-segment display (can multiplex 4 of them on 12 pins)
  - External Shift Register (can do a lot of I/Os with just a few pins, but relatively slow)
  - Read-in from microcontroller
  - ???

# Project Ideas

Doable using only drag-and-drop tools

- Hex to Seven-Segment Converter
- Combination lock
- LFSR-based Random Number Generator
- Popcount or First-Set Bit
- LED Light Show
- BCD Counter
- ??? (your idea here)

# Project Ideas

Fairly straightforward with SystemVerilog and Yosys.

- Multiplier
- Calculator
- PIN code lock
- RGB LED Controller / Light Show
- UART transceiver
- Hamming Code
- PWM Motor Controller
- ??? (your idea here)

# Project Ideas

The fun stuff!

- Tiny “FPGA”
- CORDIC
- 4-bit CPU (like a 4004?) - can use external memory
- Caesar cipher, AES-SBox, etc.
- Conway’s Game of Life
- Serial port (UART)
- Sound synthesizer
- ??? (your idea here)