**Self-Evaluation**

I believe the design is comprehensive with room for improvement.

**The Good Things**

The best thing about this design is that it incorporates all the core architectural requirements, with as much efficiency as possible in this short span of time.

The thing I’m most excited to share is that the pipelining techniques used in this design have allowed me to achieve an average of 3.38 clock cycles per opcode.

Another major thing that I focused on was crafting an automated excel sheet, and so I was able to spend less time on manual conversions and more time on the CPU.

**The Bad Things**

The wiring could be done better. In its current state, the circuit looks a little messy in some areas, where components have been added without adequate spacing.

In some places, comparators are used, and they may have a better replacement.

Moreover, some of my custom circuits have default Logisim appearance, whereas some others have custom appearance. This leads to confusion and errors when designing the circuit and so I provided the suffix ‘styled’ to most custom circuits.

One of the mistakes I made was trying to finish the matmult operation is one clock cycle using a circuit with 8 inputs and 4 outputs. It required a lot of computation power and the Logisim app would freeze on my system. A friend suggested a better approach of dividing it into 4 clock cycles, doing it one by one for each element.

**Improvements if given time**

After my final viva, I would like to add more opcodes and instructions, taking inspiration from the assembly language, and make this a more powerful CPU.

I would also clean up wires in my circuit, possibly reconstructing it from scratch.