CS 223 Computer Organization & Architecture

Lecture 35 [12.05.2020]

# Introduction to Tiled Chip Multicore Processors

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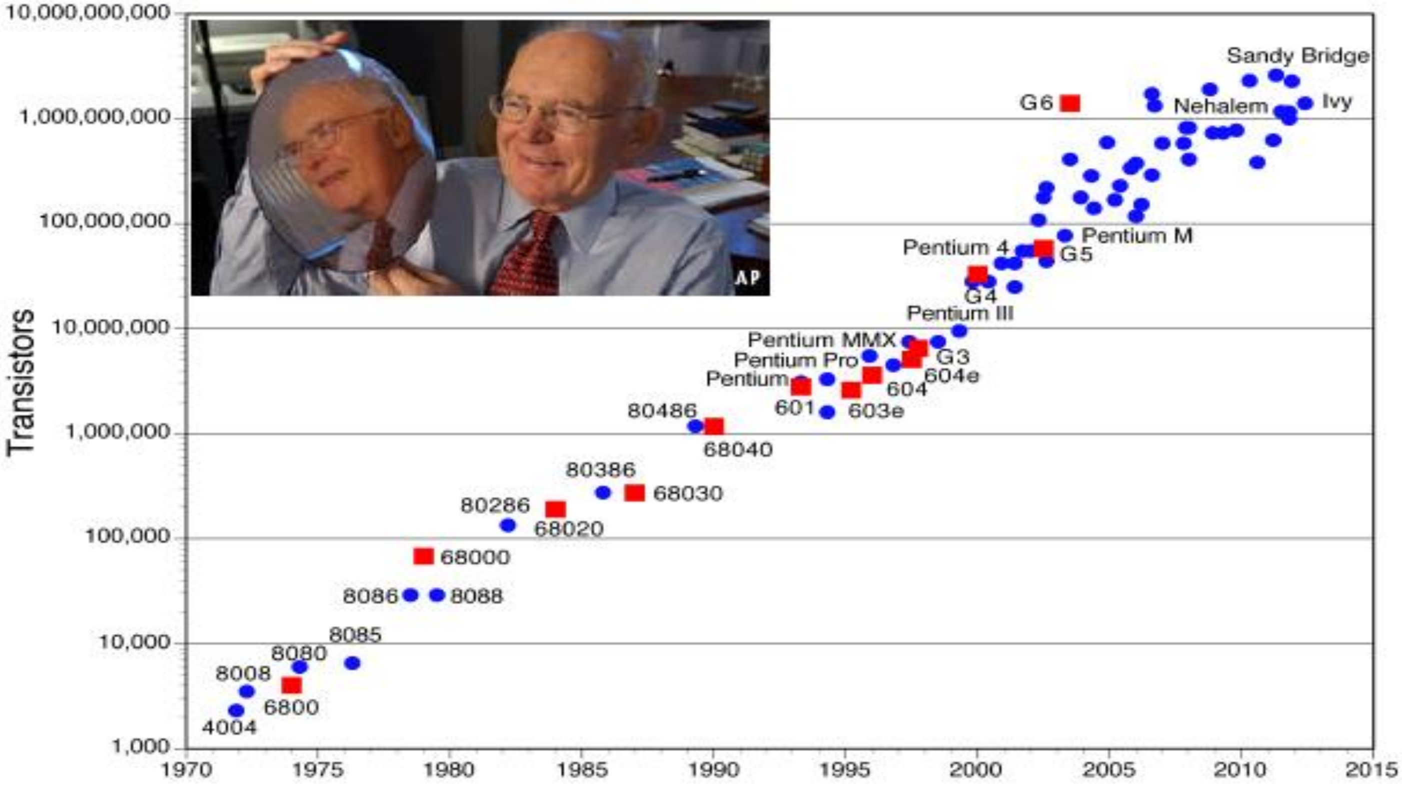
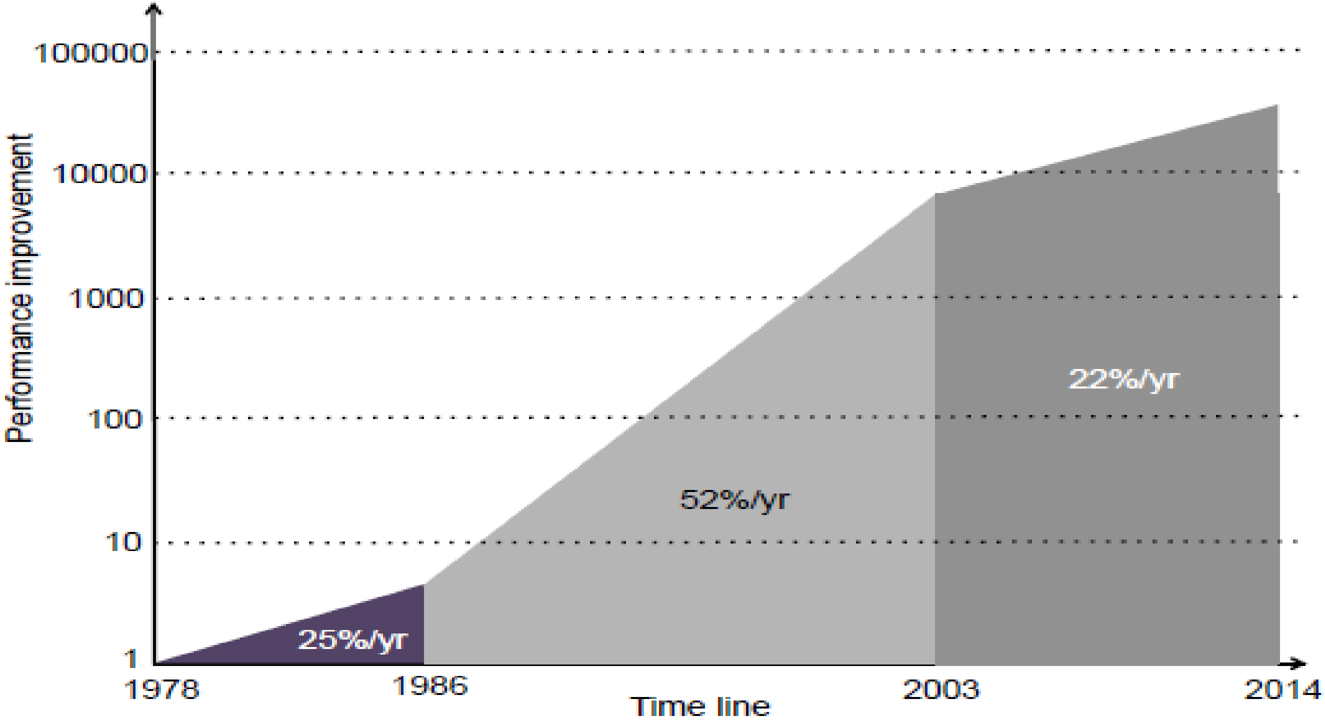
Department of Computer Science & Engineering

Indian Institute of Technology Guwahati, Assam.

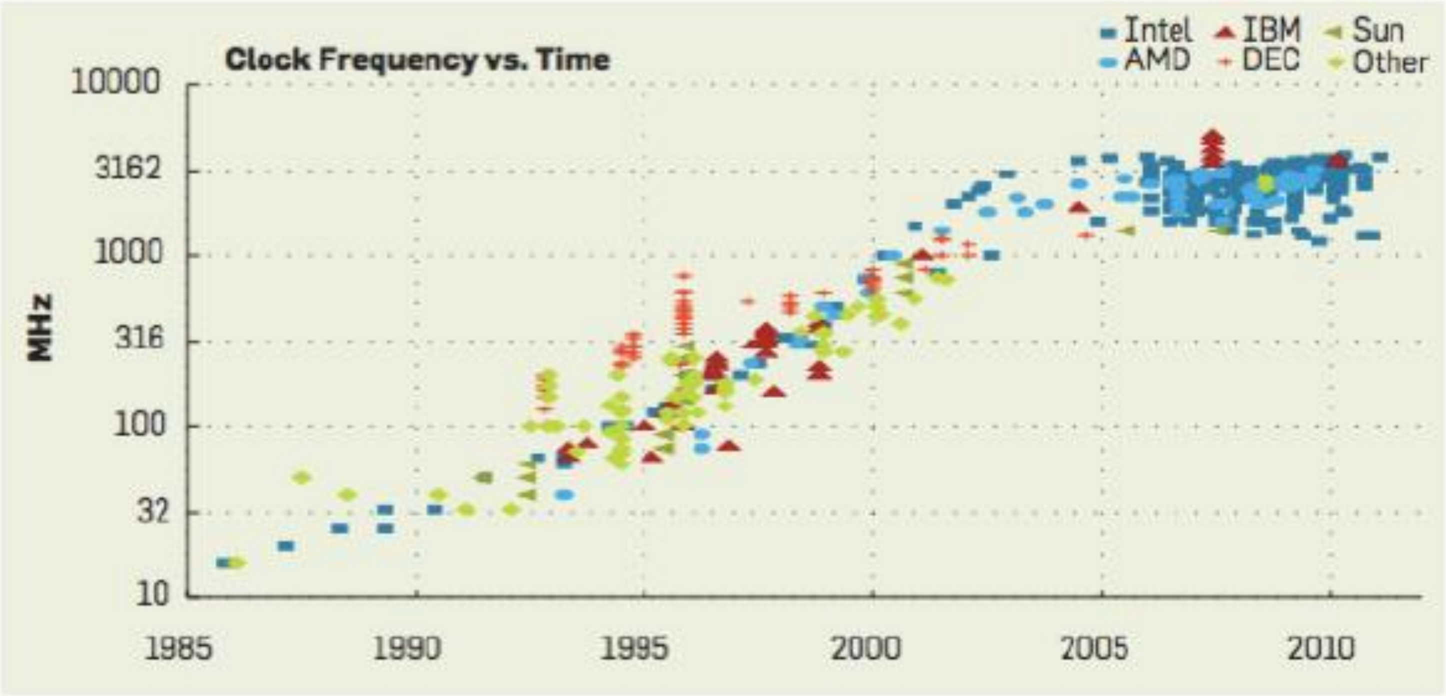
# Impact of VLSI in processor trends



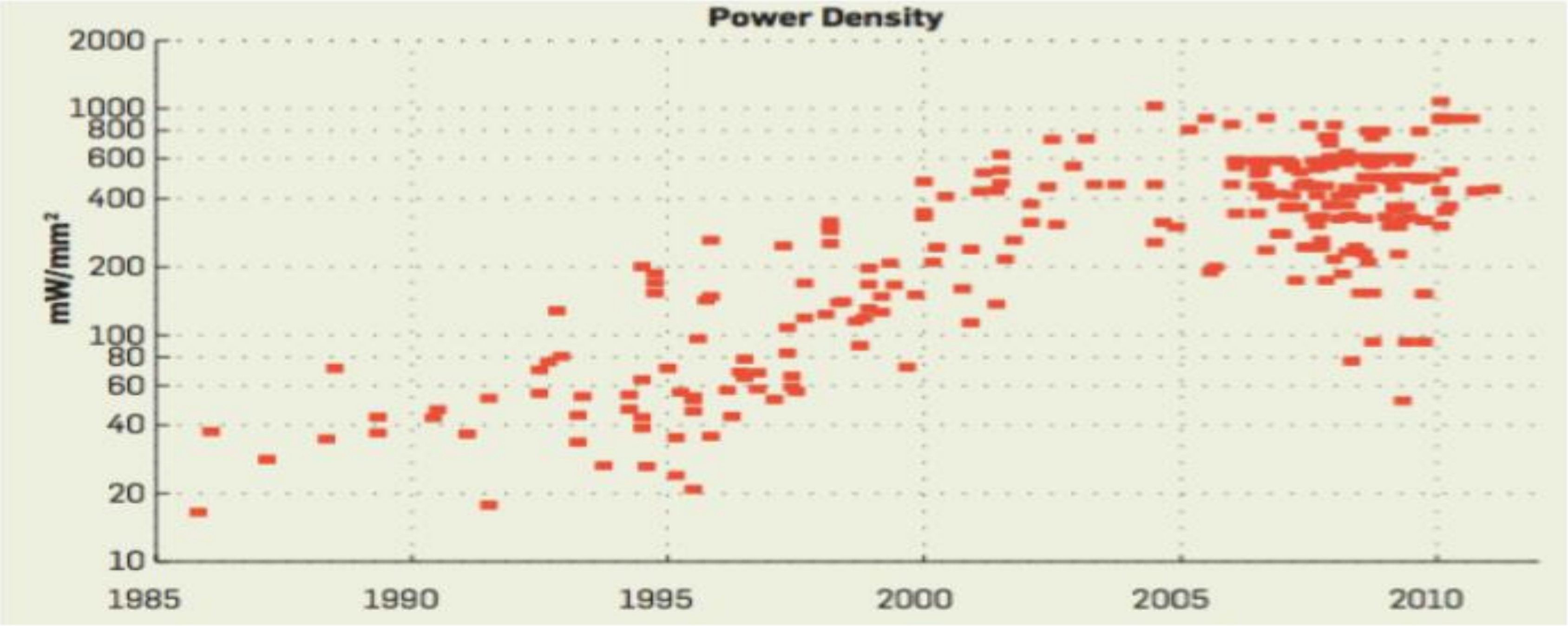
# Processors Performance



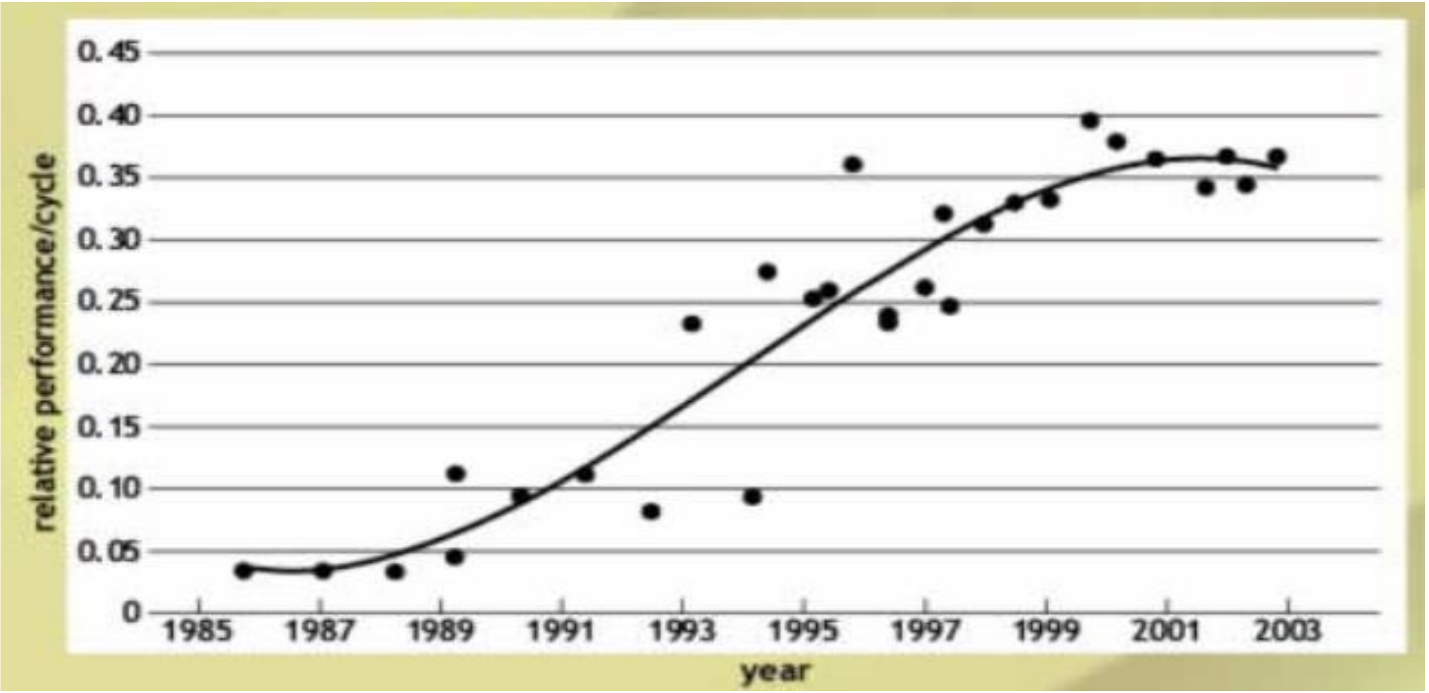
# Frequency Wall



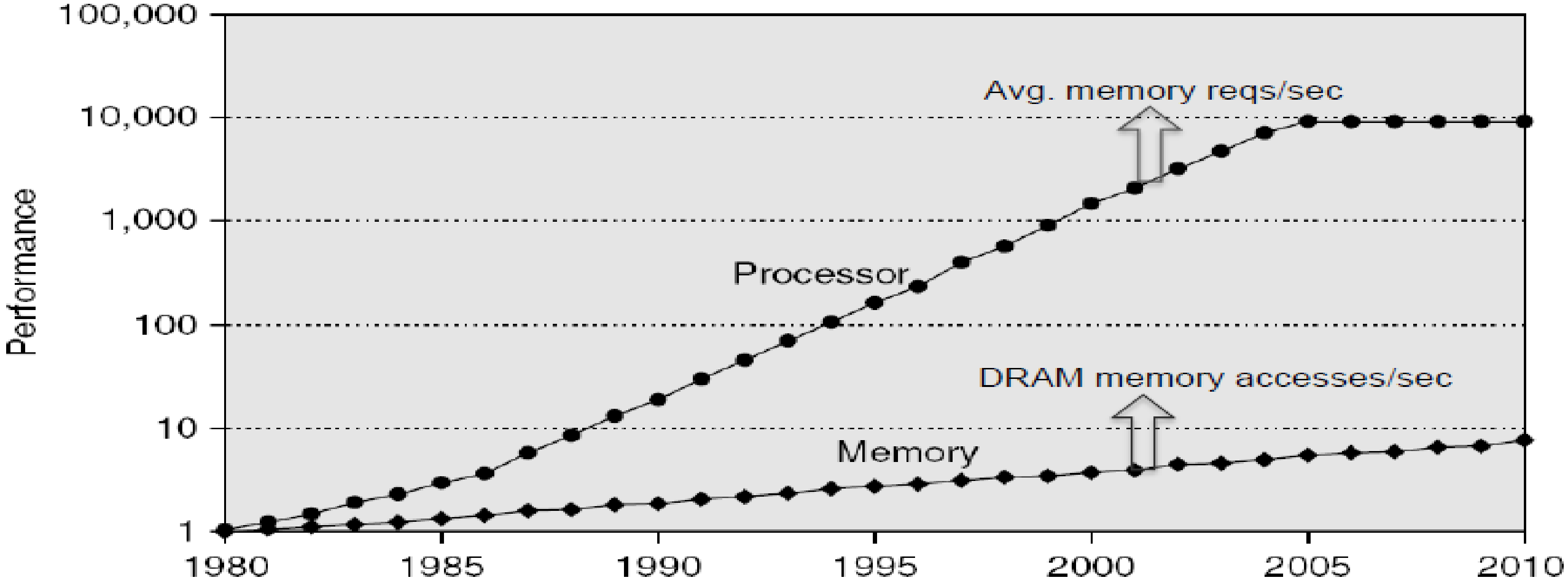
# Power Wall


Power Density
mW/mm²
2000
1000
800
600
400
200
100
80
60
40
20
10
1985
1990
1995
2000
2005
2010

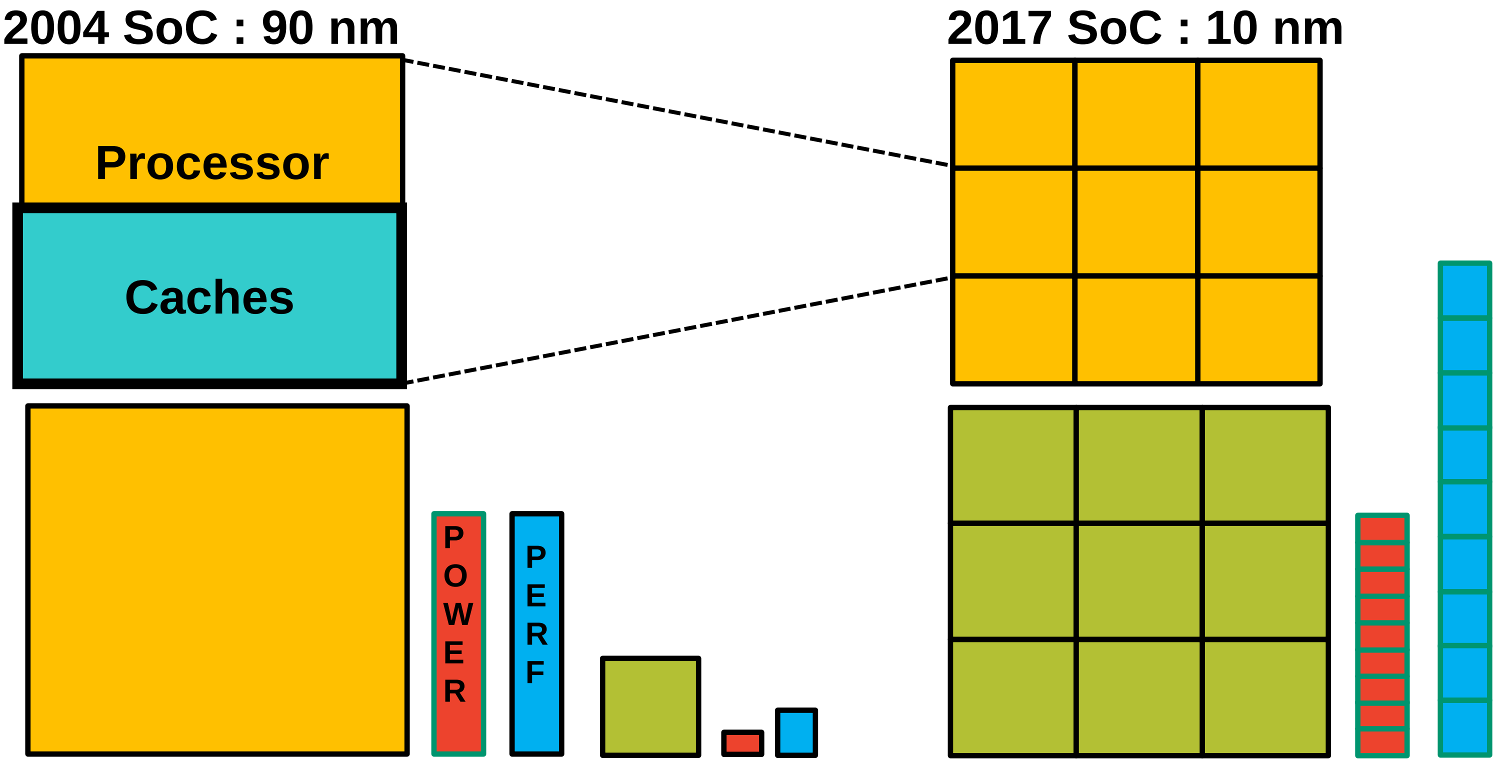
# ILP Wall


relative performance/cycle
0.45
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0
1985
1987
1989
1991
1993
1995
1997
1999
2001
2003
year

# Memory Wall


Performance
100,000
10,000
1,000
100
10
1
1980
1985
1990
1995
2000
2005
2010
Avg. memory reqs/sec
Processor
DRAM memory accesses/sec
Memory

# Paradigm Shift to Multicore

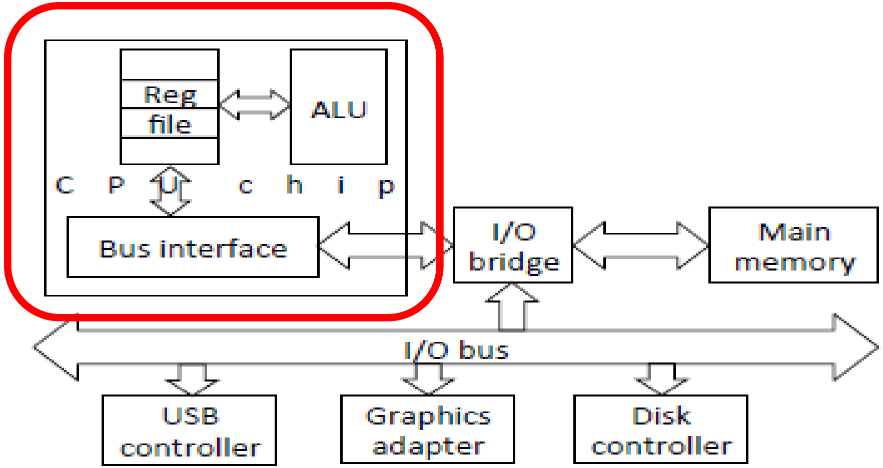


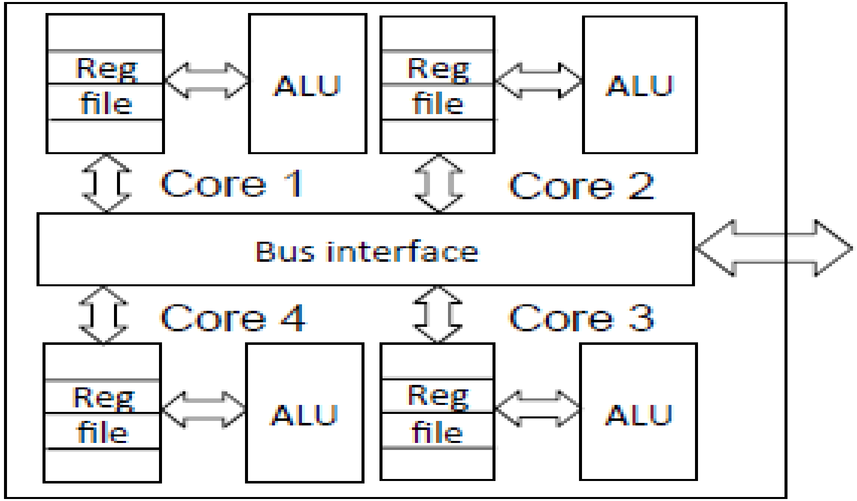
Multiple slower processors vs single fast powerful processor

# Paradigm Shift to Multicore

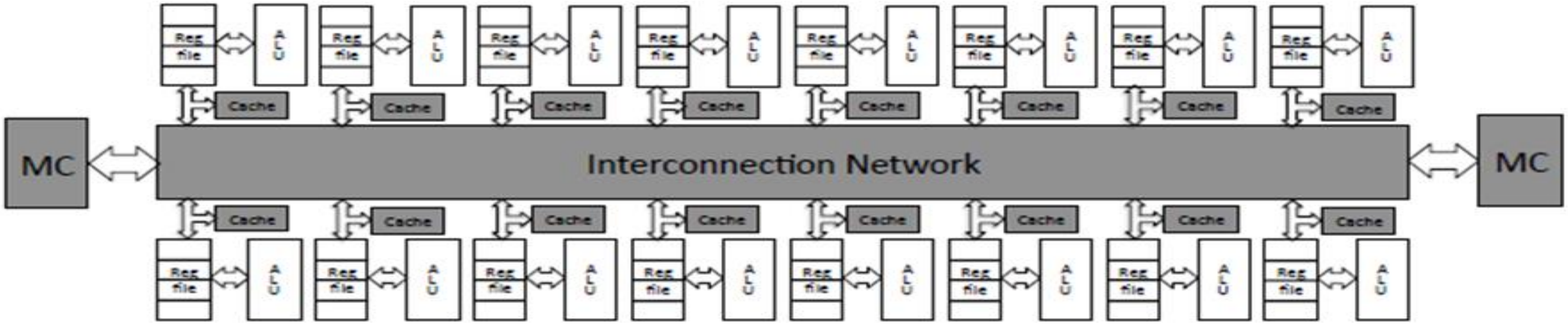
**Multiple slower processors is better that single fast powerful processor**

# What is Multicore ?



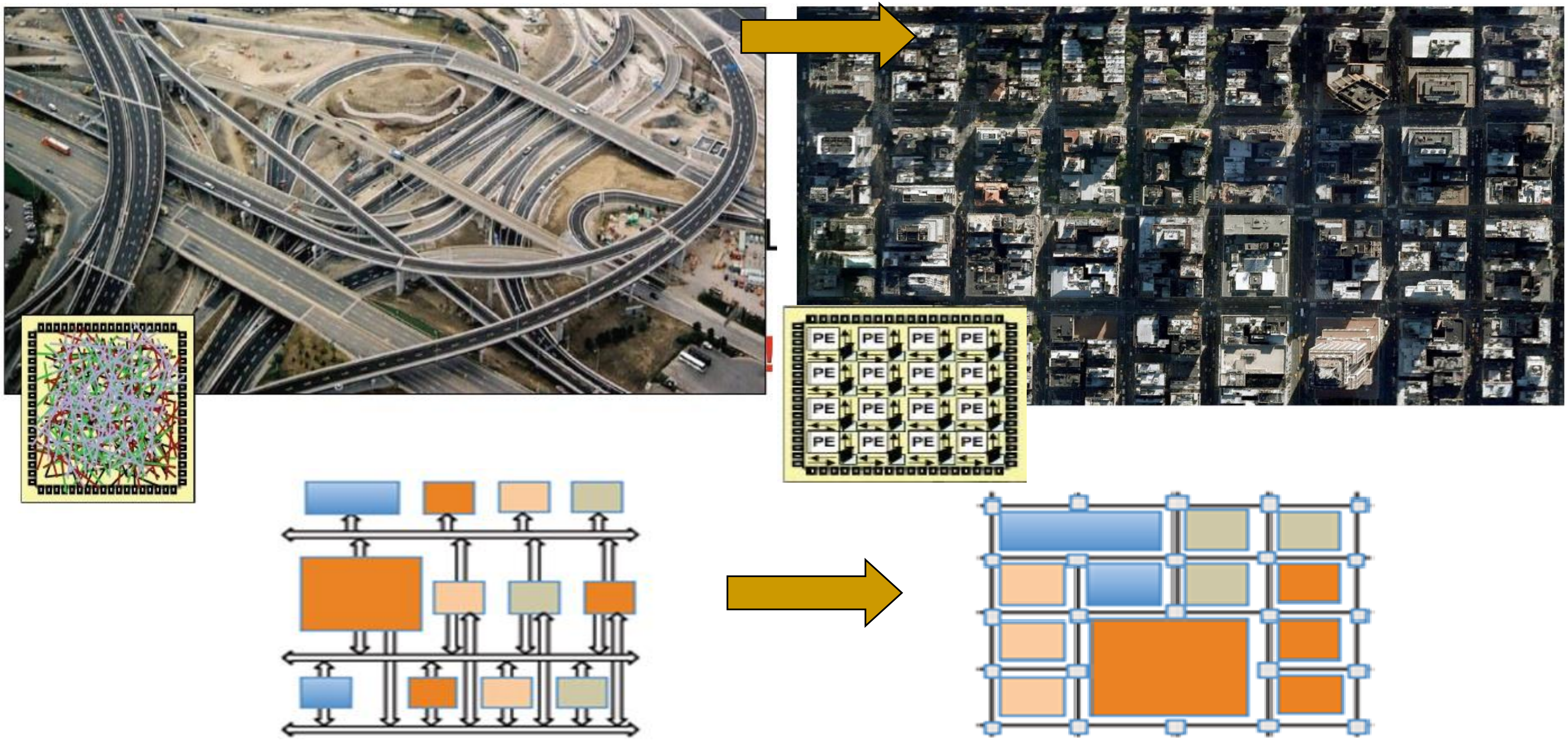


# What is Multicore ?

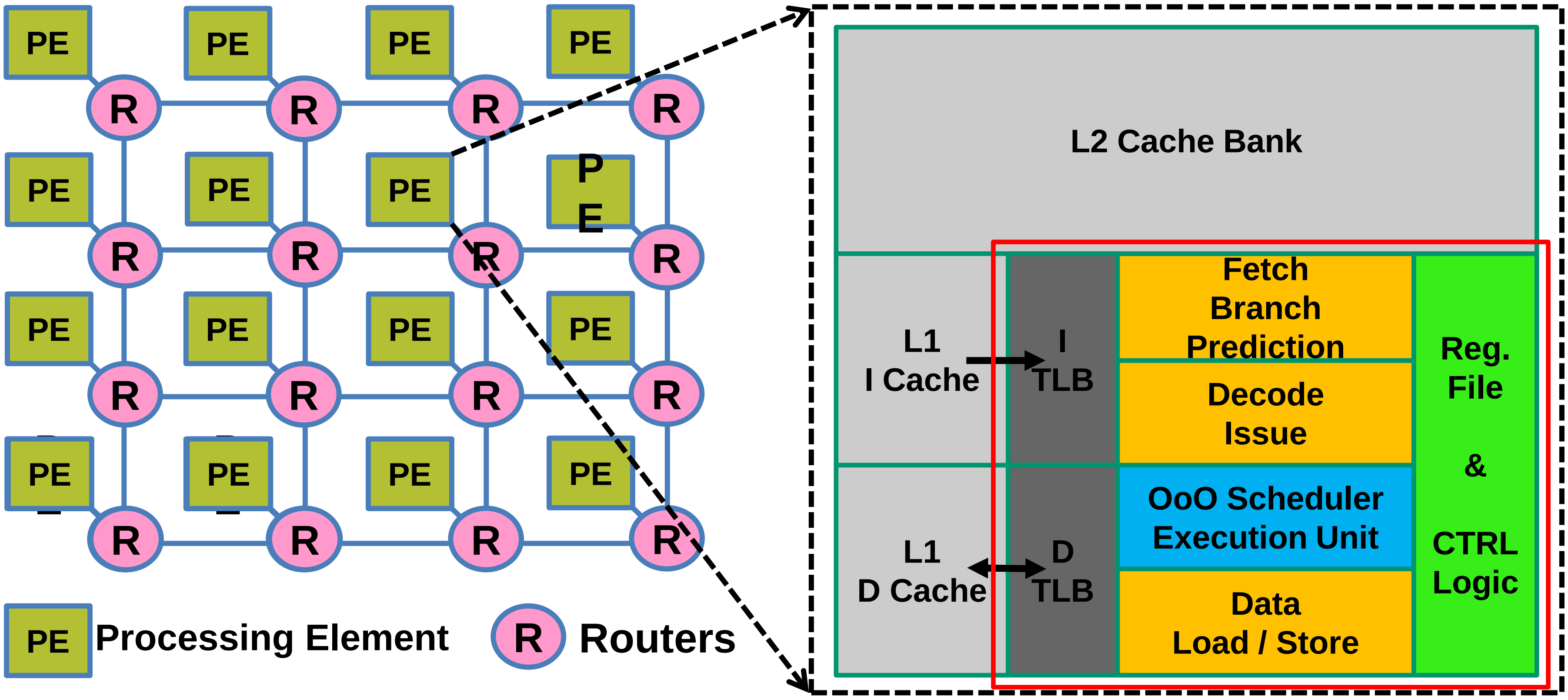


- ❖How these cores communicate ?
- ❖What is the best interconnection mechanism ?

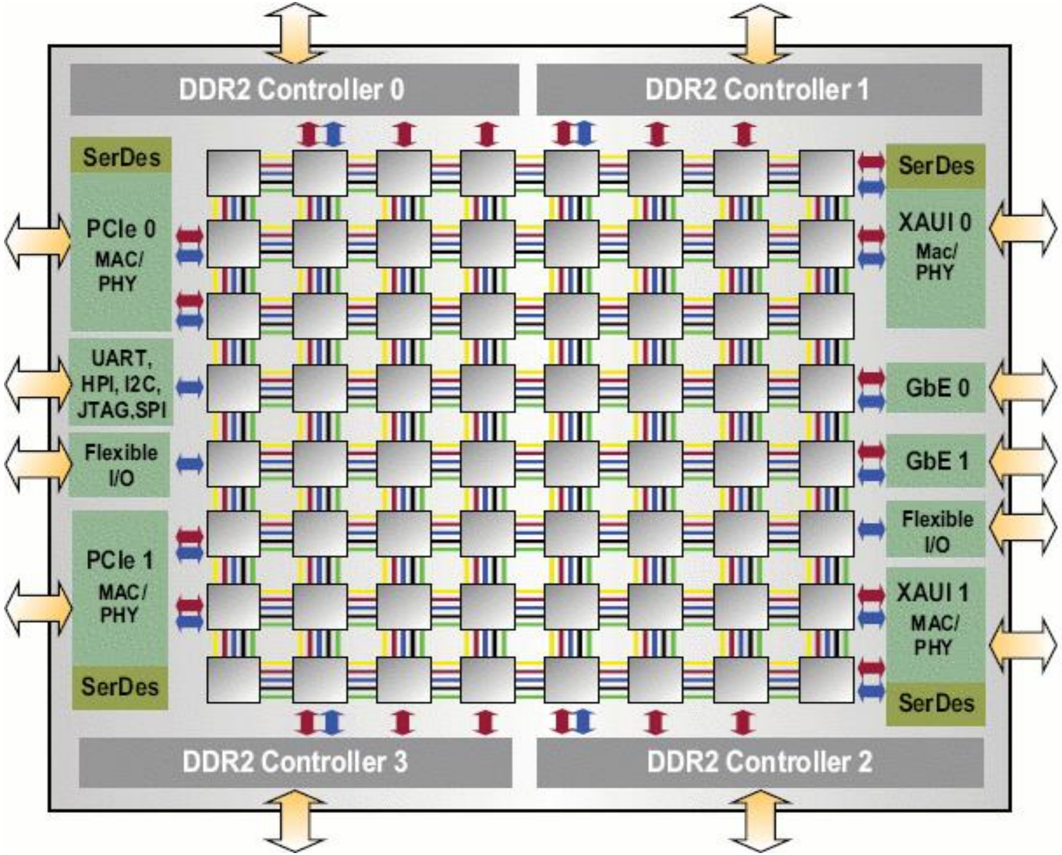
# The Paradigm Shift

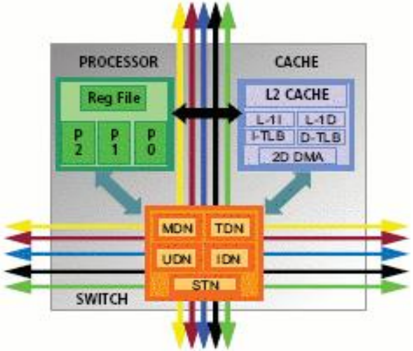


# Tiled Chip Many-Core Processor (TCMP)



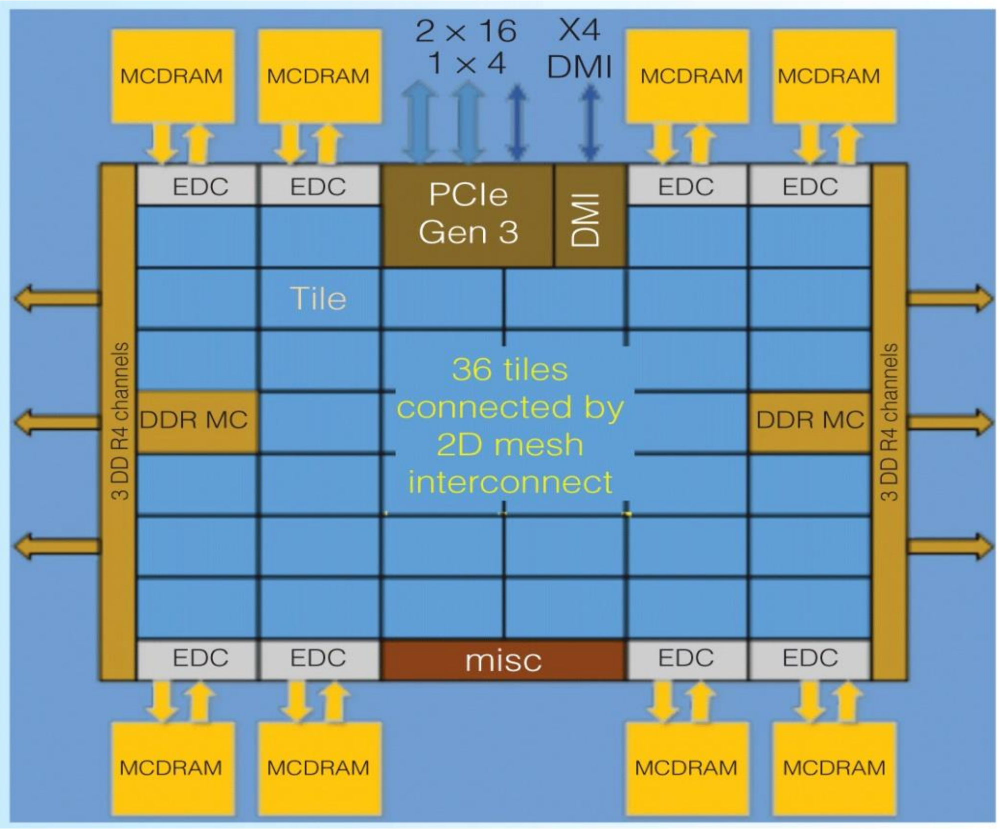
# State-of-the-Art Architectures

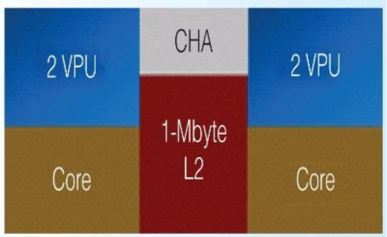




Tilera64

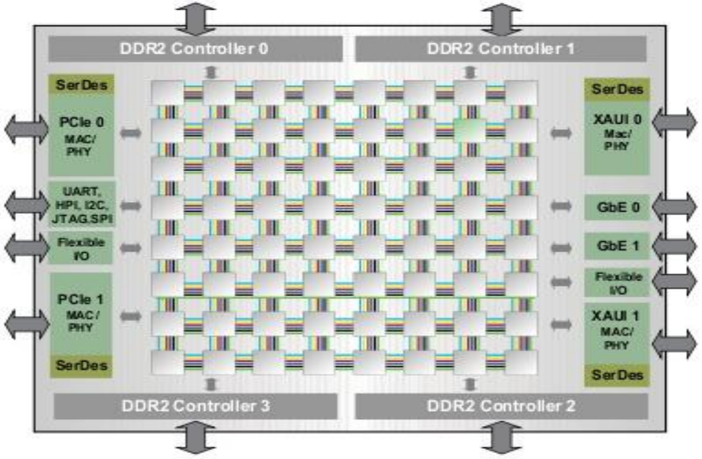
# State-of-the-Art Architectures

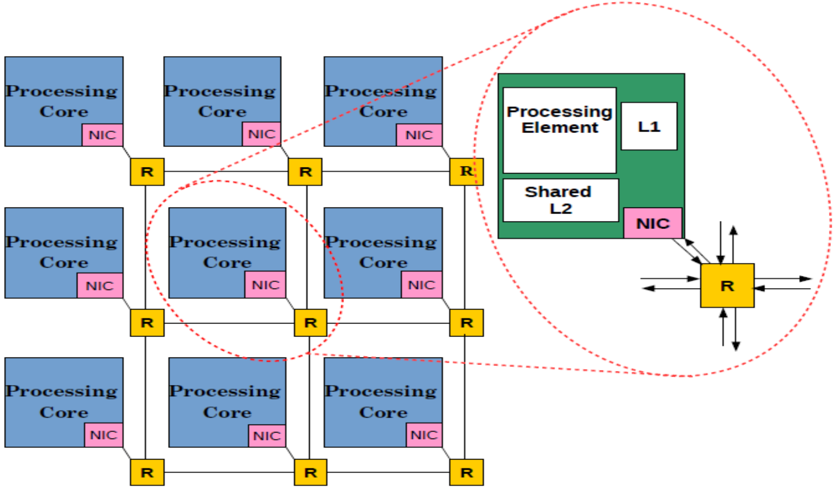




**Intel KNL**

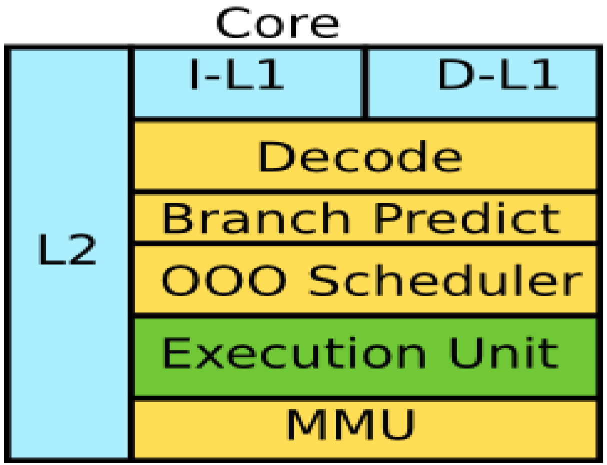
# Routers and Tiles





- ❖East, West, North and South neighbors
- ❖Packets are divided into flow control units called flits
- ❖L1 and L2 cache misses create NoC traffic packets

# What is the role of on-chip cache ?

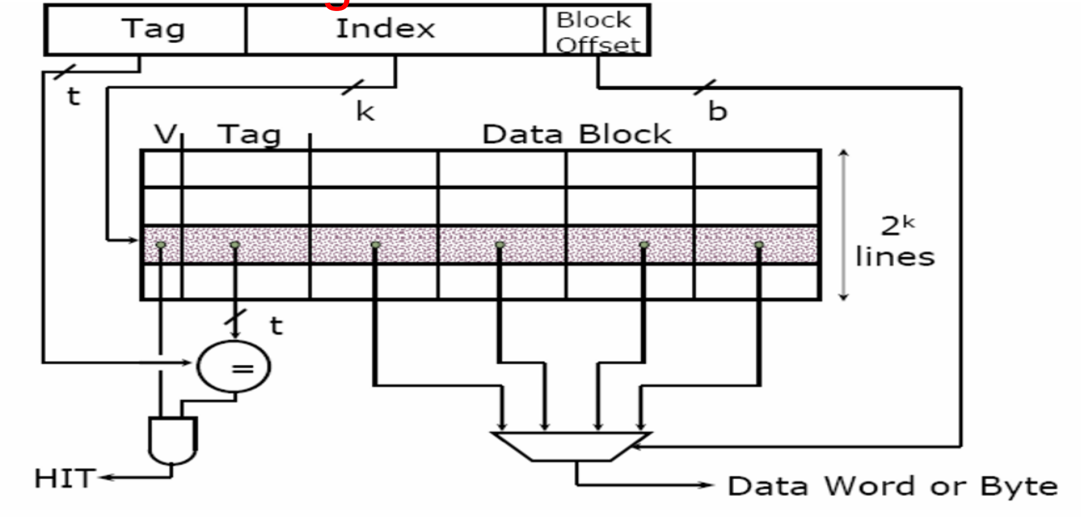


**Address A:** 1001 0011 0101 1010

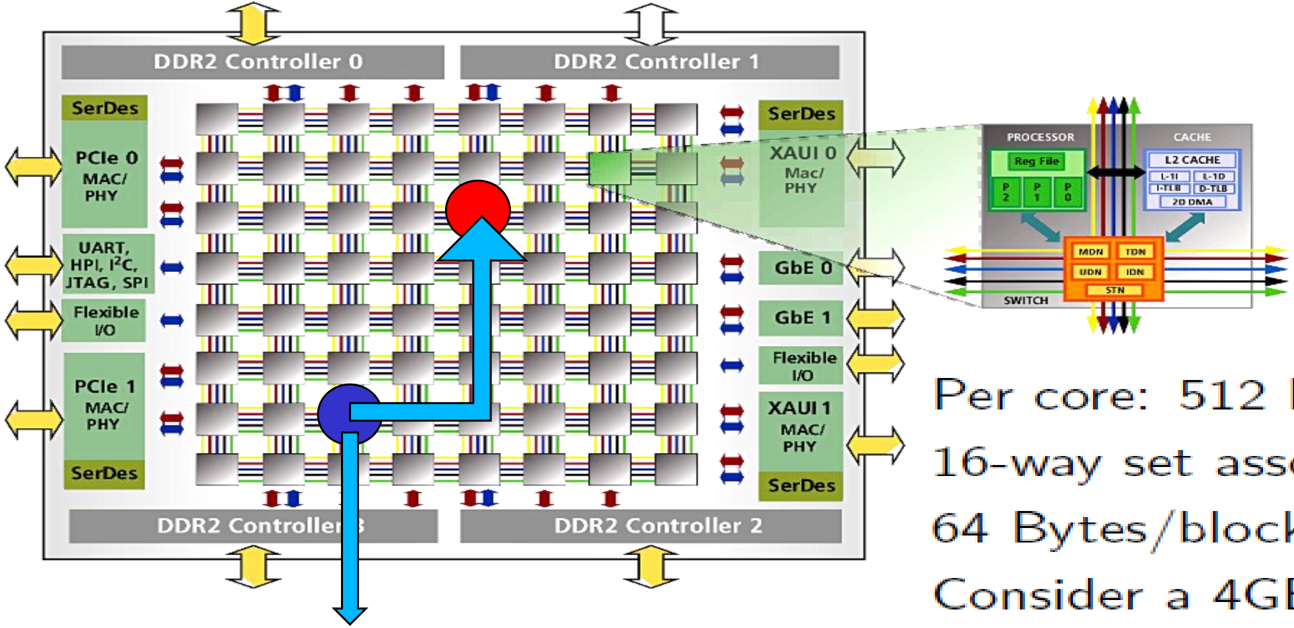
t bits s bits b bits

m-1 0

<tag> <set index> <block offset>



# On-Chip Cache Address Mapping



Per core: 512 KB

16-way set associative mapping

64 Bytes/block

Consider a 4GB RAM ( $2^{32}$bits)

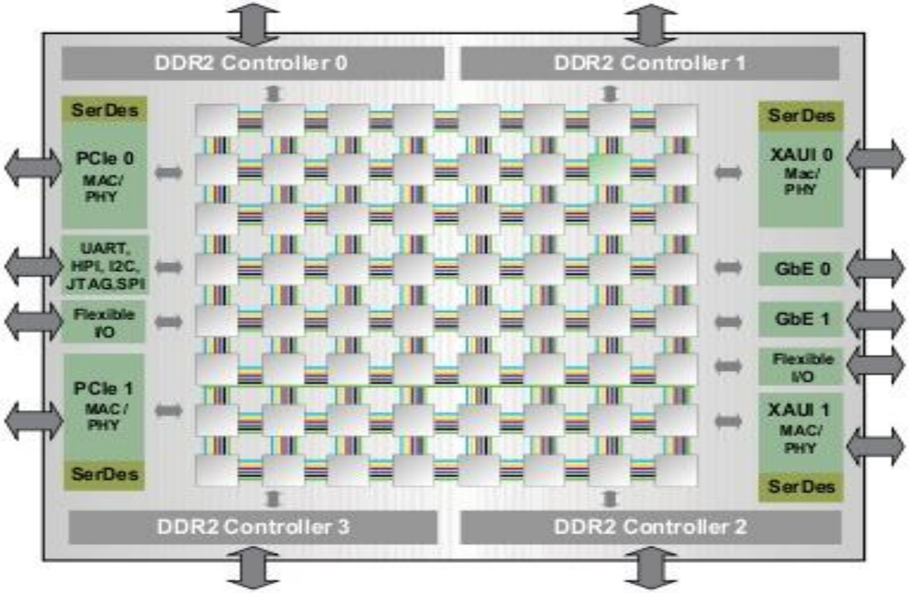
Hex Address : 0x764254

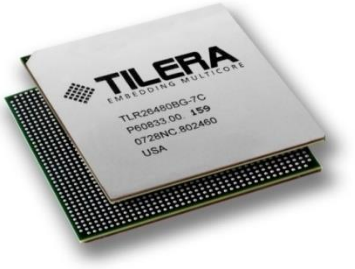
| 11 bits | 15 bits | 6 bits |
|---|---|---|
| Tag | Index | Block offset |

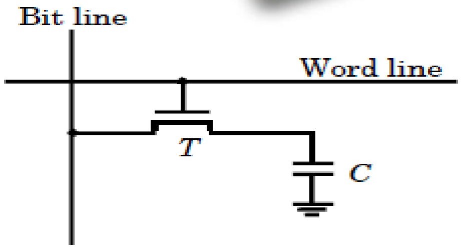
| 00000000011 | 101100 100001001 | 010100 |
|---|---|---|
| Tag | Index | Block offset |

Core No. 44

# What is the role of memory controllers?

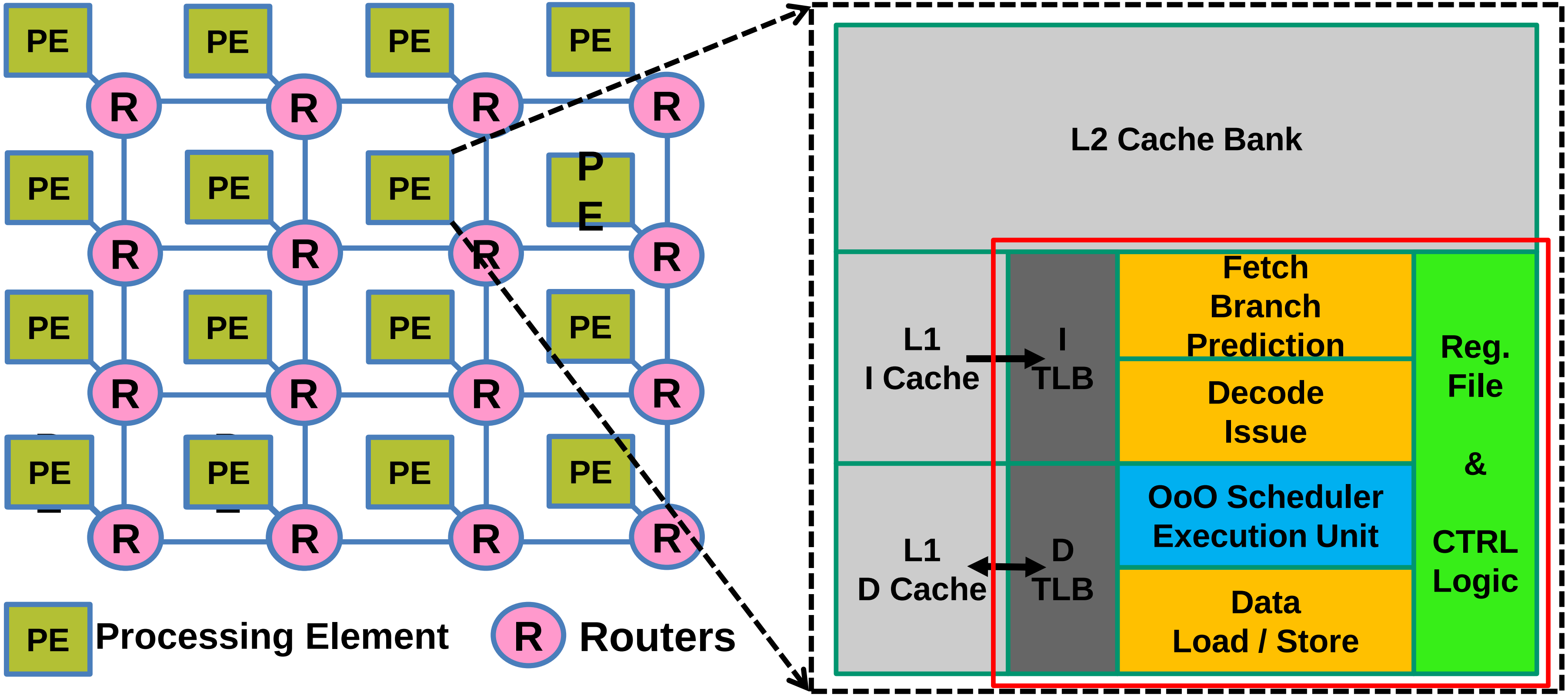






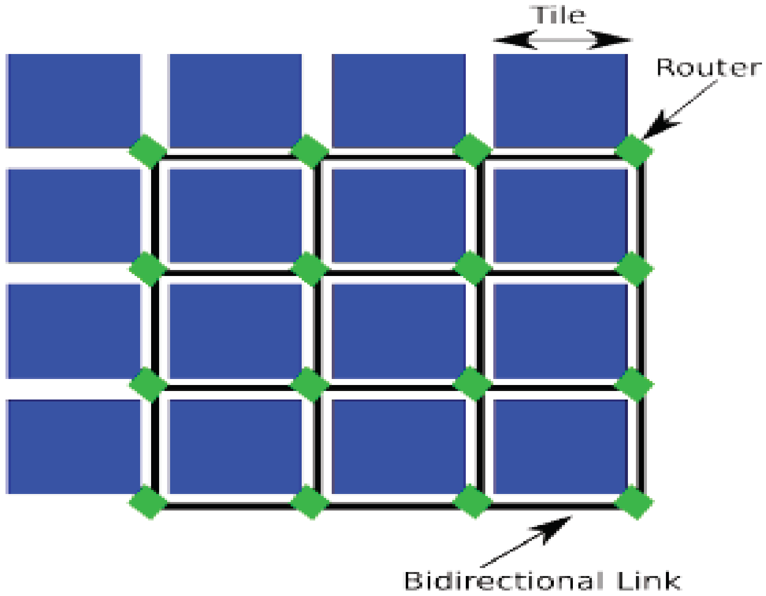
A single-transistor dynamic memory cell

# Tiled Chip Many-Core Processor (TCMP)



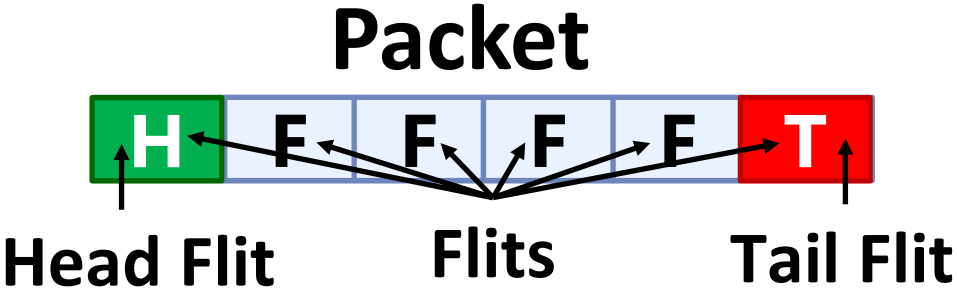
# What is NoC ?

- Processing units  interconnected via packet based  network
- Each resource is called as a ***‘tile’***
- All resources organized as rectangular tiles on the chip.
- Each tile have an address - ***(X,Y)***
- Tiles interconnected by network of routers
- Communication by packet transmission

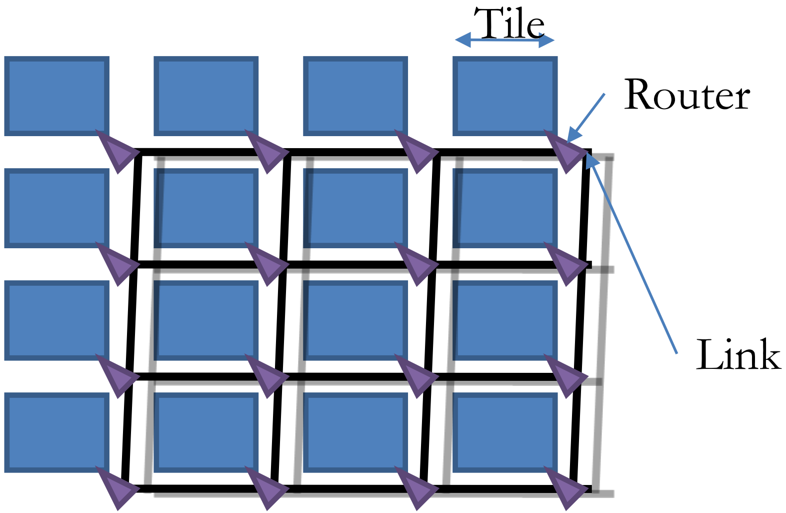


# Packets & Flits

- **Packet**
  - Unit of transfer for network
- **Flit**
  - Basic unit of transfer between a pair of routers
  - Unit of flow control within network



# Building Blocks of NoC



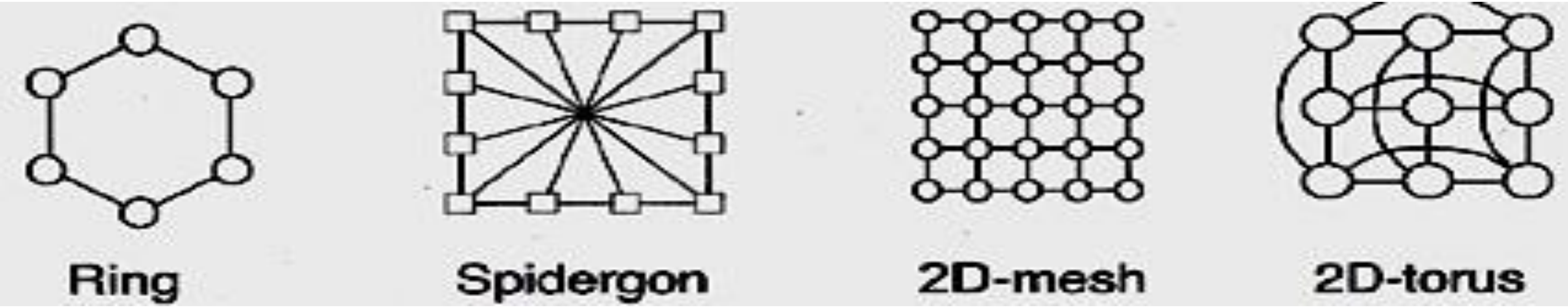
- Topology
- Routing
- Flow control
- Router micro-architecture

# Building Blocks of NoC

- Topology
  - Specifies the way switches are wired
- Routing (algorithm)
  - How does a message move from source to destination
- Buffering and Flow Control
  - What do we store within the network?
    - Entire packets, parts of packets, etc?
    - What is basic unit of transfer

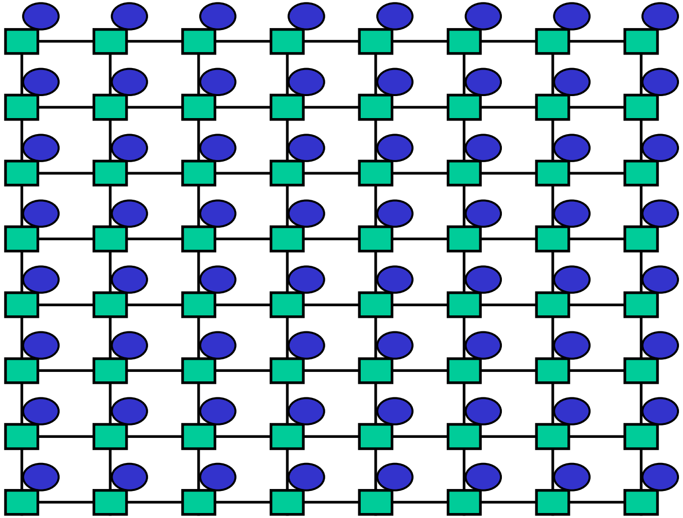
# Topology

- Determines the physical layout and connection pattern between nodes and channels in the network.



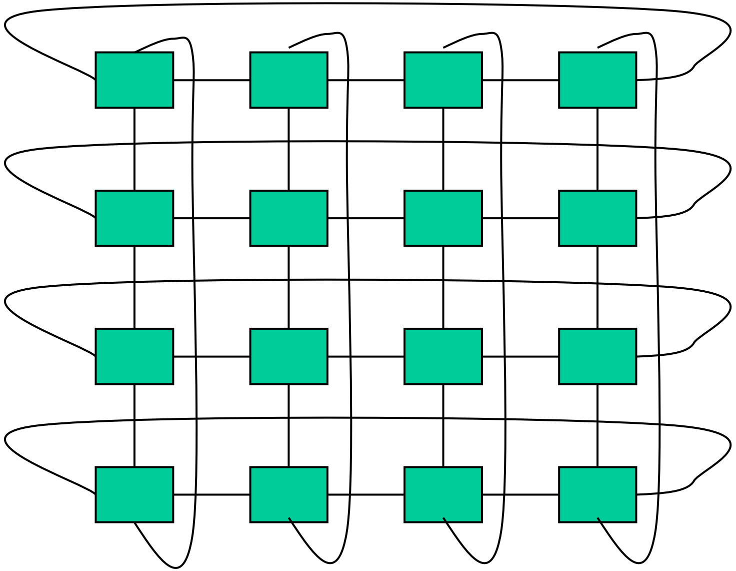
# Mesh

- Each node connected to 4 neighbors (N, E, S, W)
- Easy to layout on-chip: regular and equal-length links
- Path diversity: many ways to get from one node to another

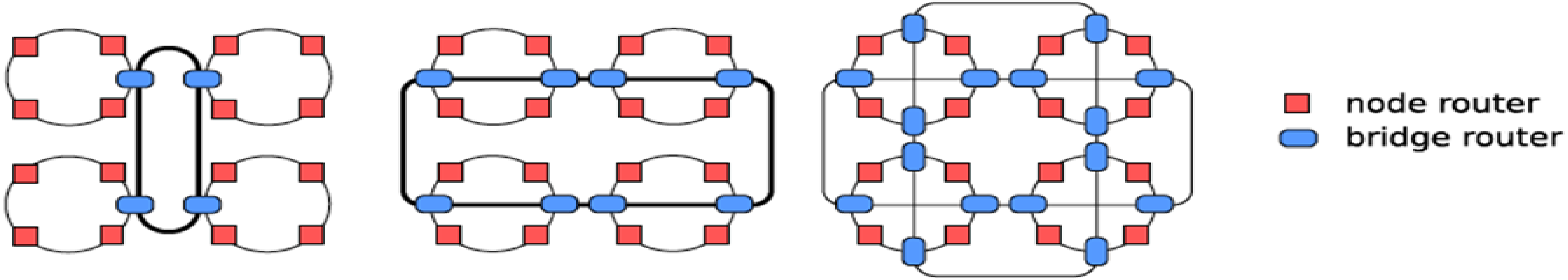


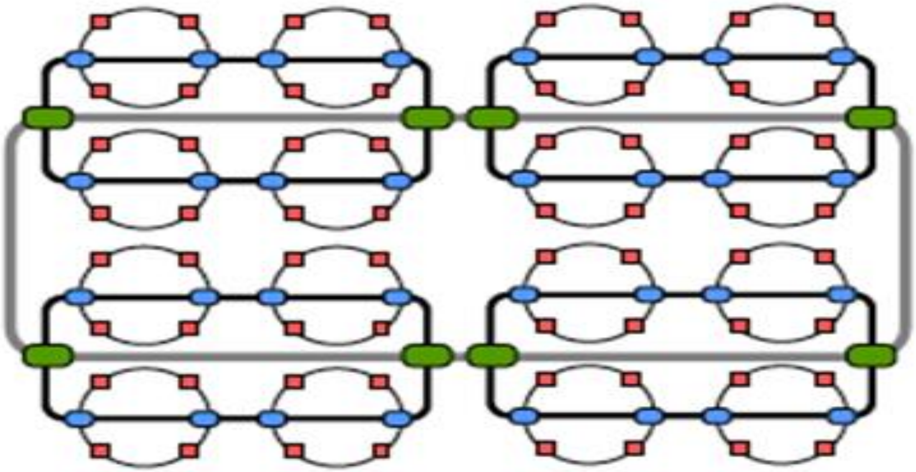
# Torus

- Mesh is not symmetric on edges: performance very sensitive to placement of task on edge vs. middle
- Torus avoids this problem
- Harder to lay out on-chip
- Unequal link lengths



# Hierarchical Rings

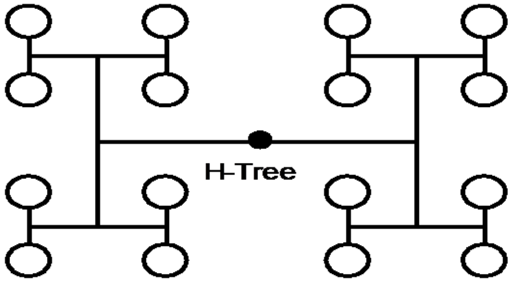


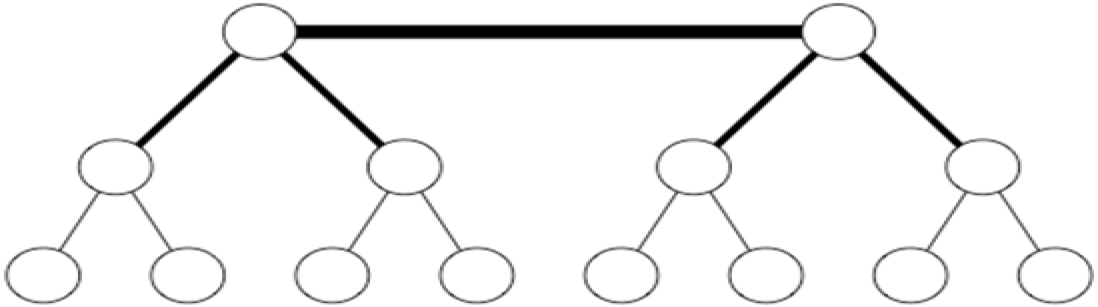


- ❖More scalable
- ❖Lower latency
- ❖More complex

# Trees

- Planar, hierarchical topology
- Good for local traffic
- Easy to Layout
- Root can become a bottleneck
- Fat trees avoid this problem (CM-5)





Fat Tree

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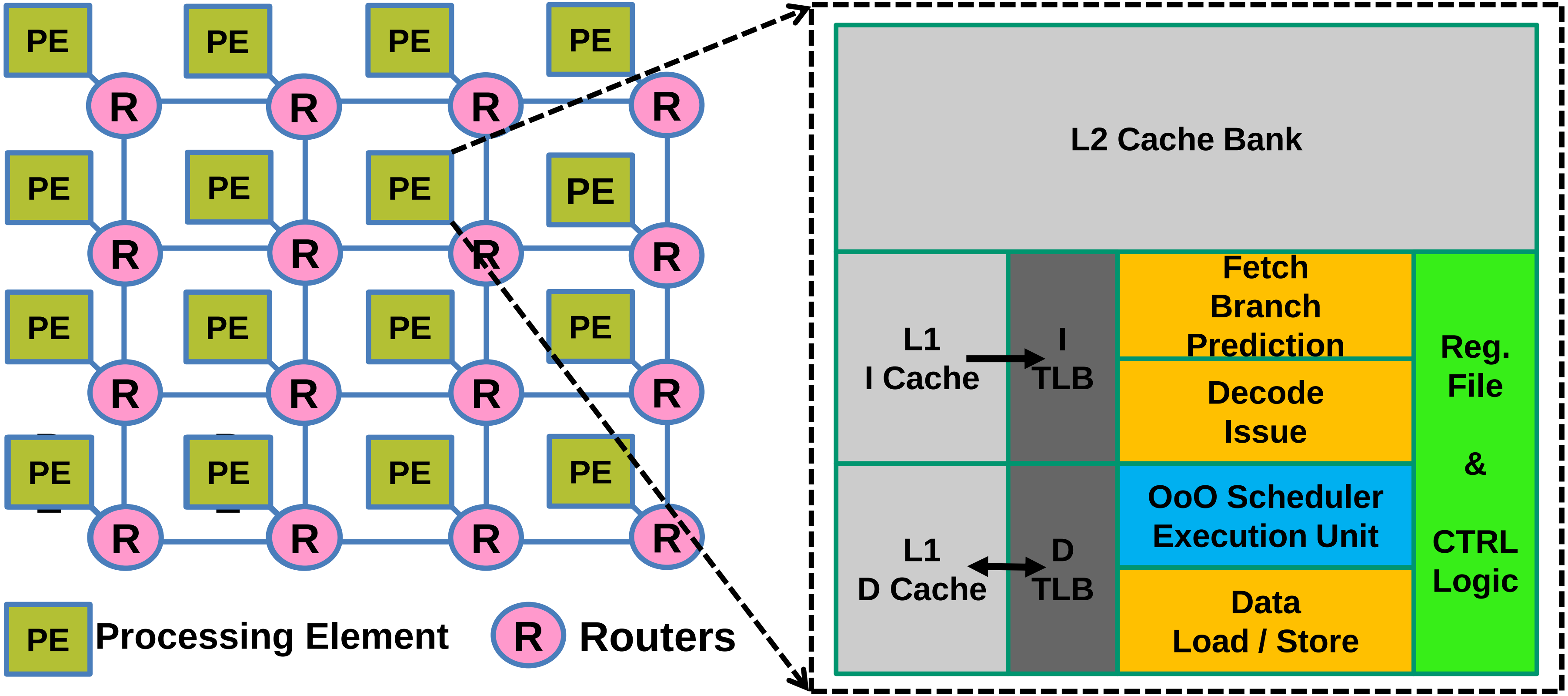

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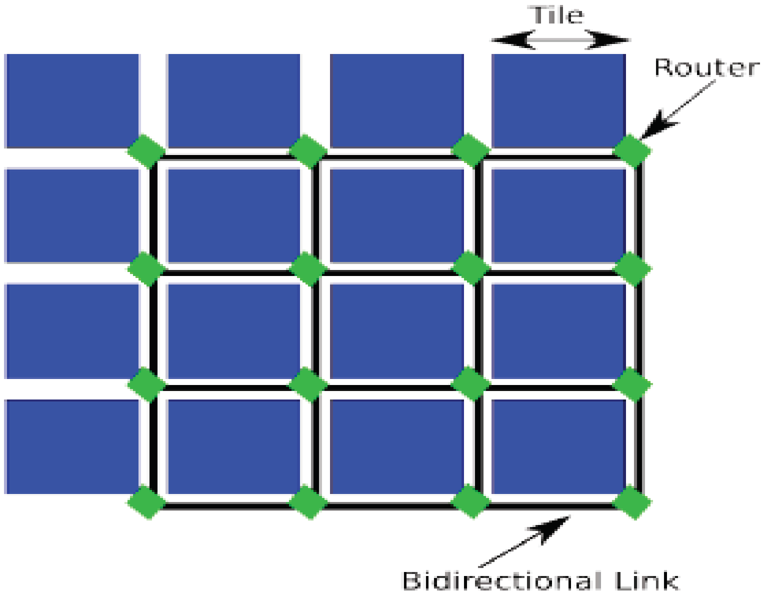
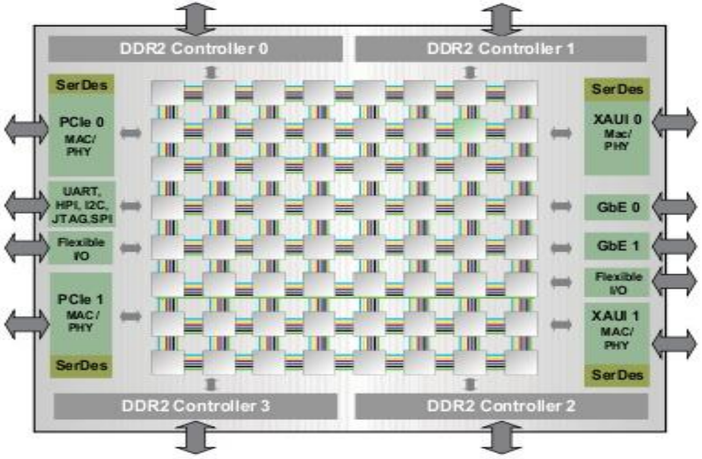
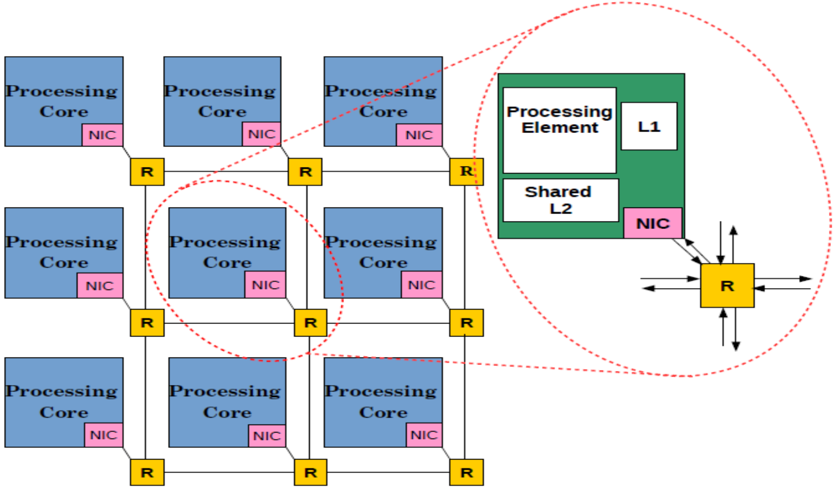


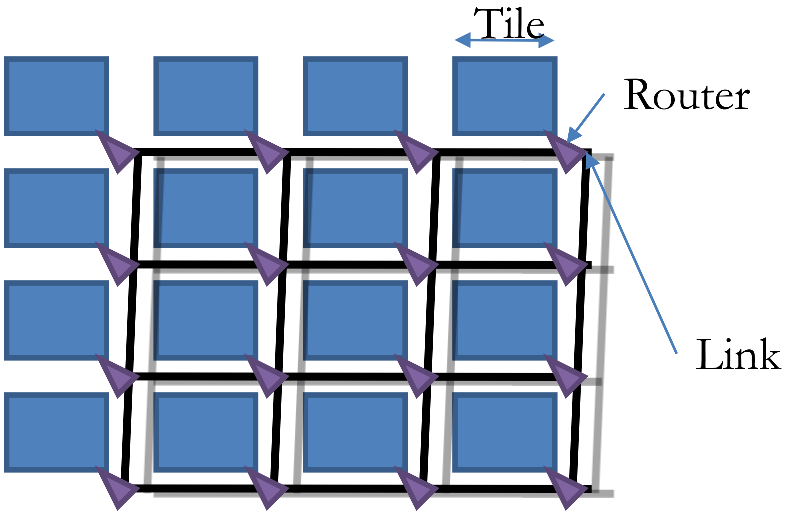
# Routers and Tiles





- ❖East, West, North and South neighbors
- ❖Packets are divided into flow control units called flits
- ❖L1 and L2 cache misses create NoC traffic packets

# Building Blocks of NoC



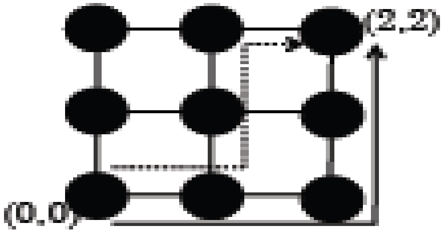
- ❖Topology
- ❖Routing
- ❖Flow control
- ❖Router micro-architecture

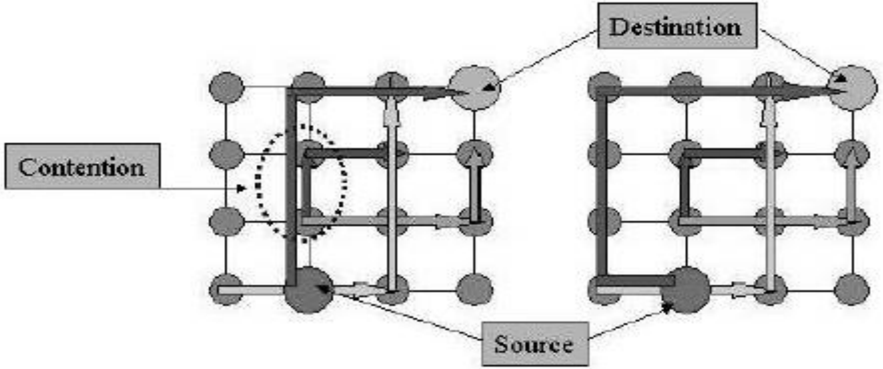
# Routing Algorithm

- Compute the path route for packets to reach destination.
  - **Deterministic:** always chooses the same path for a communicating source-destination pair
  - **Oblivious:** chooses different paths, without considering network state
  - **Adaptive:** can choose different paths, adapting to the state of the network
- Minimal Routing vs Non-Minimal Routing
- Source Routing vs Node Routing
- Deterministic Routing vs Adaptive Routing

# Minimal & Non-Minimal Routing

- **Profitable route:** The route that always leads the packet closer to the destination.
- **Misroute:** A route that leads the packet away from the destination.



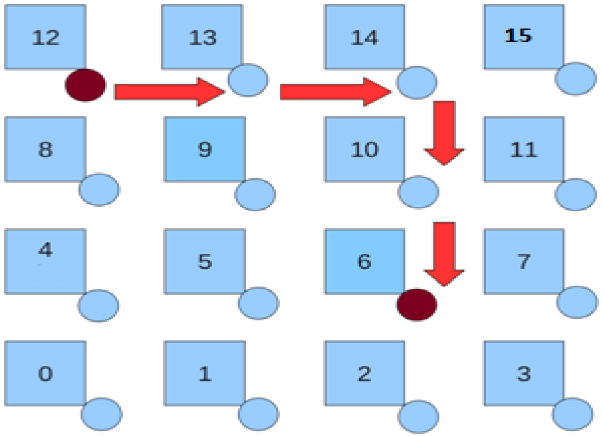


**Minimal routing**

**Non-Minimal routing**

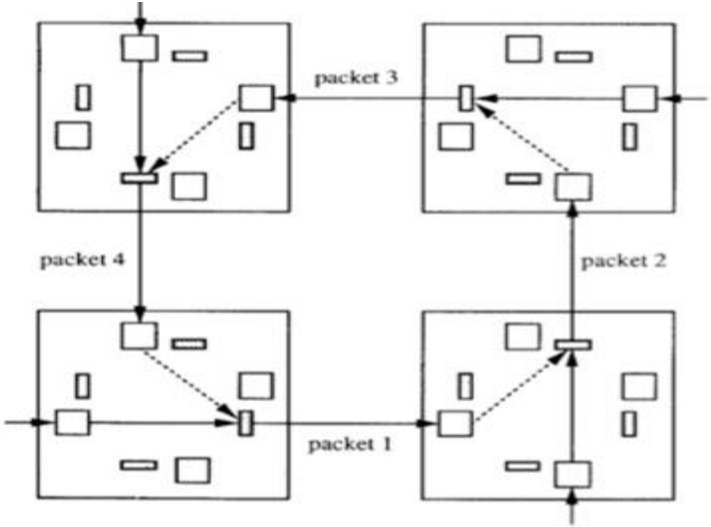
# Deterministic Routing

- All packets between the same (source, dest) pair take the same path
- Dimension-order routing – Eg.  XY routing
  - First traverse dimension X, then traverse dimension Y
  - Simple
  - Deadlock freedom
  - Could lead to high contention
  - Does not exploit path diversity



# Deadlock

- No forward progress
- Caused by circular dependencies on resources
- Each packet waits for a buffer occupied by another packet downstream

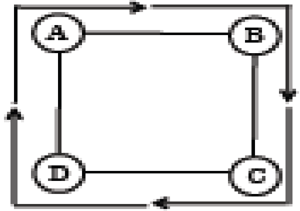


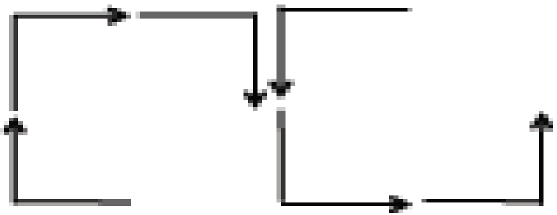
# Handling Deadlock

- Avoid cycles in routing - Dimension order routing cannot build a circular dependency
- Restrict the turns each packet can take
- Avoid deadlock by adding more buffering (escape paths)
- Detect and break deadlock by preemption of buffers

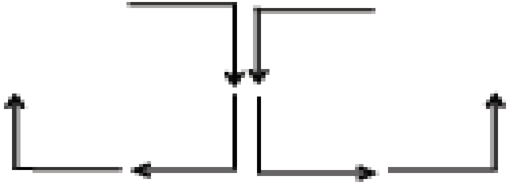
# Turn Model to Avoid Deadlock

- Analyze directions in which packets can turn in the network
- Determine turns the can form cycles
- Prohibit just enough turns to break possible cycles

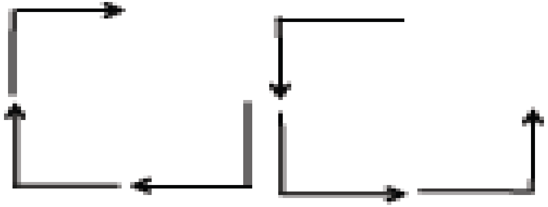




West First Turns

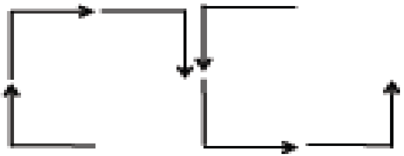


North Last Turns

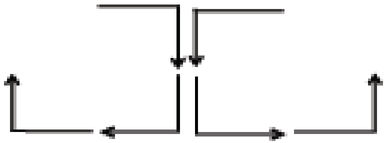


Negative First Turns

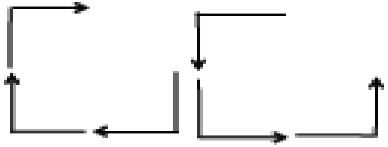
# Turn Model to Avoid Deadlock



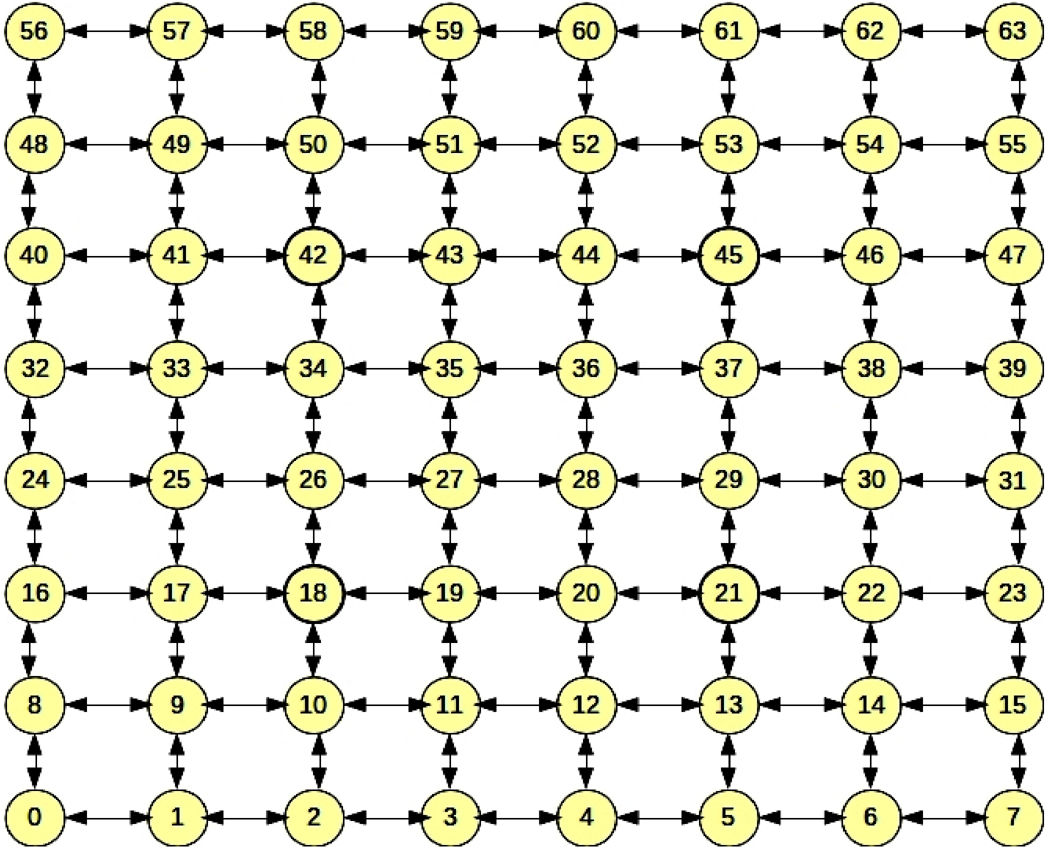
West First Turns



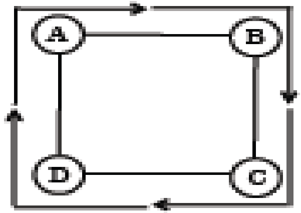
North Last Turns



Negative First Turns

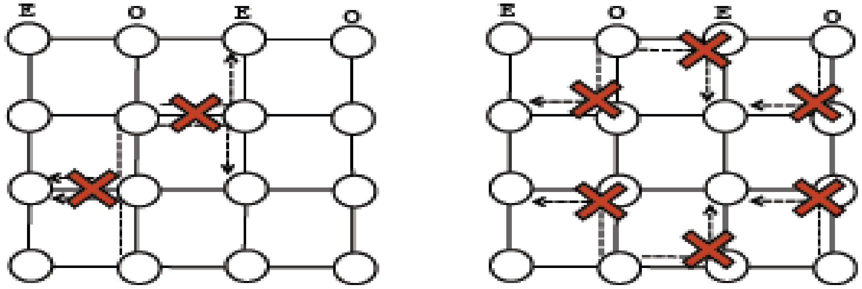


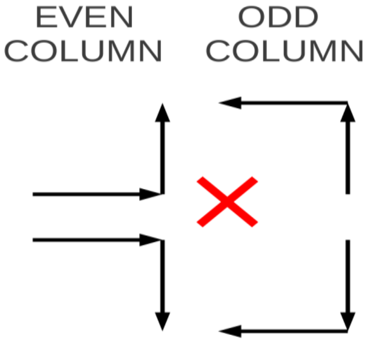
# Adaptive Odd-Even Turn Routing



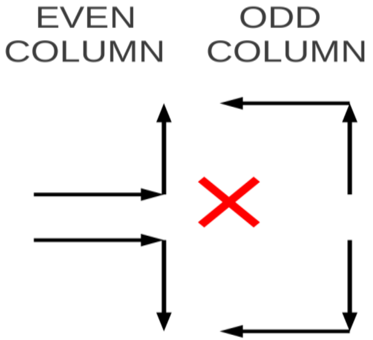
**Non restrictive turns leads to deadlocks**

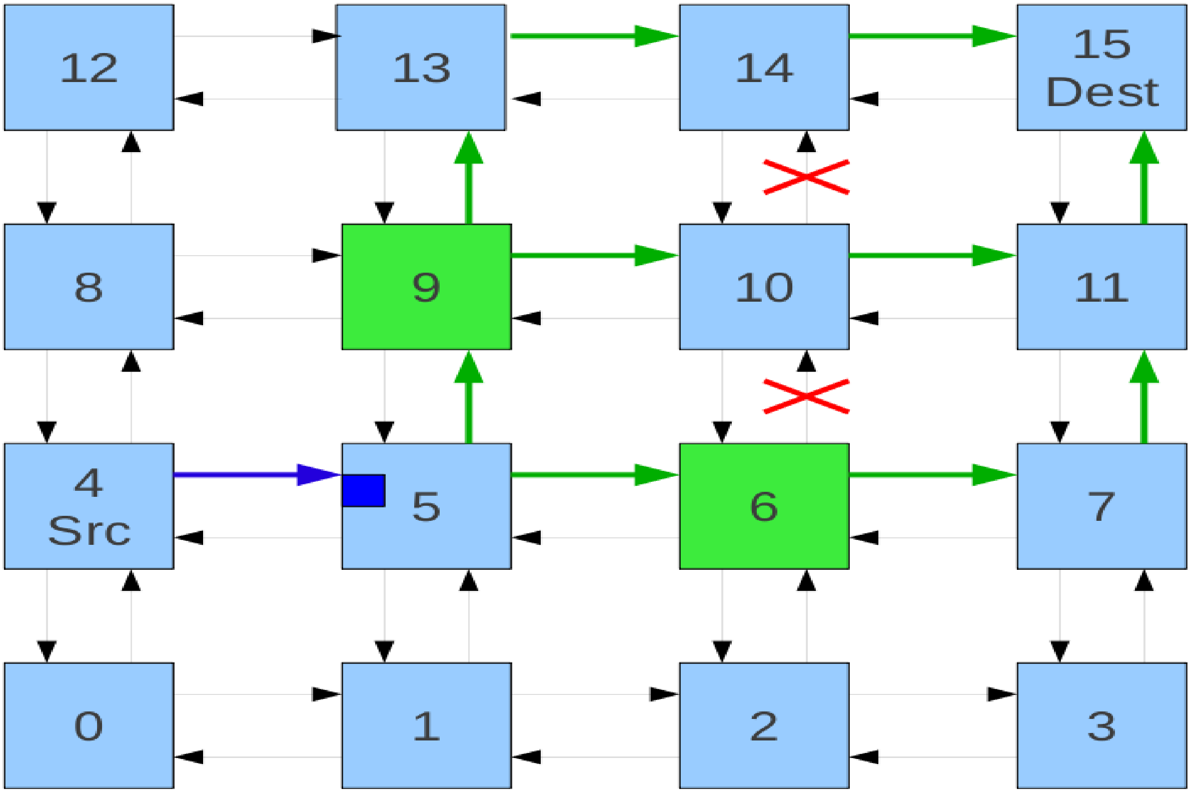
- ❖ Prohibited Turns at certain junctions
- ❖ For nodes in even column EN and ES.
- ❖ For nodes in odd column NW and SW.



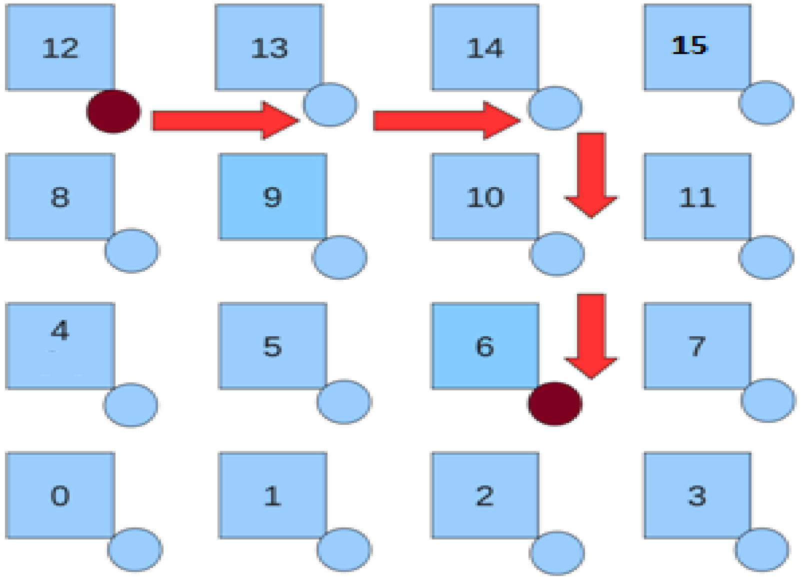


# The Minimal Odd-Even Routing

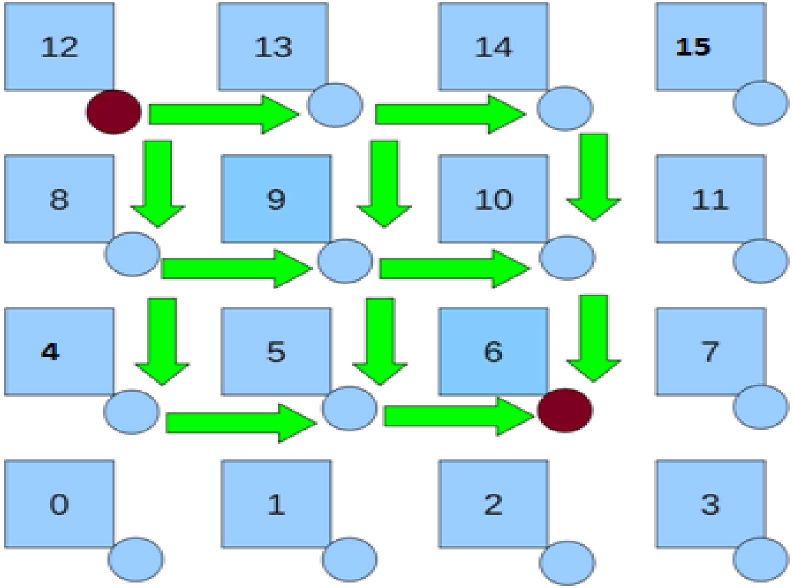




# Static vs Adaptive Routing



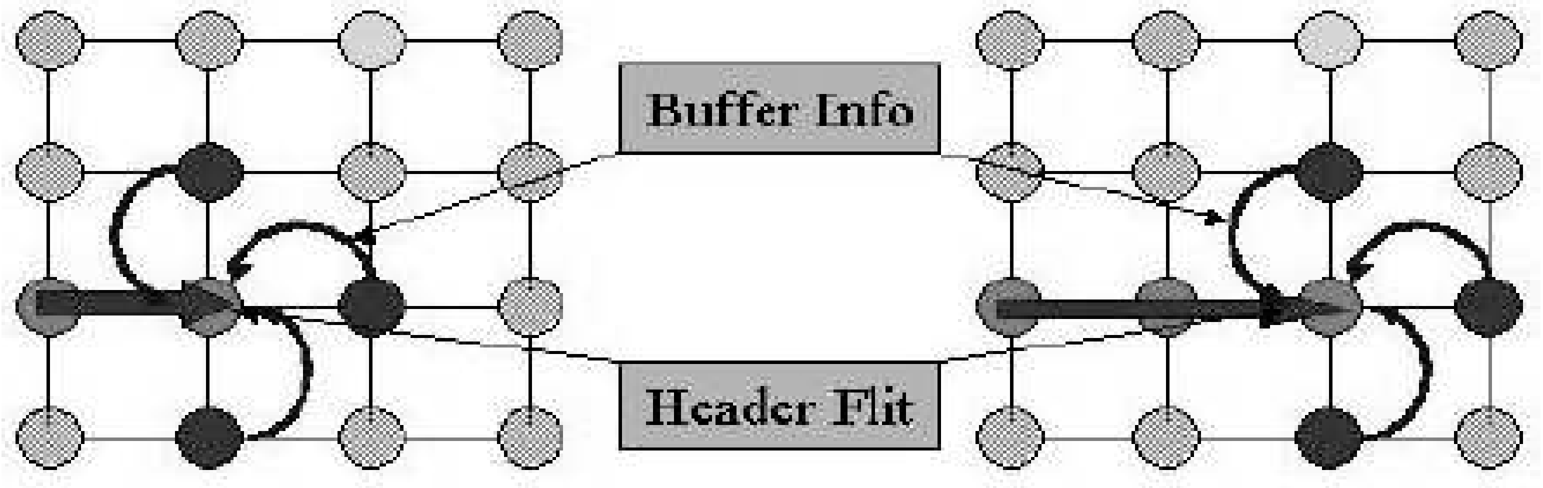
Static routing – XY routing



Adaptive Routing

# Contention-look-ahead Routing

- Can forese the contention of neighbors using control wires.
- The traffic condition of the neighboring nodes are obtained through the control signal wires.



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