Solutions

1. Deactivate the independent sources. The equivalent circuit looks as shown in Fig. 1.

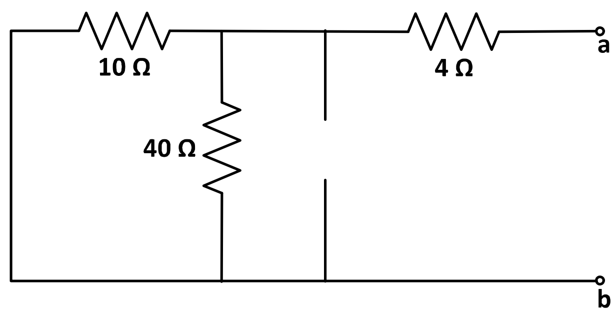

Fig. 1 Thevenin's equivalent circuit after deactivating the independent source.

The network shown in Fig. 1 can be simplified (Fig. 2a) and the equivalent resistance, as seen from nodes a-b, is determined (Fig. 2b). The equivalent resistance shown in Fig. 2b is the Thevenin's resistance:

$$Z_{th} = 12\Omega \qquad (1)$$

Next we determine the open circuit voltage across a-b. The current is $I_x = 0$ because the terminals a-b are open (Fig. 3a). Hence, there is no voltage drop across the 4Ω resistance and this resistance can be ignored (Fig. 3b).

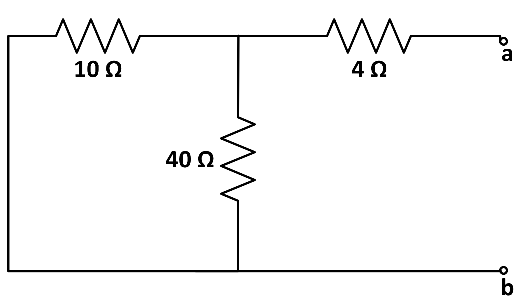

Fig. 2a Simplified circuit

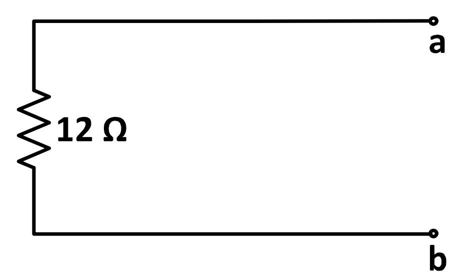

Fig. 2b Equivalent resistance

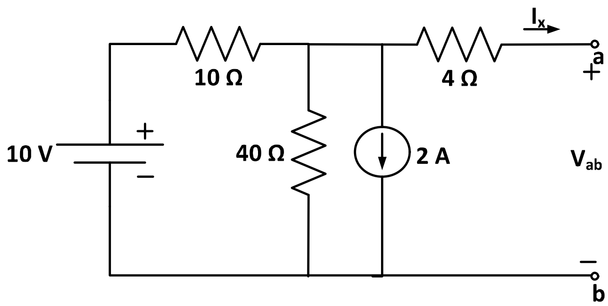

Fig. 3a Current I_x=0

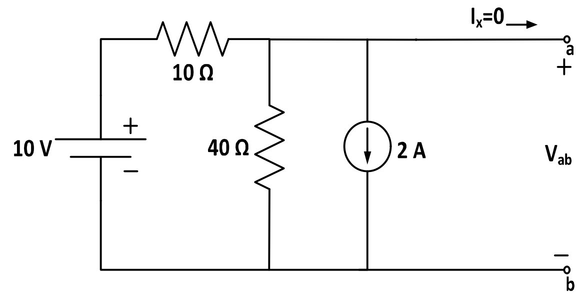

Fig. 3b Simplified circuit

Using a super node and applying KCL (Fig. 4) gives

$$\frac{V_{ab}-10}{10}+\frac{V_{ab}}{40}+2=0 \tag{2}$$

$$V_{ab}=-8V=V_{th} \tag{3}$$

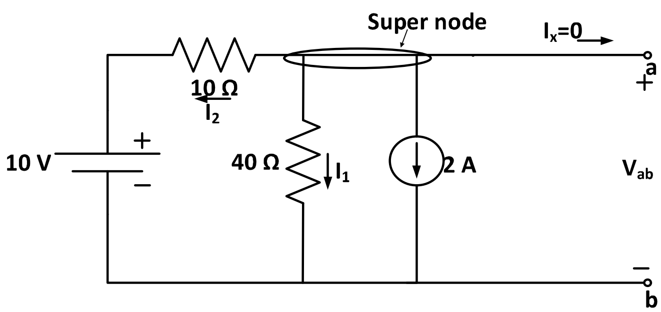

Fig. 4 KCL at Supernode

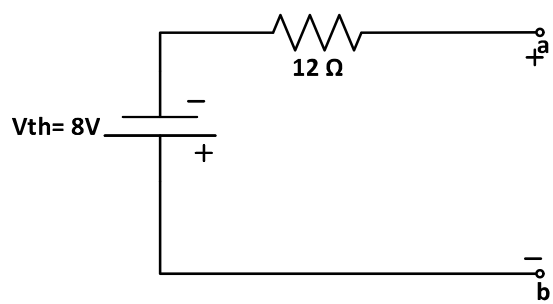

Fig. 5 Thevenin's equivalent circuit

The Thevenin's equivalent circuit is shown in Fig. 5.

2. The equivalent circuit the arc welding system is shown in Fig.6.In this figure V_{in} is the internal voltage of the source and R_{int} is the internal resistance of the source. The welding stick is connected across the terminals **a-b**.

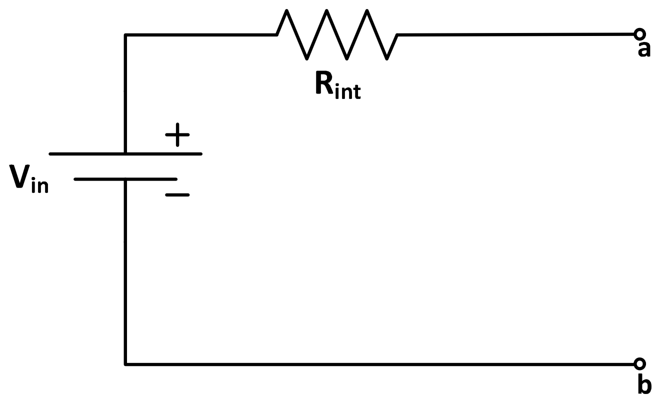

Fig. 6 Thevenin's equivalent circuit of the arc welding system

When the arc welder is loaded, the equivalent circuit is as shown in Fig. 7 and when it is under no load, its equivalent circuit is shown in Fig. 8.

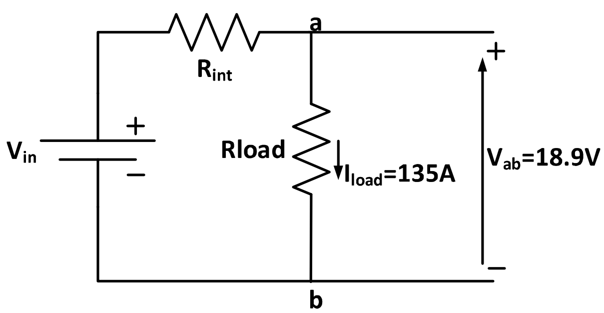

Fig. 7 Thevenin's equivalent circuit under load condition

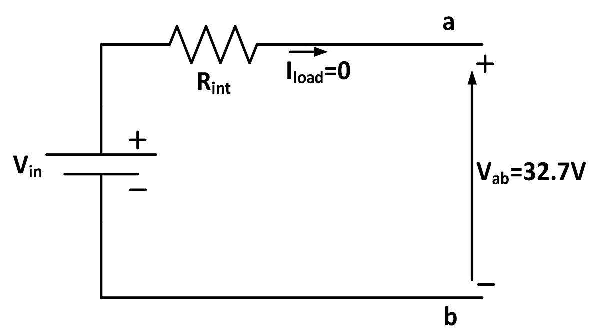

Fig. 8 Thevenin's equivalent circuit under no load condition

From the Fig.7 and 8 we can determine the open circuit voltage and it is:

$$V_{in} = V_{oc} = V_{th} = 32.7V \tag{4}$$

The internal resistance R_{int} is given by

$$R_{\text{int}} = \frac{V_{in} - V_{ab}\text{(during load condition)}}{I_{load}\text{(during load condition)}} = \frac{32.7 - 18.9}{135} = 0.102 = R_{th} \tag{5}$$

The Norton's current is given by

$$I_{Norton} = \frac{V_{th}}{R_{th}} = \frac{32.7}{0.102} = 320.5A \tag{6}$$

3.

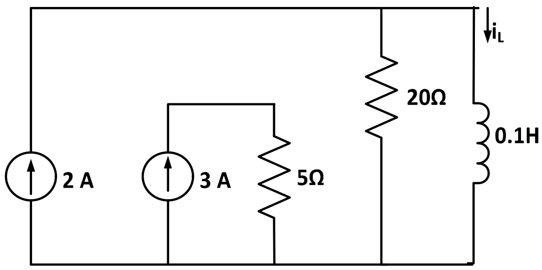

Fig. 9

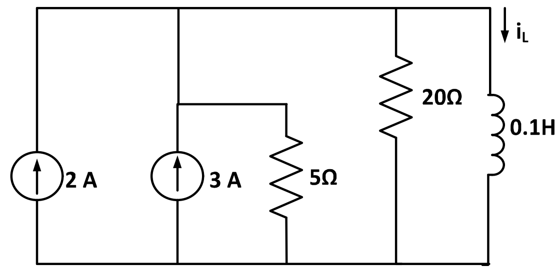

Fig. 10

Inductor behaves as a short circuit to D.C. source

$\therefore\ i_L = 2A.$ for $t < 0$ (Fig. 9)

For $t > 0$ the circuit becomes as shown in Fig. 10

$i_L(t) = i_f + i_n$

i_f = forced response

i_n = natural response

Inductor behaves as a short circuit to D.C. sources.

$\therefore\ i_f = 2A + 3A = 5A.$

$i_n = A\, e^{-t/\tau}$

τ = time constant $= \dfrac{L}{R_{eq}}$

$R_{eq} = 20 \| 5 = 4\Omega.$

$\therefore\ \tau = \dfrac{0.1}{4} = 0.025 \sec$

$\therefore\ i_n = A\, e^{-t/0.025} = A\, e^{-40t}$

$\therefore$ Total response for $t > 0$ is, $i_L(t) = 5 + A\, e^{-40t}$

putting initial condition , $i_L(0^-) = i_L(0^+)$

since the inductor cannot change the current through it instantaneously

$i_L(0^-) = 2A$

$\therefore\ 2 = 5 + A$ (put $t = 0$)

$\therefore\ A = -3$

$\therefore\ i_L(t) = 5 - 3\, e^{-40t}$ for $t > 0$

For all time t,

$i_L(t) = 2 + (3 - 3\, e^{-40t})\, u(t)$ for all t. [u(t) is the unit step function].

4.

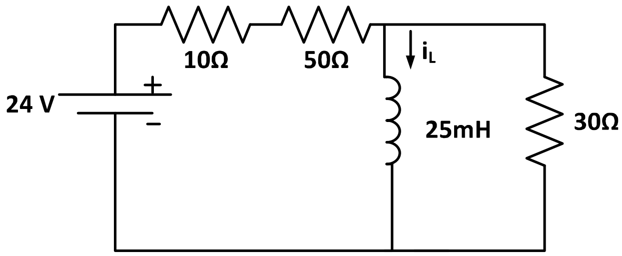

Fig. 11

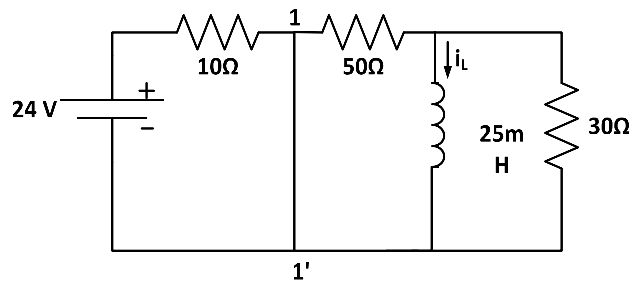

Fig. 12

For t < 0, the circuit is shown in Fig. 11.

Inductor will be short circuiting to D.C. source,

$\therefore\ i_L = \dfrac{24}{10+50} = 0.4\text{ A}$ for t < 0.

For t > 0, the circuit is shown in Fig. 12

$i_L(t) = i_f + i_n$

i_f = forced response = 0 (since current will follow short circuit path 11')

i_n = natural response = $A\ e^{-t/\tau}$

τ = time constant = $\dfrac{L}{R_{eq}} = \dfrac{L}{R_{eq}} = \dfrac{25\times10^{-3}}{R_{eq}}$,

$R_{eq} = 30 \parallel 50 = 18.75\ \Omega$

$\therefore\ \tau = \dfrac{25\times10^{-3}}{18.75}$ sec,

Now, $i_n = Ae^{-t/\frac{25\times10^{-3}}{18.75}} = Ae^{-750t}$

$\therefore\ i_L(t) = A\ e^{-750\,t}$ for t > 0

$i_L(0^-) = i_L(0^+)$

$\therefore\ 0.4 = A\ e^{-750 \times 0} = A$ for t = 0

$\therefore\ i_L(t) = 0.4\ e^{-750\,t}$ for t > 0

5.

Select MUX

Output

	S_3	S_2	S_1	S_0	y	
Select MUX 1	0	0	0	0	I_0	I_0
	0	0	0	1	I_1	I_1
	0	0	1	0	I_2	I_2
	0	0	1	1	I_3	I_3
	0	1	0	0	I_4	I_4
	0	1	0	1	I_5	I_5
	0	1	1	0	I_6	I_6
	0	1	1	1	I_7	I_7
Select MUX 2	1	0	0	0	I_8	I_0
	1	0	0	1	I_9	I_1
	1	0	1	0	I_{10}	I_2
	1	0	1	1	I_{11}	I_3
	1	1	0	0	I_{12}	I_4
	1	1	0	1	I_{13}	I_5
	1	1	1	0	I_{14}	I_6
	1	1	1	1	I_{15}	I_7

Fig. 13

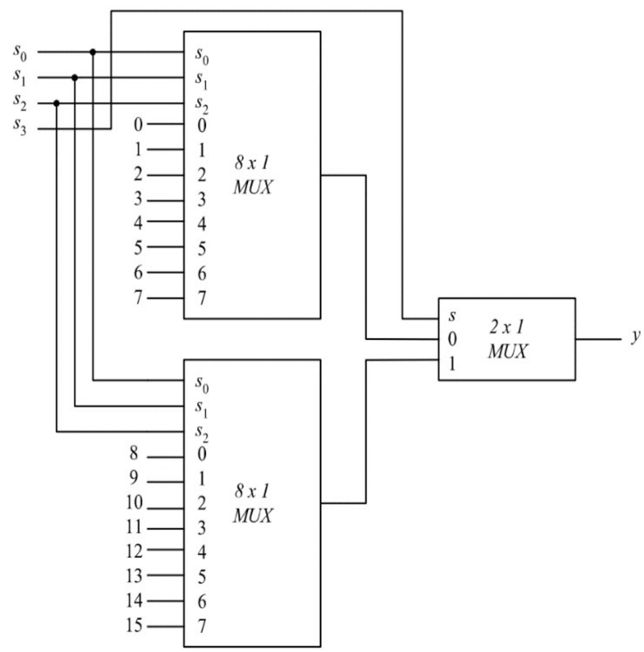

Fig. 14

6.

Fig. 15 shows Full-adder truth table. Where, Sum $S = \sum(1,2,4,7)$ and carry $C = \sum(3,5,6,7)$

X	Y	Z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig. 15 Truth Table of Full adder

X \ YZ	I_0 00	I_1 01	I_3 11	I_2 10
0	0	1	0	1
1	1	0	1	0

Fig. 16 Truth table for Sum

I_0	I_1	I_2	I_3
X	$\overline{X}$	$\overline{X}$	X

Fig. 17 Inputs of Sum MUX in terms of X

X \ YZ	I_0 00	I_1 01	I_3 11	I_2 10
0	0	0	1	0
1	0	1	1	1

Fig. 18 Truth table for Carry

I_0	I_1	I_2	I_3
0	X	X	1

Fig. 19 Inputs of Carry MUX in terms of X

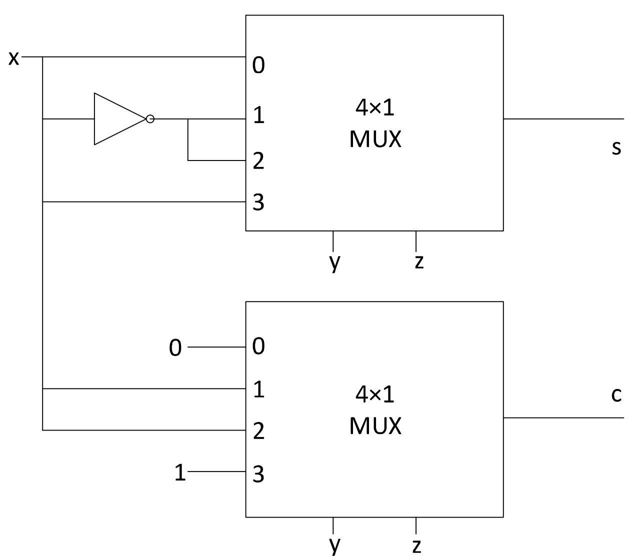

Fig. 20 Full adder using two 4 × 1 multiplexers