Tutorial-6 (Solutions)

Q-1:

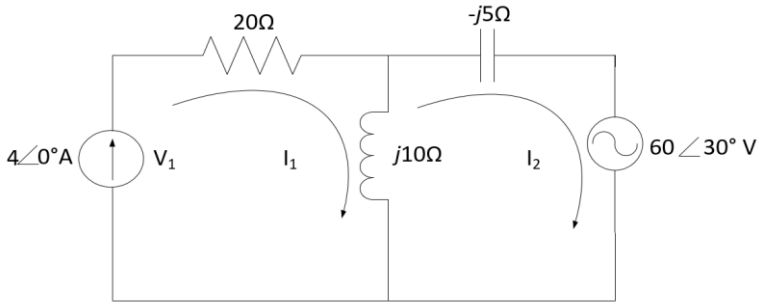

Fig. 1a

Applying mesh analysis, for mesh 1

$I_1 = 4A$ (1)

For mesh 2,

$(j10 - j5)I_2 - j10I_1 + 60\angle 30^o = 0$ (2)

Solving eq.1 and eq.2 gives

$I_2 = -12\angle -60^o + 8 = 10.58\angle 79.1^o A$ (3)

a. For the current source, the current through it is $I_1 = 4\angle 0^o A$ and the voltage across it is:

$V_1 = 20I_1 + j10(I_1 - I_2) = 183.9 + j20 = 184.984\angle 6.21^o V$

The average power suppied by the current source is

$P_1 = \frac{1}{2}(184.984) \times (4) \times \cos(6.21^o - 0^o) = 367.8W$

b. The current through the voltage source is:

$I_2 = -12\angle -60^o + 8 = 10.58\angle 79.1^o A$

The power delivered by the voltage source is

$P_2 = \frac{1}{2} \times 10.58 \times 60 \times \cos(30^o - 79.1^o) = 207.8W$

In view of the direction of I_2 and the polarity of the voltage source, the circuit is delivering average power to the voltage source.

c. For the resistor, the current through it is I_1 and the voltage across it is 20 I_1. Hence,

$P_3 = \frac{1}{2} \times 80 \times 4 = 160W$

d. For the inductor, the current through it is I_1-I_2 =10.58∠-79.1^o

The voltage across it is j10(I_1-I_2)=10.58∠-79.1^o + 90^o

hence, the average power absorbed by inductor is

$$P_4 = \frac{1}{2} \times 105.8 \times 10.58 \times \cos(90^o) = 0$$

e. For the capacitor, the current through it is I2 and the voltage across it is -j5I_2 =52.9∠79.1^o − 90^o. The average power absorbed by the capacitor is

$$P_5 = \frac{1}{2} \times 52.9 \times 10.58 \times \cos(-90^o) = 0$$

Q-2: The impedance seen by the load is: $Z = 2j + \frac{(2+2j)(-2j)}{2} = 2\Omega$

For maximum power transfer, the load impedance should be 2Ω

Q-3:

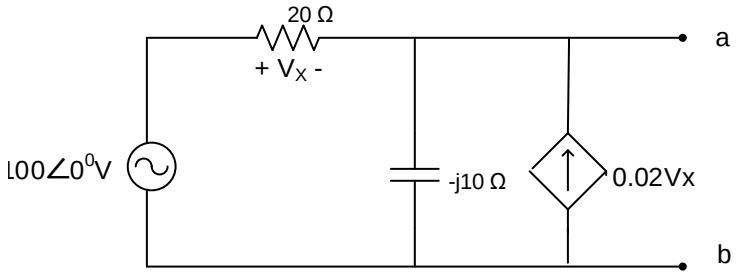

Fig. 3a

V_{th}: *Using source transformation, we get,*

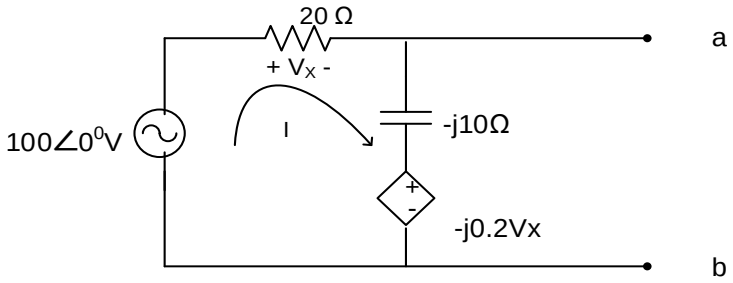

Fig. 3b

$$I = \frac{100 - (j\ 0.2V_X)}{20 - j10} = \frac{100 + j0.2V_X}{20 - j10}$$

Applying KVL for circuit shown in Fig. 3b -

- $100 - V_X - I(-j10) - (-j0.2V_X) = 0$

  $\Rightarrow 100 - V_X + \left(\frac{100+j0.2V_X}{20-j10}\right)(j10) + j0.2V_X = 0$

  $\Rightarrow (100 - V_X)(20 - j10) + j1000 - 2V_X + j0.2V_X(20 - j10) = 0$

$\Rightarrow 2000 - j1000 - 20V_X + j10V_X + j1000 - 2V_X + j4V_X + 2V_X = 0$

$\Rightarrow V_X = 67.11 + j46.98 = 81.92\angle 35°$

- $V_{\text{th}} = 100\angle 0° - V_X = 100\angle 0° - (81.92\angle 35°)$

  $\Rightarrow V_{\text{th}} = 32.89 - j46.98 = 57.35\angle -55°$ V

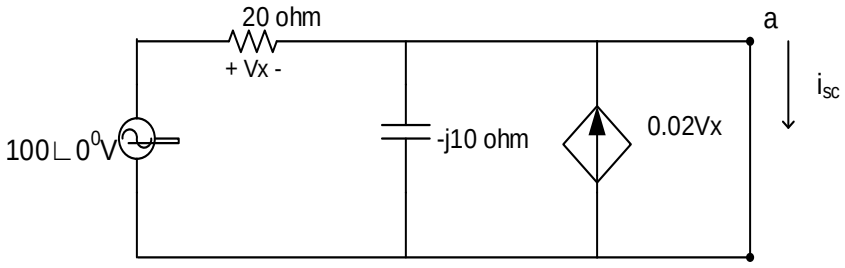

Fig. 3c

- As shown in Fig. 3c, $I_{\text{SC}} = \frac{100}{20} + 0.02V_X = 5 + 0.02(100) = 7\ A$
- $Z_{\text{th}} = \frac{V_{\text{th}}}{I_{\text{SC}}} = 57.35\angle -55°/7 \Rightarrow Z_{\text{th}} = (4.699 - j6.711)\Omega$
- Thevenin's equivalent circuit (shown in Fig. 3d):

$V_{\text{th}} = 57.35\angle -55°$ V and, $Z_{\text{th}} = 4.699 - j6.711\ \Omega$

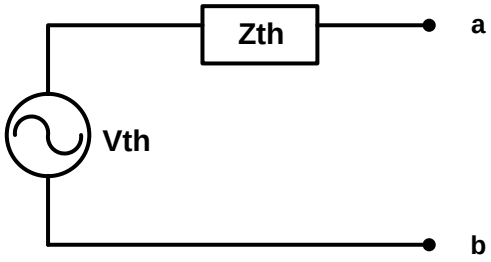

Fig. 3d

Q-4: It is clear that the clock signal arriving at the JK Flip-flop should be inverted before being connected to the T Flip-flop for the desired behaviour. Now, the table describing the transitions of the JK Flip-flop and the input to the T Flip-flop is as follows:

Q(k)	J	K	Q(k+1)	T
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1

Fig. 4a. State transition of JK flip-flop

Q(k) \ JK	00	01	11	10
0	0	0	1	1
1	0	1	1	0

Fig. 4b. The Karnaugh map for T

The minimal SOP is: T = JQ(k)' + KQ(k)

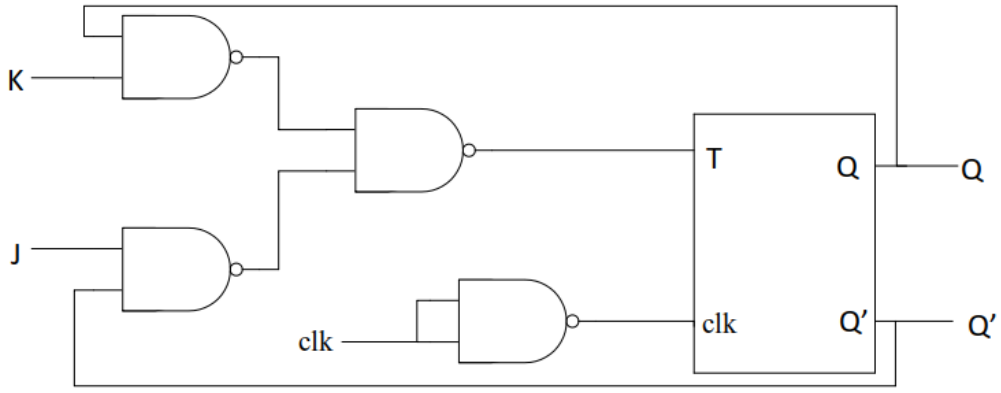

Fig. 4c. JK flip flop using positive edge triggered T flip-flop and NAND gates

Q-5: a)

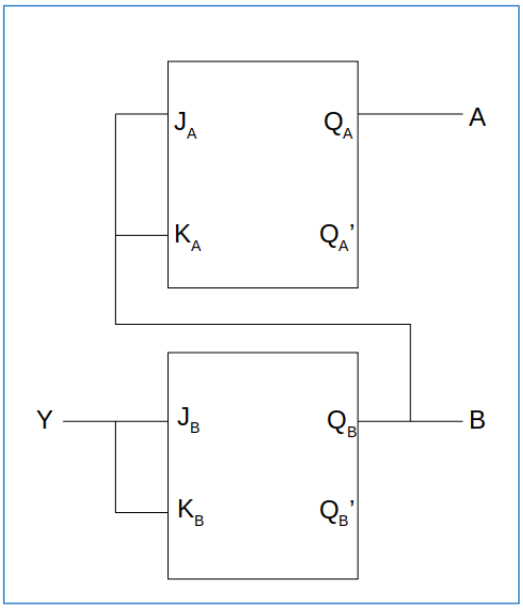

Fig. 5. Sequential circuit using 2 JK flip-flops

Present state		Input	Next state		Flip-Flop Inputs			
A	B	Y	A	B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	1	1	X	X	0
0	1	1	1	0	1	X	X	1
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	0	1	X	1	X	0
1	1	1	0	0	X	1	X	1

Fig. 5a. JK flip-flop state table

b) To solve A(t+1)

AB / Y	00	01	11	10
0	0	1	0	1
1	0	1	0	1

Fig. 5b.

A(t+1) = A'B + AB' = A XOR B

To solve B(t+1)

AB / Y	00	01	11	10
0	0	1	1	0
1	1	0	0	1

Fig. 5c.

B(t+1) = Y'B + YB' = Y XOR B

c) To solve J_A

AB / Y	00	01	11	10
0	0	1	X	X
1	0	1	X	X

Fig. 5d.

$J_A = B(t)$

To solve K_A

AB / Y	00	01	11	10
0	X	X	1	0
1	X	X	1	0

Fig. 5e.

$K_A = B(t)$

To solve J_B

AB / Y	00	01	11	10
0	0	X	X	0
1	1	X	X	1

Fig. 5f .

$J_B = Y(t)$

To solve K_B

AB / Y	00	01	11	10
0	X	0	0	X
1	X	1	1	X

Fig. 5g.

$K_B = Y(t)$

Note: Characteristic table for JK flip-flop

Flip-Flop Input		Next State	
J	K	Q(t+1)	Q'(t +1)
0	0	Q(t)	Q(t)
0	1	0	1
1	0	1	0
1	1	Q'(t)	Q(t)

Fig. 5h.

Present State	Next State	Flip-Flop Input	
Q(t)	Q(t+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Fig. 5i.

Q-6: The circuit takes 4-bit input word (X, Y, Z, P) with P as the least significant bit (LSB) and outputs '1' for inputs {0, 1, 3, 4, 5, 6, 7, 8, 9, A, B, D}

a)

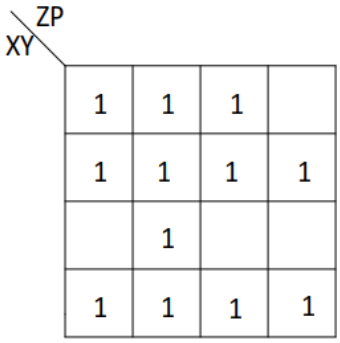

Fig. 6a.

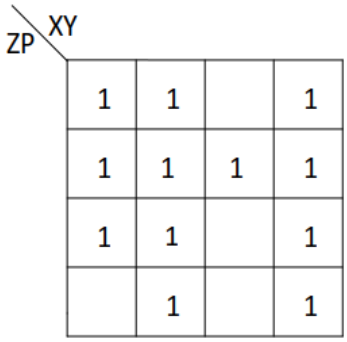

Fig. 6b.

b) Minimized SOP:

X'Z' + X'P + Z'P + X'Y + XY' **OR**

X'Z' + Y'P + Z'P + X'Y + XY' **OR**

Y'Z' + X'P + Z'P + X'Y + XY' **OR**

Y'Z' + Y'P + Z'P + X'Y + XY'

c) Minimized POS: (X' + Y' + P) (X' + Y' + Z') (X + Y + Z' + P)