CS 223 Computer Organization & Architecture

Lecture 28 [16.04.2020]

Pipeline Hazard Analysis

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True/False

- Which of the following statements is/are TRUE?

(I) RAW data hazard could be reduced by operand forwarding.

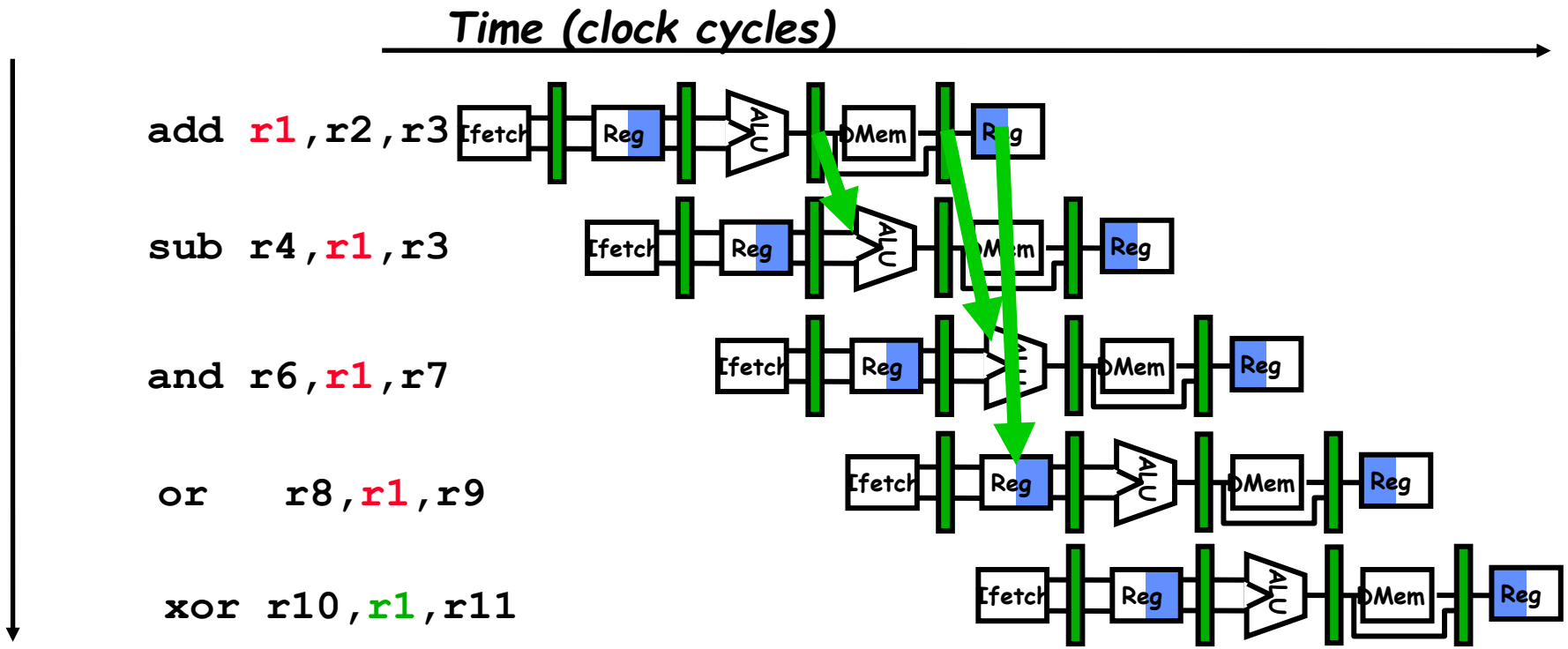
(II) A normal in-order 5 stage MIPS pipeline can achieve an IPC larger than 1.

(III) For a MIPS instruction STR R2, 16(R3), some contents stored in its ID/EX pipeline register will bypass the EX unit directly to EX/MEM pipeline register.

(IV) A normal 5 stage in order RISC pipeline without operand forwarding can have RAW and WAR hazards.

(A) I only (B) I & III only (C) II & IV only (D) III & IV only

Operand Forwarding to Avoid Data Hazard



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Visualizing Pipelining

	Clock number							
Instruction number	1	2	3	4	5	6	7	8
i	IF	ID	EX	MEM	WB			
i+1		IF	ID	EX	MEM	WB		
i+2			IF	ID	EX	MEM	WB	
i+3				IF	ID	EX	MEM	WB
i+4					IF	ID	EX	MEM

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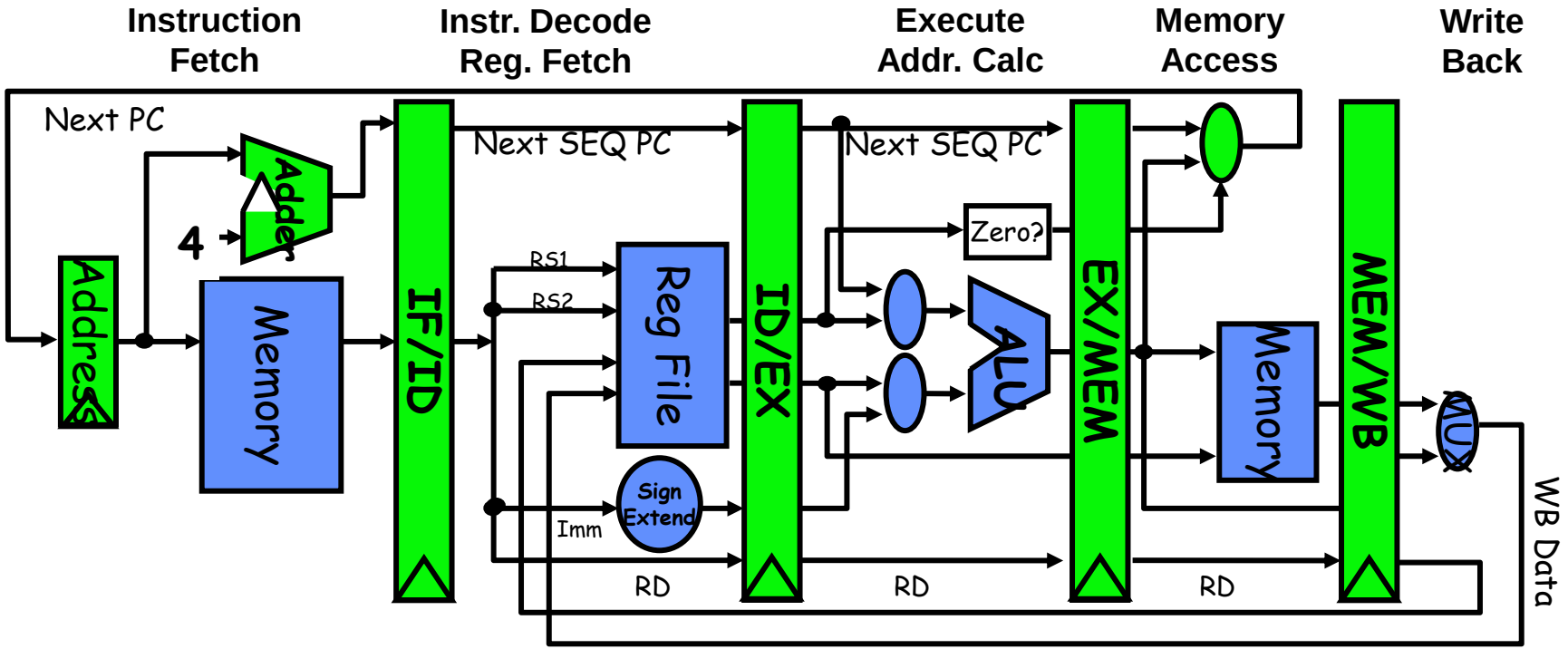
Pipelined RISC Data path



STR R2, 16(R3)

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i+3				IF	ID	EX	MEM	WB
i+4					IF	ID	EX	MEM

```
add r1,r2,r3
sub r4,r1,r3
and r6,r1,r7
```

```
add r1,r2,r3
sub r3,r1,r4
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```

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True/False

- Which of the following statements is/are FALSE?

(I) For a MIPs multi-cycle floating point pipeline the initiation interval of FP-mul is larger than that of FP-add

(II) WAW hazard cannot happen in a MIPS multi-cycle floating point pipeline.

(III) In a MIPS multi-cycle floating point pipeline that supports operand forwarding, there will be 7 stalls between a pair of adjacent MUL instructions that has a RAW dependency between them.

(IV) If a 32 bit value (0x12345678) is stored in memory byte addresses 2000, 2001, 2002 and 2003 in big-endian format, then location 2001 holds the value 0x56.

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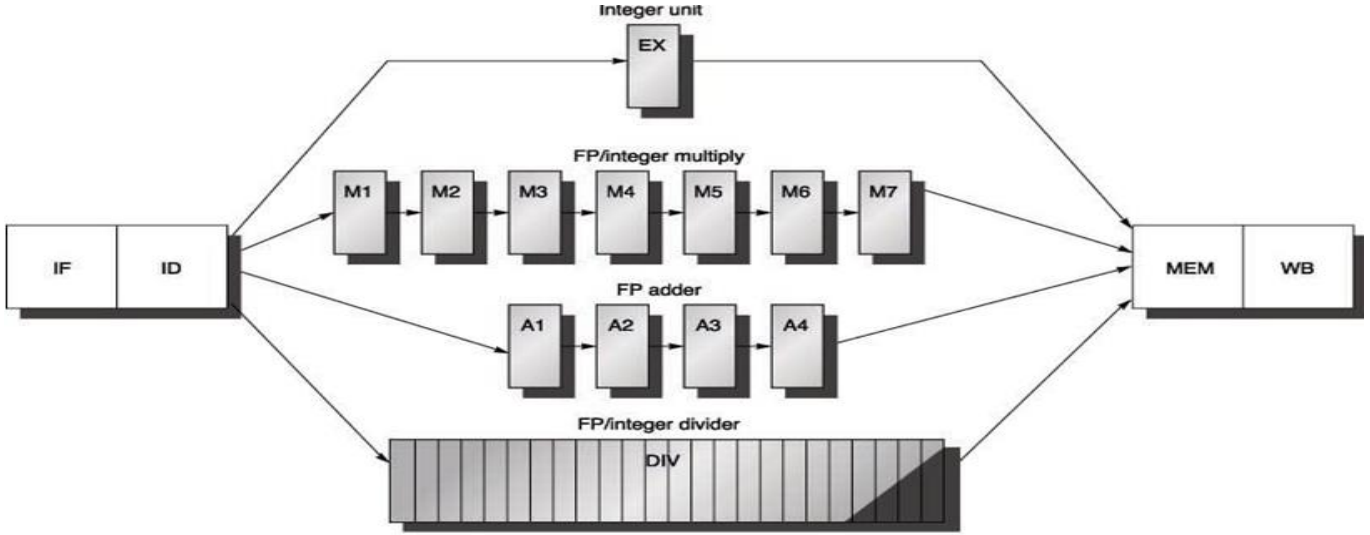
Multi-cycle Operations



Functional unit	Latency	Initiation interval
Integer ALU	0	1
Data memory (integer and FP loads)	1	1
FP add	3	1
FP multiply (also integer multiply)	6	1
FP divide (also integer divide)	24	25

Latencies and initiation intervals for functional units.

True/False

- Which of the following statements is/are FALSE?

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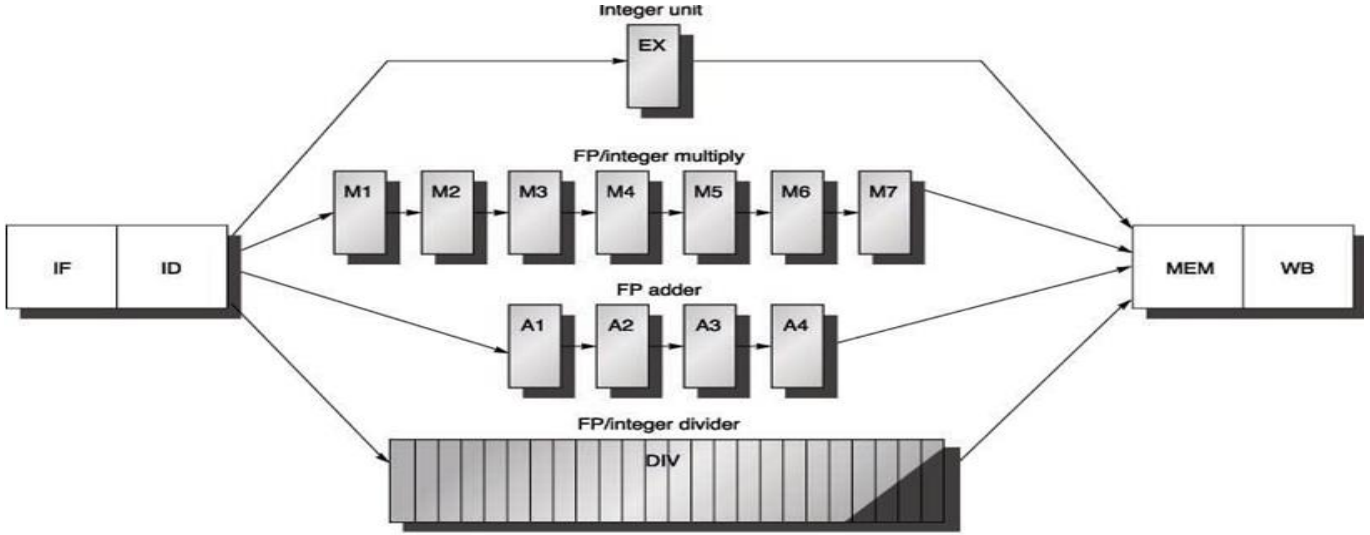

MUL.D	IF	ID	*M1*	M2	M3	M4	M5	M6	M7	MEM	WB
ADD.D		IF	ID	*A1*	A2	A3	**A4**	**MEM**	WB		
L.D			IF	ID	*EX*	**MEM**	WB				
S.D				IF	ID	*EX*	*MEM*	WB			

The pipeline timing of a set of independent FP operations. The stages in italics show where data are needed, while the stages in bold show where a result is available. The ".D" extension on the instruction mnemonic indicates double-precision (64-bit) floating-point operations. FP loads and stores use a 64-bit path to memory so that the pipelining timing is just like an integer load or store.

True/False

❖ Which of the following statements is/are FALSE?

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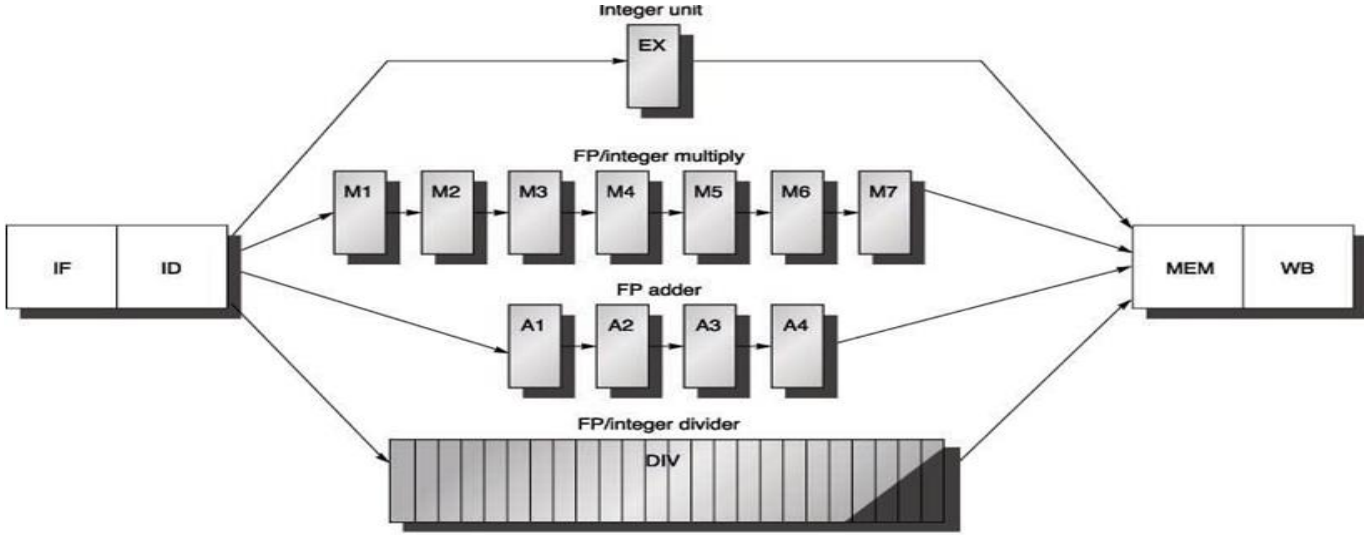
Multi-cycle Operations



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Byte Ordering

Big Endian vs. Little Endian

True/False

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Pipeline Hazards

Given a non-pipelined architecture running at 1.5 GHz, that takes 5 cycles to finish an instruction. You want to make it pipelined with 5 stages. Due to hardware overhead the pipelined design will operate only at 1 GHz. 5% of memory instructions cause a stall of 50 cycles, 30% of branch instruction cause a stall of 2 cycles and load-ALU combinations cause a stall of 1 cycle. Assume that in a given program, there exist 20% of branch instructions and 30% of memory instructions. 10% of instructions are load-ALU combinations. What is the speedup of pipelined design over the non-pipelined design?

Pipeline Hazards

(a) CPI_up = 5 1.5Ghz→0.67 ns : 1 Ghz→1 ns

Ex_T up= CPI x CCT = 5 x 0.66 ns = 3.33 ns / instruction

(b) Effective CPIp = Base CPI + stall CPI

{stalls= Memory stalls+ Branch stalls+ Load –ALU stalls}

= 1 + (0.3x0.05x50) + (0.2x0.3x2) + (0.1x1) = 1 + 0.75 + 0.12 +0.1 = 1.97

Ex_p = CPI x CCT = 1.97 x 1 ns = 1.97 ns / instruction

Speedup = Ex_up/ Ex_p = 3.33/1.97 = 1.69

Pipeline Hazards

A program has 2000 instructions in the sequence L.D, ADD.D, L.D, ADD.D,..... L.D, ADD.D. The ADD.D instruction depends on the L.D instruction right before it. The L.D instruction depends on the ADD.D instruction right before it. If the program is executed on the 5-stage pipeline what would be the actual CPI with and without operand forwarding technique?

Pipeline Hazards

Without operand forwarding.

ID of nth instruction can be only after WB of n-1th instruction.

3 stalls in each instruction.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
L.D	IF	ID	EX	ME	WB									
ADD		IF	*	*	*	ID	EX	ME	WB					
L.D						IF	*	*	*	ID	EX	ME	WB	
ADD										IF	*	*	*	ID

Instructions reach WB at clock cycles 5, 9, 13, 17, 21, 25, 29,…..

Last instruction (ADD) reaches WB in 5 + (1999x4) = 8001 cycles.

CPI= 8001/2000=4.0005

Pipeline Hazards

With operand forwarding.

Every ADD after L.D has a stall,
but L.D after ADD do not have a stall.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
L.D	IF	ID	EX	ME	WB									
ADD		IF	*	ID	EX	ME	WB							
L.D				IF	ID	EX	ME	WB						
ADD					IF	*	ID	EX	ME	WB				

Instructions reach WB at clock cycles **5,7, 8,10, 11,13, 14,16**

Last instruction (ADD) reaches WB in 7 + (999x3) = 3004 cycles.

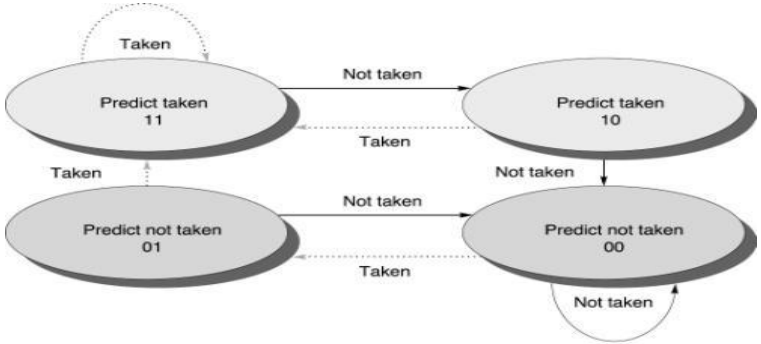
CPI= 3004/2000=1.502

Branch Prediction

Consider the last 16 actual outcomes of a single static branch. T means branch is taken and N means not taken.

{oldest→ T T N N T N T T T N T N T T N T ← latest}

A two level branch predictor of (1,2) type is used. Since there is only one branch in the program indexing to BHT with PC is irrelevant. Hence only last branch outcome only is used to index to the BHT. How many mis-predictions are there and which of the branches in this sequence would be mis-predicted? Fill up the table for 16 branch outcomes.



Branch Prediction

Sl.No	Last Outcome	BHT N/T	Prediction	Outcome	Mis-Pre Y/N ?
1	N (initial)	00 / 11	N	T	YES
2	T	01 / 11	T	T	NO
3	T	01 / 11	T	N	YES
4	N	01 / 10	N	N	NO
5	N	00 / 10	N	T	YES
6	T	01 / 10	T	N	YES
7	N	01 / 00	N	T	YES
8	T	11 / 00	N	T	YES
9	T	11 / 01	N	T	YES
10	T	11 / 11	T	N	YES
11	N	11 / 10	T	T	NO
12	T	11 / 10	T	N	YES
13	N	11 / 00	T	T	NO
14	T	11 / 00	N	T	YES
15	T	11 / 01	N	N	NO
16	N	11 / 00	T	T	NO

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