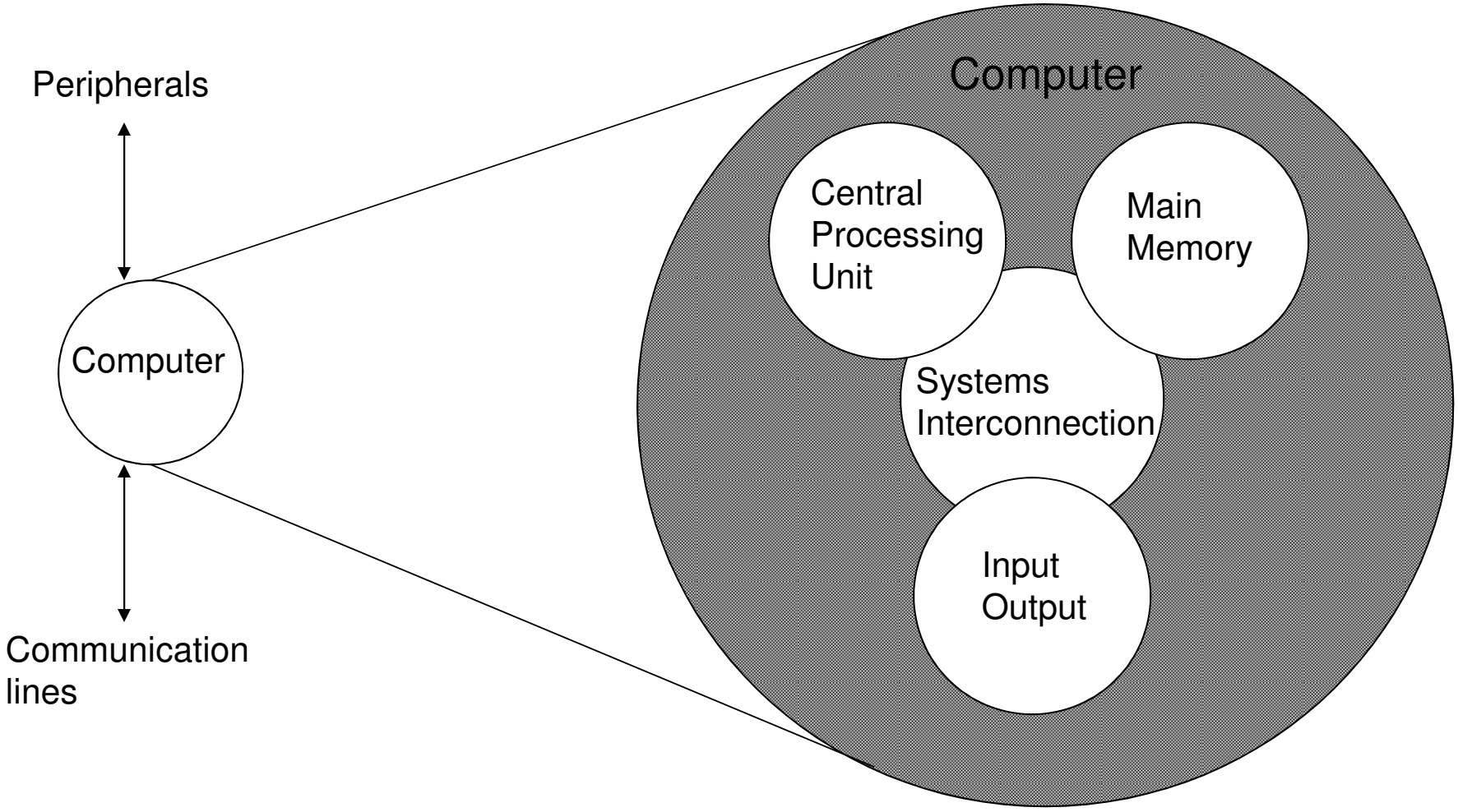
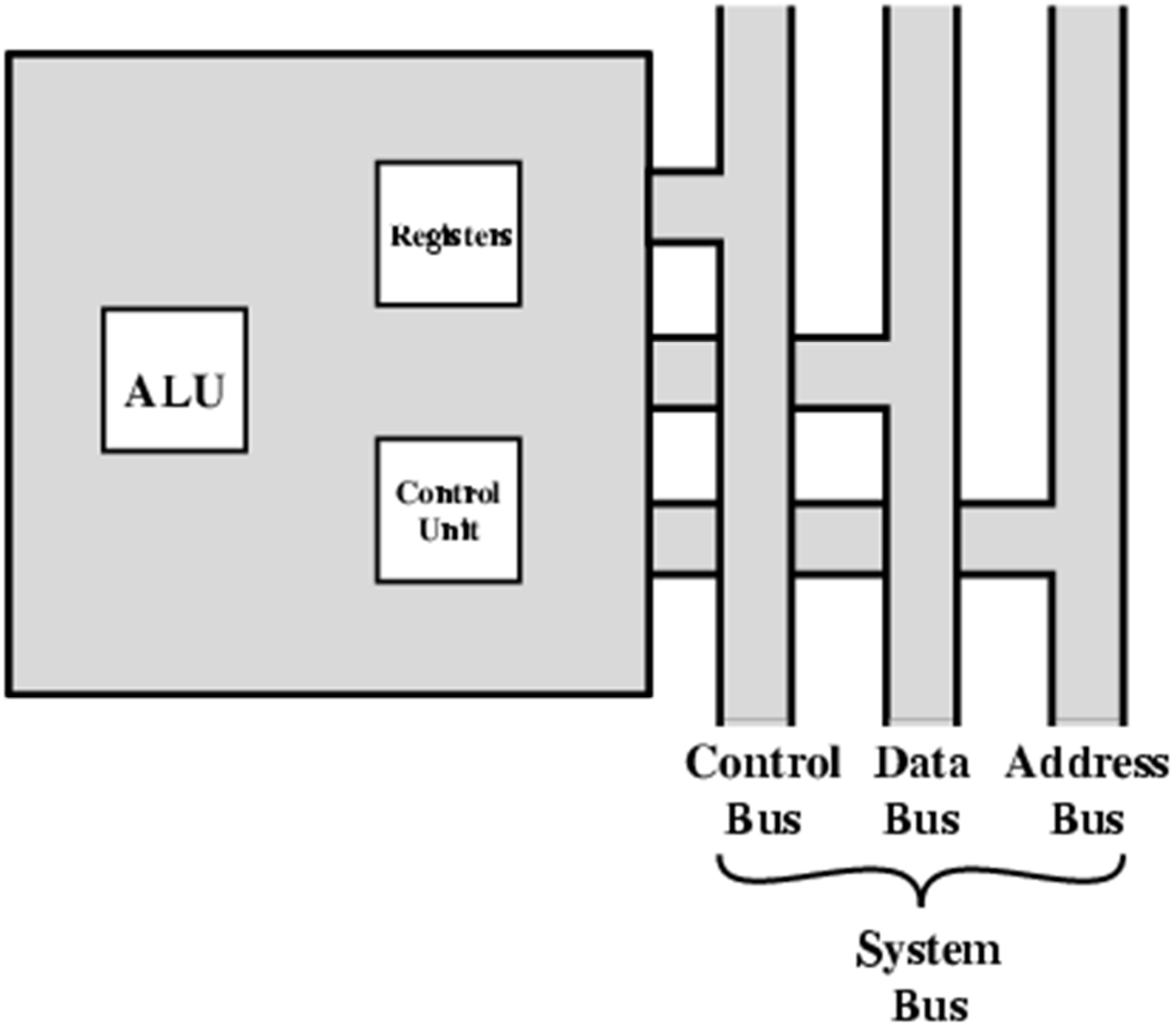
Internal Memory

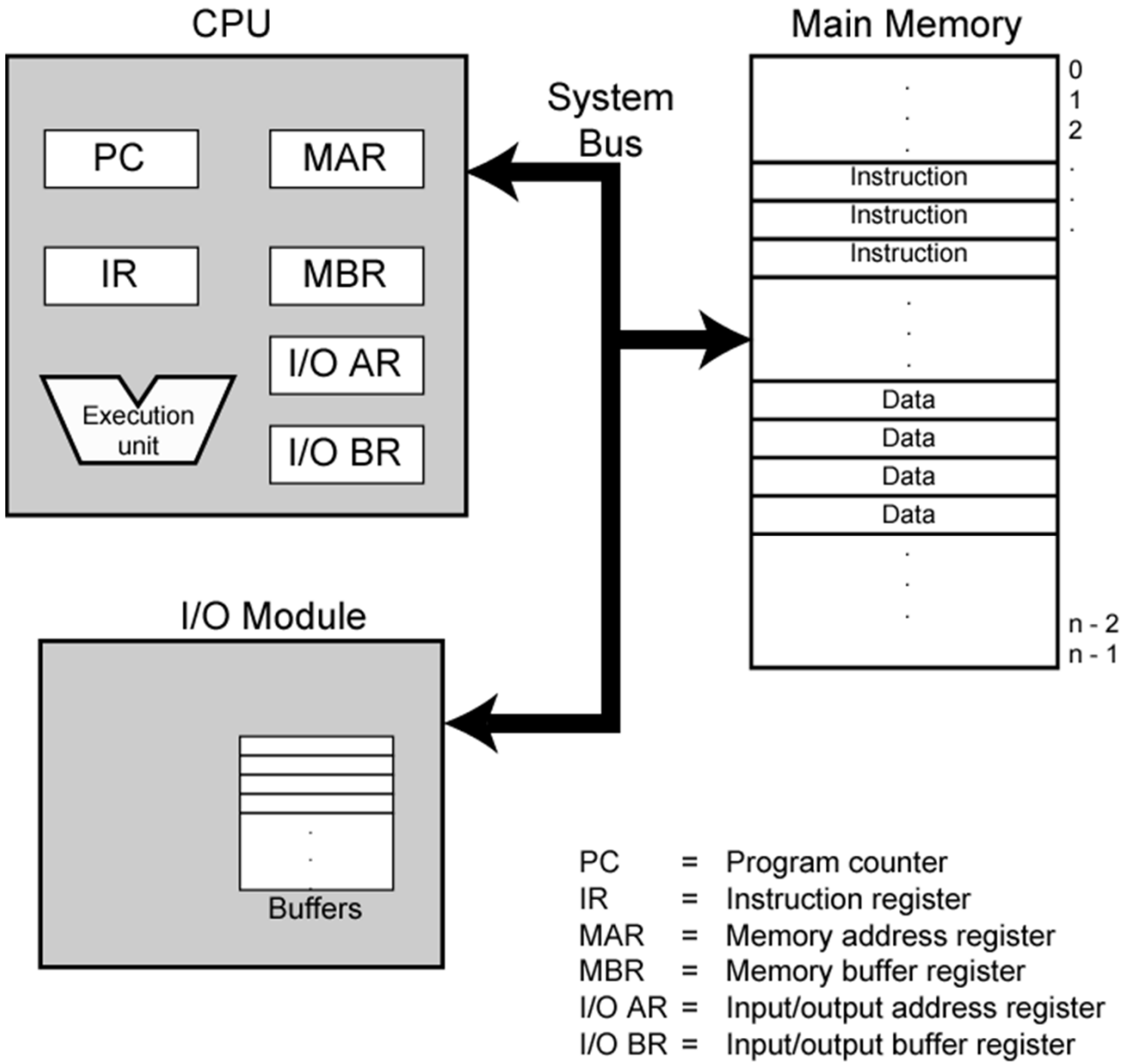
Structure - Top Level



CPU With Systems Bus



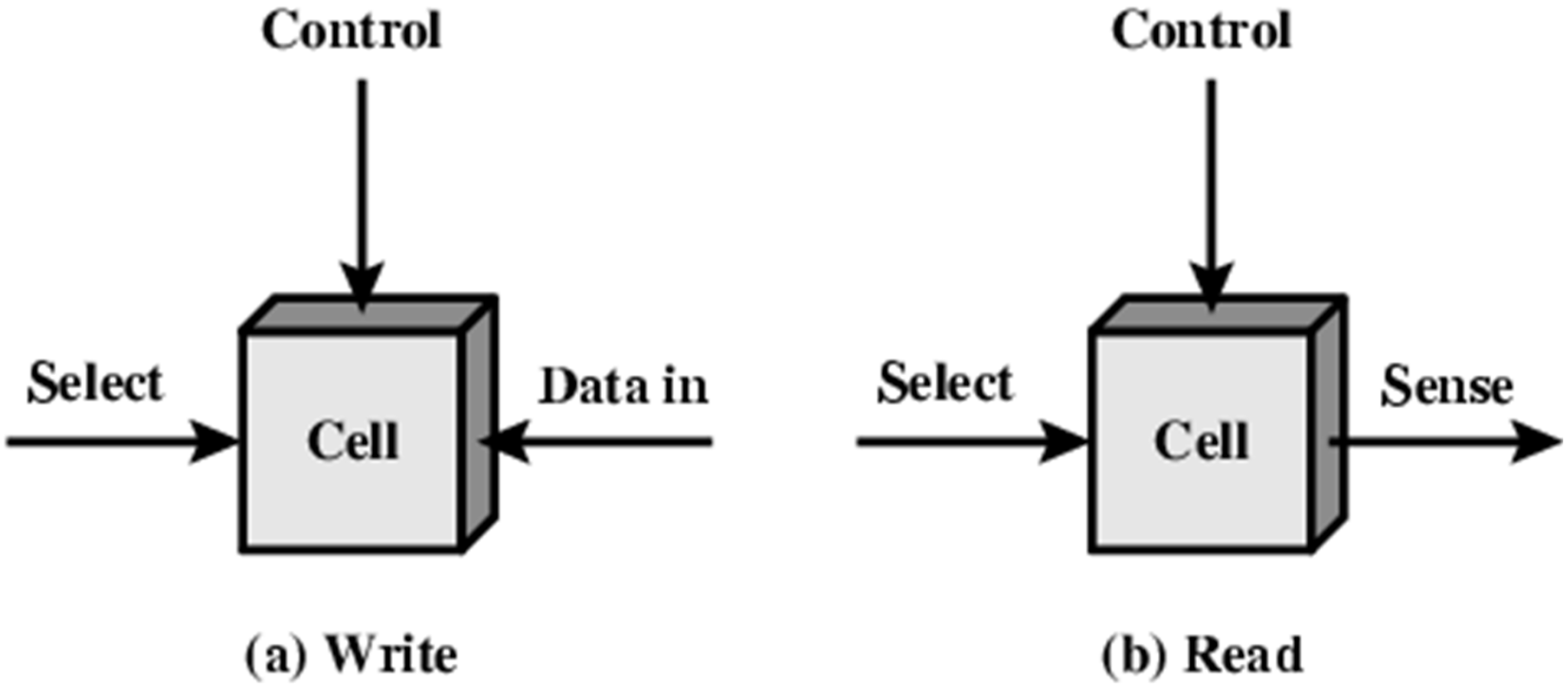
Computer Components: Top Level View



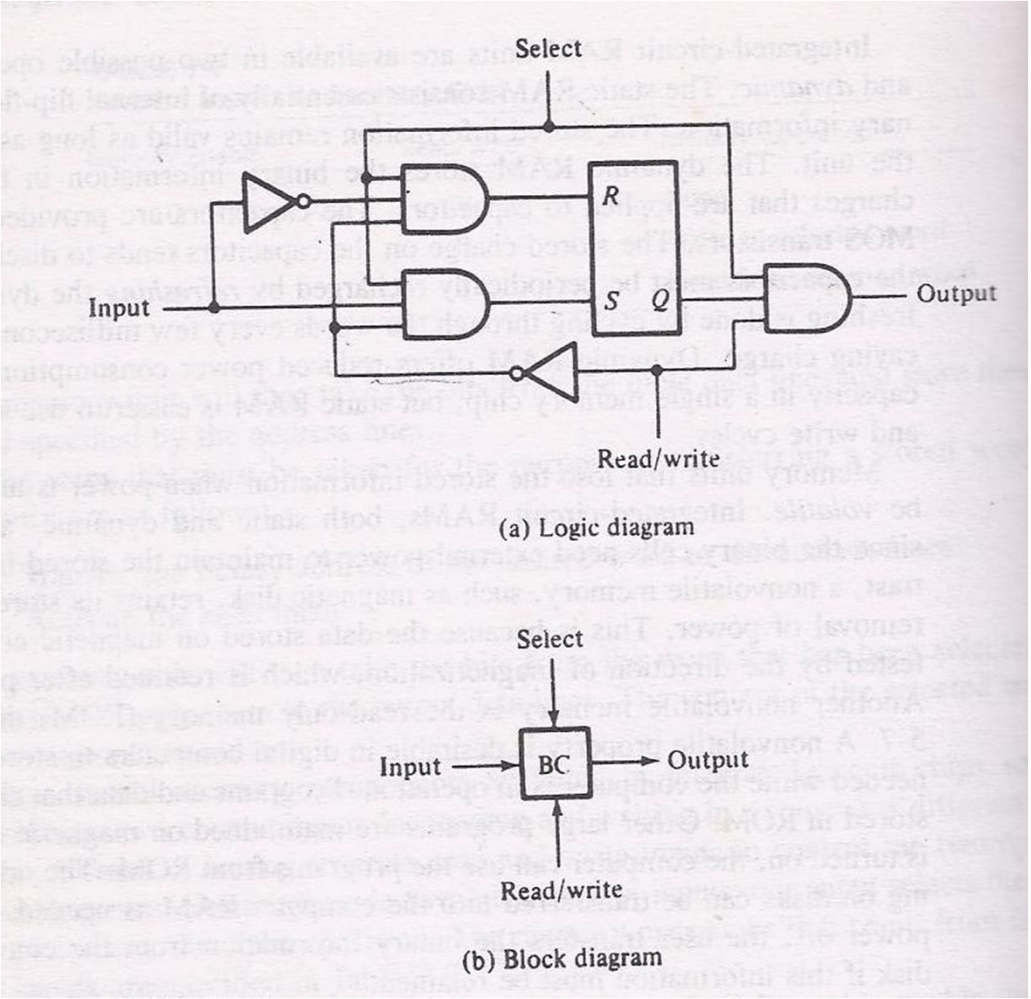
Semiconductor Memory

- RAM
  - —Misnamed as all semiconductor memory is random access
  - —Read/Write
  - —Volatile
  - —Temporary storage
  - —Static or dynamic

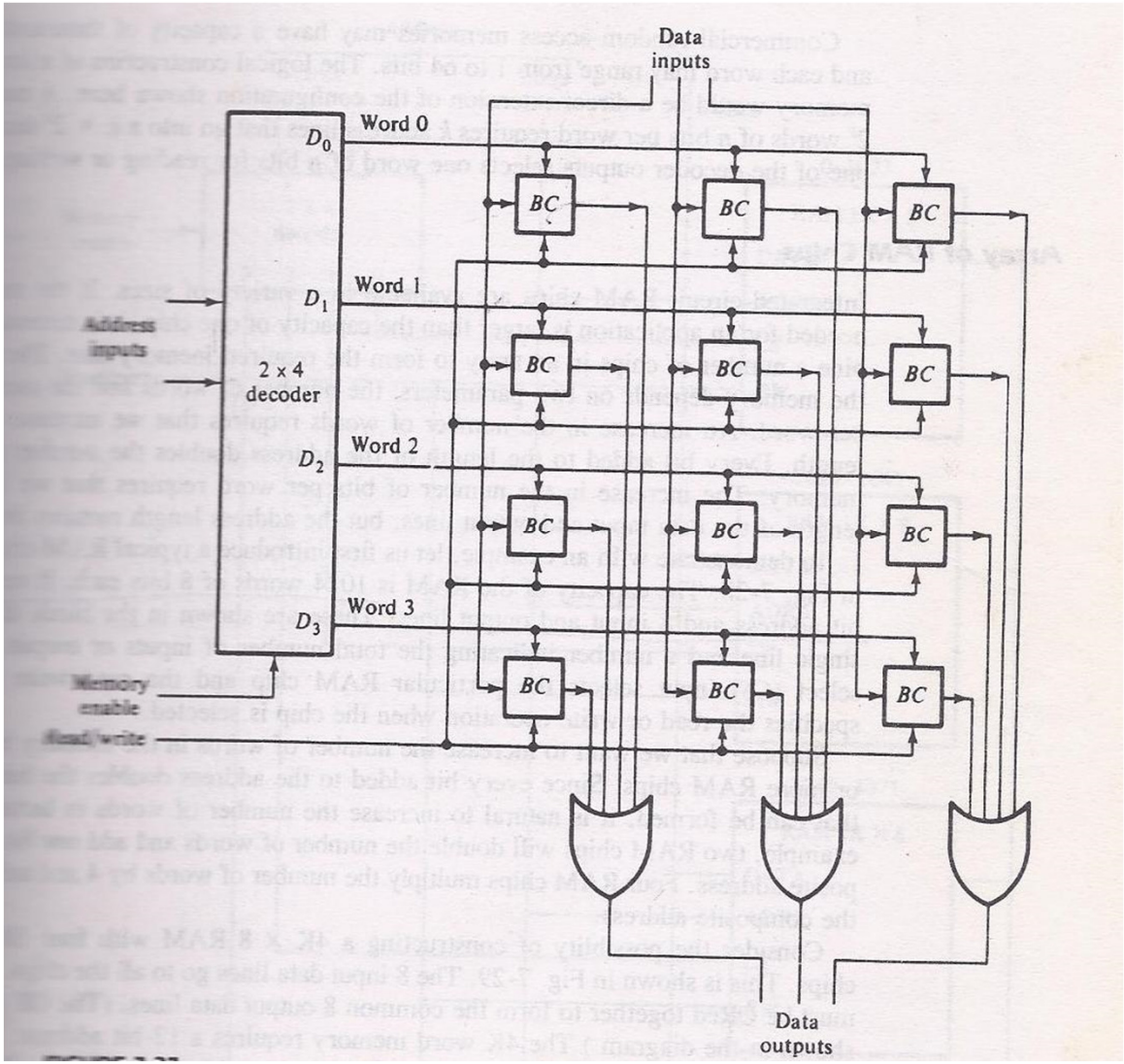
Memory Cell Operation



Memory Cell


Select
R
Input
S
Q
Output
Read/write
(a) Logic diagram
Select
Input
BC
Output
Read/write
(b) Block diagram

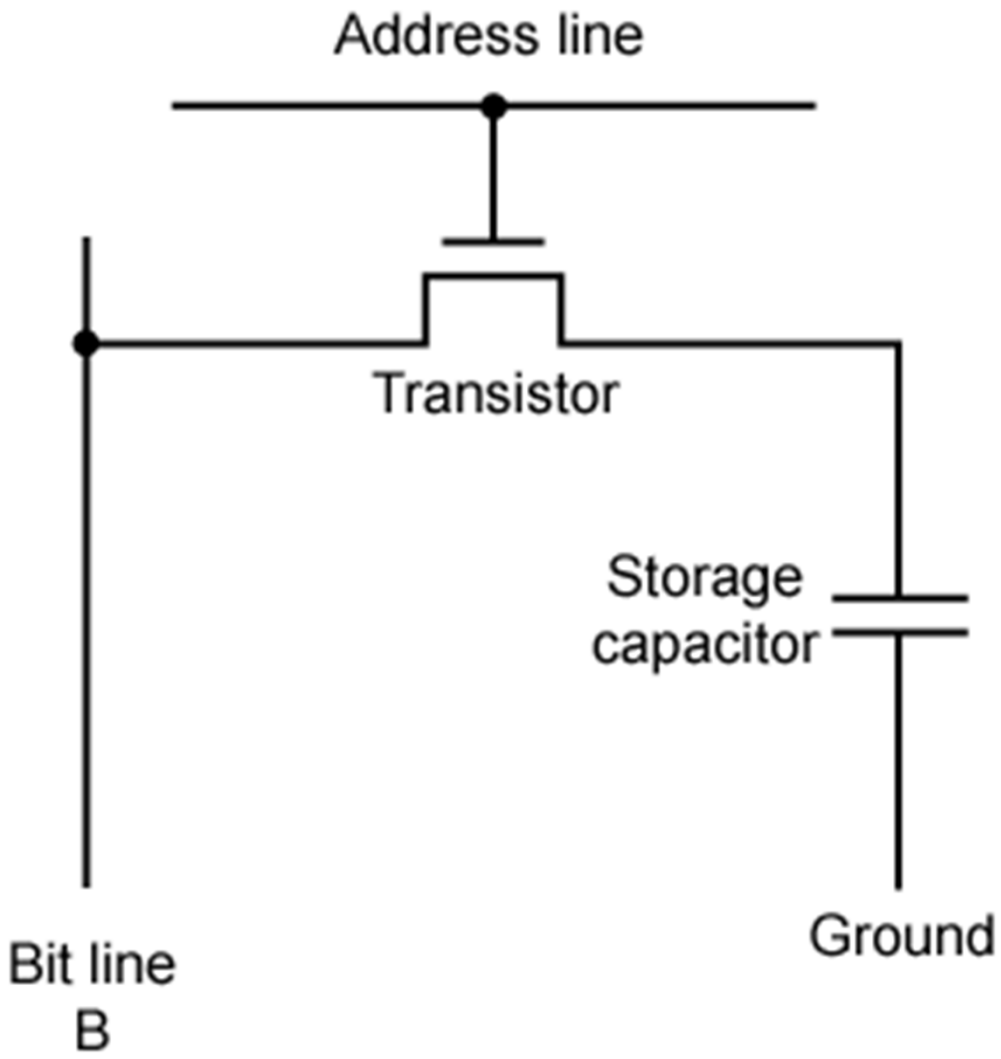
Memory Module



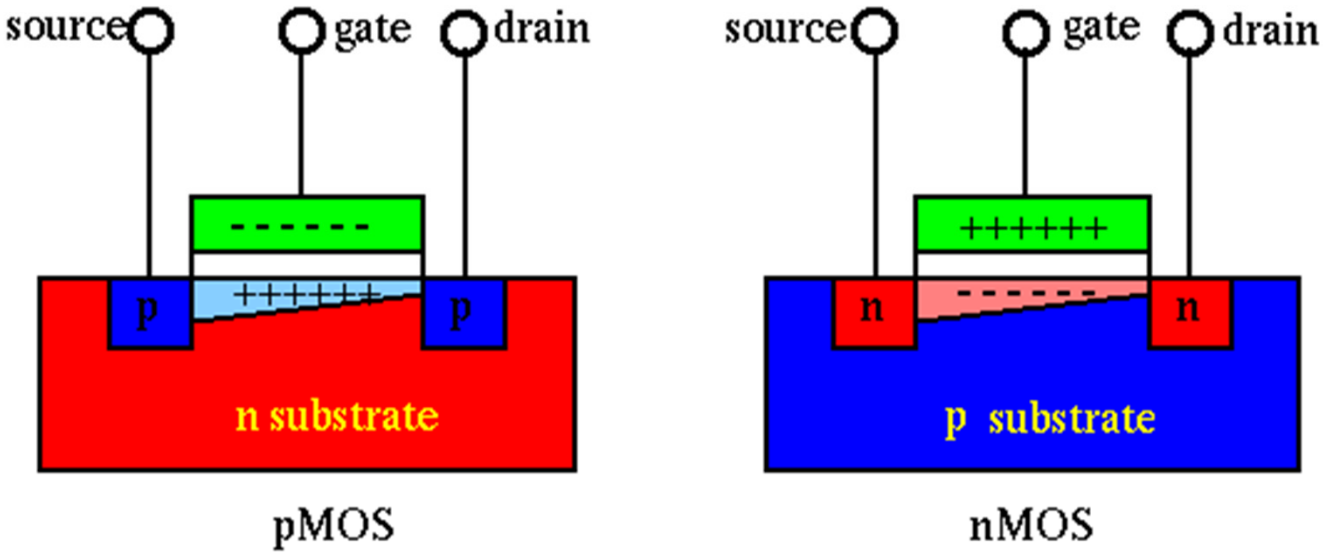
Dynamic RAM

- Bits stored as charge in capacitors
- Charges leak
- Need refreshing even when powered
- Simpler construction
- Smaller per bit
- Less expensive
- Need refresh circuits
- Slower
- Main memory
- Essentially analogue
  - Level of charge determines value

Dynamic RAM Structure



Structure of MOSFET



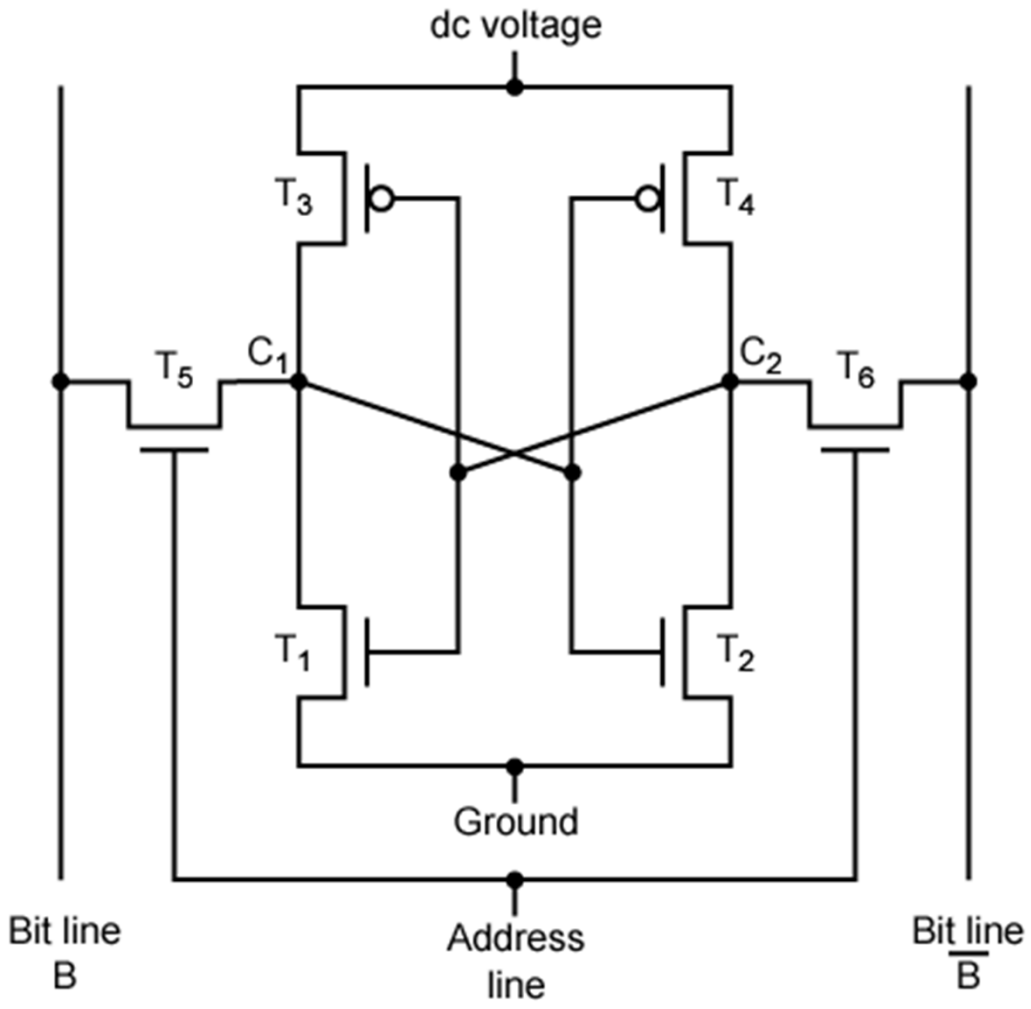
DRAM Operation

- Address line active when bit read or written
  - Transistor switch closed (current flows)
- Write
  - Voltage to bit line
    - High for 1 low for 0
  - Then signal address line
    - Transfers charge to capacitor
- Read
  - Address line selected
    - transistor turns on
  - Charge from capacitor fed via bit line to sense amplifier
    - Compares with reference value to determine 0 or 1
  - Capacitor charge must be restored

Static RAM

- Bits stored as on/off switches
- No charges to leak
- No refreshing needed when powered
- More complex construction
- Larger per bit
- More expensive
- Does not need refresh circuits
- Faster
- Cache
- Digital
  - —Uses flip-flops

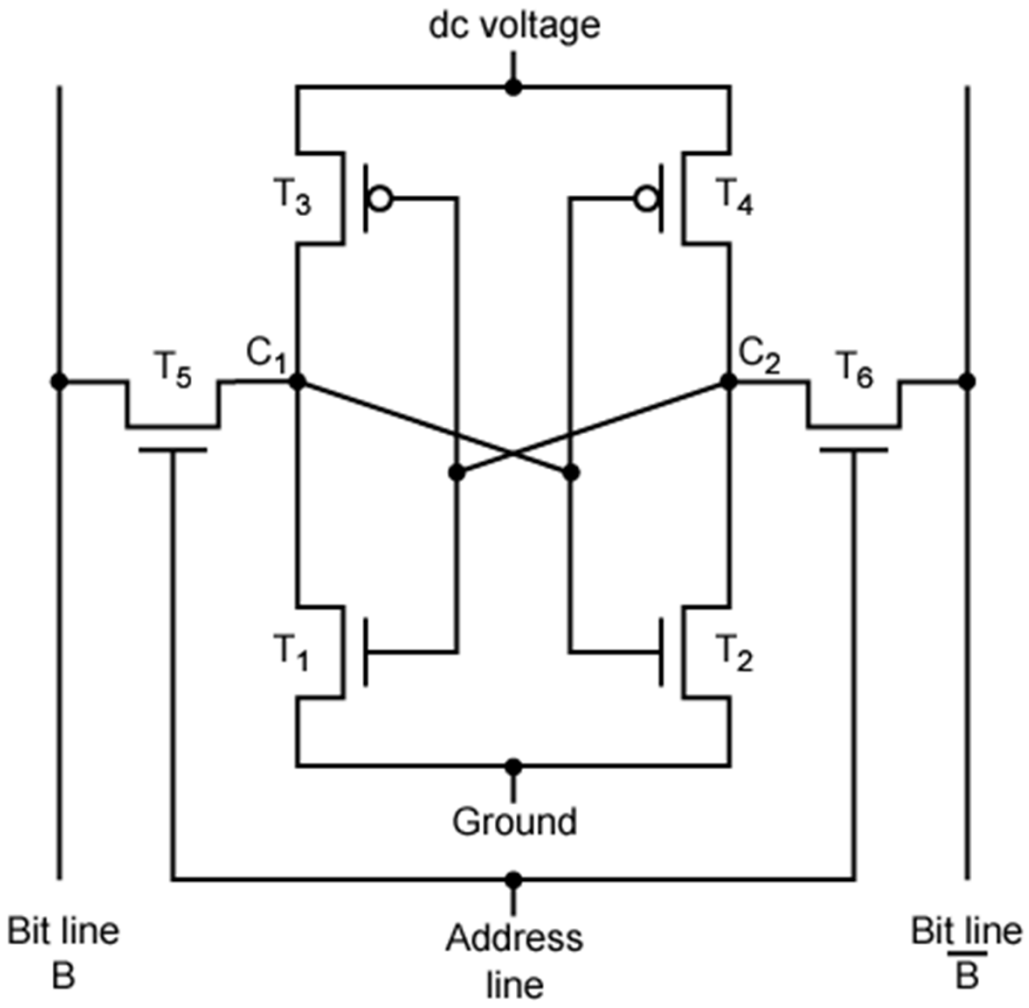
Stating RAM Structure



Static RAM Operation

- Transistor arrangement gives stable logic state
- State 1
  - C_1 high, C_2 low
  - T_1 T_4 off, T_2 T_3 on
- State 0
  - C_2 high, C_1 low
  - T_2 T_3 off, T_1 T_4 on
- Address line transistors T_5 T_6 is switch
- Write – apply value to B & compliment to B
- Read – value is on line B

Stating RAM Structure



State 1

C_1 high, C_2 low

T_1 T_4 off, T_2 T_3 on

State 0

C_1 low, C_2 high

T_1 T_4 on, T_2 T_3 off

SRAM v DRAM

- Both volatile
  - —Power needed to preserve data
- Dynamic cell
  - —Simpler to build, smaller
  - —More dense
  - —Less expensive
  - —Needs refresh
  - —Larger memory units
- Static
  - —Faster
  - —Cache

Read Only Memory (ROM)

- Permanent storage
  - Nonvolatile
- Microprogramming
- Library subroutines
- Systems programs (BIOS)
- Function tables

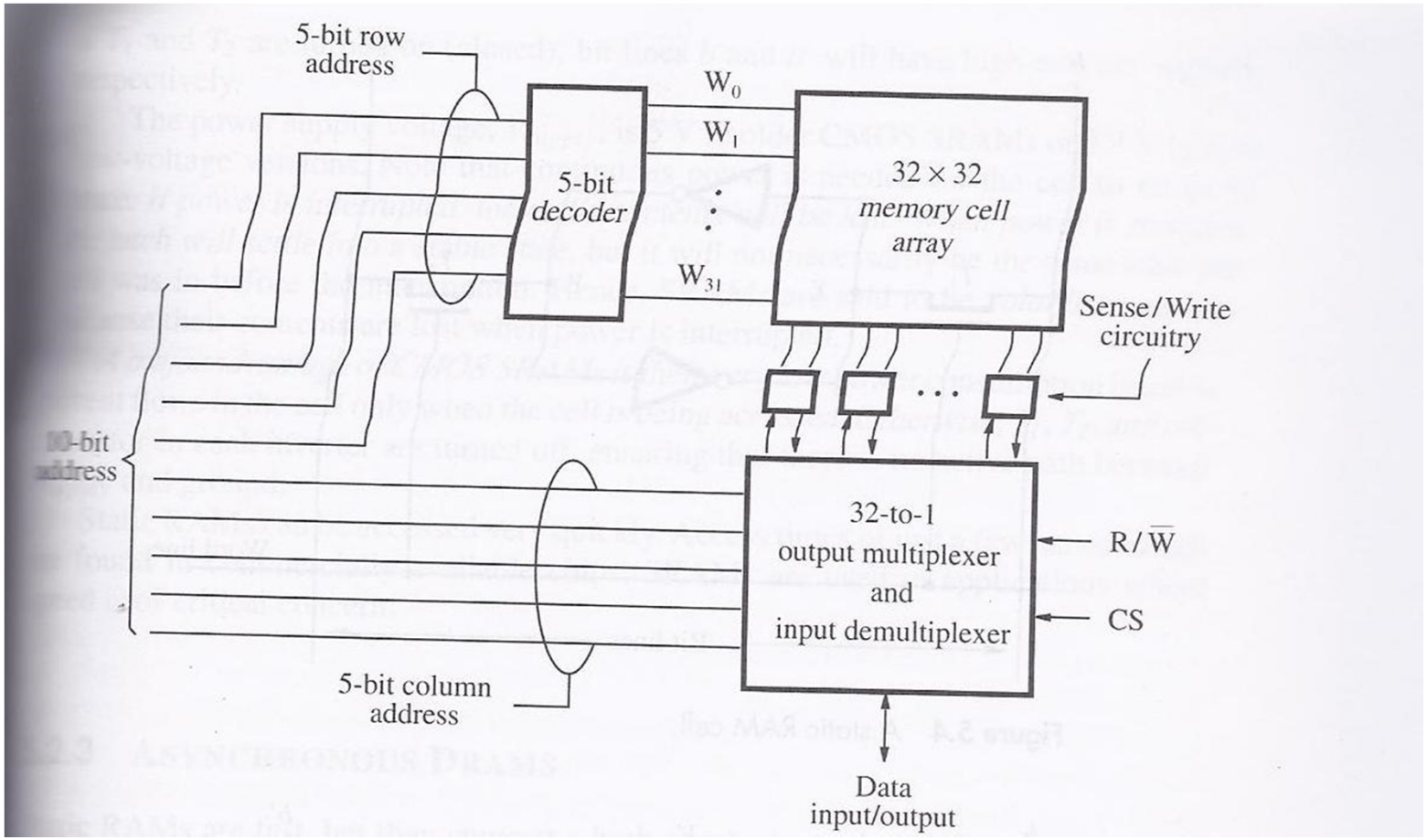
Types of ROM

- Written during manufacture
  - —Very expensive for small runs
- Programmable (once)
  - —PROM
  - —Needs special equipment to program
- Read "mostly"
  - —Erasable Programmable (EPROM)
    - – Erased by UV
  - —Electrically Erasable (EEPROM)
    - – Takes much longer to write than read
  - —Flash memory
    - – Erase whole memory electrically

Organisation in detail

- A 8Kbit chip can be organised as 1K of 8 bits word
  - Size of Address Bus: 10 (2^{10} = 1024 = 1K)
  - Size of Data Bus: 8
- A 8Kbit chip can also be organised as a 32 x 32 x 8bit array
- Address has two parts:
  - Row Address (2^5 = 32)
  - Column Address (2^5 = 32)

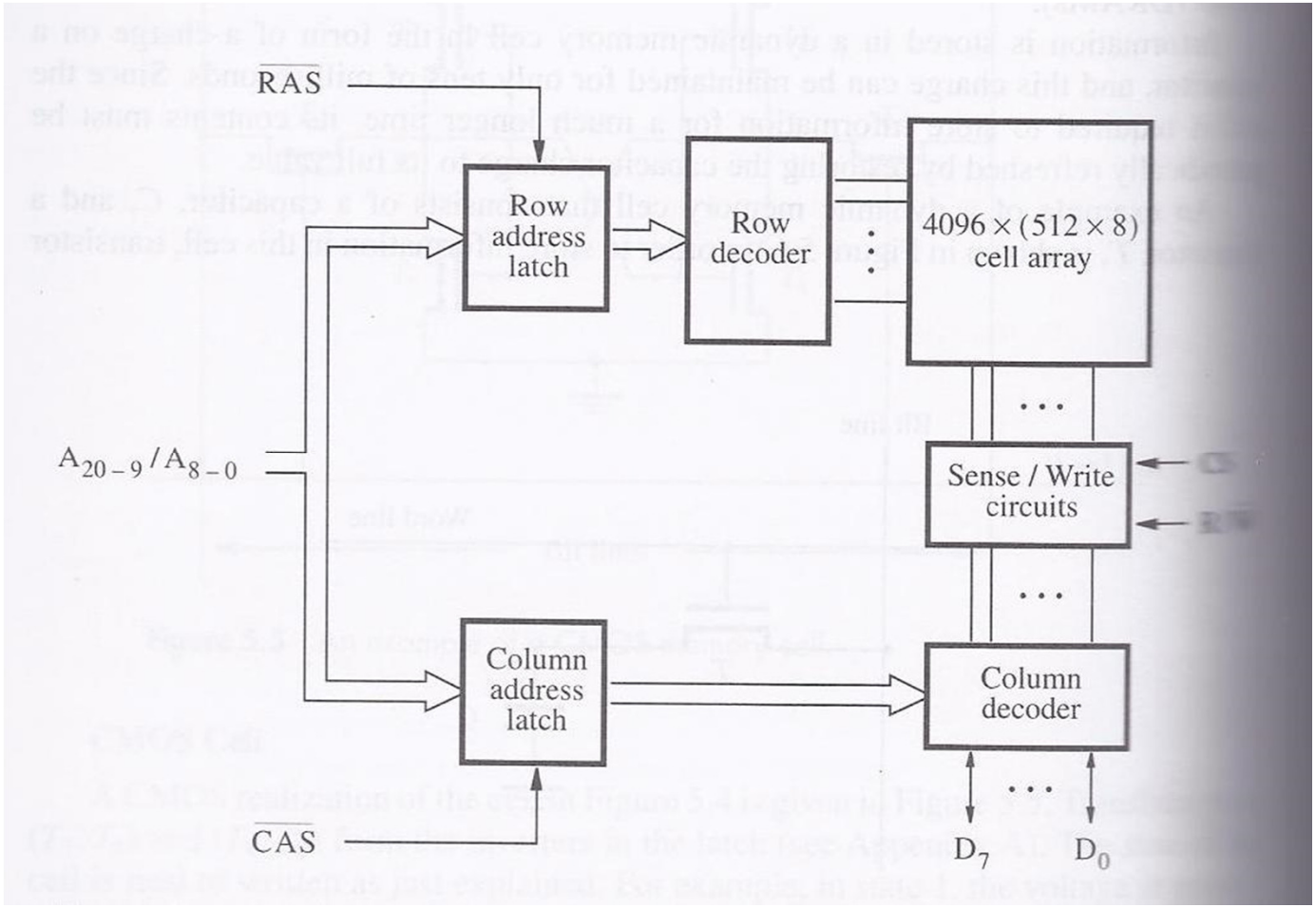
Organisation in detail



Organisation in detail

- A 16Mbit chip is organised as a 4096 x (512 x 8) bit array
- 2MByte chip having 2M location of 1 Byte each
- It helps to reduce the address pins
  - Multiplex row address and column address
  - 12 pins for address (2^{12}=4096)
  - 12 for row address (2^{12} = 4096)
  - 9 for column address (2^{9} = 512)
  - Adding one bit in column address doubles the memory capacity

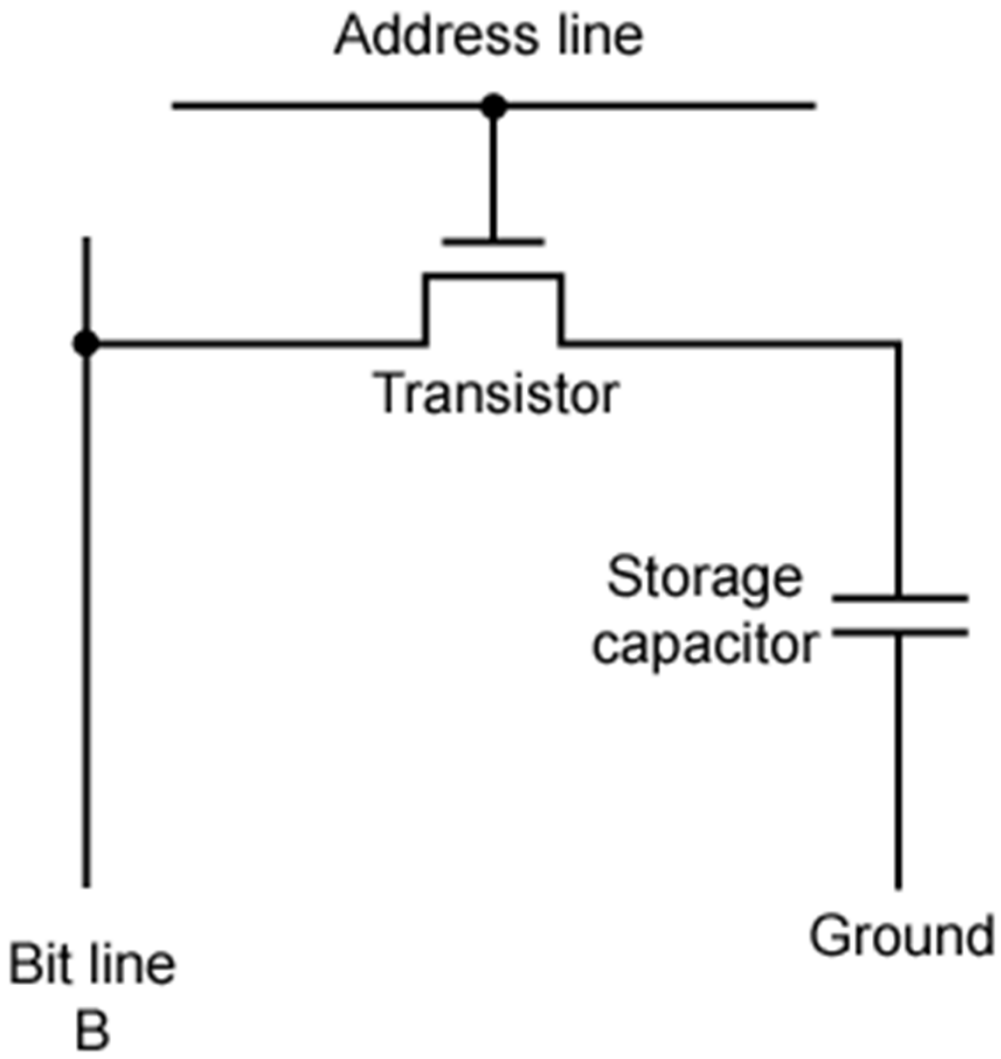
Organisation in detail



Organisation in detail

- A 16Mbit chip can be organised as 1M of 16 bit words
- A bit per chip system has 16 lots of 1Mbit chip with bit 1 of each word in chip 1 and so on
- A 16Mbit chip can be organised as a 2048 x 2048 x 4bit array
  - Reduces number of address pins
    - Multiplex row address and column address
    - 11 pins to address (2^{11}=2048)
    - Adding one more pin doubles range of values so x4 capacity

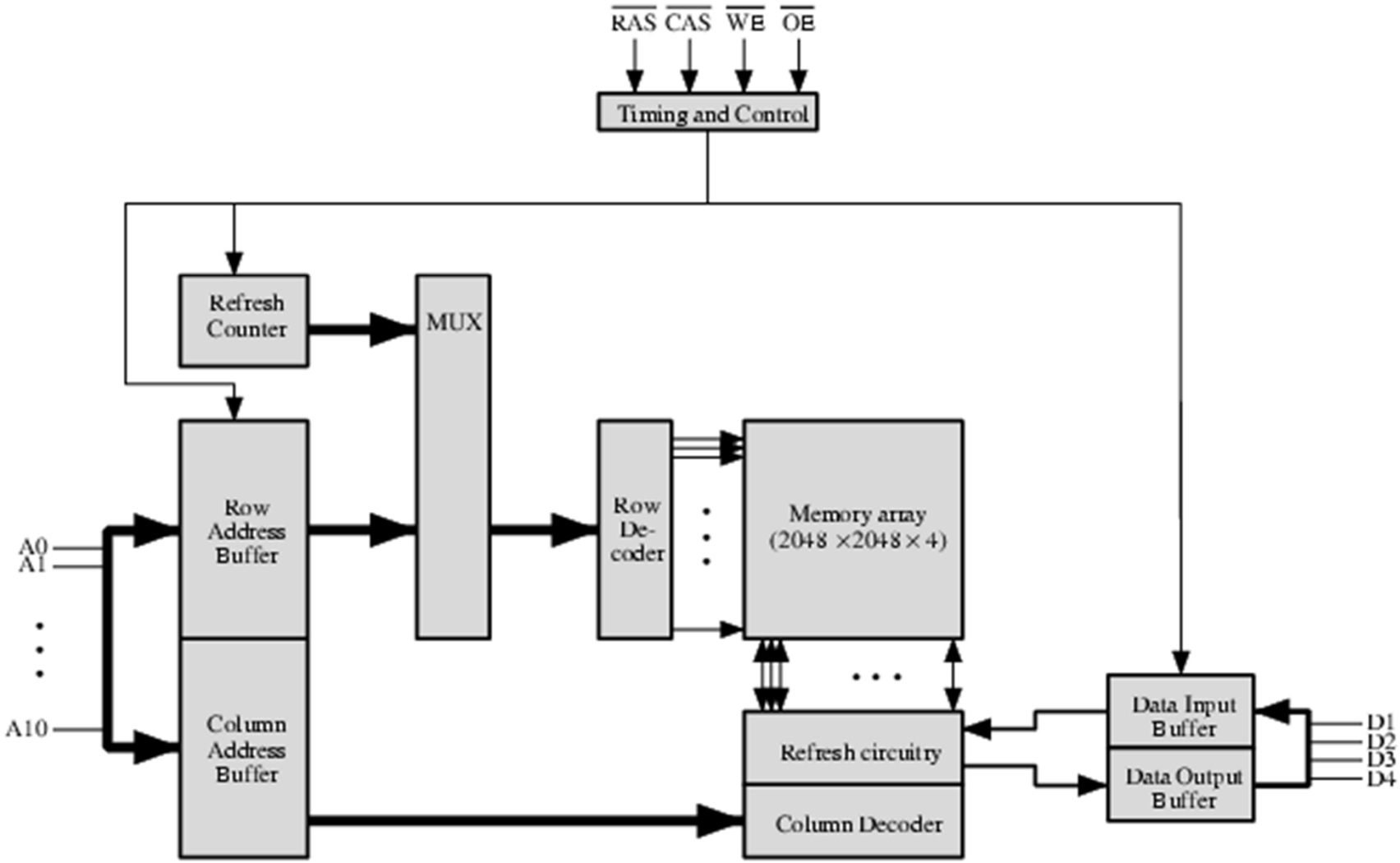
Dynamic RAM Structure



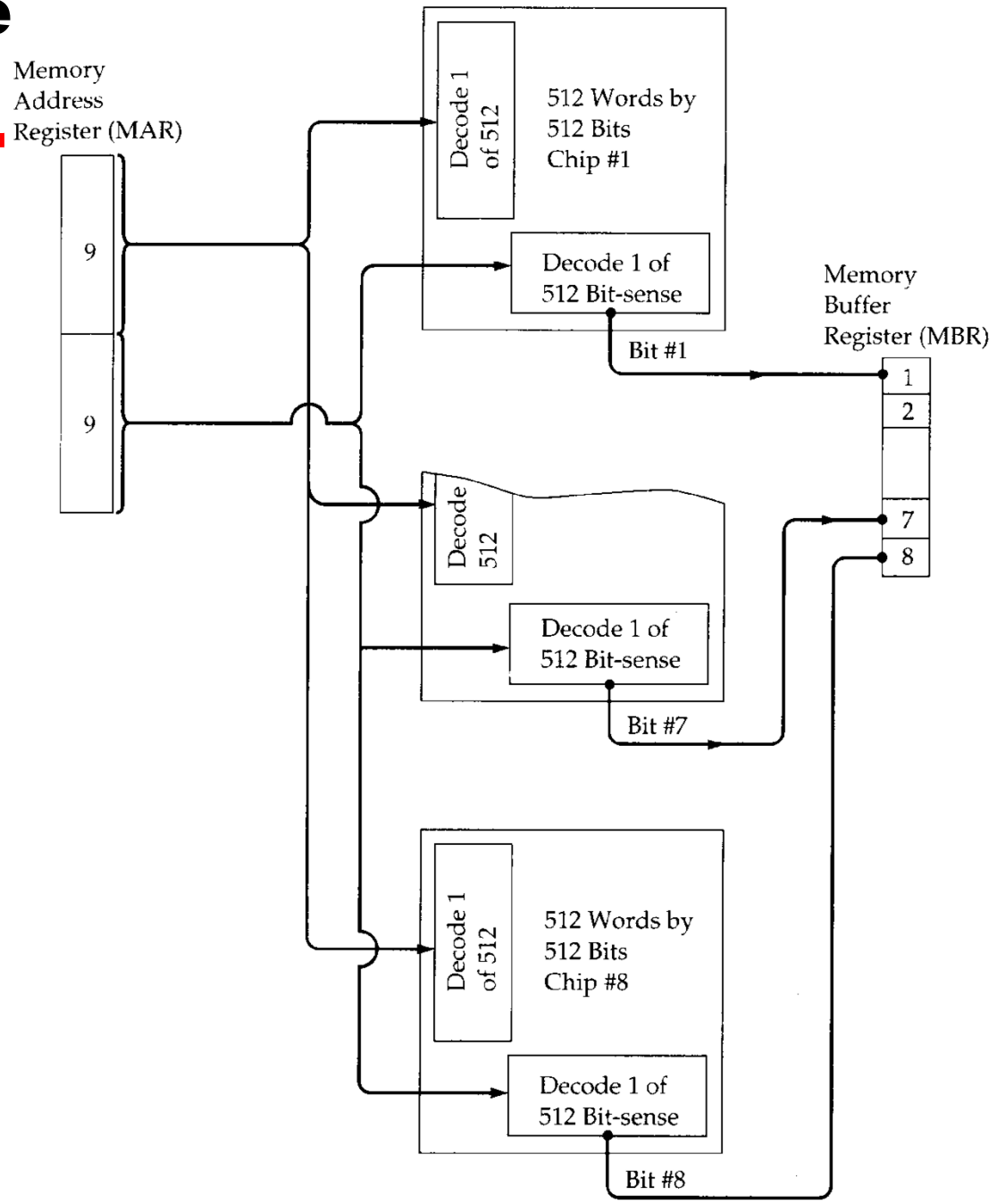
Refreshing

- Refresh circuit included on chip
- Disable chip
- Count through rows
- Read & Write back
- Takes time
- Slows down apparent performance

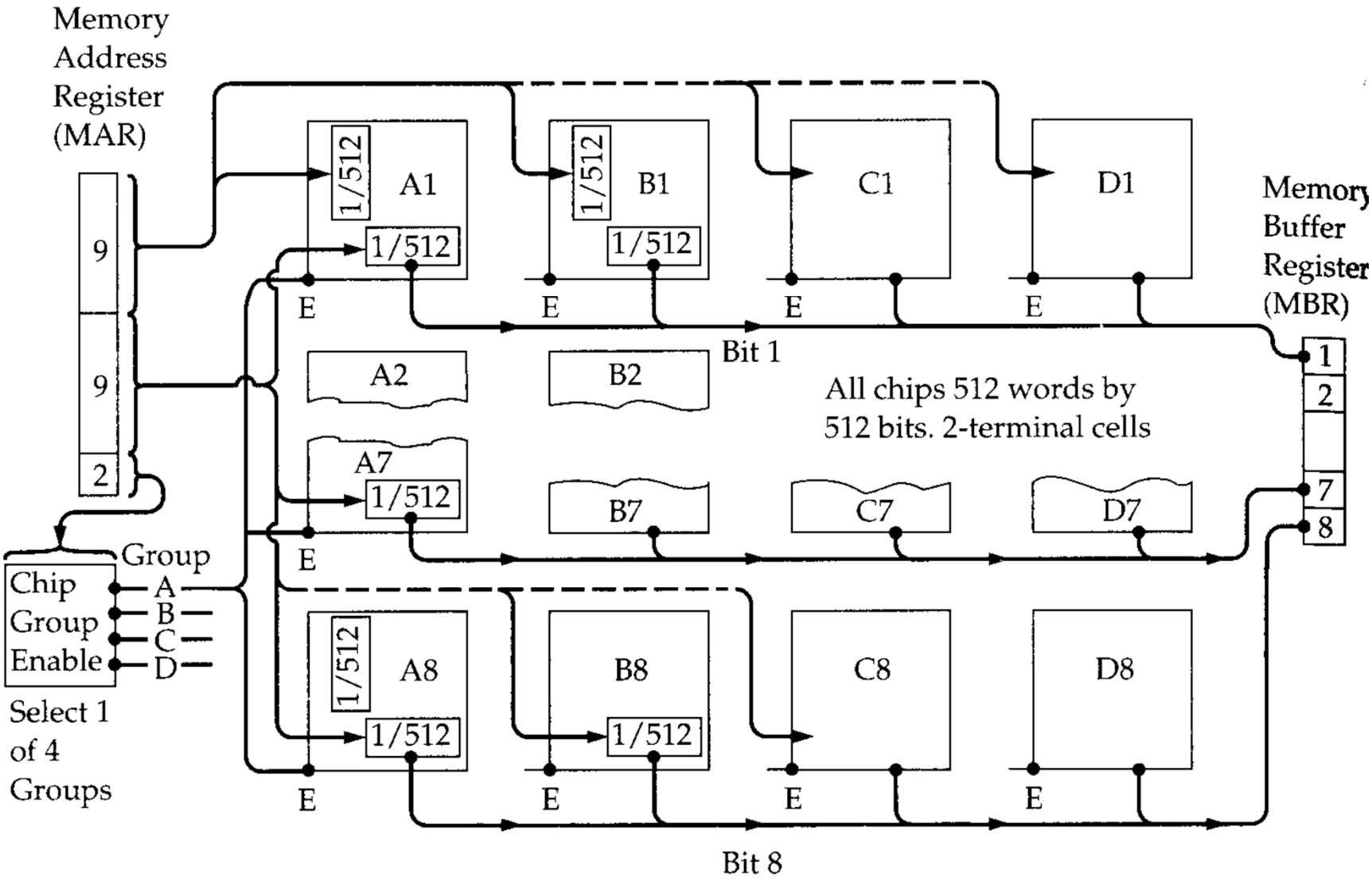
Typical 16 Mb DRAM (4M x 4)



256kByte Module Organisation



1MByte Module Organisation



Fetch Sequence (symbolic)

- t1: MAR <- (PC)
- t2: MBR <- (memory)
- PC <- (PC) +1
- t3: IR <- (MBR)

—(tx = time unit/clock cycle)

Memory Read(symbolic)

- t1: MAR <- (R1)
- t2: MBR <- (memory)
- t3: R2 <- (MBR)

  - (tx = time unit/clock cycle)

Address of the memory location is in register R1 and data to be stored in register R2

Memory Write(symbolic)

- t1: MAR <- (R1)
- t2: MBR <- (R2)
- t3: (memory) <- (MBR)
  - (tx = time unit/clock cycle)

Address of the memory location is in register R1 and data is in register R2