# SUB-20 User Manual

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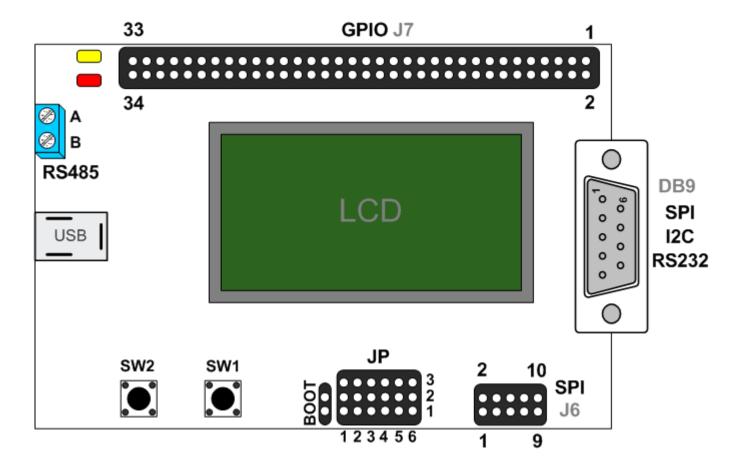
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### **Document Revision History** 1

- 2.9
- 1. sub\_spi\_transfer\_ess
- 2.8
- 1. GPIOB
- 2. FIFO\_READ\_FULL
- 3. MDIO1
- 2.7
- Bit-bang I2C Masters
   Updated GPIO Header for I2Cx, SPIx, UARTx

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# 2 SUB-20 Layout



SUB-20 SUB-20 Layout

### 2.1 GPIO Header

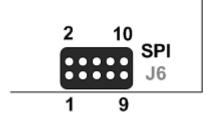
6

Header Pin	GPIO	Alternative Function Notes	
1	GPIO8	I2C SCL	Pulled up 1.5KOhm DB9.8
2	GPIO9	I2C SDA	Pulled up 1.5KOhm DB9.6
3	GPIO10	RS232 RXD_TTL	For Configurations with RS232 or RS485
4	GPIO11	RS232 TXD_TTL	
5	GPIO12		
6	GPIO13		
7	GPIO14	MDC	
8	GPIO15	MDIO	
9	GPIO24	PWM_0, SCLx0, MISOx0 <sup>1</sup>	
10	GPIO25	PWM_1, SDAx0, MOSIx0 <sup>1</sup>	
11	GPIO26	PWM_2, SCLx1, SCKx0 <sup>1</sup>	
12	GPIO27	PWM_3, SDAx1, SSx0 <sup>1</sup>	
13	GPIO28	PWM_4, SCLx2, MISOx1 <sup>1</sup> , UARTx0_RX <sup>1</sup>	
14	GPIO29	PWM_5, SDAx2, MOSIx1 <sup>1</sup> , UARTx0_TX <sup>1</sup>	
15	GPIO30	PWM_6, SCLx3, SCKx1 <sup>1</sup> , UARTx1_RX <sup>1</sup>	
16	GPIO31	PWM_7, SDAx3, SSx1 <sup>1</sup> , UARTx1_TX <sup>1</sup>	
17	GPIO0	LCD_D0	For Configurations with LCD
18	GPIO1	LCD_D1	
19	GPIO2	LCD_D2	
20	GPIO3	LCD_D3	
21	GPIO4	IR_TX	For Configurations with IR
22	GPIO5		
23	GPIO6	LCD_En	For Configurations with LCD
24	GPIO7	LCD_RS	
25	GPIO23	ADC7	
26	GPIO22	ADC6	
27	GPIO21	ADC5	
28	GPIO20	ADC4	
29	GPIO19	ADC3	
30	GPIO18	ADC2	
31	GPIO17	ADC1	
32	GPIO16	ADC0	
33		VCC	
34		GND	

<sup>&</sup>lt;sup>1</sup> - Under development

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### 2.2 SPI Header

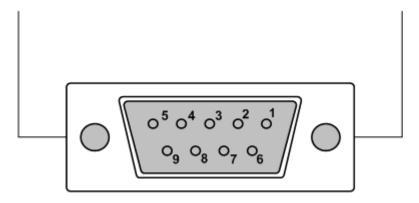


Header Pin	SPI Function	Fast PWM	GPIOB	MDIO1	Notes
1	MOSI - Master Out Slave In		GPIOB1	MDC1	Optional Level Converter*
2	SS1		GPIOB0		GPIO Voltage**
3	MISO - Master In Slave Out		GPIOB3		Optional Level Converter*
4	SS2	FPWM_0	GPIOB2		GPIO Voltage**
5	SS0		GPIOB5		Output,Optional Level Converter*
6	SS3	FPWM_1	GPIOB4		GPIO Voltage**
7	SCK - Master Clock		GPIOB7	MDIO1	Optional Level Converter*
8	SS4	FPWM_2	GPIOB6		GPIO Voltage**
9	SPI_EXT_PWR - External SPI Power		EXT_PWR		
10	GND		GND		

Level Converter\* - Adjustable operating voltage in configurations with Level Converters (see <u>Jumpers</u> and <u>Ordering Information</u>).

GPIO Voltage\*\* - Operates at the same voltage as GPIO according to SUB-20 configuration (see <u>Ordering Information</u>).

### 2.3 DB9 Connector

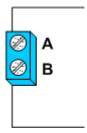


Pin	Function	Configuration
1	SPI SS0	
2	I2C_EXT_PWR	
	RS232 PC_RX	Serial2
3	SPI_EXT_PWR	Lxxx

SUB-20 SUB-20 Layout

	RS232 PC_TX	Serial2
4	SPI SCK	
5	GND	
6	I2C SDA	
7	SPI MISO	
8	I2C SCL	
9	SPI MOSI	

### 2.4 RS485 Connector

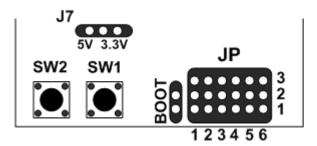


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RS485 Connector is installed only in Serial4 configuration.

Pin	Function		
Α	inverting or '-' pin		
В	non-inverting or '+' pin		

## 2.5 Jumpers, SW1,SW2



SUB-20 SUB-20 Layout

	IOC Dull and Valte as when IDO 4.0	1-2	3.3V	
JP1	I2C Pull-ups Voltage when JP2 1-2 closed	2-3	5V	Should not be used with 3.3V configurations
		1-2	Internal	
JP2	I2C Pull-ups Voltage	2-3	External DB9.2	Can not be used in Serial configurations
JP3	SCL Pull-up	1-2	On	
JF3	SCL Pull-up	2-3	Off	
JP4	SDA Pull-up	1-2	On	
		2-3	Off	
JP5	SPI Voltage when JP6 1-2 closed	1-2	3.3V	
JFS		2-3	5V	
		1-2	Internal	
JP6	SPI Voltage	2-3	External J6.9 or DB9.3	Only for Lxxx configurations. DB9.3 Can not be used as SPI Voltage in Serial configurations
J7	GPIO Voltage	left	5V	
] ]/		rigth	3.3V	
BOOT, SW1		Closed		
	Force Bootloader on Power Reset	or		
		Pressed		
SW2	Force Monitor on Power Reset	Pressed		Only for Serial2 configurations

For additional information about SUB-20 configurations please see Ordering Information.

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## 3 SUB-20 API

### **API Function List**

sub\_find\_devices

sub open

sub\_get\_serial\_number

sub\_get\_product\_id

sub\_get\_version

sub\_i2c\_freq

sub\_i2c\_config

sub\_i2c\_start

sub\_i2c\_stop

sub\_i2c\_scan

sub\_i2c\_read

sub\_i2c\_write

sub\_bb\_i2c\_config

sub\_bb\_i2c\_scan

sub\_bb\_i2c\_read

sub\_bb\_i2c\_write

sub\_spi\_config

sub\_spi\_transfer

sub\_gpio\_config

sub\_gpio\_read

sub\_gpio\_write

sub\_fpwm\_config

sub\_fpwm\_set

sub\_adc\_config

sub\_adc\_read

sub\_adc\_single

sub\_lcd\_write

sub\_rs\_set\_config

sub\_rs\_get\_config

sub\_rs\_timing

sub\_rs\_xfer

sub\_fifo\_config

sub\_fifo\_read

sub\_fifo\_write

### 3.1 Device Initialization

#### **Functions**

```
sub_find_devices
sub_open
sub_get_serial_number
sub_get_product_id
```

### 3.1.1 sub\_find\_devices

#### **Synopsis**

```
sub_device sub_find_devices( sub_device first )
```

Function scans USB devices currently connected to the host looking for SUB-20 device(s). If parameter *first* is NULL function will initiate new search, otherwise it will continue to search from the place it finished during last call.

#### Return value

Function returns next found SUB-20 device descriptor or NULL if no more devices were found. Returned value can be used as parameter for <a href="sub\_open">sub\_open</a>. Device descriptor is not a device handle required by API calls. Handle is returned by <a href="sub\_open">sub\_open</a>.

### **Example**

```
sub_device dev=0;
while( dev = sub_find_devices(dev) )
{
    /* Check device serial number */
}
```

### 3.1.2 **sub\_open**

### **Synopsis**

```
sub_handle sub_open( sub_device dev )
```

Open SUB-20 device. If parameter **dev** is NULL function will try to open first available SUB-20 device. In this case it will call internally <u>sub\_find\_devices(0)</u>. Otherwise function will try to open SUB-20 device referenced by **dev**. If your application intended to work with single SUB-20 device you can always call sub\_open with **dev** = NULL.

### Return value

On success function returns non zero handler that should be used in all subsequent calls to SUB-20 API functions. In case of error function returns NULL and set <a href="mailto:sub\_errno">sub\_errno</a>

### **Example**

```
handle = sub_open( 0 );
if( !handle )
{
    printf("sub_open: %s\n", sub_strerror(sub_errno));
    return -1;
}
```

### 3.1.3 sub\_get\_serial\_number

#### **Synopsis**

```
int sub get serial number( sub handle hndl, char *buf, int sz)
```

Get serial number string descriptor

#### **Parameters**

- \*buf buffer to store descriptor
- sz buffer size

### Return value

On success function returns string descriptor size. Otherwise negative number.

#### Example

```
if( sub_get_serial_number(hndl, buf, sizeof(buf)) >= 0 )
    printf( "Serial Number : %s\n", buf );
else
{
    /* Error */
}
```

### 3.1.4 sub\_get\_product\_id

### **Synopsis**

```
int sub_get_product_id( sub_handle hndl, char *buf, int sz);
```

Get product ID string descriptor

### **Parameters**

- \*buf buffer to store descriptor
- sz buffer size

### Return value

On success function returns string descriptor size. Otherwise negative number.

### Example

```
if( sub_get_product_id(hndl, buf, sizeof(buf)) >= 0 )
    printf( "Product ID : %s\n", buf );
else
{
    /* Error */
}
```

### 3.1.5 sub\_get\_version

#### **Synopsis**

```
const struct sub_version* sub_get_version( sub_handle hndl );
```

Get version of shared (DLL) or static library, driver, SUB-20 device and bootloader.

#### Return value

Function fills internal structure with gathered versions and returns pointer to this structure.

### Example

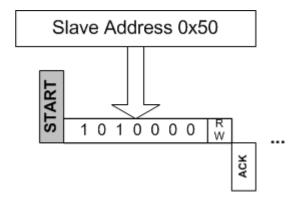
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```
const struct sub_version* sub_ver;
sub_ver = sub_get_version( hndl );
```

### 3.2 I2C functions

### **Slave Address Convention**

Slave address parameter referenced in I2C related functions is 7 bit number representing I2C slave device address without R/W bit. For example with slave address parameter equal 0x50 slave address stage of the I2C transaction will look like:



### **Acknowledge Polling**

I2C EEPROM slave devices may enter internal memory write cycle. Once the internally-timed write cycle has started EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device slave address and R/W bit. Only if the internal write cycle has completed will the EEPROM respond with an ACK, allowing the read or write sequence to continue. Acknowledge polling should be performed on application level. SUB-20 knows nothing about nature of I2C slave device it is connected to.

### **EEPROM Page Write**

I2C EEPROMs are usually capable of no more then 64-byte page writes. The internal EEPROM data address lower 6 bits are internally incremented following the receipt of each data byte. The higher data address bits are not incremented, retaining the memory page row location. When the data address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data bytes are transmitted to the EEPROM, the data address will "roll over" and previous data will be overwritten. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

#### **Functions**

sub\_i2c\_freq

sub\_i2c\_config

sub\_i2c\_start

sub i2c stop

sub\_i2c\_read

sub i2c write

SUB-20 can work in both I2C master and I2C slave modes. Detailed description of I2C slave mode can be found here: SUB-20 as I2C Slave.

### 3.2.1 **sub\_i2c\_freq**

#### **Synopsis**

```
int sub_i2c_freq( sub_handle hndl, int* freq )
```

Set and get SUB-20 I2C master clock frequency. If \*freq is non zero I2C clock frequency will be set to value equal or close to \*freq. SUB-20 has I2C frequency generator that can generate clock frequencies in range form 444,444 KHz down to 489 Hz. Function will calculate close possible frequency from the available range. If function succeed \*freq will reflect the resulting I2C clock frequency. Some of available I2C clock frequencies are listed below

```
444444 Hz (Maximal)
421052 Hz
400000 Hz
...
100000 Hz
...
491 Hz
489 Hz (Minimal)
```

#### **Parameters**

\*freq - Desired frequency or zero. On return will be filled with resulting frequency

### Return value

On success function returns 0. Otherwise error code.

### 3.2.2 sub i2c config

#### **Synopsis**

```
int sub_i2c_config( sub_handle hndl, int sa, int flags )
```

Configure SUB-20 I2C module.

#### **Parameters**

- sa slave address for SUB-20 in I2C slave mode. See <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Slave Address Convention">I2C Slave Address Convention</a> and <a href="I2C Sl
- flags set of below flags

I2C GCE

Enable general call address (0x00) detection in I2C slave mode

### Return Value

On success function returns 0. Otherwise error code.

### 3.2.3 sub\_i2c\_start

### **Synopsis**

```
int sub_i2c_start( sub_handle hndl )
```

Generate I2C start condition.

#### Return value

On success function returns 0. Otherwise error code.

### See also

Error Codes, I2C Status

### 3.2.4 **sub\_i2c\_stop**

#### **Synopsis**

```
int sub_i2c_stop( sub_handle hndl )
```

Generate I2C stop condition.

#### Return value

On success function returns 0. Otherwise error code.

#### See also

Error Codes, I2C Status

### 3.2.5 sub\_i2c\_scan

### **Synopsis**

```
int sub_i2c_scan( sub_handle hndl, int* slave_cnt, char* slave_buf )
```

Scan I2C bus looking for connected slave devices.

#### **Parameters**

- \*slave cnt Buffer to store number of found slave devices
- slave\_buf Buffer to store found <u>slave device addresses</u>

#### Return value

On success function returns 0. Otherwise error code.

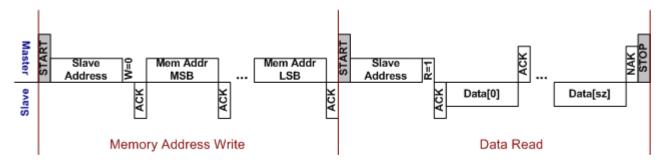
### See also

Error Codes, I2C Status

### 3.2.6 sub\_i2c\_read

#### **Synopsis**

Perform complete I2C master read transaction with optional memory address write. Transaction will have following format:



If **ma\_sz** is zero "Memory Address Write" stage will be skipped.

Function has no limitation of the read data size - sz parameter. However internal organization of the I2C slave

device being read should be considered.

### **Parameters**

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- sa Slave Address
- ma Memory Address. Will be shifted out in "Memory Address Write" stage MSB first
- ma\_sz Memory Address size bytes
- buf Buffer to store read data
- sz Read data size bytes.

#### Return value

On success function returns 0. Otherwise error code.

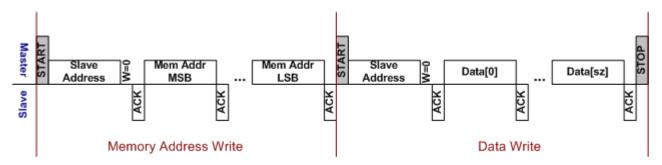
### See also

Error Codes, I2C Status

### 3.2.7 sub i2c write

### **Synopsis**

Perform complete I2C master write transaction with optional memory address write. Transaction will have following format:



If ma\_sz is zero "Memory Address Write" stage will be skipped.

Function has no limitation of the write data size - **sz** parameter. However internal organization of the I2C slave device being written should be considered especially <u>Acknowledge Polling</u> and <u>EEPROM Page Write</u>.

### **Parameters**

- sa Slave Address
- ma Memory Address. Will be shifted out in "Memory Address Write" stage MSB first
- ma\_sz Memory Address size bytes
- buf Buffer for data to be written
- sz Write data size bytes

#### Return value

On success function returns 0. Otherwise error code.

### See also

Error Codes, I2C Status

### 3.2.8 I2C Status

The status of last I2C operation successful or not successful is stored in **sub\_i2c\_status** global variable defined in *libsub.h* as

extern int sub\_i2c\_status;

Following statuses are available:

No errors
START condition transmitted
Repeated START condition transmitted
SLA+W transmitted; ACK received
SLA+W transmitted; NAK received
Data byte transmitted; ACK received
Data byte transmitted; NAK received
Arbitration lost in SLA; or NAK received
SLA+R transmitted; ACK received
SLA+R transmitted; NAK received
Data received; ACK has been returned
Data received; NAK has been returned
Arbitration lost
Arbitration lost in START
Arbitration lost in STOP
Arbitration lost in read ACK
Arbitration lost in read NAK
Arbitration lost in write
Unknown error
Illegal START or STOP condition

### 3.3 Bit-bang I2C Masters

Beginning from the FW version 0.2.6 and library version 0.1.12.16, SUB-20 provides additional four independent I2C master channels on GPIO24..31 compatible with I2C specification 3.0.

<b>Header Pin</b>	GPIO	Alternative I2C Master Function
9	GPIO24	SCLx0
10	GPIO25	SDAx0
11	GPIO26	SCLx1
12	GPIO27	SDAx1
13	GPIO28	SCLx2
14	GPIO29	SDAx2
15	GPIO30	SCLx3
16	GPIO31	SDAx3

Each channel can operate in Fast Plus (1000KHz), Fast (400KHz) and Standard (100KHz) modes. In Fast and Standard modes I2C masters support clock stretching.

#### SDAx, SCLx Pull-ups

Considering the fact that bit-bang I2C channels share the GPIO pins with other SUB-20 modules, there are no internal (mounted on SUB-20 board) pull-ups on these channels. **Pull-ups must be provided on target board**.

### **Clock Stretching**

In Fast and Standard modes bit-bang I2C masters support clock stretching. Clock stretching pauses a transaction by holding the SCL line LOW. The transaction cannot continue until the line is released HIGH again. Slaves can hold the SCL line LOW to force the master into a wait state until the slave is ready.

### **Functions**

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sub bb i2c config sub bb i2c scan sub bb i2c read sub bb i2c write

### 3.3.1 sub\_bb\_i2c\_config

#### **Synopsis**

```
int sub_bb_i2c_config( sub_handle hndl, int mode, int stretch_ms )
```

Configure SUB-20 Bit-bang I2C Masters module. Configuration is common for all Bit-bang I2C channels.

### **Parameters**

• mode - Bit-bang I2C Master mode. One of the following flags:

BB\_I2C\_FAST\_P Fast Plus mode 1000KHz
BB\_I2C\_FAST Fast mode 400KHz
BB\_I2C\_STD Standard mode 100KHz

• stretch\_ms - Clock stretching timeout up to 4194ms. Clock stretching feature is available in Fast and Standard modes. If SCL line is hold LOW by I2C slave device longer than **stretch\_ms** timeout, Bit-bang I2C function will fail and I2C Status will be set to 0xE0.

#### **Return Value**

On success function returns 0. Otherwise error code.

### Compatibility

FW version 0.2.6 or grater Library version 0.1.12.16 or grater

### 3.3.2 sub\_bb\_i2c\_scan

#### **Synopsis**

Scan I2C bus looking for connected slave devices.

### **Parameters**

- channel Bit-bang I2C Master channel 0..3
- \*slave\_cnt Buffer to store number of found slave devices
- slave\_buf Buffer to store found slave device addresses

### Return value

On success function returns 0. Otherwise error code.

#### See also

Error Codes, I2C Status

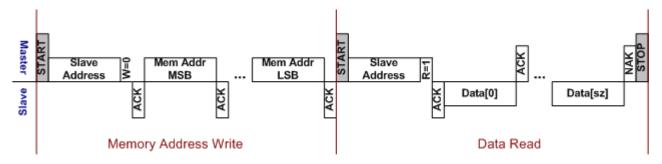
### Compatibility

FW version 0.2.6 or grater Library version 0.1.12.16 or grater

### 3.3.3 sub\_bb\_i2c\_read

#### **Synopsis**

Perform complete I2C master read transaction with optional memory address write. Transaction will have following format:



If ma\_sz is zero "Memory Address Write" stage will be skipped.

Function has no limitation of the read data size - **sz** parameter. However internal organization of the I2C slave device being read should be considered.

#### **Parameters**

- channel Bit-bang I2C Master channel 0..3
- sa Slave Address
- ma Memory Address. Will be shifted out in "Memory Address Write" stage MSB first
- ma\_sz Memory Address size bytes
- buf Buffer to store read data
- sz Read data size bytes.

#### Return value

On success function returns 0. Otherwise error code.

### See also

Error Codes, I2C Status

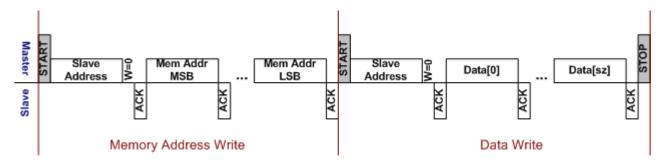
### Compatibility

FW version 0.2.6 or grater Library version 0.1.12.16 or grater

### 3.3.4 sub bb i2c write

### **Synopsis**

Perform complete I2C master write transaction with optional memory address write. Transaction will have following format:



If ma\_sz is zero "Memory Address Write" stage will be skipped.

Function has no limitation of the write data size - **sz** parameter. However internal organization of the I2C slave device being written should be considered especially Acknowledge Polling and EEPROM Page Write.

### **Parameters**

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- channel Bit-bang I2C Master channel 0..3
- sa Slave Address
- ma Memory Address. Will be shifted out in "Memory Address Write" stage MSB first
- ma\_sz Memory Address size bytes
- buf Buffer for data to be written
- sz Write data size bytes

### Return value

On success function returns 0. Otherwise error code.

### See also

Error Codes, I2C Status

### Compatibility

FW version 0.2.6 or grater Library version 0.1.12.16 or grater

### 3.4 SPI Functions

### **SPI Pins Configuration**

After SPI is enabled SUB-20 SPI module will take control over SPI pins.

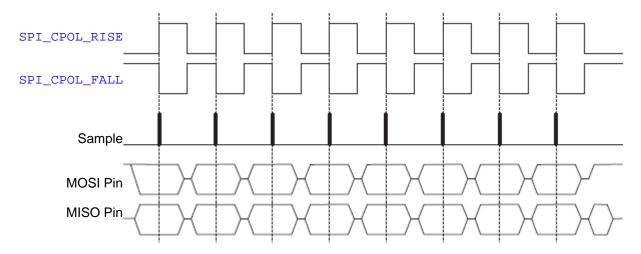
Pin	Function	Master mode	Slave mode	Disabled
SCK	SPI Master Clock	Output	Input	
MOSI	Master Out Slave In	Output	Input	
MISO	Master In Slave Out	Input	Output**	
SS0	Slave Select 0	Output Hi (Configurable by sub_spi_transfer)	Input	HiZ
SS1 SS2 SS3 SS4	Slave Select 14	HiZ (Configurable by sub_spi_transfer)	Not in use	

<sup>\*</sup>If SPI is disabled all SPI pins are in HiZ.

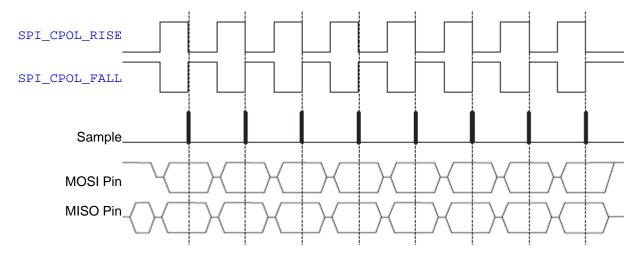
### **SPI SCK Polarity and Phase explanations**

<sup>\*\*</sup> In SPI slave mode MISO is output only when SS0 is low





### SPI Transfer format with SPI\_SETUP\_SMPL



### **Functions**

sub\_spi\_config
sub\_spi\_transfer
sub\_sdio\_transfer

### 3.4.1 sub\_spi\_config

### **Synopsis**

```
int sub_spi_config( sub_handle hndl, int cfg_set, int* cfg_get )
```

Configure SUB-20 SPI module or read current configuration. If \*cfg\_get is NULL function will configure SPI according to the cfg\_set parameter. Otherwise it will read current SPI configuration into \*cfg\_get

### **Parameters**

• cfg\_set - Desired SPI configuration. This parameter is effective only if \*cfg\_get is NULL. cfg\_set should be assembled as a combination of below flags

SPI_ENABLE	Enable SUB-20 SPI module.
SPI_SLAVE	SPI module is in Slave mode. <a href="mailto:sub_spi_transfer">spi_transfer</a> can work only when SPI module is in Master mode
SPI_CPOL_RISE	SCK is low when idle. See SPI Polarity and Phase explanations
SPI_CPOL_FALL	SCK is high when idle. See SPI Polarity and Phase explanations
SPI_SMPL_SETUP	Sample data on leading SCK edge, setup on trailing. See <u>SPI Polarity and Phase explanations</u>
SPI_SETUP_SMPL	Setup data on leading SCK edge, sample on trailing. See <u>SPI Polarity and Phase explanations</u>

Below flags are relevant only for SPI master mode (SPI\_SLAVE not set)

Transmit LSB first
Transmit MSB first
SPI SCK frequency 8 MHz
SPI SCK frequency 4 MHz
SPI SCK frequency 2 MHz
SPI SCK frequency 1 MHz
SPI SCK frequency 500 KHz
SPI SCK frequency 250 KHz
SPI SCK frequency 125 KHz

• \*cfg\_get - Pointer to store current configuration read from SUB-20 device or NULL

### Return value

On success function returns 0. Otherwise error code.

### Example

```
/* Read current SPI configuration */
sub_spi_config( hndl, 0, &spi_config );

/* Configure SPI */
sub_spi_config( hndl,
SPI_ENABLE|SPI_CPOL_RISE|SPI_SMPL_SETUP|SPI_MSB_FIRST|SPI_CLK_4MHZ, 0 );

/* Disable SPI */
sub_spi_config( hndl, 0, 0 );
```

### 3.4.2 sub\_spi\_transfer

#### **Synopsis**

Perform SPI master transaction. Depending on **out\_buf** and **in\_buf** parameters transaction can be either read ( **out buf**==0), write (**in buf**==0) or read-write ( both **in buf** and **out buf** are non zero).

#### **Parameters**

- out\_buf Output data buffer or NULL. If NULL there will be no write transaction and MOSI pin will stay unchanged.
- in\_buf Input buffer to store read data or NULL. If NULL there will be no read transaction and data on MISO pin will be ignored.
- sz Transaction size
- ss\_config Determines selection and operation of SS pin. ss\_config value must be created with macro SS CONF(SS N.SS MODE) ,

where **SS\_N** is SS pin number and **SS\_MODE** is one of the following flags:

```
SS H
                SS goes high and stays high during and after transaction
SS HL
                SS goes high and stays high during first byte transfer, after that it goes low
SS_HHL
                SS goes high and stays high during first 2 bytes transfer, after that it goes low
SS HHHL
                SS goes high and stays high during first 3 bytes transfer, after that it goes low
SS HHHHL
                SS goes high and stays high during first 4 bytes transfer, after that it goes low
SS HI
                SS goes high and stays high during entire transfer, after that it goes low
SS L
                SS goes low and stays low during and after transaction
SS LH
                SS goes low and stays low during first byte transfer, after that it goes high
SS LLH
                SS goes low and stays low during first 2 bytes transfer, after that it goes high
SS LLLH
                SS goes low and stays low during first 3 bytes transfer, after that it goes high
SS LLLLH
                SS goes low and stays low during first 4 bytes transfer, after that it goes high
SS LO
                SS goes low and stays low during entire transfer, after that it goes high
SS HiZ
                SS stays in HiZ mode (Except SS0)
```

#### 55\_HIZ 55 stays III FIZ IIIoue (Except 550)

If **ss\_config** is zero there will be no SS activity (changes).

#### Return value

On success function returns 0. Otherwise error code.

#### **Example**

```
/* Write 10 bytes. Use SS0 low */
rc = sub_spi_transfer( hndl, out, 0, 10, SS_CONF(0,SS_LO) );
/* Transfer 10 bytes out and 10 bytes in. Use SS2 high */
rc = sub_spi_transfer( hndl, out, in, 10, SS_CONF(2,SS_HI) );
/* Read 10 bytes. No SS */
rc = sub_spi_transfer( hndl, 0, in, 10, 0 );
```

### 3.4.3 sub\_spi\_transfer\_ess

#### **Synopsis**

Perform SPI master transaction with Extended Slave Select control (ESS). Depending on **out\_buf** and **in\_buf** parameters transaction can be either read (**out\_buf**==0), write (**in\_buf**==0) or read-write (both **in\_buf** and **out\_buf** are non zero).

#### **Parameters**

- out\_buf Output data buffer or NULL. If NULL there will be no write transaction and MOSI pin will stay unchanged.
- in\_buf Input buffer to store read data or NULL. If NULL there will be no read transaction and data on MISO pin will be ignored.
- sz Transaction size
- ess\_str string defining SS selection and activity during SPI transfer. Characters of the ess\_str have following meaning
  - 0 Select SS0
    1 Select SS1
    2 Select SS2
    3 Select SS3
    4 Select SS4
    H SS High
    L SS Low

H SS High Byte Transfer
L SS Low Byte Transfer

No Byte Transfer
V SS Low No Byte Transfer
V SS Low No Byte Transfer
Small delay without SS changes No Byte Transfer

### Return value

On success function returns 0. Otherwise error code.

#### **Example**

```
/* Write 5 bytes with SSO Low. Make SSO High to Low pulse after each byte */
rc = sub_spi_transfer( hndl, out, 0, 5, "OL^-vL^-vL^-vL^-vL^-vL^-v" );

/* Transfer 10 bytes with SS High. Use SS1 for first 5 bytes and SS2 for last */
rc = sub_spi_transfer( hndl, out, in, 10, "1HHHHHHV-2HHHHHHV" );

/* Read 10 bytes. SSO High for first 2 bytes and low after that */
rc = sub_spi_transfer( hndl, 0, in, 10, "OHHV" );
```

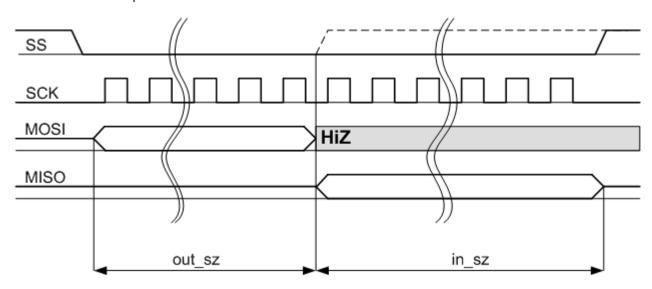
### Compatibility

FW version 0.2.9 or grater Library version 0.1.12.19 or grater

### 3.4.4 sub\_sdio\_transfer

### **Synopsis**

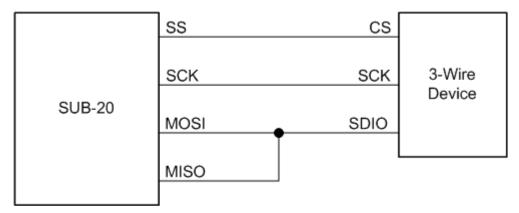
Perform 3-Wire compatible SPI master transaction like one shown below.



- 1. SS changes according to **ss\_config** parameter.
- 2. out\_sz bytes are transmitted via MOSI. MOSI will be in output state during transfer.
- 3. MOSI state is changed to HiZ after last bit transmitted. If required SS changes.
- 4. in\_sz bytes received from MISO input. MOSI left in HiZ state.
- 5. SS changes according to ss\_config parameter

SPI Clock - SCK phase and polarity can be configured with sub\_spi\_config.

Above implementation of SPI transaction allows using of the SUB-20 as 3-Wire SPI master. In this case connection to 3-Wire device should be as following:



#### **Parameters**

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- out\_buf Output data buffer.
- in\_buf Input buffer to store read data.
- out\_sz Number of bytes to transmit in range 0..60.
- in\_sz Number of bytes to receive in range 0..60.
- ss\_config Determines selection and operation of SS pin. ss\_config value must be created with macro SS\_CONF(SS\_N,SS\_MODE) ,

where **SS\_N** is SS pin number and **SS\_MODE** is one of the following flags:

SS\_HL SS goes high and stays high during transmit stage, after that it goes low

SS_HI	SS goes high and stays high during entire transaction (transmit and receive), after that it goes low
SS_LH SS_LO	SS goes low and stays low during transmit stage, after that it goes high SS goes low and stays low during entire transaction (transmit and receive), after that it goes high
SS_HiZ If <b>ss_config</b> is	SS stays in HiZ mode (Except SS0) zero there will be no SS activity (changes).

#### Return value

On success function returns 0. Otherwise error code.

#### Example

```
/* Transmit one byte and receive 3 bytes */
/* SS1 goes low during transaction */
sub_sdio_transfer( hndl, out_buf, in_buf, 1, 3, SS_CONF(1,SS_LO) );
```

### Compatibility

FW version 0.1.9 or grater Library version 0.1.12.11 or grater

### 3.5 MDIO Functions

MDIO is a Management Data Input/Output Interface defined in IEEE 802.3 Clause 22 and extended in Clause 45. It is two signal based interface between Station Management (SUB-20 in our case) and a Physical Layer device (PHY). Where a PHY, or grouping of PHY's, is an individually manageable entity, known as an MDIO Manageable Device (MMD).

### **Signals**

- MDC management data clock. MDC is sourced by SUB-20 to the PHY as the timing reference for transfer of information on the MDIO signal.
- MDIO management data input/output. MDIO is a bidirectional signal between PHY and the SUB-20 It is used to transfer control information and status between the PHY and the SUB-20. Control information is driven by the SUB-20 synchronously with respect to MDC and is sampled synchronously by the PHY. Status information is driven by the PHY synchronously with respect to MDC and is sampled synchronously by the SUB-20.

### **Frame Format**

SUB-20 supports both MDIO frame formats defined in IEEE 802.3 Clause 22 and Clause 45.

• Clause 22 MDIO frame format

READ	
WDITE	

	PREAMBLE	ST	OP	PHYAD	REGAD	TA	DATA
Г	111111	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDD
	111111	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDD

Clause 45 MDIO frame format

	PREAMBLE	ST	OP	PRTAD	DEVAD	TA	ADDRESS / DATA
Addres	111111	00	00	PPPPP	EEEEE	10	AAAAAAAAAAAAA
Write	111111	00	01	PPPPP	EEEEE	10	DDDDDDDDDDDDDD
Read	111111	00	11	PPPPP	EEEEE	ZO	DDDDDDDDDDDDDD
Post-	111111	00	10	PPPPP	EEEEE	Z0	DDDDDDDDDDDDDDD

read-increment-address

#### Channels

Beginning from FW version 0.2.8 and library version 0.1.12.18 additional MDIO1 channel is available on SPI header (see <a href="SPI Header">SPI Header</a>). To access MDIO1 channel use <a href="sub\_mdio\_xfer\_ex">sub\_mdio\_xfer\_ex</a> function with **channel**=1.

#### **Functions**

sub\_mdio22
sub\_mdio45
sub\_mdio\_xfer, sub\_mdio\_xfer\_ex

### 3.5.1 sub\_mdio22

### **Synopsis**

Generate IEEE 802.3 Clause 22 MDIO READ or WRITE frame. Frame format is shown here: <u>Clause 22 MDIO</u> frame.

#### **Parameters**

• op - operation code

SUB\_MDIO22\_READ READ operation SUB\_MDIO22\_WRITE WRITE operation

- phyad 5 bit PHY address
- regad 5 bit register address
- data 16 bit data for WRITE operation
- \*content 16 bit register content placeholder for READ operation

### Return value

On success function returns 0. Otherwise error code.

#### **Example**

```
/* Read register 0x12 in PHY 1 */
rc = sub_mdio22( hndl, SUB_MDIO22_READ, 0x01, 0x12, 0, &content );
/* Write register 0x5 in PHY 2 */
rc = sub_mdio22( hndl, SUB_MDIO22_WRITE, 0x02, 0x05, 0x55AA, 0 );
```

### Compatibility

FW version 0.2.1 or grater Library version 0.1.12.12 or grater

### 3.5.2 **sub\_mdio45**

#### **Synopsis**

Generate IEEE 802.3 Clause 45 MDIO frame. Frame format is shown here: Clause 45 MDIO frame.

#### **Parameters**

op - operation code

```
SUB_MDIO45_ADDRADDRESS operationSUB_MDIO45_WRITEWRITE operationSUB_MDIO45_PRIAPOST-READ-INCREMENT-ADDRESS operationSUB_MDIO45_READREAD operation
```

- prtad 5 bit port address
- devad 5 bit device address
- data 16 bit address or data for ADDRESS or WRITE operation
- \*content 16 bit register content placeholder for READ or POST-READ-INCREMENT-ADDRESS operation

#### Return value

On success function returns 0. Otherwise error code.

#### Compatibility

```
FW version 0.2.1 or grater
Library version 0.1.12.12 or grater
```

### 3.5.3 sub\_mdio\_xfer, sub\_mdio\_xfer\_ex

### Synopsis

Generate a sequence of independent MDIO frames. Frames in sequence can be Clause 22 or Clause 45 format with different operations and addresses.

### **Parameters**

- channel mdio channel (see MDIO Channels )
- count number of frames to generate (currently up to 15).
- \*mdios array of count sub\_mdio\_frame unions

```
union sub_mdio_frame
{
    struct
    {
        int op;
        int phyad;
        int regad;
        int data;
    }clause22;
    struct
```

```
{
    int     op;
    int     prtad;
    int     devad;
    int     data;
    }clause45;
};
```

Frame operation is defined by **op** field value.

### clause22.op can be

SUB_MDIO22_READ	<b>READ</b> operation
SUB_MDIO22_WRITE	WRITE operation

### clause45.op can be

SUB\_MDIO45\_ADDR ADDRESS operation SUB\_MDIO45\_WRITE WRITE operation

SUB\_MDIO45\_PRIA POST-READ-INCREMENT-ADDRESS operation

SUB\_MDIO45\_READ READ operation

For READ and POST-READ-INCREMENT-ADDRESS operations **clause22.data** or **clause45.data** will be filled with data read from PHY.

#### Return value

On success function returns 0. Otherwise error code.

#### Example

```
union sub_mdio_frame mdios[2];
mdios[0].clause22.op = SUB_MDIO22_READ;
mdios[0].clause22.phyad = 0x01;
mdios[0].clause22.regad = 0x12;
mdios[1].clause45.op = SUB_MDIO45_ADDR;
mdios[1].clause45.prtad = 0x04;
mdios[1].clause45.devad = 0x02;
mdios[1].clause45.data = 0x55AA;
rc = sub_mdio_xfer( hndl, 2, mdios );
```

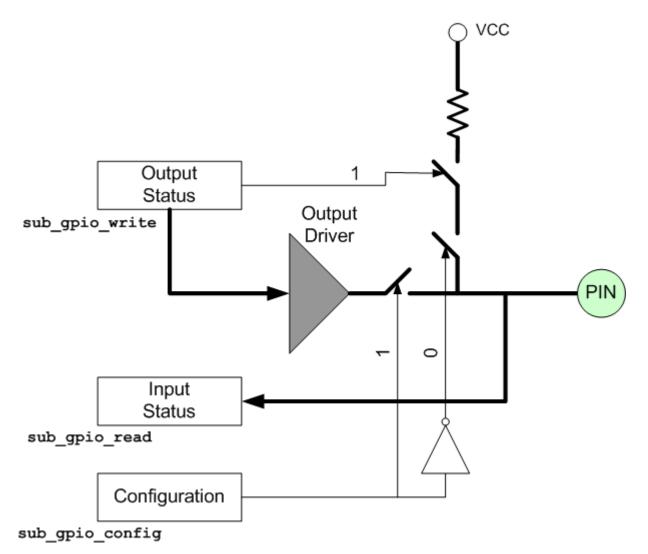
#### Compatibility

sub\_mdio\_xfer
FW version 0.2.1 or grater
Library version 0.1.12.12 or grater
sub\_mdio\_xfer\_ex
FW version 0.2.8 or grater
Library version 0.1.12.18 or grater

### 3.6 GPIO Functions

### **GPIO Functional Description**

SUB-20 GPIO can be in input or output state. GPIO state is defined by configuration bit. In output state GPIO will drive high or low level depending on output status. In input state GPIO can be pulled high by internal weak pull-up resistor.



GPIO Pin configuration

Configuration	Stata	Output Status				
Configuration	State	"0"	"1"			
"0"	Input state	HiZ	pull-up			
"1"	Output state	LOW	HIGH			

### **GPIOB**

GPIOB are located on SPI header (see <u>SPI Header</u>). GPIOB module shares I/O pins with SPI module. If SPI is enabled MISO,MOSI,SCK and SS0 pins are partially controlled by SPI module, although they can be accessed by GPIOB functions with restrictions.

Special care should be taken for SUB-Lxxx models where SPI Level Converters are installed. In this case **GPIOB pins direction should respect direction of the corresponding Level Converter** to prevent short circuit on this pins.

### **Functions**

sub gpio config
sub gpio read
sub gpio write
sub gpiob config

sub\_gpiob\_read sub\_gpiob\_write

### 3.6.1 sub\_gpio\_config

#### **Synopsis**

```
int sub_gpio_config( sub_handle hndl, int set, int* get, int mask )
```

Configure GPIO state (direction) as input or output.

#### **Parameters**

- set Bits 0..31 of **set** parameter correspond to GPIO0..GPIO31 configuration bits. If GPIOn configuration bit is "1" then GPIOn direction is output, otherwise it is input.
- \*get Pointer to store current GPIO configuration read from SUB-20.
- mask Bit in set parameter will take effect only if corresponding mask bit is "1". With mask=0 function will
  only read current GPIO configuration.

### Return value

On success function returns 0. Otherwise error code.

### Example

```
/* gpio0..6 - input, gpio7 - output */
rc = sub_gpio_config( hndl, 0x00000080, &config, 0x000000FF );
/* read gpio configuration */
rc = sub_gpio_config( hndl, 0, &config, 0 );
```

### See also

**Error Codes** 

### 3.6.2 sub\_gpio\_read

#### **Synopsis**

```
int sub_gpio_read( sub_handle hndl, int* get )
```

Read GPIO input status. Function reads logic value "1"-high, "0"-low directly from GPIO pin.

#### **Parameters**

 \*get - Pointer to store received GPIO input status. Bits 0..31 of \*get correspond to GPIO0..GPIO31 input statuses.

### Return value

On success function returns 0. Otherwise error code.

#### See also

**Error Codes** 

### 3.6.3 sub\_gpio\_write

#### **Synopsis**

```
int sub_gpio_write( sub_handle hndl, int set, int* get, int mask )
```

Set GPIO output status. For GPIO in output state function will set output driver to drive "1"-high, "0"-low. For

GPIO in input state function will "1"-enable, "0"-disable weak pull-up on corresponding GPIO pin.

### **Parameters**

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- set Bits 0..31 of **set** parameter correspond to GPIO0..GPIO31 output statuses.
- \*get Pointer to store current GPIO output status read from SUB-20.
- mask Bit in set parameter will take effect only if corresponding mask bit is "1". With mask=0 function will
  only read current GPIO output status.

#### Return value

On success function returns 0. Otherwise error code.

### See also

**Error Codes** 

### 3.6.4 sub gpiob config

### **Synopsis**

```
int sub_gpiob_config( sub_handle hndl, int set, int* get, int mask )
```

Configure GPIOB state (direction) as input or output.

#### **Parameters**

- set Bits 0..7 of **set** parameter correspond to GPIOB0..GPIOB7 configuration bits. If GPIOBn configuration bit is "1" then GPIOBn direction is output, otherwise it is input.
- \*get Pointer to store current GPIOB configuration read from SUB-20.
- mask Bit in **set** parameter will take effect only if corresponding **mask** bit is "1". With **mask**=0 function will only read current GPIOB configuration.

#### Return value

On success function returns 0. Otherwise error code.

### See also

**Error Codes** 

#### Compatibility

FW version 0.2.7 or grater Library version 0.1.12.17 or grater

### 3.6.5 sub\_gpiob\_read

### **Synopsis**

```
int sub_gpiob_read( sub_handle hndl, int* get )
```

Read GPIOB input status. Function reads logic value "1"-high, "0"-low directly from GPIOB pin.

#### **Parameters**

\*get - Pointer to store received GPIOB input status. Bits 0..7 of \*get correspond to GPIOB0..GPIOB7 input statuses.

### Return value

On success function returns 0. Otherwise error code.

### See also

**Error Codes** 

### Compatibility

FW version 0.2.7 or grater Library version 0.1.12.17 or grater

### 3.6.6 sub\_gpiob\_write

#### **Synopsis**

```
int sub_gpiob_write( sub_handle hndl, int set, int* get, int mask )
```

Set GPIOB output status. For GPIOB in output state function will set output driver to drive "1"-high, "0"-low. For GPIO in input state function will "1"-enable, "0"-disable weak pull-up on corresponding GPIOB pin.

#### **Parameters**

- set Bits 0..7 of **set** parameter correspond to GPIOB0..GPIOB7 output statuses.
- \*get Pointer to store current GPIOB output status read from SUB-20.
- mask Bit in **set** parameter will take effect only if corresponding **mask** bit is "1". With **mask**=0 function will only read current GPIOB output status.

#### Return value

On success function returns 0. Otherwise error code.

#### See also

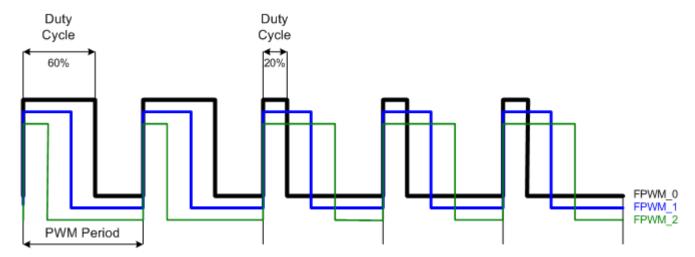
### **Error Codes**

### Compatibility

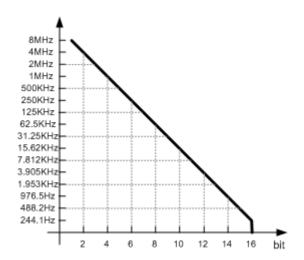
FW version 0.2.7 or grater Library version 0.1.12.17 or grater

### 3.6.7 Fast PWM

Fast PWM outputs are available on SPI header pins 4,6,8 (see <u>SPI Header</u>). Outputs are referenced as FPWM\_0, FPWM\_1 and FPWM\_2. All three outputs share the same PWM generation module in SUB-20 and have the same PWM frequency but separate duty cycle configuration.



Fast PWM frequency range is 8Mhz .. 0.238Hz. Duty cycle precision is 2..16 bits depending on the PWM frequency.



#### **Functions**

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sub\_fpwm\_config sub\_fpwm\_set

### 3.6.7.1 sub\_fpwm\_config

### **Synopsis**

```
int sub_fpwm_config( sub_handle hndl, double freq_hz, int flags )
```

Configure fast PWM module.

### **Parameters**

- freq hz Desired fast PWM frequency in Hz. Frequency can be in a range 8MHz .. 0.238Hz
- · flags Set of configuration flags listed below

FPWM\_ENABLE General fast PWM enable. If this flag is not set fast PWM module will be

disabled and FPWM outputs will go to HiZ.

FPWM\_EN0 Enable FPWM\_0 output. Otherwise FPWM\_0 will stay low. FPWM\_EN1 Enable FPWM\_1 output. Otherwise FPWM\_1 will stay low. FPWM\_EN2 Enable FPWM\_2 output. Otherwise FPWM\_2 will stay low.

### Return value

On success function returns 0. Otherwise error code.

### **Example**

```
/*
   Enable fast PWM module with FPWM_0 and FPWM_2 outputs.
   PWM frequency 10.6Hz
*/
sub_fpwm_config( hndl, 10.6, FPWM_ENABLE|FPWM_EN0FPWM_EN2 );
```

### See also

sub\_fpwm\_set Error Codes

### 3.6.7.2 **sub\_fpwm\_set**

### **Synopsis**

```
int sub_fpwm_set( sub_handle hndl, int pwm_n, double duty )
```

Configure specific fast PWM output.

### **Parameters**

- pwm\_n number of FPWM output to configure. Can be 0,1,2
- duty desired duty cycle % in range 0..100. Can be not integer.

#### Return value

On success function returns 0. Otherwise error code.

### **Example**

```
sub_fpwm_set( hndl, 0, 20 );
sub_fpwm_set( hndl, 1, 30.5 );
sub_fpwm_set( hndl, 2, 12.25 );
```

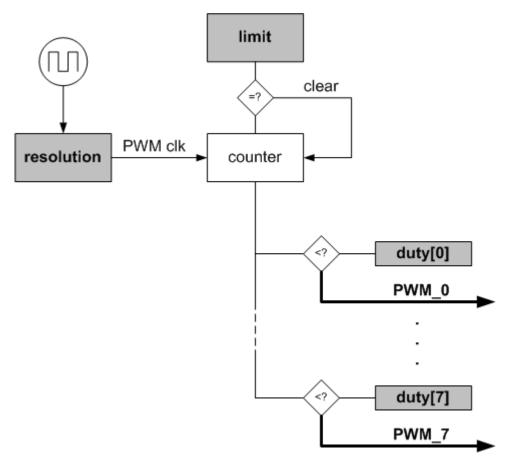
### See also

sub\_fpwm\_config Error Codes

### 3.6.8 PWM

PWM outputs are available on GPIO24..GPIO31 pins (see GPIO Header). Outputs are referenced as PWM\_0 .. PWM\_7.

PWM generation module shown below has configurable source clock, counter limit and separate comparator for each PWM output.



PWM module resolution and limit are configured with <u>sub\_pwm\_config</u>. Duty cycle of each PWM output can be set with <u>sub\_pwm\_set</u>.

PWM module output signal controls output driver of the corresponding GPIO (see GPIO Functions). To get high/low transition of the GPIO pin it should be configured to output state with sub\_gpio\_config. Otherwise PWM module will enable/disable internal pull-up.

### **Functions**

sub\_fpwm\_config sub\_pwm\_set

### 3.6.8.1 sub pwm config

### **Synopsis**

```
int sub_pwm_config( sub_handle hndl, int res_us, int limit )
```

Configure PWM module.

#### **Parameters**

- res\_us PWM module clock resolution in μs. Resolution range is 20μs 16384μs.
- limit PWM module counter limit in range 0-255. If limit is 0 PWM module will be turned off.

### **PWM frequency**

Resolution and limit define PWM module frequency

```
Fpwm = 1000000/(res_us * limit) Hz
```

### PWM frequency range is

```
Fpwm_min = 1000000/(20 * 2) = 25000 Hz = 25KHz
Fpwm_max = 1000000/(16384 * 255) = 0.238 Hz
```

### Return value

On success function returns 0. Otherwise error code.

### See also

sub\_pwm\_set Error Codes

### Compatibility

FW version 0.1.8 or grater Library version 0.1.12.10 or grater

### 3.6.8.2 **sub\_pwm\_set**

#### **Synopsis**

```
int sub_pwm_set( sub_handle hndl, int pwm_n, int duty )
```

Configure specific PWM output.

#### **Parameters**

- pwm\_n number of PWM output to configure. Can be 0..7.
- duty Duty cycle in range 0..255

### **Duty cycle**

- If duty cycle is 0, PWM output will be constantly low
- If duty cycle is grater or equal to the limit set by <a href="mailto:sub\_pwm\_config">sub\_pwm\_config</a>, PWM output will be constantly high

Effective duty cycle in percent can be calculated as

```
DUTY% = duty/limit * 100%
```

Duty cycle resolution in bits depends on limit. It can be in range of 1 bit for limit=2 up to 8 bit for limit=255

### Return value

On success function returns 0. Otherwise error code.

### **Example**

```
/* Set PWM resolution=10ms, limit=100, frequency=1Hz */
sub_pwm_config( hndl, 10000, 100 );

/* Set PWM_0 pin (GPIO24) to output state */
sub_gpio_config( hndl, 0x01000000, &config, 0x01000000 );

/* Output 50% duty cycle on PWM_0 pin */
sub_pwm_set( hndl, 0, 50 );
```

### See also

sub\_pwm\_config Error Codes

# Compatibility

FW version 0.1.8 or grater

Library version 0.1.12.10 or grater

# 3.7 Analog to Digital Converter - ADC

SUB-20 has 8 single ended and a 16 differential analog input combinations with x1 x10 or x200 input gain amplifier. Analog inputs are referenced as ADC0..ADC7 see <u>GPIO Header</u>. The SUB-20 ADC module features a 10-bit successive approximation ADC. The ADC contains a Sample and Hold circuit which ensures that the input voltage to the ADC is held at a constant level during conversion.

### **Functions**

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sub\_adc\_config sub\_adc\_single sub\_adc\_read

# 3.7.1 sub\_adc\_config

#### **Synopsis**

```
int sub_adc_config( sub_handle hndl, int flags )
```

Configure SUB-20 ADC module.

### **Parameters**

• flags - set of below flags

ADC\_ENABLE Enable ADC module. If this flag is not set ADC module will be disabled

ADC\_REF\_VCC Use VCC as ADC reference
ADC\_REF\_2\_56 Use internal 2.56V reference

# Return value

On success function returns 0. Otherwise error code.

# 3.7.2 sub\_adc\_single

See sub\_adc\_read.

# 3.7.3 sub\_adc\_read

### **Synopsis**

```
int sub_adc_single( sub_handle hndl, int* data, int mux );
int sub_adc_read( sub_handle hndl, int* data, int* mux, int reads );
```

Read single or multiple ADC conversion result(s)

### **Parameters**

- data buffer to store conversion result(s)
- mux ADC input channel multiplexer control code(s). See table below.
- · reads number of results to read

ADC mux code Single Ended	Differential Positive	Differential Negative	Gain	
---------------------------	--------------------------	--------------------------	------	--

ADC SO	ADC0					
ADC_S0						
	ADC1					
ADC_S2	ADC2					
ADC_S3	ADC3		N.A.			
ADC_S4	ADC4					
ADC_S5	ADC5					
ADC_S6	ADC6					
ADC_S7	ADC7					
ADC_D10_10X		ADC1	ADC0	10		
ADC_D10_200X		ADC1	ADC0	200		
ADC_D32_10X		ADC3	ADC2	10		
ADC_D32_200X		ADC3	ADC2	200		
ADC_D01		ADC0	ADC1			
ADC_D21		ADC2	ADC1			
ADC_D31		ADC3	ADC1			
ADC_D41	N.A.	ADC4				
ADC_D51	] N.A.	ADC5	ADC1			
ADC_D61		ADC6	ADC1	N.A.		
ADC_D71		ADC7	ADC1	IN.A.		
ADC_D02		ADC0	ADC2			
ADC_D12		ADC2	ADC2			
ADC_D32		ADC3	ADC2			
ADC_D42		ADC4	ADC2			
ADC_D52		ADC5	ADC2			
ADC_1_1V	Internal 1.1V					
ADC_GND	Analog GND	N.A.				

### **ADC Result**

For single ended conversion:

$$ADC = \frac{V_{IN} \cdot 1023}{V_{REF}}$$

For differential:

$$ADC = \frac{(V_{POS} - V_{NEG}) \cdot GAIN \cdot 512}{V_{REF}}$$

ADC is a result of conversion. Note that the result of differential conversion is signed and can be negative.

# Return value

On success function returns 0. Otherwise error code.

### **Example**

```
int adc, adc_buf[3], adc_mux[3];
sub_adc_single( fd, &adc, ADC_SO );  /* Read ADC on ADCO input */
adc_mux[0] = ADC_SO;
adc_mux[1] = ADC_S2;
adc_mux[2] = ADC_S3;
sub_adc_read( fd, adc_buf, adc_mux, 3 );  /* Read ADC on ADCO,2,3 inputs */
```

### 3.8 LCD Functions

### **Functions**

• sub\_lcd\_write

# 3.8.1 sub\_lcd\_write

### **Synopsis**

```
int sub lcd write( sub handle hndl, char* str );
```

This function will work only on SUB-20 configurations with LCD.

Characters from \*str are written to the LCD beginning from the current LCD position. Special characters and sequences listed below are used to format LCD output and control current position.

ANSI C notation	Hex value	Description	Example
\f	0x0C	Clear LCD and go to first position	"\fHello"
\r	0x0D	Go to first position	"\r0123"
\n	0x0A	Go to next string	"\rHello\nWorld"
\eXY	0x1B X Y	Go to position X,Y	"\e00Hello\e01World"

Every string written to LCD will be space padded till the end of the string.

### **Parameters**

• \*str - LCD string

### Return value

On success function returns 0. If LCD is not supported function will return "Feature not supported".

### Example

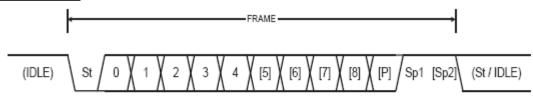
```
sub_lcd_write( hndl,
   "\fHello\nWorld" );
sub_lcd_write( hndl,
   "\f\e20Hello\e21World" );
sub_lcd_write( hndl, "\r1\n2" );
sub_lcd_write( hndl, "\fT:\nR:"
);
sub_lcd_write( hndl,
   "\e20abc\e21def" );
```

# Compatibility

- Required firmware version > 0.0.4
- Required DLL version > 0.1.12.2

### 3.9 RS232 RS485 Functions

#### RS232 RS485 Frame format



St Start bit, always low.

(n) Data bits (0 to 8).

P Parity bit. Can be odd or even.

Sp Stop bit, always high.

#### **Functions**

sub rs set config sub rs get config sub rs timing sub rx xfer

# 3.9.1 sub\_rs\_set\_config

### **Synopsis**

int sub\_rs\_set\_config( sub\_handle hndl, int config, int baud)

Configure SUB-20 UART (Universal Asynchronous Receiver Transmitter).

### **Parameters**

config - UART configuration. Config should be assembled as a combination of the following flags

RS_RX_ENABLE RS_TX_ENABLE	Enable UART receiver Enable UART transmitter
RS_CHAR_5	
RS_CHAR_6	
RS_CHAR_7	Data Bits
RS_CHAR_8	
RS_CHAR_9	
RS_PARITY_NONE	
RS_PARITY_EVEN	Parity
RS_PARITY_ODD	
RS_STOP_1	Stop Bits
RS_STOP_2	Stop bits

To disable UART provide configuration without RS\_RX\_ENABLE and RS\_TX\_ENABLE.

• baud - Desired baudrate. Maximum baudrate is 2Mbps. The actual baudrate may slightly differ from the desired as actual baudrate is an integer quotient from dividing the 16MHz reference clock.

### Return value

On success function returns 0. Otherwise error code.

#### Example

```
/* Set 9660 bps, 8 data bits, no parity, 1 stop bit */
sub_rs_set_config( hndl,
RS_RX_ENABLE|RS_TX_ENABLE|RS_CHAR_8|RS_PARITY_NONE|RS_STOP_1, 9600 );
```

# 3.9.2 sub\_rs\_get\_config

### **Synopsis**

```
int sub_rs_get_config( sub_handle hndl, int* config, int* baud)
```

Read current SUB-20 UART configuration.

#### **Parameters**

- \*config will be filled with UART configuration see sub\_rs\_set\_config for details
- \*baud will be filled with actual UART baudrate

#### Return value

On success function returns 0. Otherwise error code.

# 3.9.3 sub\_rs\_timing

#### **Synopsis**

Configure UART transfer timing and order of transmit and receive operations. Actual transfer is initiated by sub\_rx\_xfer function.

#### **Parameters**

• flags - one or none of the below flags:

RS\_RX\_BEFORE\_TX
RS\_RX\_AFTER\_TX
Receive message and after that transmit message
Transmit message and after that receive message
Receive and transmit simultaneously

- tx space us delay in \u03c4s between subsequent byte transmit
- rx\_msg\_us message reception timeout in μs
- rx\_byte\_us byte to byte reception timeout in us

Delay and timeouts precision is  $\pm$  64  $\mu$ s. They should not exceed 4.000.000 $\mu$ s = 4s.

Following table explains relation between rx\_msg\_us and rx\_byte\_us parameters

```
rx_msg_us=0rx_byte_us=0Message reception will last no more then 4srx_msg_us=0rx_byte_us>0First byte reception will last no more then 4s. Every next byte should be received in rx_byte_us timerx_msg_us>0rx_byte_us=0Message reception will last no more then rx_msg_us timerx_msg_us>0rx_byte_us>0First byte reception will last no more then rx_msg_us time. Every next byte should be received in rx_byte_us time
```

#### Return value

On success function returns 0. Otherwise error code.

#### Example

```
/* Request message transmit and after that receipt */
/* No space between transmitted bytes */
/* Message should be received in 1s */
sub_rs_timing( hndl, RS_RX_AFTER_TX, 0, 1000000, 0 );
```

# 3.9.4 sub\_rs\_xfer

#### **Synopsis**

Transmit and/or receive message(s) via UART configured with <u>sub\_rs\_set\_config</u> and in accordance with transfer timing set with <u>sub\_rs\_timing</u>.

#### **Parameters**

- tx\_buf buffer with data to be transmitted
- tx\_sz number of bytes to transmit (can be 0 if transmit not required)
- rx buf buffer to store received data
- rx\_sz maximal number of bytes to receive (can be 0 if reception is not required)

### rx\_sz and tx\_sz should not be grater then 62 bytes.

Function will terminate after following conditions fulfilled: **tx\_sz** bytes transmitted and either **rx\_sz** bytes received or one of the timeouts occurs (see <a href="sub\_rs\_timing">sub\_rs\_timing</a>)

For 9bit transfer data in tx\_buf and rx\_buf has following format

byte 0	byte 1	 byte n	byte n+1
bit8 LSB	bits 70	 bit8 LSB	bits 70

Even bytes (0,2,4,...) contain 8'th bit in LSB. Odd bytes (1,3,5,...) contain bits 7..0. Data is shifted out beginning from bit 0 (see RS232 RS485 Frame format). Parameters **tx\_sz** and **rx\_sz** should correspond to total number of bytes in **tx\_buf** and **rx\_buf**.

### Return value

On success function returns non negative value that denotes number of received bytes. It can be less then **rx sz** if timeout occurs.

Otherwise -1 will be returned and sub\_errno will contain error code.

### **Example**

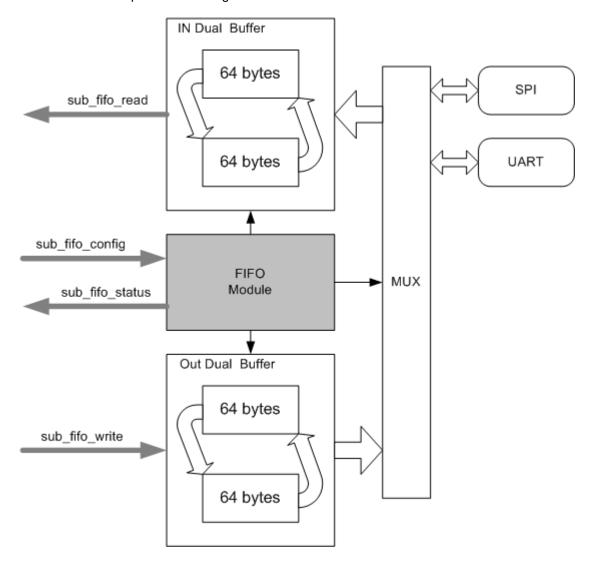
```
/* Set timing */
sub_rs_timing( hndl, RS_RX_AFTER_TX, 0, 1000000, 200000 );
/*
   Transmit 3 bytes and try to receive up to 5 bytes
   in 1s with 200ms byte to byte timeout
*/
sub_rs_xfer( hndl, "at\r", 3, rx_buf, 5 );
```

### Compatibility

FW version 9-bit transfer support - 0.2.2 or grater

# 3.10 FIFO, Streaming, Slave Modes

FIFO is used for implementation of streaming data transfer and slave modes functionality such as SPI slave, I2C slave. Below is simplified block diagram of the SUB-20 FIFO module.



# 3.10.1 FIFO Functions

sub\_fifo\_config sub\_fifo\_read sub\_fifo\_write

### 3.10.1.1 sub\_fifo\_config

#### **Synopsis**

```
int sub fifo config( sub handle hndl, int config )
```

Configure FIFO.

### **Parameters**

· config - set of FIFO configuration flags listed below

FIFO\_SELECT\_SPI Connect SPI module to FIFO
FIFO\_SELECT\_I2C Connect I2C slave module to FIFO

FIFO\_SELECT\_UART Connect UART to FIFO

FIFO\_CLEAR Clear IN and OUT FIFO buffers
FIFO\_READ\_FULL Read only full 64 byte FIFO buffers

### Return value

On success function returns 0. Otherwise error code.

#### Compatibility

FW version FIFO\_CLEAR - 0.1.3 or grater

FIFO\_SELECT\_UART - 0.2.0 or grater

Library version 0.1.12.10 or grater

### 3.10.1.2 sub\_fifo\_write

### **Synopsis**

```
int sub_fifo_write( sub_handle hndl, char* buf, int sz, int to_ms )
```

Function attempts to transfer sz bytes from buffer into OUT FIFO in no more then to ms time.

### **Parameters**

- · buf source buffer
- sz buffer size
- · to\_ms timeout in milliseconds

#### **Return Value**

On success a non negative number of actually written bytes is returned. It can be less then or equal to **sz**. In case of error negative error code (defined in errno.h) will be returned and if applicable <a href="mailto:sub\_errno">sub\_errno</a> will be set to the corresponding value. Possible error codes are

```
-ENOENT (-2) USB failure
-EIO (-5) USB failure
-ENOMEM (-12) Memory failure
-EINVAL (-22) Invalid parameter
-EFBIG (-27) Buffer overflow
-ETIMEDOUT (-116) Timeout
```

### 3.10.1.3 sub\_fifo\_read

#### **Synopsis**

```
int sub fifo read( sub handle hndl, char* buf, int sz, int to ms )
```

Function attempts to read **sz** bytes from IN FIFO into buffer in no more then **to ms** time.

#### **Parameters**

• buf - destination buffer

sz - buffer size. Considering internal FIFO structure it is highly recommended to <u>use only 64 divisible sz</u>
 <u>values</u> and corresponding buffer size. It will guarantee better performance and no buffer overflow error
 (-EFBIG).

• to\_ms - timeout in milliseconds

#### **Return Value**

On success a non negative number of actually read bytes is returned. It can be less then or equal to **sz**. In case of error negative error code (defined in errno.h) will be returned and if applicable <a href="sub\_errno">sub\_errno</a> will be set to the corresponding value. Possible error codes are

```
-ENOENT (-2) USB failure

-EIO (-5) USB failure

-ENOMEM (-12) Memory failure

-EINVAL (-22) Invalid parameter

-EFBIG (-27) Buffer overflow. To prevent this error use 64 divisible sz

-ETIMEDOUT (-116) Timeout
```

### **Known Issue**

If IN FIFO contains exactly 64 or 128 bytes, attempt to read more then 64 or 128 bytes correspondingly with sub\_fifo\_read will cause to timeout (-116). As a workaround always call sub\_fifo\_read with sz=64.

### 3.10.2 SPI Slave

### Configuration

To use SUB-20 in SPI slave mode following should be done:

- Configure SPI module with <a href="mailto:sub\_spi\_config">sub\_spi\_config</a>. Make sure to set <a href="mailto:SPI\_SLAVE">SPI\_SLAVE</a> flag.
- Connect SPI module to FIFO with <a href="mailto:sub\_fifo\_config">sub\_fifo\_config</a>. FIFO\_SELECT\_SPI must be set.
- If required, write data to FIFO with <a href="mailto:sub\_fifo\_write">sub\_fifo\_write</a>. This data will be read by external SPI master.
- If required, read data from FIFO with <a href="mailto:sub\_fifo\_read">sub\_fifo\_read</a>. This will be data written by external SPI master.

#### Example

Below is an example to exchange 12 bytes with SPI master:

```
sub_spi_config( hndl, SPI_ENABLE|SPI_SLAVE|SPI_CPOL_RISE|SPI_SMPL_SETUP, 0 );
sub_fifo_config( hndl, FIFO_SELECT_SPI );
sub_fifo_write( hndl, "Hello Master", 12, 100 );
read_sz=0;
while( read_sz < 12 )
{
   rc = sub_fifo_read( hndl, in_buff, 64, 10000 ); /* wait 10 sec */
   if( rc < 0 )
        return rc; /* error */
   read_sz += rc;
}</pre>
```

### **Slave Select**

SUB-20 SPI Slave module use SS0 pin as slave select. SS0 must be pulled low by external SPI master to enable SUB-20 SPI module functionality. When SS0 is held low, the SPI is activated, and MISO becomes an output. All other pins are inputs. When SS is driven high, all pins are inputs, and the SPI is passive.

### 3.10.3 I2C Slave

### Configuration

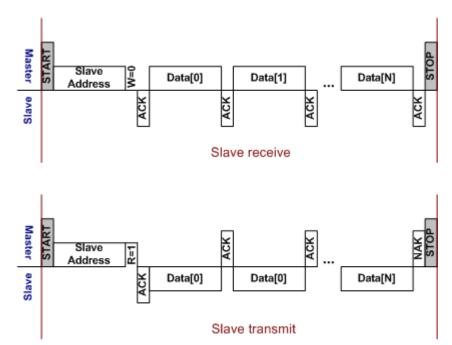
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To use SUB-20 in I2C slave mode following should be done:

- Configure I2C Slave module with sub\_i2c\_config. Set desired I2C slave address and optional flag(s).
- Connect I2C Slave module to FIFO with sub\_fifo\_config. Set FIFO\_SELECT\_I2C flag.
- If required write data to FIFO with sub\_fifo\_write. This data will be read by external I2C master.
- If required read data from FIFO with <u>sub\_fifo\_read</u>. This will be data written by external I2C master.

### **Transactions**

SUB-20 I2C slave module acts as zero address I2C slave device. Below are diagrams of receive and transmit transactions.



### 3.11 Error Codes

API functions may return error code and/or set global variable <u>sub\_errno</u> to provide information about completion of requested operation. The string describing error code can be received with <u>sub\_strerror</u> function call.

### 3.11.1 sub errno

Global variable **sub\_errno** contains status of last SUB-20 API call. Variable **sub\_errno** defined in *libsub.h.* Following error codes are available:

- 0 OK
- 1 SUB Device not found
- 2 Can't open SUB device
- 3 Can't set configuration

4	Can't claim interface
5	Failed to setup async transaction
6	Failed to submit async transaction
7	Bulk write failed
8	Bulk read failed
9	Bulk read incomplete
10	Out buffer overflow
11	I2C error
12	Wrong tag code in response
13	Wrong tag size in response
14	Wrong parameters
15	SPI Disabled
16	Feature not supported

# 3.11.2 sub\_strerror

### **Synopsis**

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```
char* sub_strerror( int errnum )
```

Return string describing error number. This function is similar to strerror().

# **Parameters**

• errnum - error number

# **Return Value**

Function returns pointer to string with error description. If error number is unknown function will return pointer to string "Unrecognized error <error\_number>".

# 4 Electrical Characteristics

# 4.1 Absolute Maximum Ratings

Operating Temperature	-20°C to +65°C	
Voltage on any Pin with respect to Ground	-0.5V to VCC+0.5V	
Maximum Operating Voltage	+6V	
DC Current per I/O Pin	40mA	
DC Current Vcc and GND Pins	200mA	

### 4.2 DC Characteristics

Symbol	Parameter	Condition	Min	Тур	Max	Units
VIL	Input Low Voltage	Vcc = 3.3V - 5.5V	0.5		0.2Vcc	V
VIH	Input High Voltage	Vcc = 3.3V - 5.5V	0.6Vcc		Vcc + 0.5	V
Vol		IOL = 10mA, VCC = 5V IOL = 5mA, VCC = 3.3V		0.3 0.2	0.7 0.5	V
Vон		IOH = -20mA, VCC = 5V IOH = -10mA, VCC = 3.3V	4.2 2.3	4.5 2.6		V
lı∟	Input Leakage Current I/O Pin	Vcc = 5.5V, pin low			1	μΑ
Iн	Input Leakage Current I/O Pin	Vcc = 5.5V, pin high			1	μΑ
Icc	Power Consumption Current	Vcc = 5V		19	30	mΑ

Although each I/O port can sink or source more than the test conditions under steady state conditions (non-transient), the following must be observed:

- 1. The sum of all IoL, for GPIO4-GPIO7 should not exceed 100 mA.
- 2. The sum of all IoL, for GPIO0-GPIO3, GPIO8-GPIO15 should not exceed 100 mA.
- 3. The sum of all IoL, for GPIO24-GPIO31 should not exceed 100 mA.
- 4. The sum of all lot, for GPIO16-GPIO23 should not exceed 100 mA.
- 5. If IoL exceeds the test condition, VoL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test condition.
- 6. The sum of all Iон, for GPIO4-GPIO7 should not exceed 100 mA.
- 7. The sum of all IoH, for GPIO0-GPIO3, GPIO8-GPIO15 should not exceed 100 mA.
- 8. The sum of all IoH, for GPIO24-GPIO31 should not exceed 100 mA.
- 9. The sum of all IoH, for GPIO16-GPIO23 should not exceed 100 mA.

### 4.3 AC Characteristics

Symbol	Parameter	Condition	Min	Тур	Max	Units	
		SPI					
Fspi	SPI Master frequency		0.125		8	MHz	
FSPI_SLAVE   SPI Slave frequency					2	MHz	
	MDIO						
FMDC	MDC frequency			1		MHz	

#### **Ordering Information** 5

**SUB-20** 

Ordering Code	I2C	SPI	SPI	GPIO	LCD	RS232	<b>RS485</b>	SW1/2	IR	Notes
•		Master	Slave							
SUB-20-B <b>Basic</b>	V	V	V	V						
SUB-20-EB <b>Basic</b>	V	V	V							Heavy duty enclosure
Enclosure										with DB9 Connector
SUB-20-V Visual	V	V	V	V	V					
SUB-20-R25 Serial2	V	V	V	V	>	V		V		
SUB-20-R45 Serial4	V	V	V	V	>		V	V		
SUB-20-I5 Infra5	V	\ \	V	V	V			V	V	
SUB-20-Lxxx	V	V		V	Х	х	Х	Х	Х	SPI Level Converters
SUB-20-Cxxx	Custom Configuration									

For SUB-20-Lxxx, 'xxx' - can be any of the above configuration with addition of SPI Level Converters and without SPI Slave option. For example SUB-20-LV is SUB-20-V board with SPI Level Converters.

