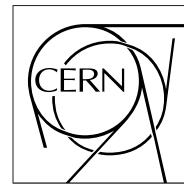


The Compact Muon Solenoid Experiment

# Detector Note

The content of this note is intended for CMS internal use and distribution only



14 April 2014

## Test results of 8 $\mu HTR$ cards (v1.3) for HCAL Forward back-end electronics upgrade at SINP

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### Abstract

After satisfactory performance of the two pre-production  $\mu HTR$  cards manufactured and tested in India and further tested at CERN, eight new  $\mu HTR$  cards (v1.3) are assembled. Initial testing of these cards are performed at SINP and results are presented in this document.

This document is very first version with minimal information and still under preparation.

## 1 Introduction

LHC has completed 3 years of data taking at  $\sqrt{s} = 7 \& 8$  TeV and will again start colliding proton beams in 2015 at  $\sqrt{s} = 13$  TeV. With increase in LHC luminosity (and energy) number of interactions (pile up) per bunch crossing will increase significantly, this will require an increase in the number of depth segmentations in the detector and hence number of electronics readout channels to collect high quality data to perform physics analysis. Very high speed Data Acquisition System (DAQ) will be needed to collect signal from more number of channels and for further processing of the signals. Current VERSABus Memory card (VME) based system being used for data taking will not serve the purpose after Long Shutdown 1 (LS1) because of their limited data taking speed, also these systems are no longer supported by the industry. So the immediate solution is to replace the existing VME based systems by microTCA ( $\mu TCA$  as shown in Figure 2 left). This requires the change in backend electronics which should be compatible with the  $\mu TCA$  standards.

During initial construction, the front-end and back-end electronics were deployed simultaneously, but this has significant schedule risk for an upgrade. The HCAL Upgrade project plans the installation of the back-end electronics in advance of the front-ends. The back-end electronics is designed to be compatible with both the current front-ends and the upgraded front-ends. For the HF, the back-end electronics will be upgraded during LS1 and the HF readout will be switched entirely to the upgraded electronics for operations at a year-end technical stop after LS1.

One  $\mu TCA$  unit (crate) can hold upto 12 Advanced Mezzanine Cards (AMC), within CMS known as micro HCAL Trigger & Readout ( $\mu HTR$  Figure 2 right) card. It includes upto two special “hub” slots. At least one of these slots must be occupied by a  $\mu TCA$  Carrier Hub (MCH) card which is responsible for the control of the power to each slot and for general house-keeping of the crate. The primary MCH site is to be used for a commercial MCH card responsible for crate management and the Ethernet network. The secondary site is to be used for a CMS-common card which will be responsible for clock and fast control distribution as well as local and global DAQ

## 2 $\mu HTR$ card and its components

The  $\mu HTR$  is designed to receive data from Front End Electronics (FEE), produced & tested in India. In addition to  $\mu HTR$  cards there are two  $\mu TCA$  Carrier Hub (MCH) cards which are used for general house keeping of the crate &  $\mu HTR$  cards, providing power to the back plane where  $\mu HTR$  cards are mounted and distribution of LHC clock and other fast control signals. The main building blocks of  $\mu HTR$  card are :

- Optical transducers : PPODs to collect optical information from FEE and SFPs to collect the information from calibration modules.
- Front and Back FPGA : The FPGA which connects directly to the front-end links is called the front FPGA, while the FPGA which connects directly to the DAQ and control links is called the back FPGA.
- Control mezzanines : EEPROM mezzanine enables the automatic reload of the firmware in FPGA during power cycle of the  $\mu HTR$  cards. The JTAG mezzanine is a simple circuitry to enable the multiplexed programming, testing and reading of front and back FPGA via IMPACT tool. When an  $\mu HTR$  is inserted into the  $\mu TCA$  crate, the MCH communicates via the I2C protocol with a sub-component of the AMC called the Mezzanine Management Controller (MMC). After a successful negotiation, including the information that sufficient electrical power will be



Figure 1:  $\mu$ TCA crate loaded with 8 production  $\mu$ HTR cards and one pre-production card ( used for HF back-end electronics design review). All the  $\mu$ HTR are accessible through MCH card via an ethernet cable connected to a PC using HCAL xDAQ software version 11.11.5.

available, the 12 V payload power to the AMC is turned on by the MCH. The communication between the MCH and MMC is also used for monitoring voltages, currents, and temperatures on the AMC card.

- Power mezzanines (PM) and Auxiliary PM : These mezzanines provides the stable and different voltage level to  $\mu$ HTR card for proper functioning. Power consumed by FPGA & other electronic components/sensors on the  $\mu$ HTR is provided by a set of 5 mezzanines (3 power & 2 auxiliary power mezzanines) shown as PM/APM in Figure 2. Any malfunctioning of power module in the  $\mu$ HTR during data taking period will lead to loss in data collection efficiency.

### 3 Testing of $\mu$ HTR cards

- 3.1 Assignment of IP address
- 3.2 Communication with  $\mu$ HTR card and its components
- 3.3 IBER Test for PPODs at 4.8 & 6.4 Gbps using crate
- 3.4 IBER Test for SFPs and front-back link testing using test bench

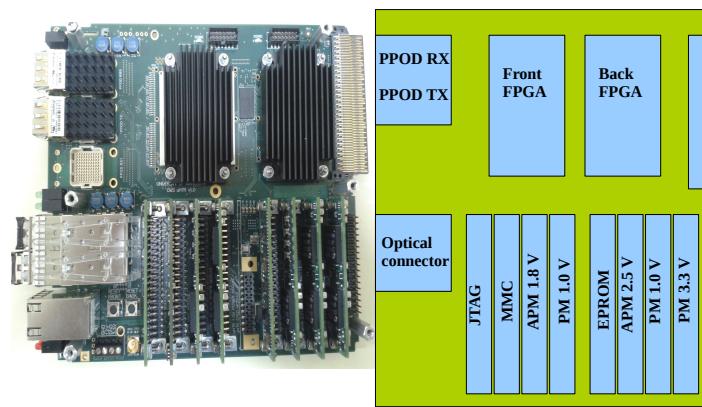


Figure 2:  $\mu$ TCA crate (left) used for testing of  $\mu$ HTR cards (middle), block diagram of  $\mu$ HTR is shown on right.

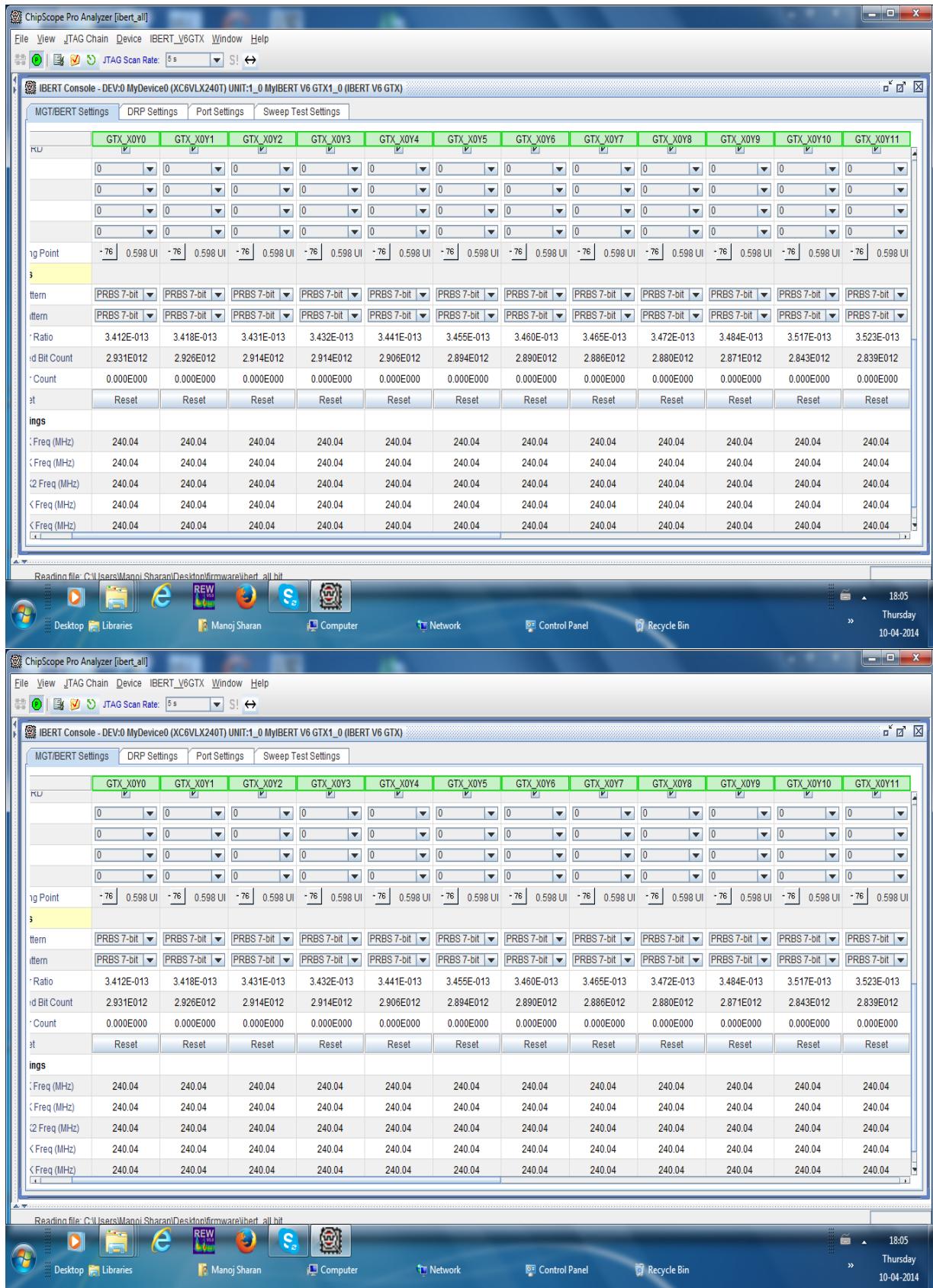


Figure 3: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0103 at a speed of 4.8 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

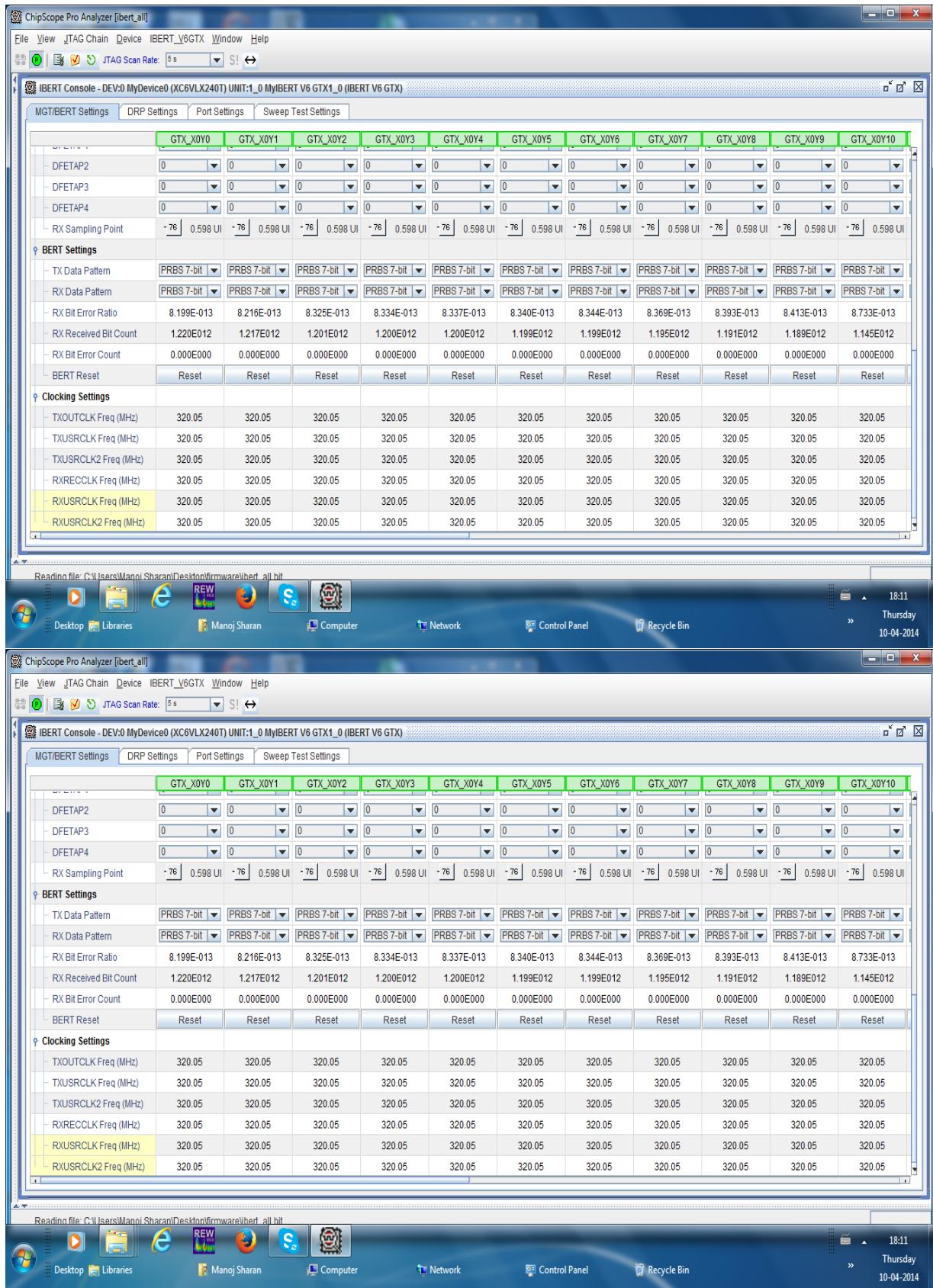


Figure 4: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0103 at a speed of 6.4 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

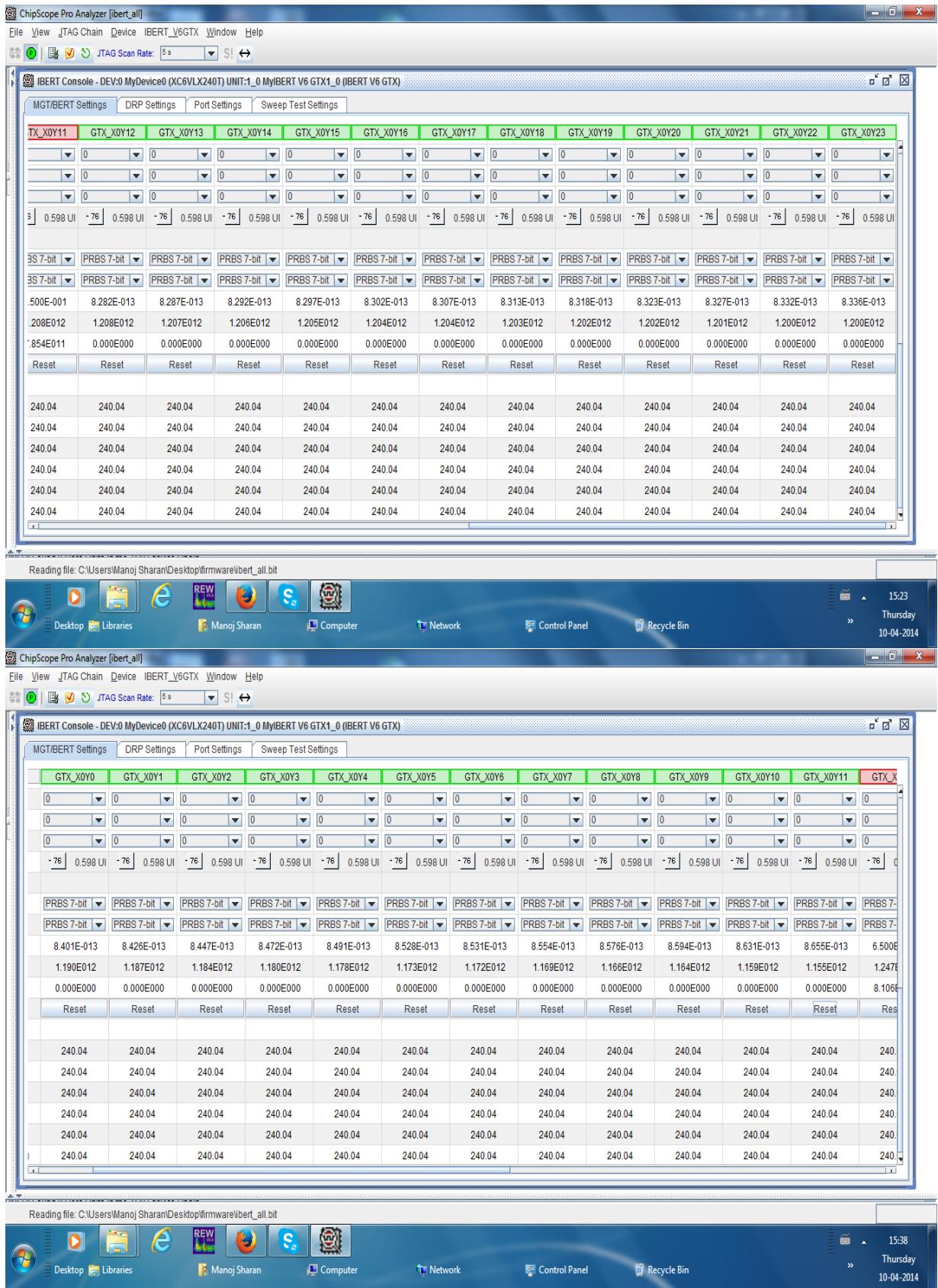


Figure 5: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0105 at a speed of 4.8 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

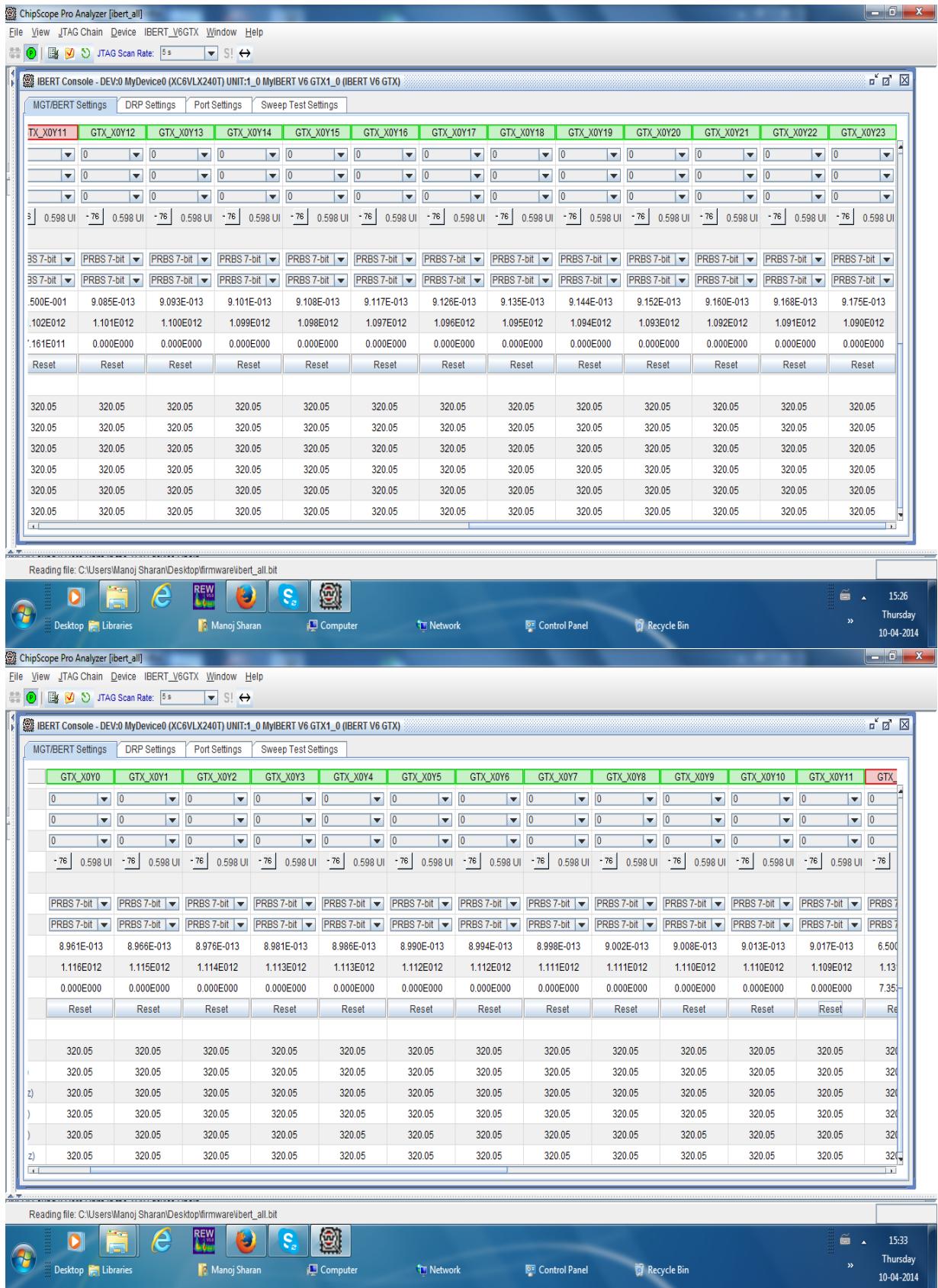


Figure 6: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0105 at a speed of 6.4 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

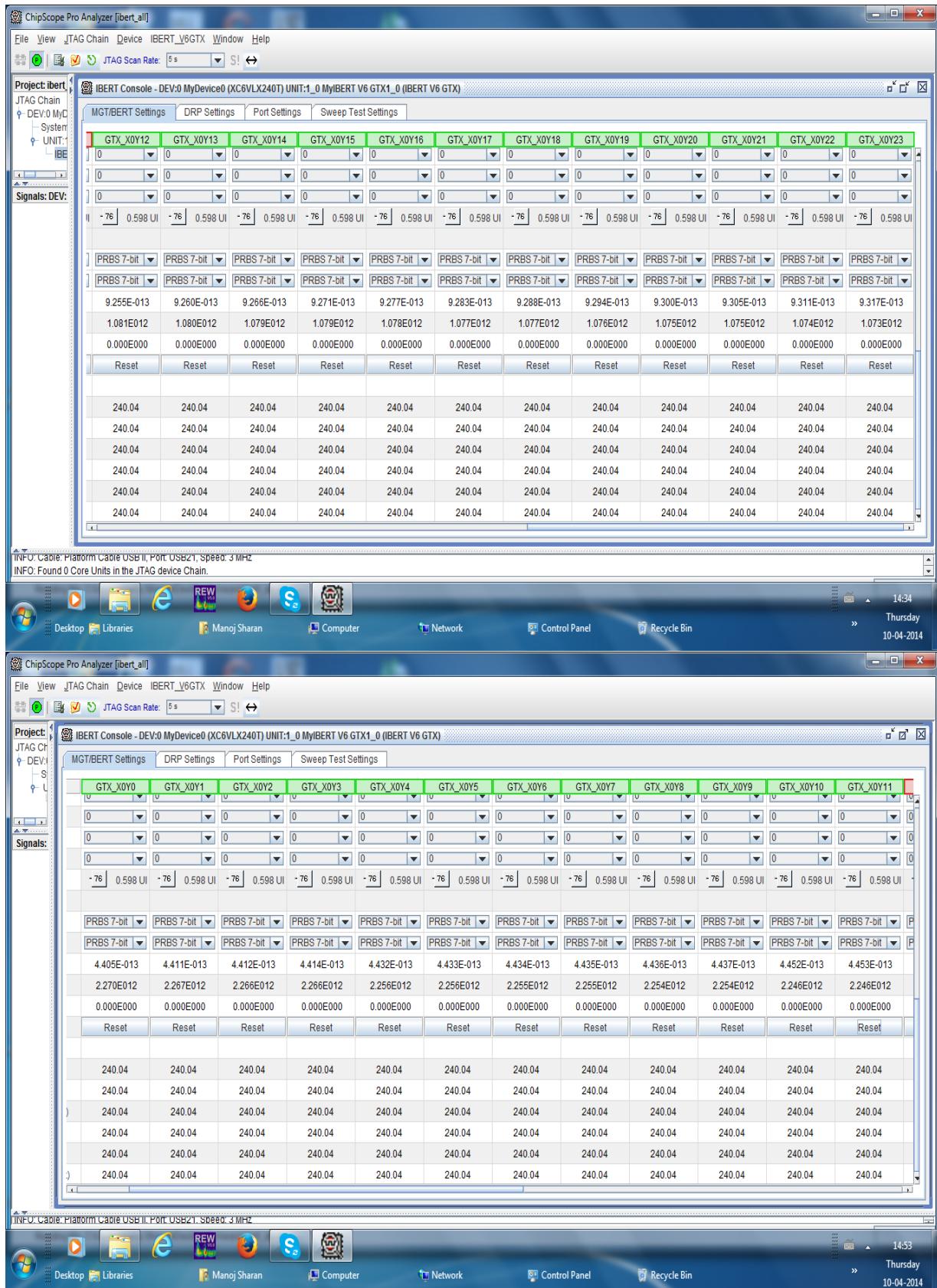


Figure 7: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0106 at a speed of 4.8 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

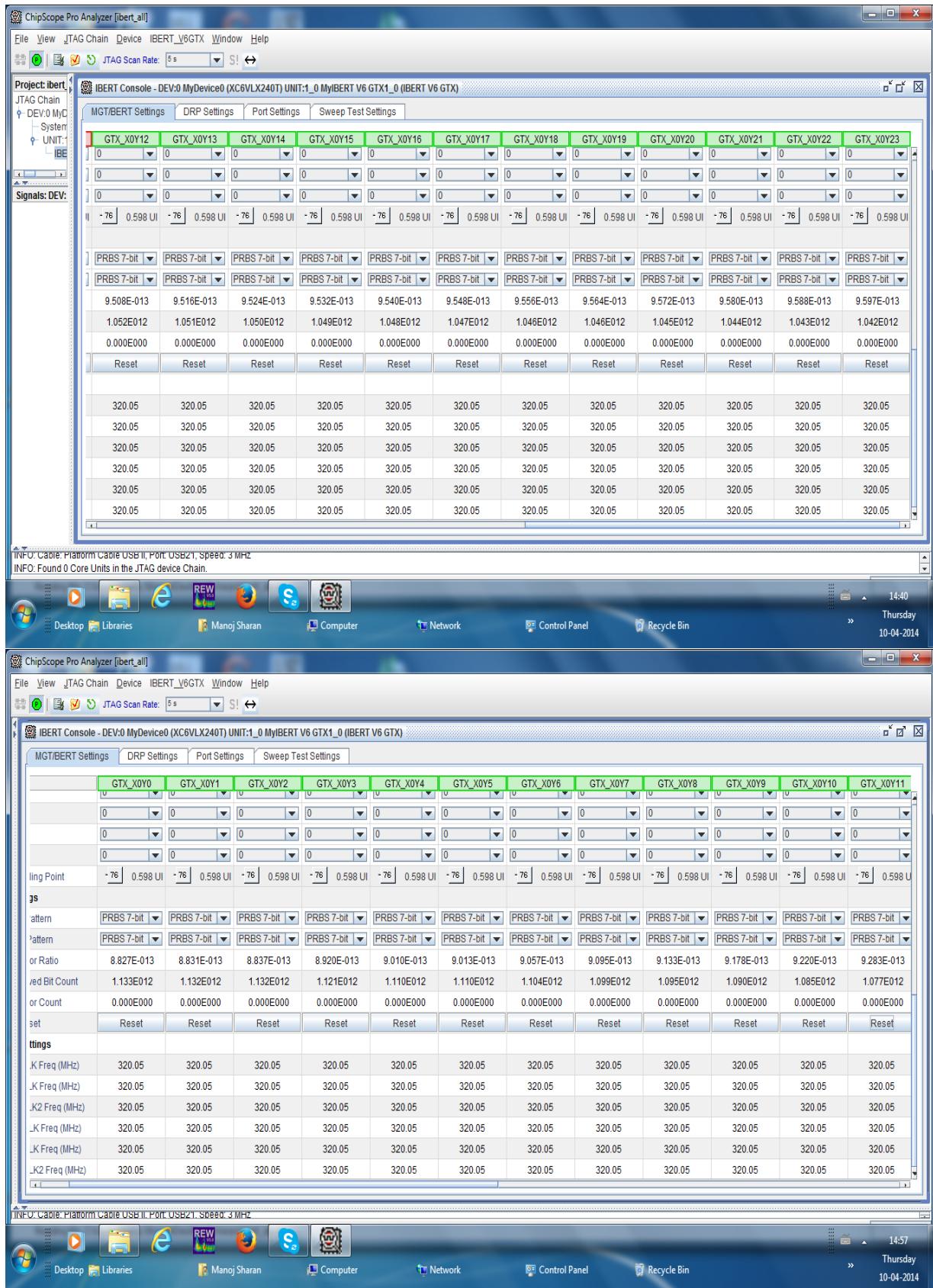


Figure 8: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0106 at a speed of 6.4 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

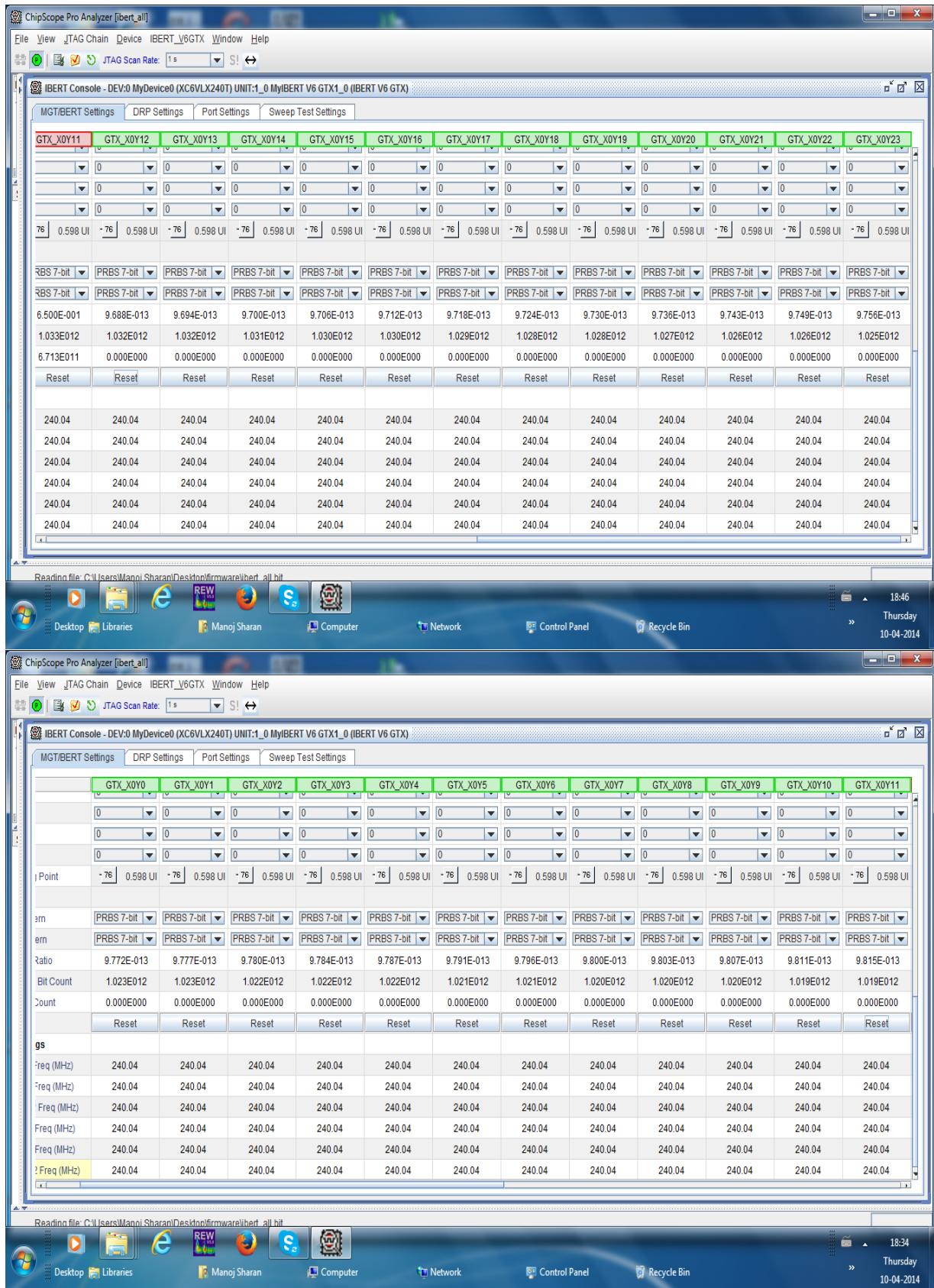


Figure 9: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0107 at a speed of 4.8 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

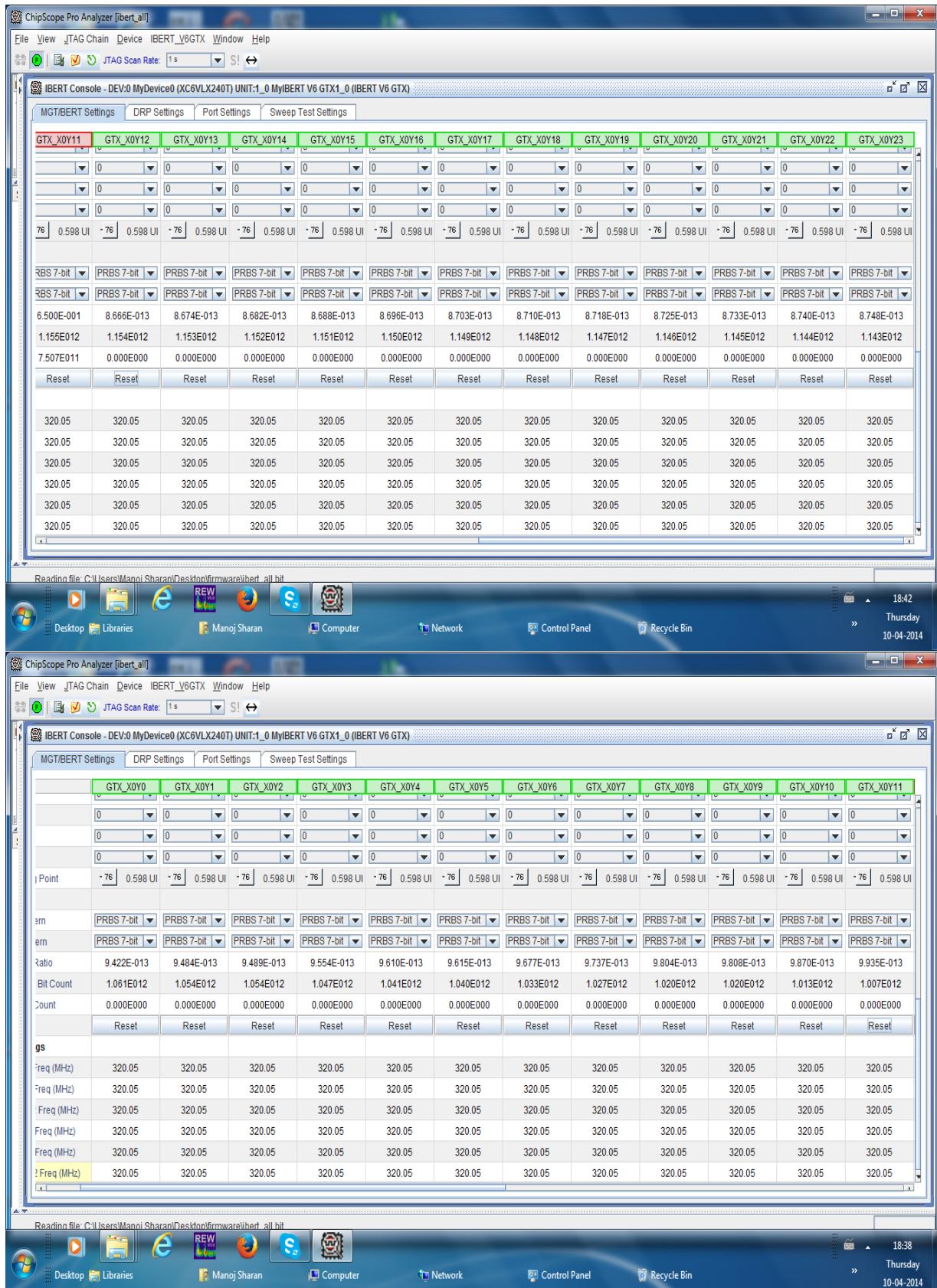


Figure 10: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0107 at a speed of 6.4 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

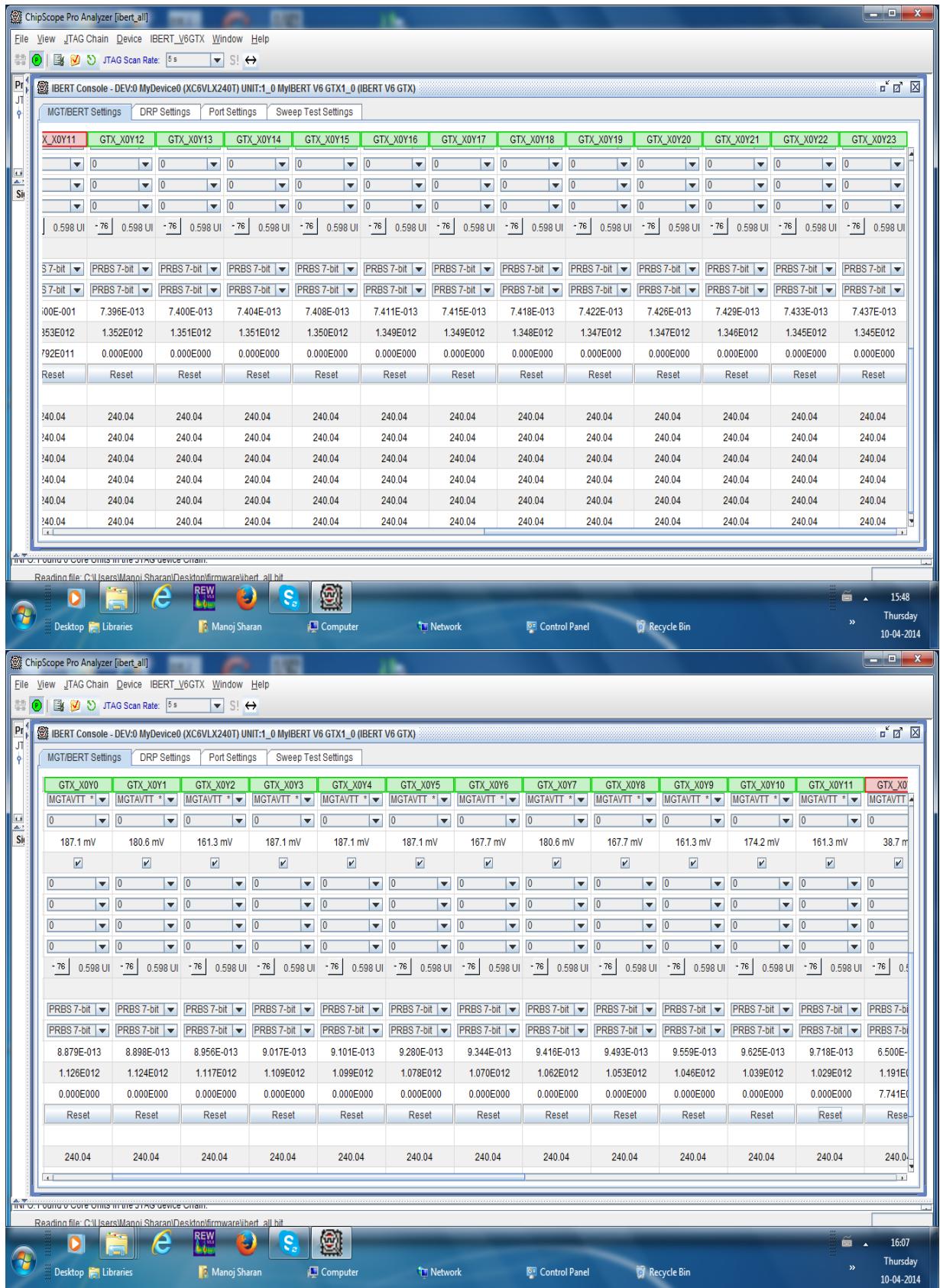


Figure 11: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0108 at a speed of 4.8 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

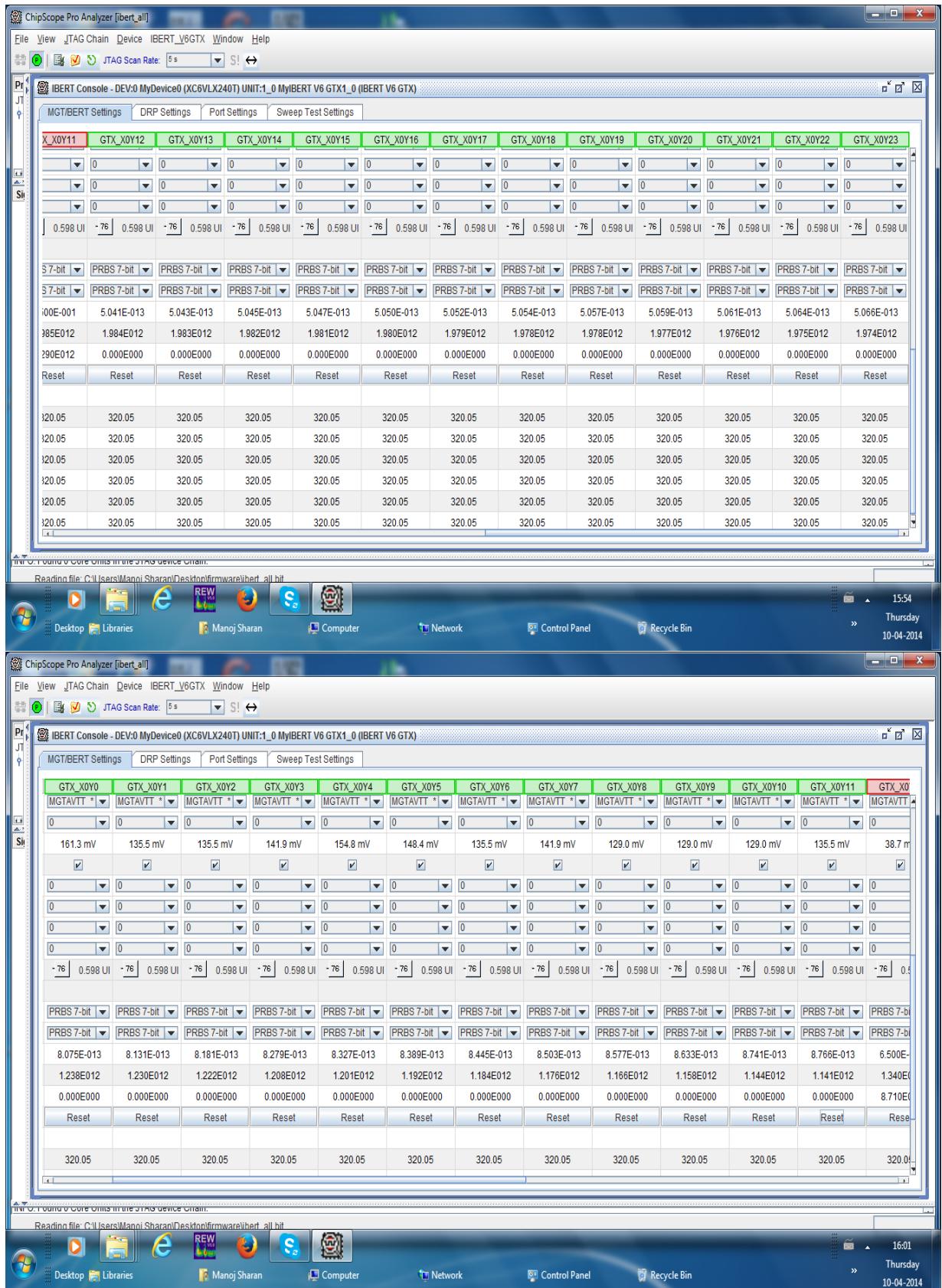


Figure 12: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0108 at a speed of 6.4 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

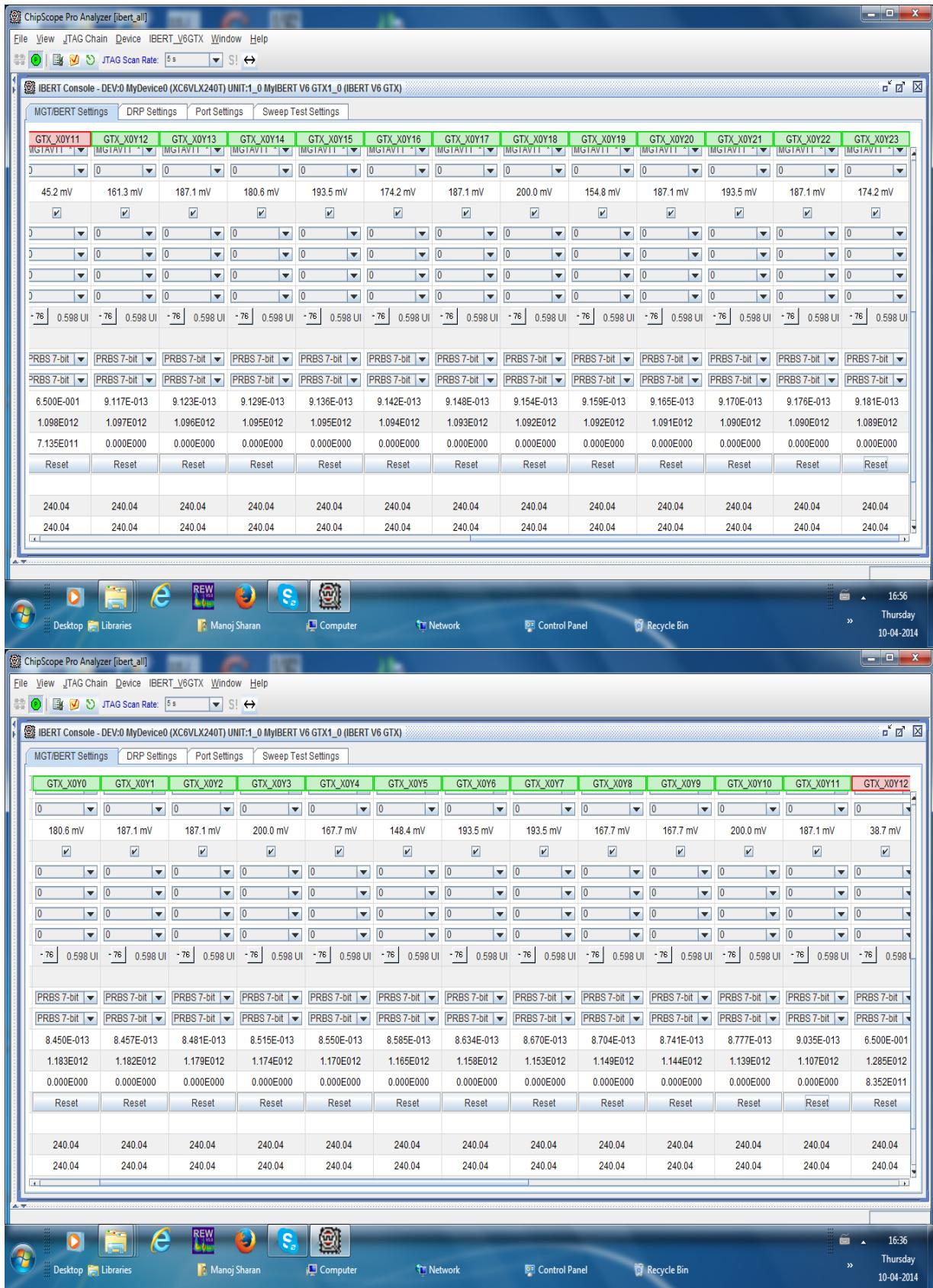


Figure 13: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0109 at a speed of 4.8 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

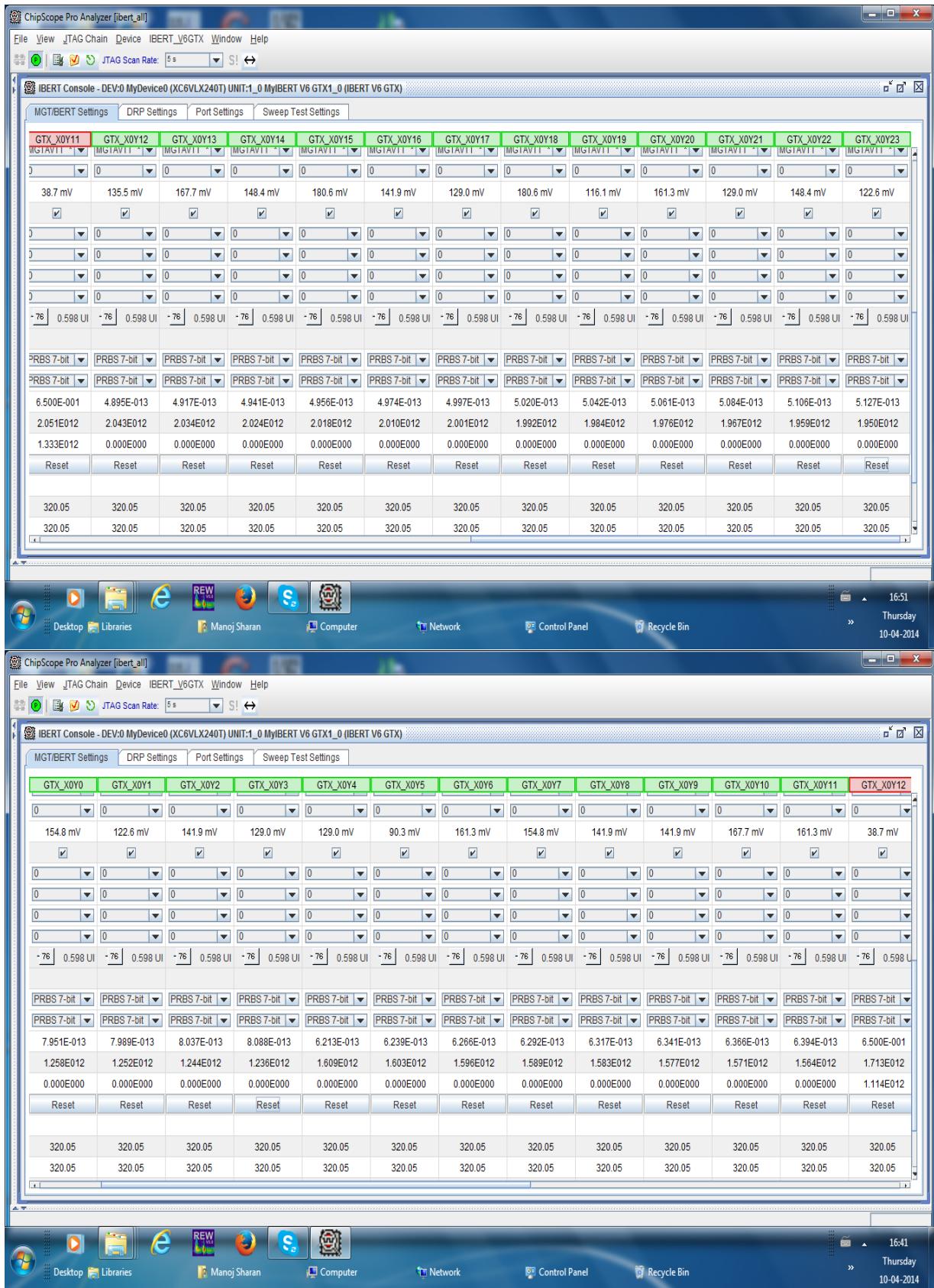


Figure 14: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0109 at a speed of 6.4 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

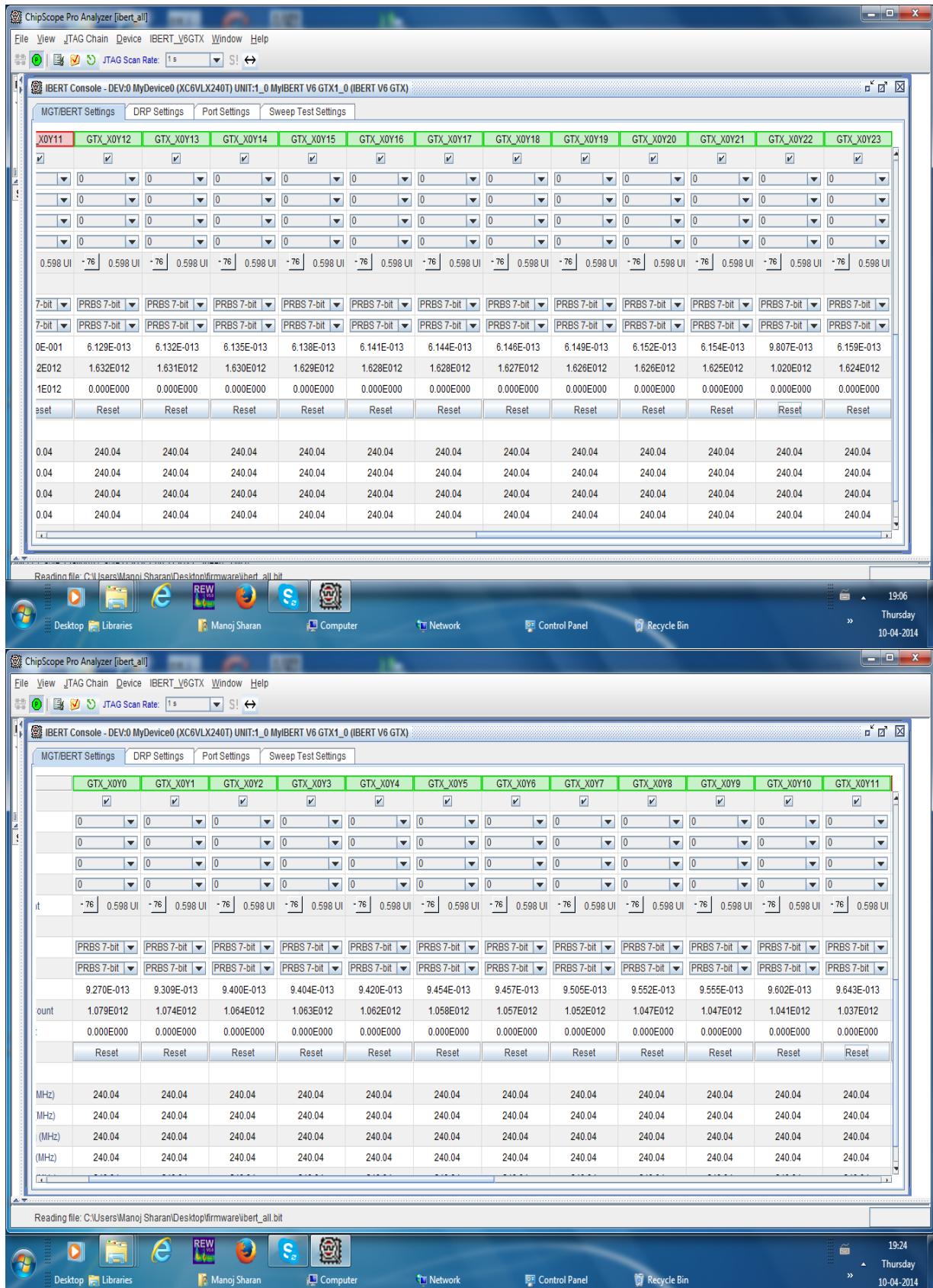


Figure 15: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0110 at a speed of 4.8 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.

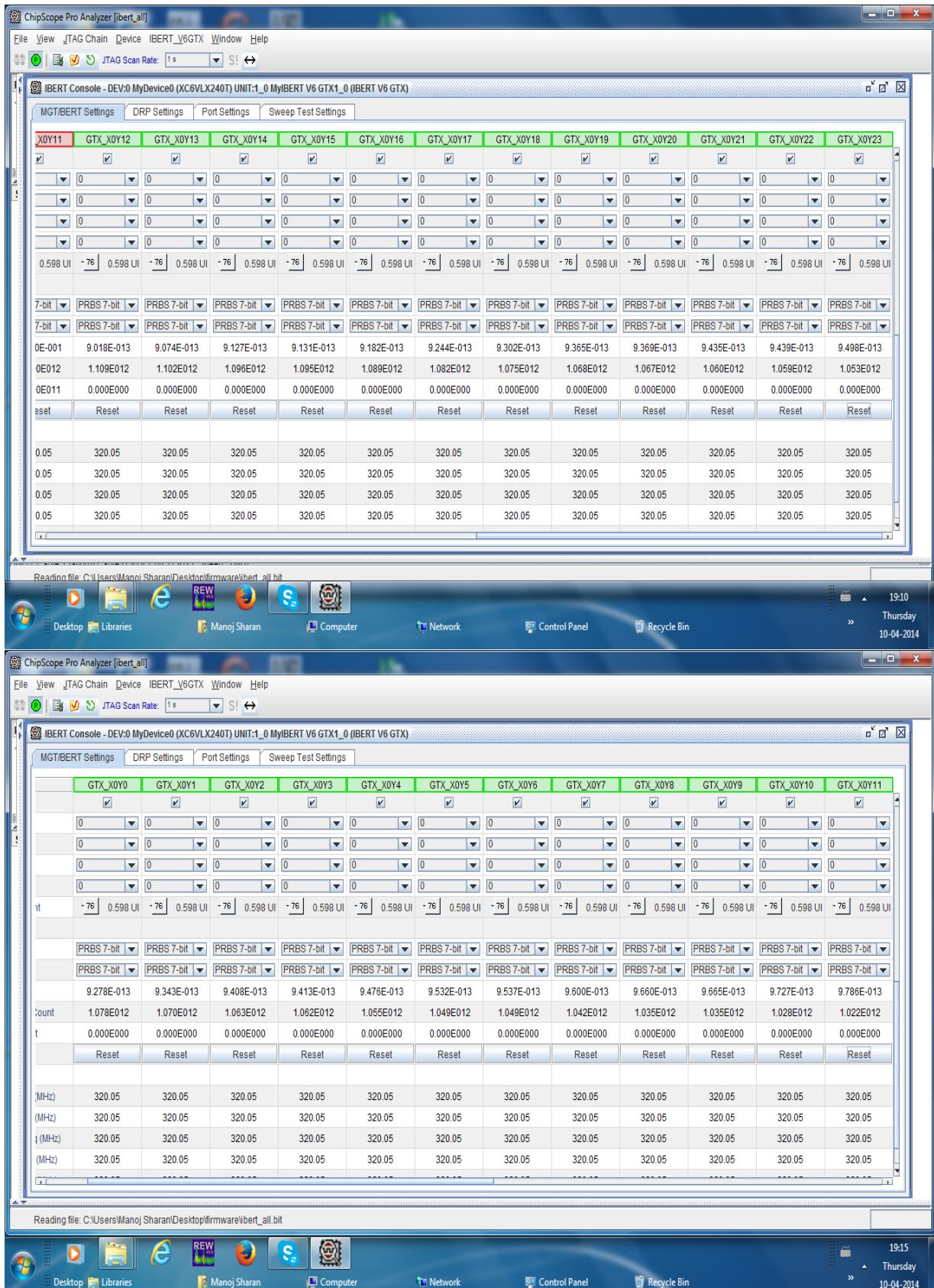


Figure 16: IBER test showing the performance of 12 channels of PPODs mounted at RX0 (top) and RX1 (bottom) of card 0110 at a speed of 6.4 Gbps. An error free transmission from optical transmitter to receiver is confirmed in  $10^{12}$  bits.