Power Mezzenine testing for HCAL backend upgrade during LS1

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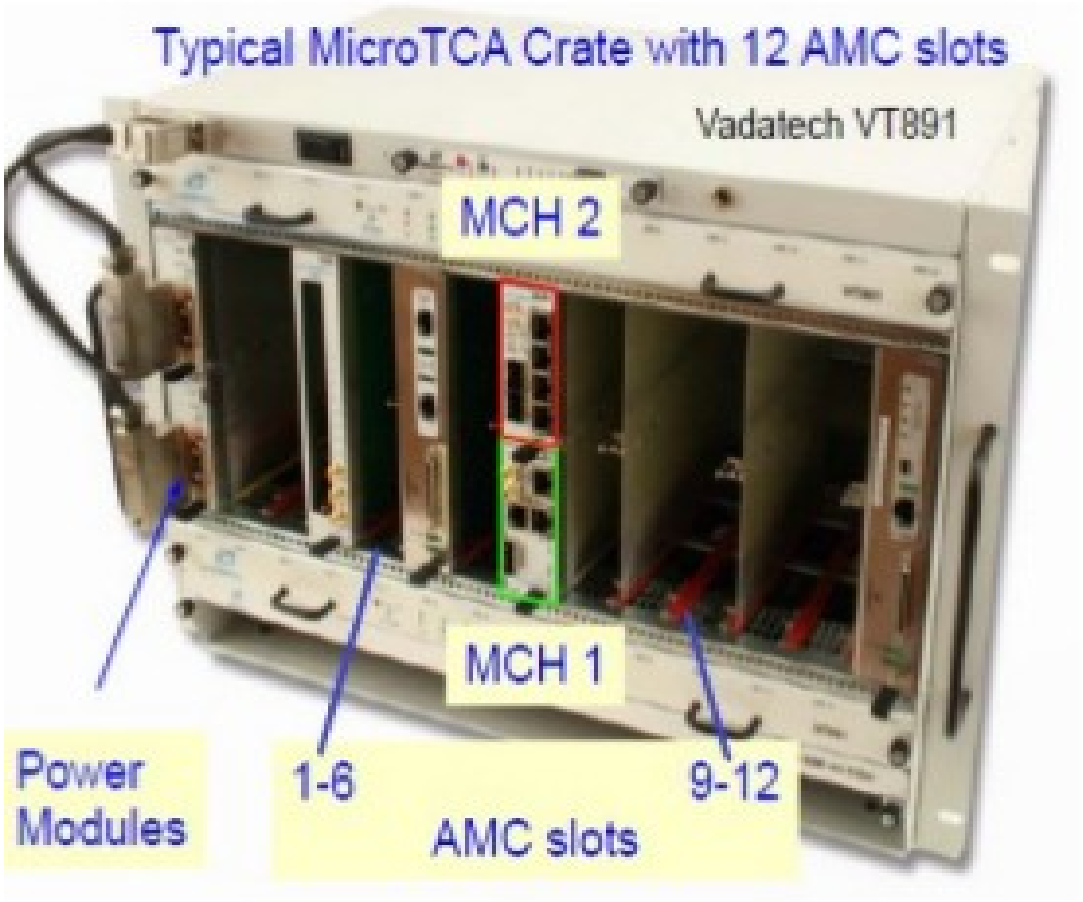
Need of upgrade

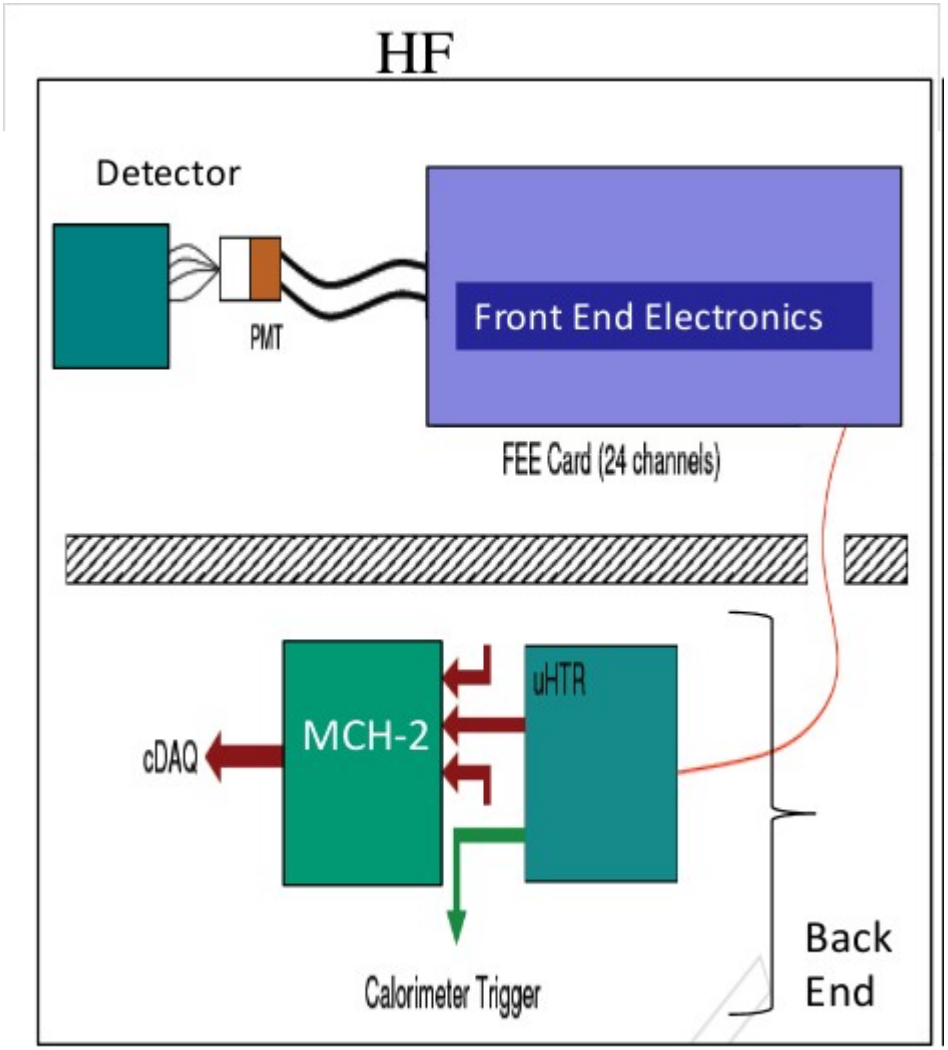
- With increase in LHC Energy & luminosity large amount of data has to be processed.
- Number of channels will increase
  - To store information of more depth in the detector.
- Very high speed DAQ needed.
  - Problem : Current VME based system doesn't support data transfer rate which we will need after LS1.
  - No industrial support available.
  - Solution : µTCA based system.
- This lead to change of electronics also.

µTCA



- Consist of 12 AMC (µHTR) cards.
  - recieves data from FEE.
- 2 MCH Modules
  - MCH1 (commercial): to provide power to all AMC cards, backplane & general house keeping of the crate.
  - MCH2 (customised for CMS): distribution of LHC clock and fast control signal
- Power Modules

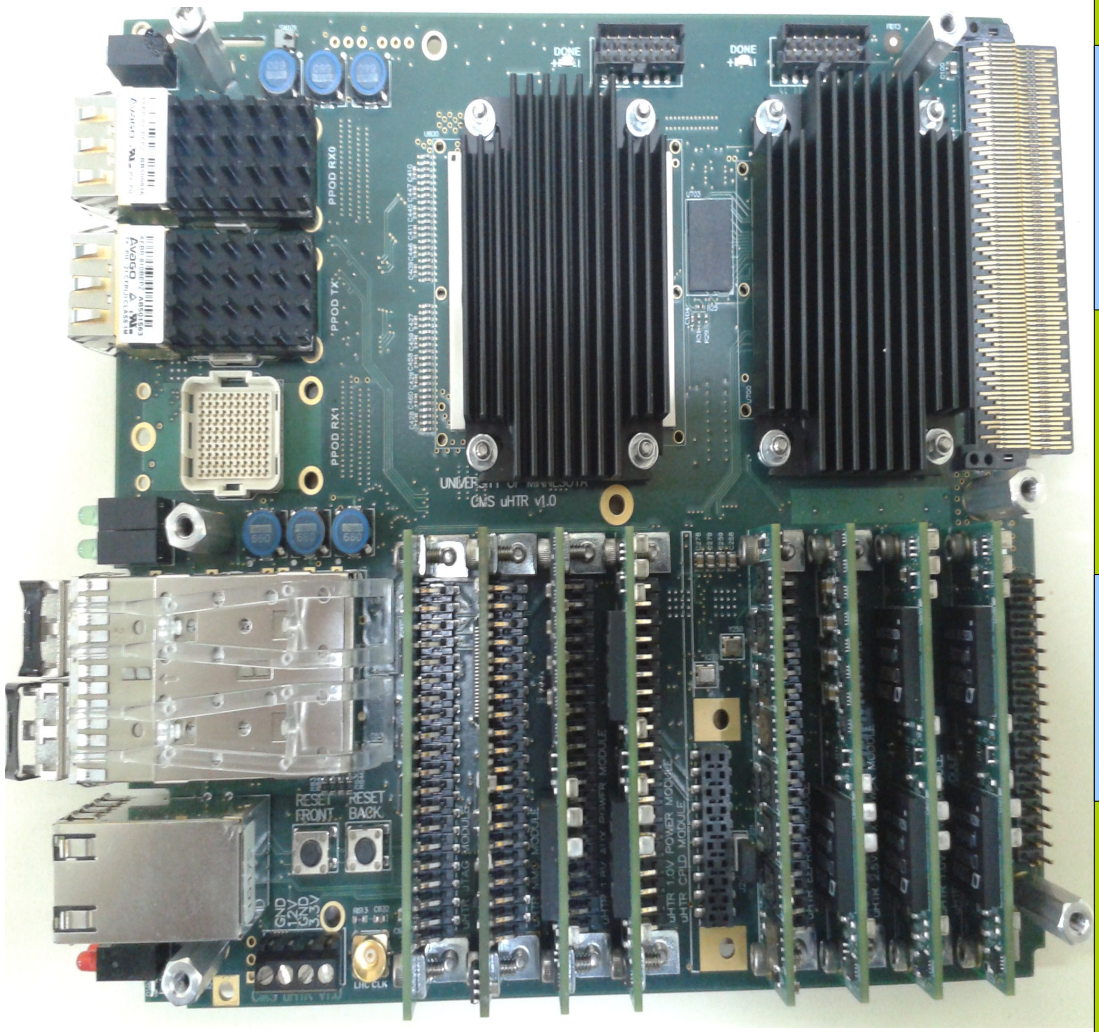
Data flow in HF

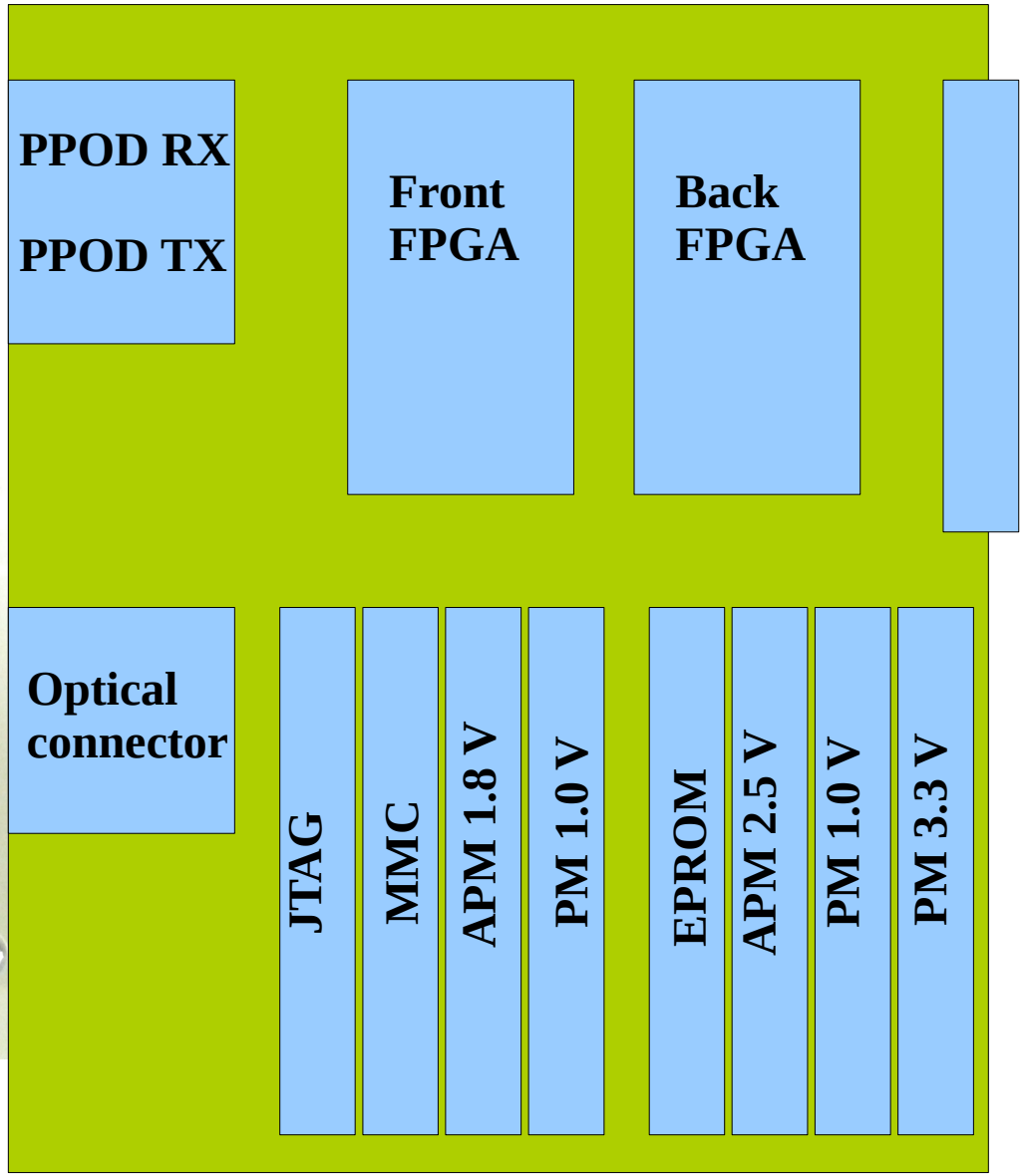


Role of backend electronics :

- Receive a continuous stream of ADC and TDC (raw optical data rate 4.8 Gbps).
- Calculate trigger primitives.
- Transmit the trigger primitives over optical fiber to the calorimeter trigger system.
- Pipeline the ADC, TDC, and trigger primitive data for the full Level 1 trigger latency period.
- use the occupancy of the forward calorimeter to measure of the LHC luminosity

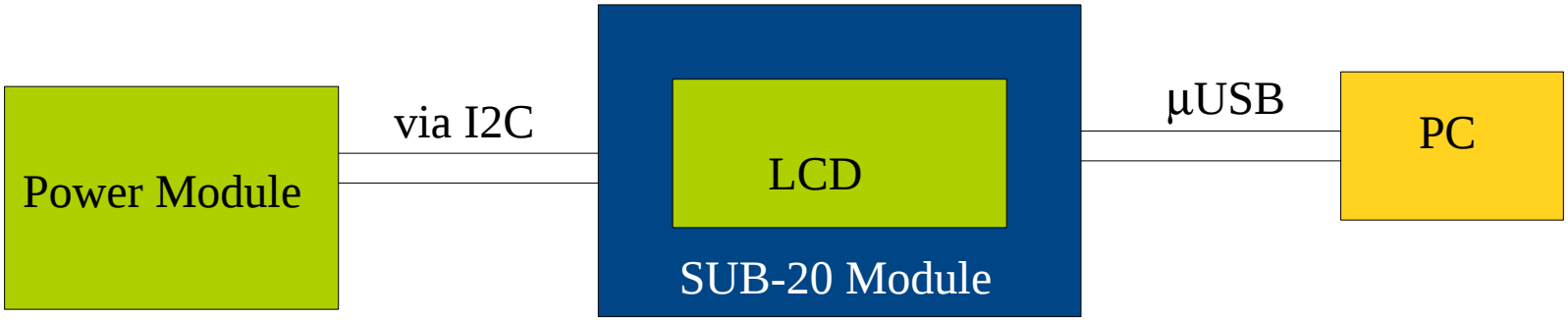
What is AMC ?


PPOD RX0
PPOD TX
PPOD RX1
CMS uHTR v1.0
RESET FRONT
RESET BACK

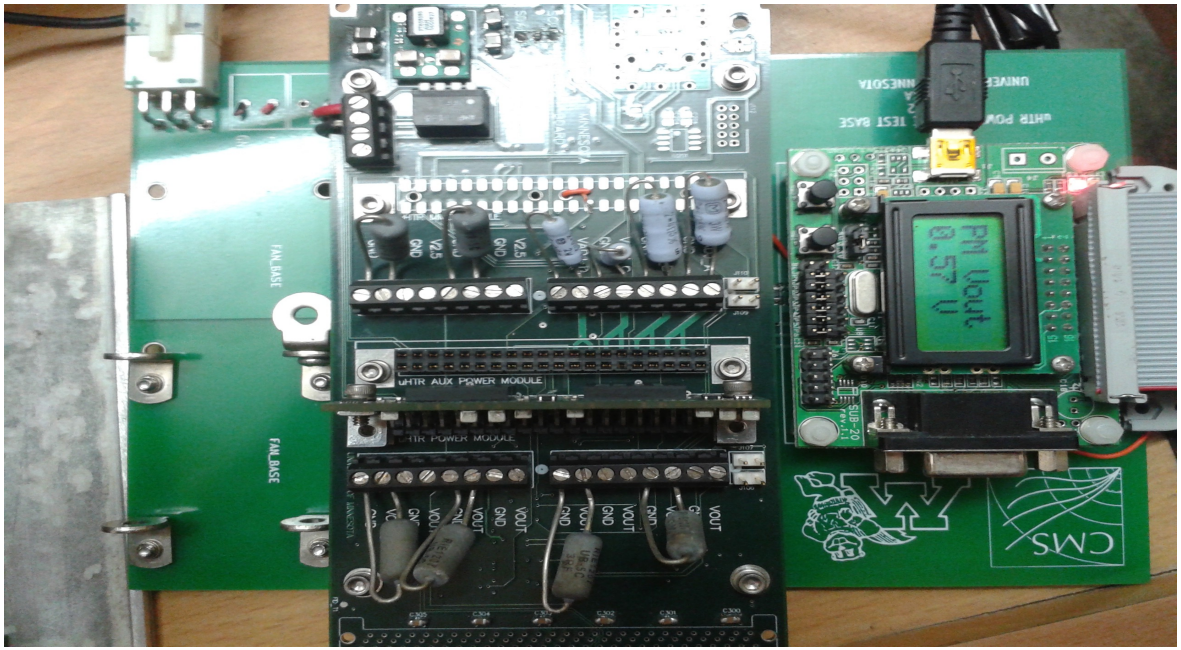

PPOD RX
PPOD TX
Front FPGA
Back FPGA
Optical connector
JTAG
MMC
APM 1.8 V
PM 1.0 V
EPROM
APM 2.5 V
PM 1.0 V
PM 3.3 V

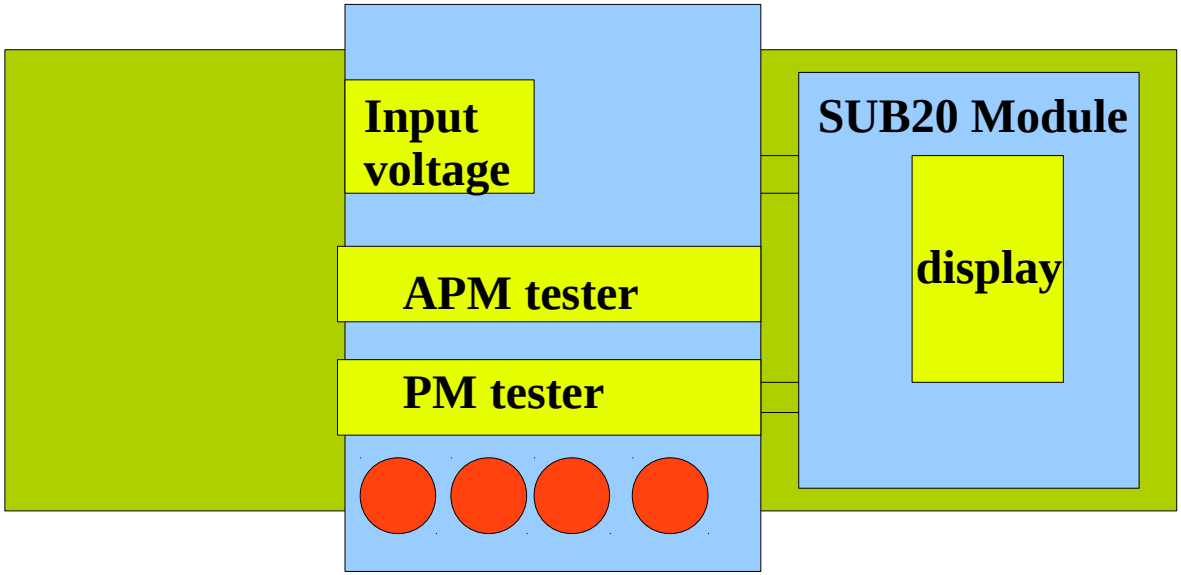
Need of PM test

- Power mezzanine provide required volatages to various parts of the µHTR.
- In any experiment power supply is the part which fails often or have problem.
  - If PM fails or malfunctions then we loose data collection efficiency
  - So, all power modules of the µHTR card will be tested for 20 hours.
- Each PM/APM have I2C chip on it which provides a unique id to the PM/APM.
  - Useful in maintaining database.
- I2C allow serial communication to other devices via two lines.
  - In our case SUB-20 is accessing the PM via I2C bus.
- 2 ADC continuously monitors T, V, I and digital I/O of the chip.
- Goal is to test all PM/APM @ SINP before mounting on µHTR.
- Current design of µHTR allows replacing the PM/APM in case of failure.



Test Setup @ SINP



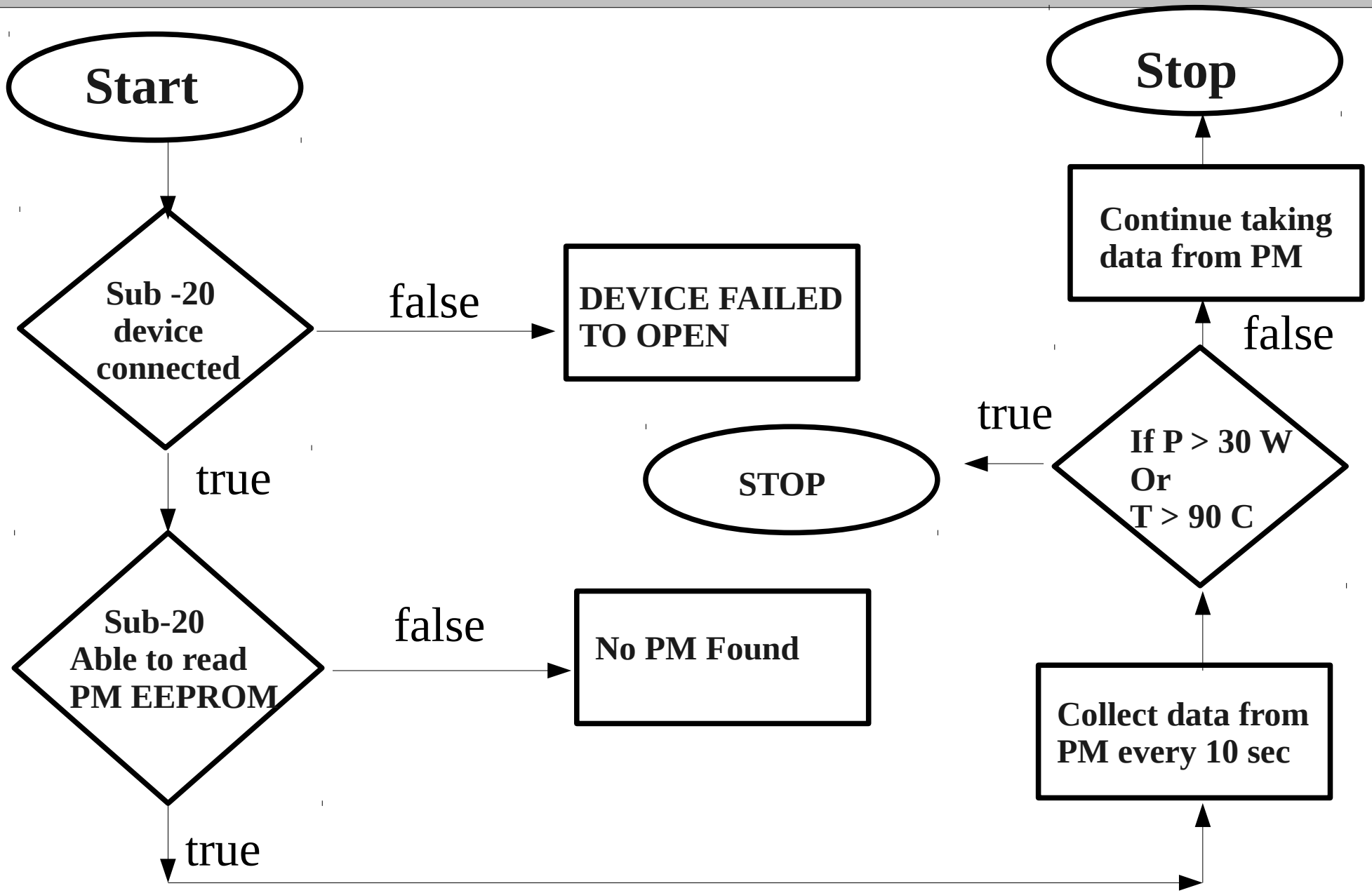


- PM is mounted on the test board as shown on left.
- Test board conneted to 12 V supply (~100W).
- SUB-20 is connected to PC via micro USB cable
- SUB-20 can talk to PM/APM via I2C chip on them.
- This configuration allows us to monitor the temperature, voltage and current drawn by the PM/APM.
- test carried out for 20 hrs for each PM/APM to monitor its stability.

How test is conducted ?

- Connect the test board to power supply
- Switch on the cooling fan.
- Connect the SUB-20 module and PC via μUSB cable.
- If this is done : ready for test !!
- Test is conducted by a C++ code using already implemented functions inside libsub and libusb.
- Code structure :
  - (A) Interface SUB-20 & PC
    - To check if SUB-20 module is connected
    - How many SUB-20 are connected
  - (B) Interface PM to SUB-20
    - Check connections and communicate with I2C bus inside PM
  - Main
    - Running & steering A & B
    - Which test to run
    - For how long
    - Debugging .,...

How test is conducted ?

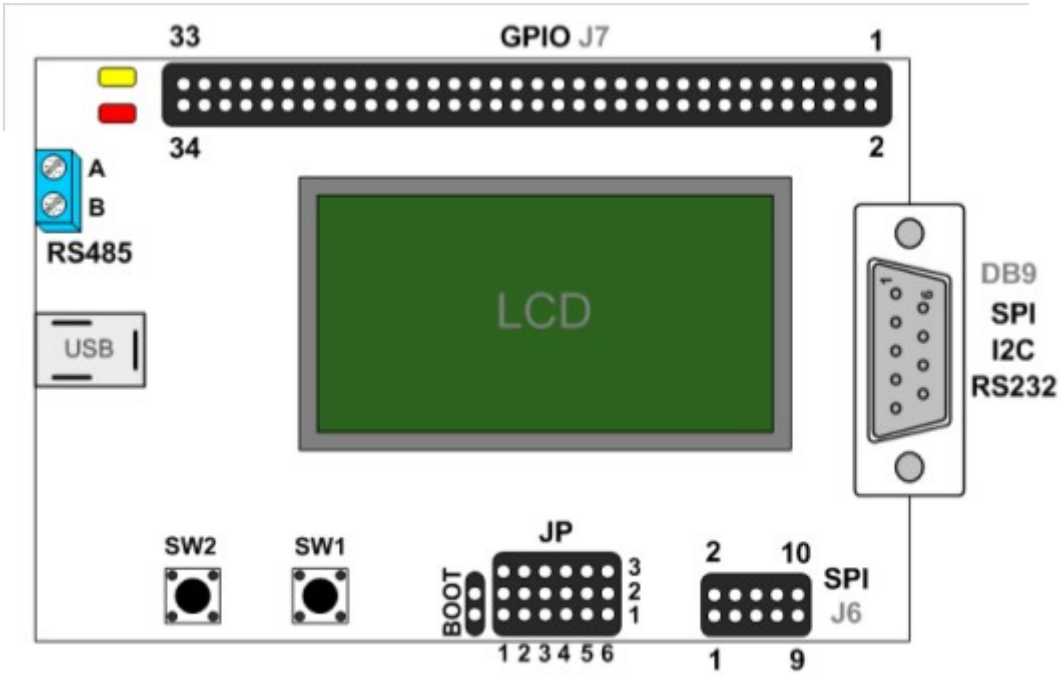


Plans

- All needed setup is now available for testing.
- We will test all PM/APM @ SINP before mounting them on μHTR card.
- Test new μHTR cards at P5 once they are ready for pre-production review.

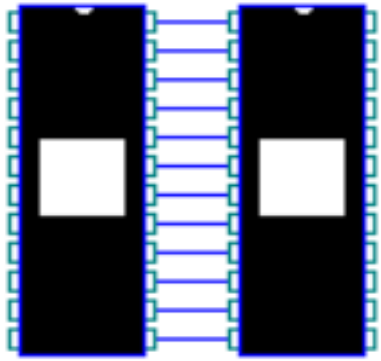
SUB-20

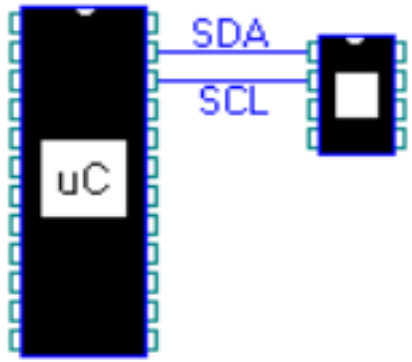
- SUB-20 is a versatile and efficient bridge device providing simple interconnect between PC (USB host) and different HW devices.
- Connect to HW via popular interfaces such as I2C, SPI, MDIO, RS232, RS485, SMBus, ModBus, IR
- It is also a full "any to any" converter between all supported interfaces and I/O features.
- SUB-20 is a powerful I/O controller with 32 GPIO, 8 Analog Inputs, PWM Outputs, Edge DEtectors, LCD, Leds and push buttons.



I2C Bus

- The Inter-integrated circuit bus
- Two wire , low-medium speed communication bus developed by Philips Semiconductors in the early 1980s.
  - Bus = a path for electronic signal
- Aim : reduce the manufacturing costs of electronic products
  - provides a low-cost, powerful, chip-to-chip communication link.
- Old days :
  - chip-to-chip communications used many wires in a parallel interface
  - often requiring ICs to have 24, 28, or more pins.
  - Many of these pins were used for inter-chip addressing, selection, control, and data transfers
  - In a parallel interface, 8 data bits are typically transferred from a sender IC to a receiver IC in a single operation
- Now :
  - performs chip-to-chip communications using only two wires in a serial interface
  - allowing ICs to communicate with fewer pins
  - The two wires in the I2C Bus are called Clock (SCL) and Data (SDA)
  - These two wires carry addressing, selection, control, and data, one bit at a time.
  - The SDA wire carries the data, while the SCL wire synchronizes the sender and receiver during the transfer.


Parallel Interface



I2C Serial Interface

Cheat Sheet

VME	VERSAbus Memory card
uTCA	Micro Telecommunications Computing Architecture
AMC	Advanced Mezzanine Card
MCH	UTCA carrier Hub
MMC	Mezzanine micro-controller card.
uHTR	Micro HCAL trigger & readout card
FEE	Front end electronics
I2C	IIC = inter integrated circuit
FPGA	Field programable gated array
PM/APM	Power module/Auxilary power module

Cheat Sheet

PPOD	Pluggable, Parallel-Fiber-Optic Transmitter / Receiver
MTP	Multi-fiber Termination Push-on : optical fibre connector

MCH1

- Support for 12 AMCs, 2 cooling units, 1-4 power modules
- GigaBit Ethernet switching
- PCI Express switching
- Management Controller (MCMC)