The SPI protocol is a shift register protocol with a possible register size ranging from 8 bits to 16 bits [**?**, sec.15]. The communication protocol is designed to keep the size of the datagram less or equal to the register size. This is to ensure a simple protocol between the Tiva and FPGA, which is still able to utilize the full duplex capabilities of a SPI protocol. The communication protocol uses the master-slave principle with the Tiva as the master and the FPGA as the slave.
When the Tiva initializes communication "Slave Enable" is driven low and one SPI clock cycle later, data will be read on rising edge from the SPI clock, as seen in figure 1. The datatypes transmitted between the FPGA and Tiva through SPI can be seen on table 1.

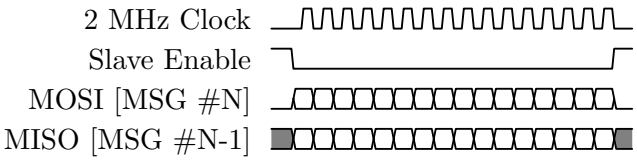

Figure 1: *SPI timing diagram*

Data	**Data type**
PWM	9 bit signed
Position	12 bit signed
Velocity	12 bit signed
Amps	12 bit unsigned
Home Index	1 bit

Table 1: *Data types*

Each datagram is 16 bits in size and the datagram format sent by the Tiva can be observed in table 2 and 3

Resp. select -¿ response select

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PWM - 9bits									MS	Resp. select		RS	Reserved		

Table 2: *Package format - Tiva*

MS	Motor Select	
Response select		
	Position	00
	Velocity	01
	Acceleration	10
	Amps	11
RS	Reset Position	

Table 3: *Package format extended*

while the package format send by the FPGA can be observed in table 4. In the package format the bit number indicates the order of transmission starting with 0.

Hvad er HS1 o HS0 ? uddyb mere evt.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Res		HS1	HS0	Requested Data											

Table 4: *Package format - FPGA*