0.0.1 Definition

Full duplex, 2MHz, Read on rising edge.
When communication initiates, Slave Enable is driven low and 1 SPI clock cycle later data will be read on rising edge from the SPI clock, as seen in figure 1.
Each datagram is 16 bits in size and the package format send by the Tiva can be seen in table 2 and the package format send by the FPGA can be seen in table 4. In the package format the bit number indicates the order of transmission starting with 0.

Hvordan refererer vi til Tivaen

Data	**Datatype**
PWM	9 bit signed
Position	12 bit signed
Velocity	12 bit signed
Amps	12 bit unsigned
Home Index	1 bit

Table 1: *Data types*

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PWM - 9bits									MS	Resp. select		RS	Reserved		

Table 2: *Package format - Tiva*

MS	Motor Select	
Response select		
	Position	00
	Velocity	01
	Acceleration	10
	Amps	11
RS	Reset Position	

Table 3: *Package format extended*

Table 4: *Package format - FPGA*

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Res		HS1	HS0	Requested Data											

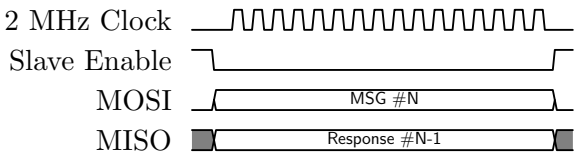

Figure 1: *SPI timing diagram*