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Istanbul Technical University

Department of Computer Engineering

BLG 231E - Digital Circuits

Assignment 4

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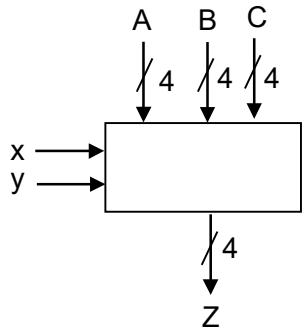
1. The combinational circuit shown on the right performs arithmetic operations on three 4-bit integers, A, B, and C based on the values of inputs x and y, as explained in the table below. We ignore carry, borrow, and overflow for this circuit.

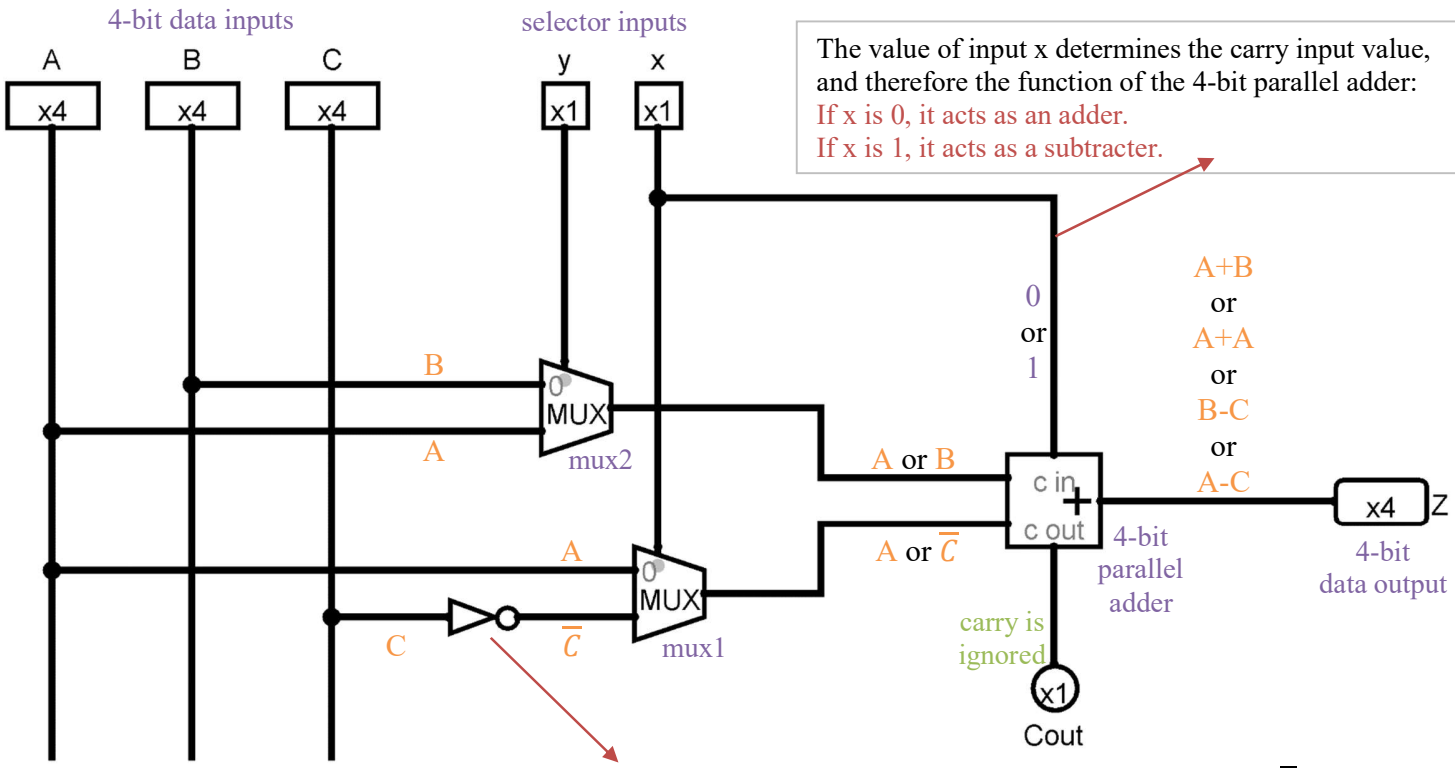
xy	Operation
00	Z = A + B
01	Z = 2A
10	Z = B - C
11	Z = A - C



Design this circuit using **only a single parallel adder**, **two 4-bit 2:1 MUXs**, and **NOT gates**. Use **the fewest possible number** of gates and multiplexers to make your circuit design as simple as possible. (**Note:** A 4-bit 2:1 MUX has **two inputs**, each having a **size of 4 bits**.)

Implement and test the circuit using the Logisim tool. Do not show the internal structure of the parallel adder; show it only as a block. Fully label all inputs and outputs. Write your name and student ID at the top of the **.circ** file.

Explain briefly how your circuit works. Create a pdf file for your explanations.



With the NOT gate here, not the integer C but the 1's complement of C ($\overline{C}$) is the input1 of mux1. This is for taking the advantage of 2's compement operation while we use parallel adder as a subtracter.

When x=1, mux1 selects $\overline{C}$ and carry input value of the parallel adder is 1. In this case;
Z = <integer selected by mux2> + $\overline{C}$ + 1
Z = <integer selected by mux2> + 2's complement(C)
Z = <integer selected by mux2> - C
A subtraction operation is carried out by the parallel adder. In our case, it is either B-C or A-C depending on the value of input y.

When x=0, mux1 selects A and carry input value of the parallel adder is 0. In this case;
Z = A + <integer selected by mux2> + 0
Z = A + <integer selected by mux2>
An addition operation is carried out by the parallel adder. In our case, it is either A+B or A+A depending on the value of input y.

While inputs of multiplexers are fixed, those of the parallel adder are not since they are a combination of the changable outputs of the multiplexers.

x	y	integer selected by mux1	integer selected by mux2	inputs of parallel adder	carry input	What happens through the circuit?	Z
0	0	A	B	A and B	0	x=0 → mux1 selects A y=0 → mux2 selects B x=0 → carry input is 0 } these ara added by the parallel adder	A+B+0 = A+B
0	1	A	A	A and A	0	x=0 → mux1 selects A y=1 → mux2 selects A x=0 → carry input is 0 } these ara added by the parallel adder	A+A+0 = 2A
1	0	$\overline{C}$	B	B and $\overline{C}$	1	x=1 → mux1 selects $\overline{C}$ y=0 → mux2 selects B x=1 → carry input is 1 } these ara added by the parallel adder	B+$\overline{C}$+1 = B-C
1	1	$\overline{C}$	A	A and $\overline{C}$	1	x=1 → mux1 selects $\overline{C}$ y=1 → mux2 selects A x=1 → carry input is 1 } these ara added by the parallel adder	A+$\overline{C}$+1 = A-C