Project Report:

Implementation of Phase Locked Loops

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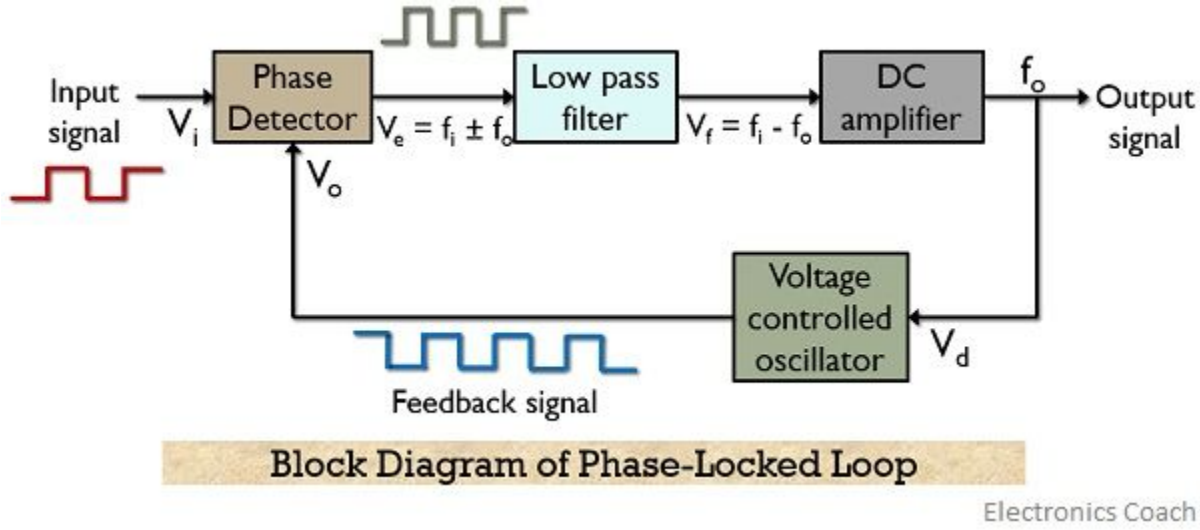
21EC37003.

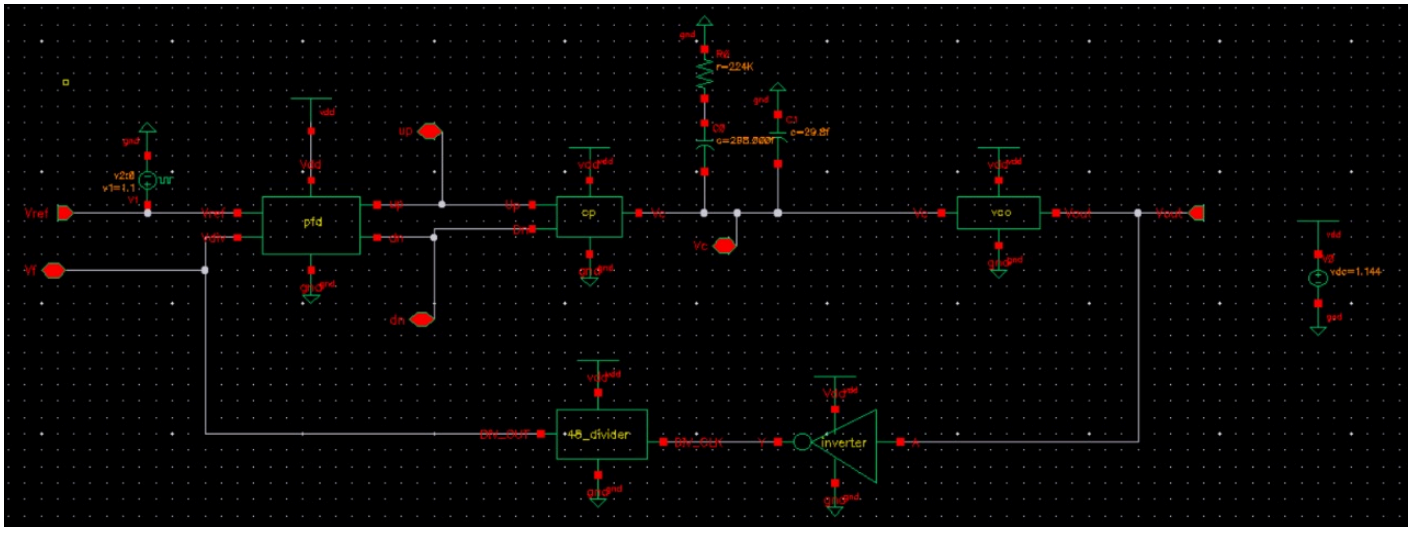
Aim:

To simulate the entire circuit for the phase-locked loops in 65-nanometer technology in Cadence software.

The phase-locked loops have a very large circuit and so many blocks; I had designed each block separately. The Block Diagram of the PLL is given below:



The final structure of the circuit implemented in the cadence is as follows:

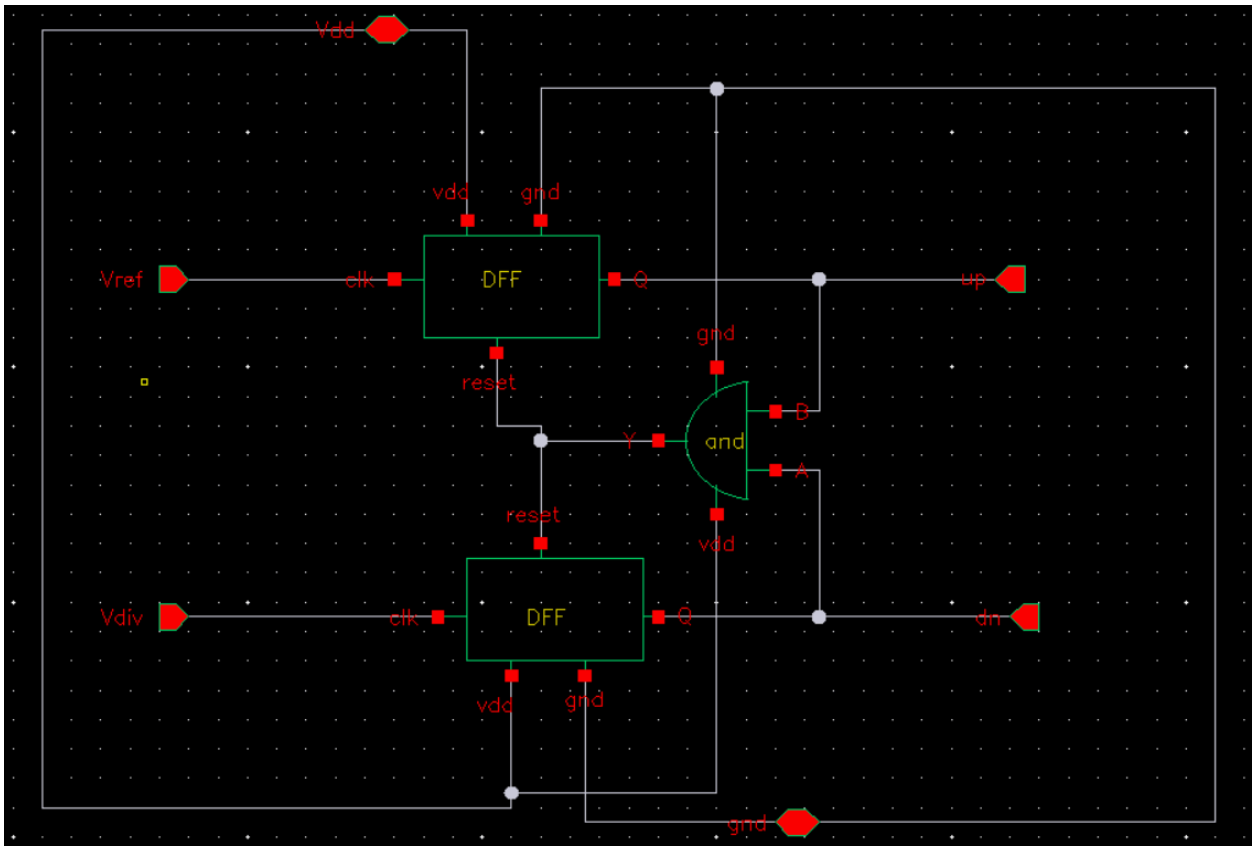


In the above circuit, there are the following blocks:

1. Phase Detector
2. Charge Pump
3. Voltage Controlled Oscillator
4. Divider(48).

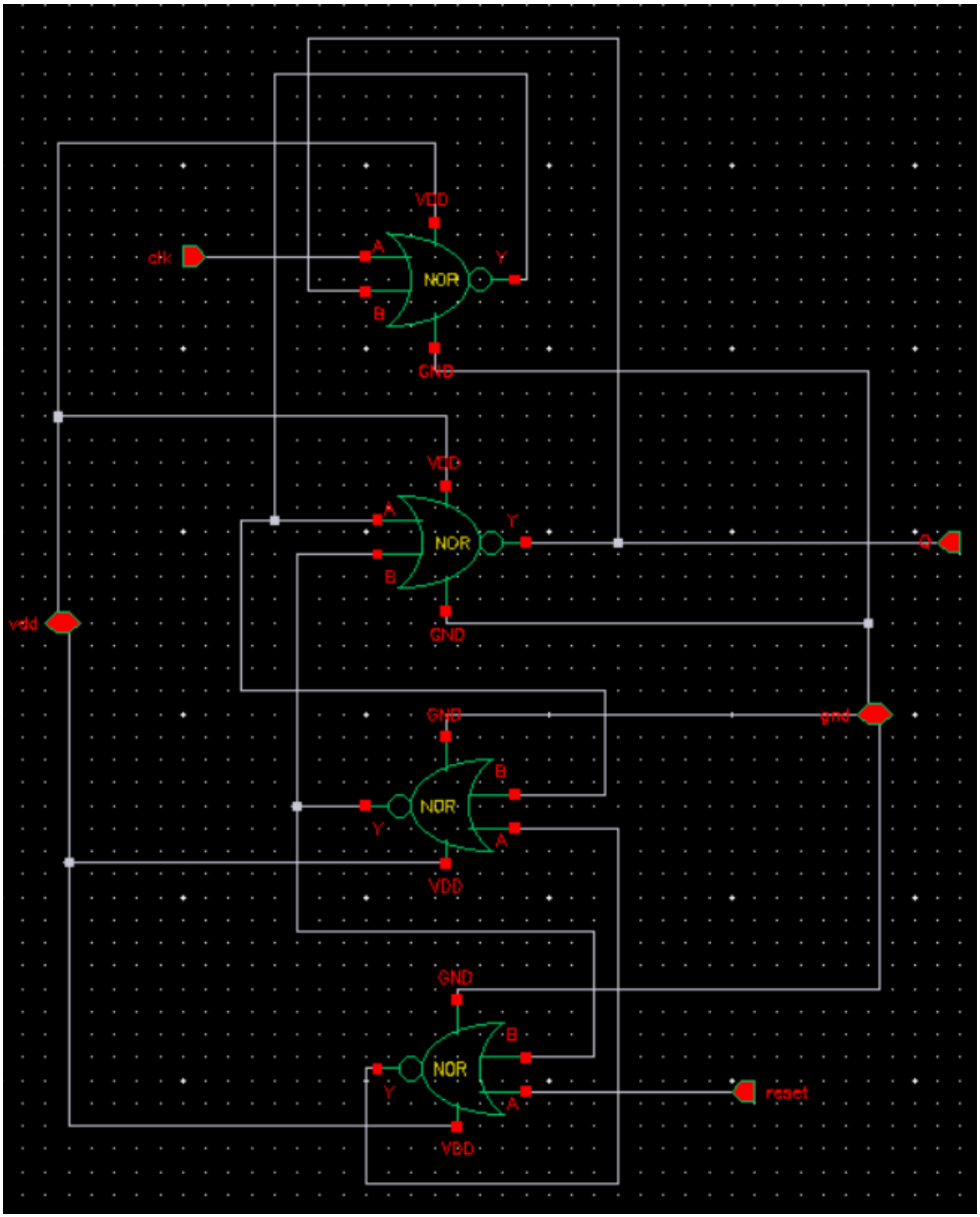
Each has been individually implemented and simulated with appropriate designs.

1. Phase Detector:

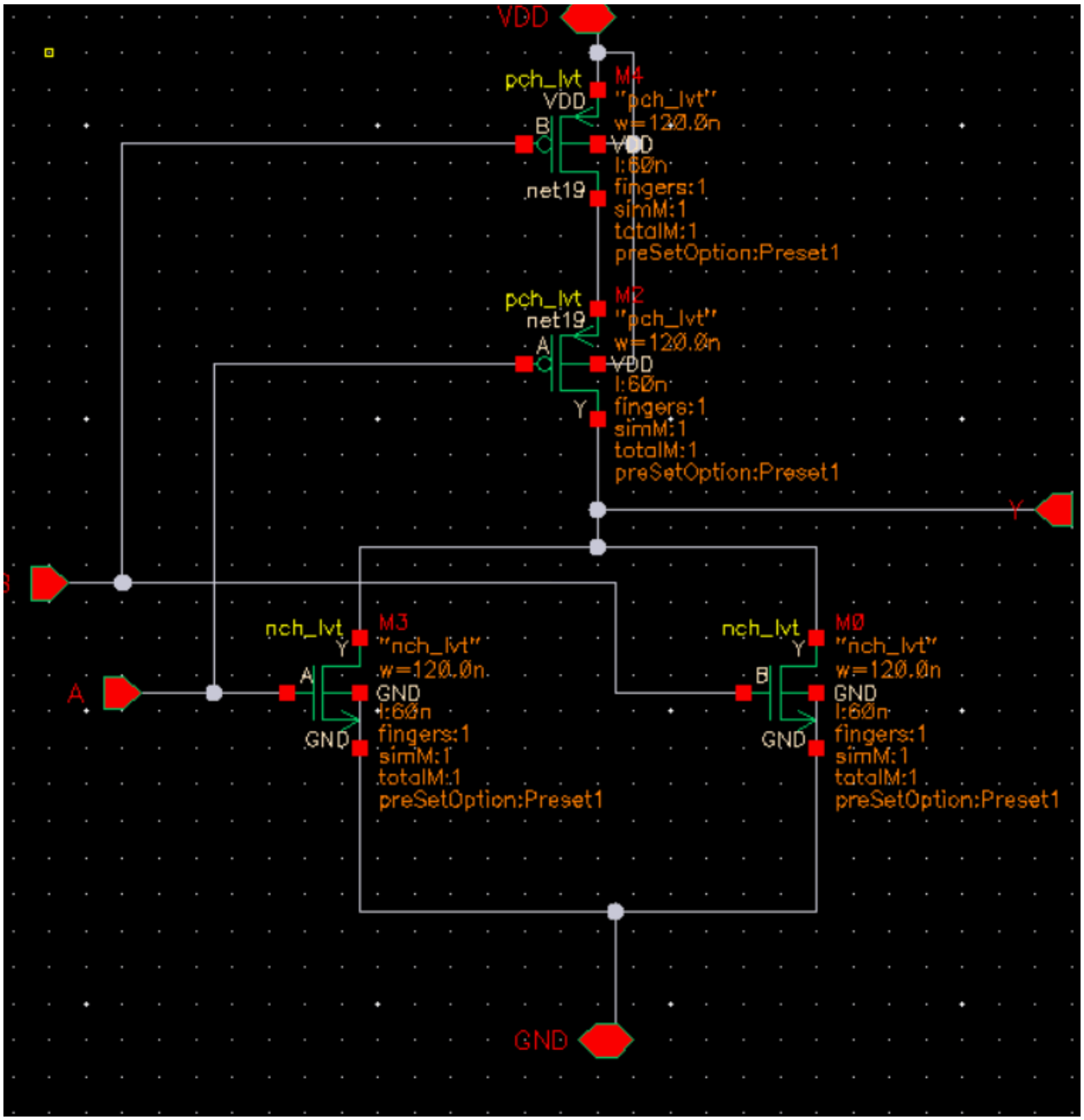


A phase detector is a crucial component in a phase-locked loop (PLL), responsible for comparing the phase of two signals and generating an error signal that helps synchronize the output frequency with the input frequency

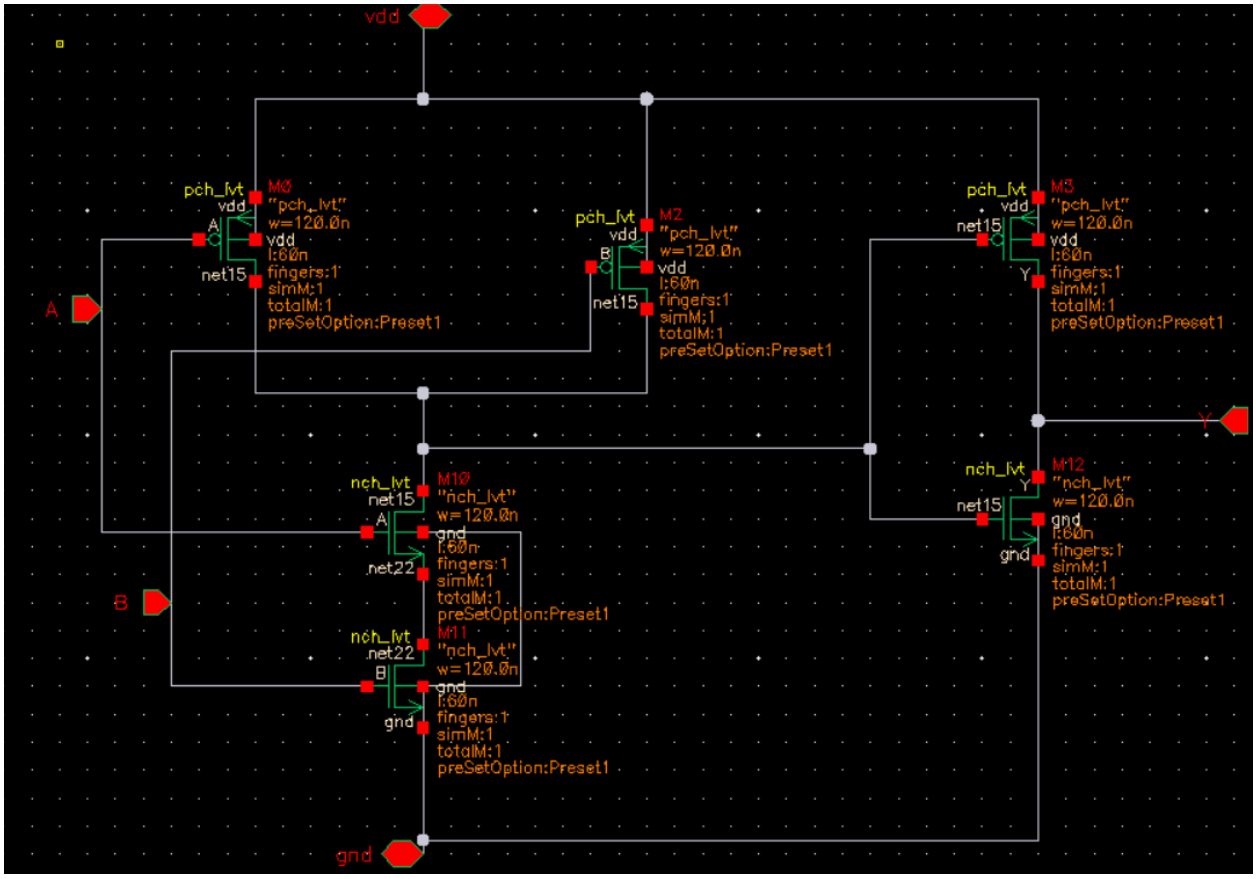
The above is the circuit of the phase detector. Here, D Flip Flops are also designed as below.



Nor gates are basic gates, and again, they are designed as follows:

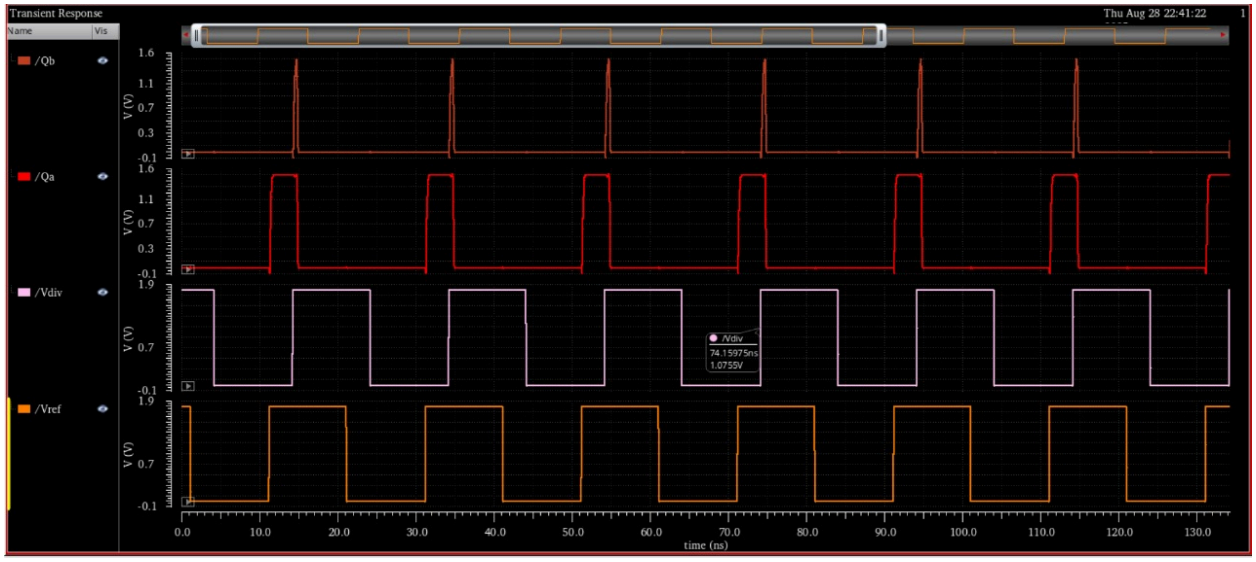


In this way, I had created the circuit for the nor gates. In between, there is an AND gate in the main phase detector circuit that is implemented as below.

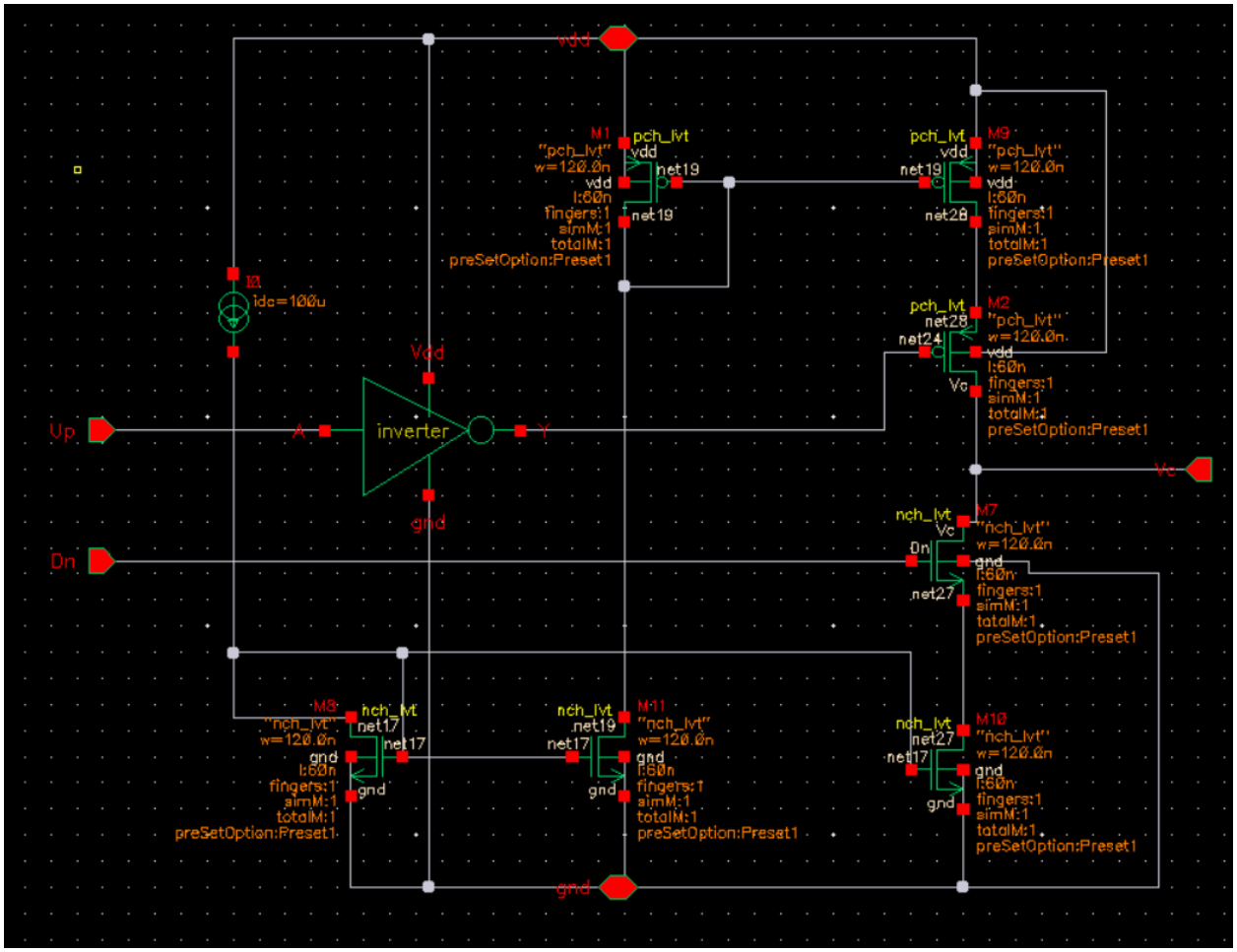


Coming to the measurements of the above schematics, I had taken the width of the nmos to be equal to 120 nanometers, and the width of the pmos is also taken as 120 nanometers. It has a power supply of 1.1 volts. And then all the connections are there.

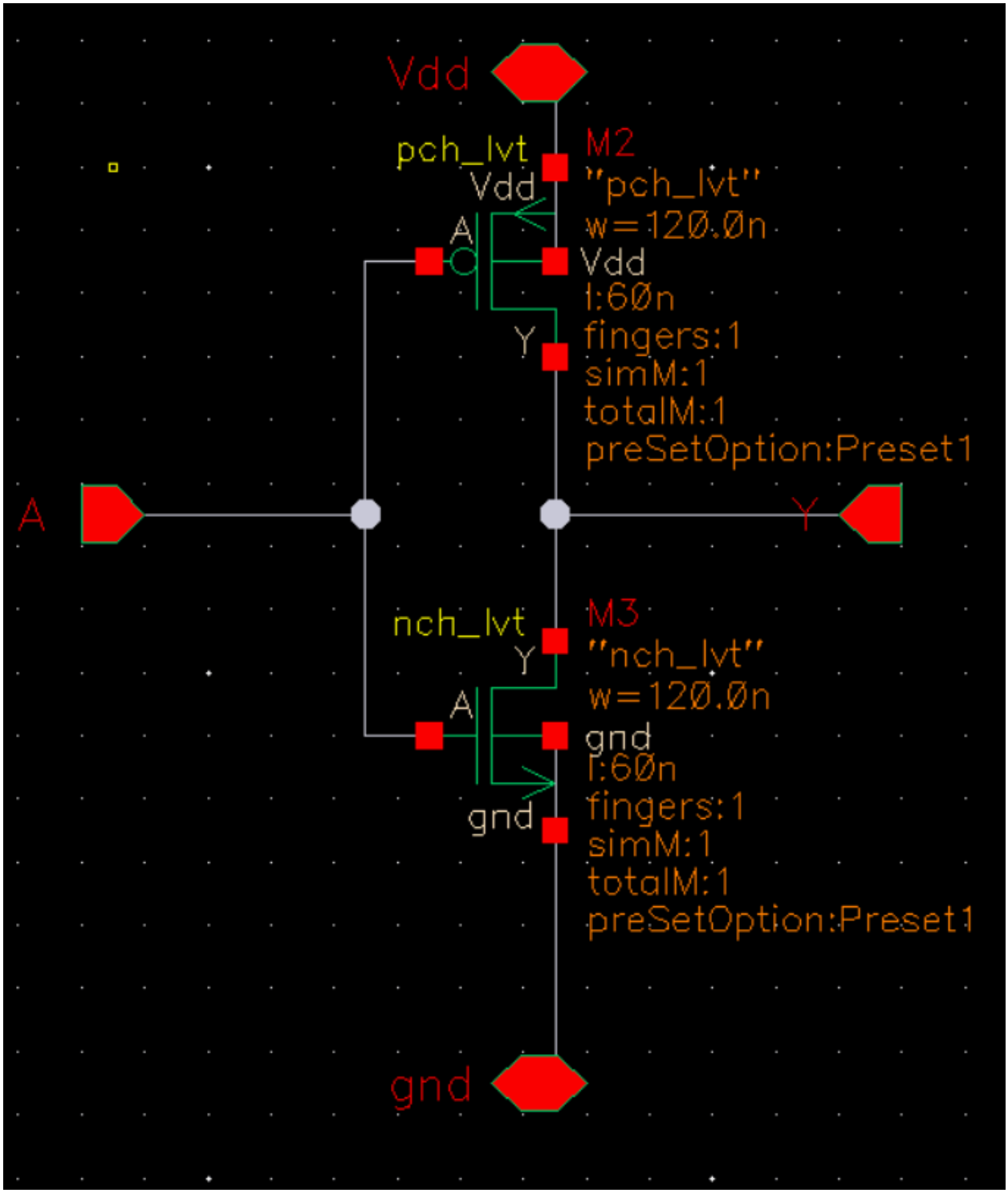
Testing:
Here, for the two inputs, we need to give two pulse signals, and when the main reference signal is lagging, then the down will be high till the lag is covered. And when the reference signal is leading, then the up signal will be high. This is clearly observed in the following plot.



2. Charge Pump Design:

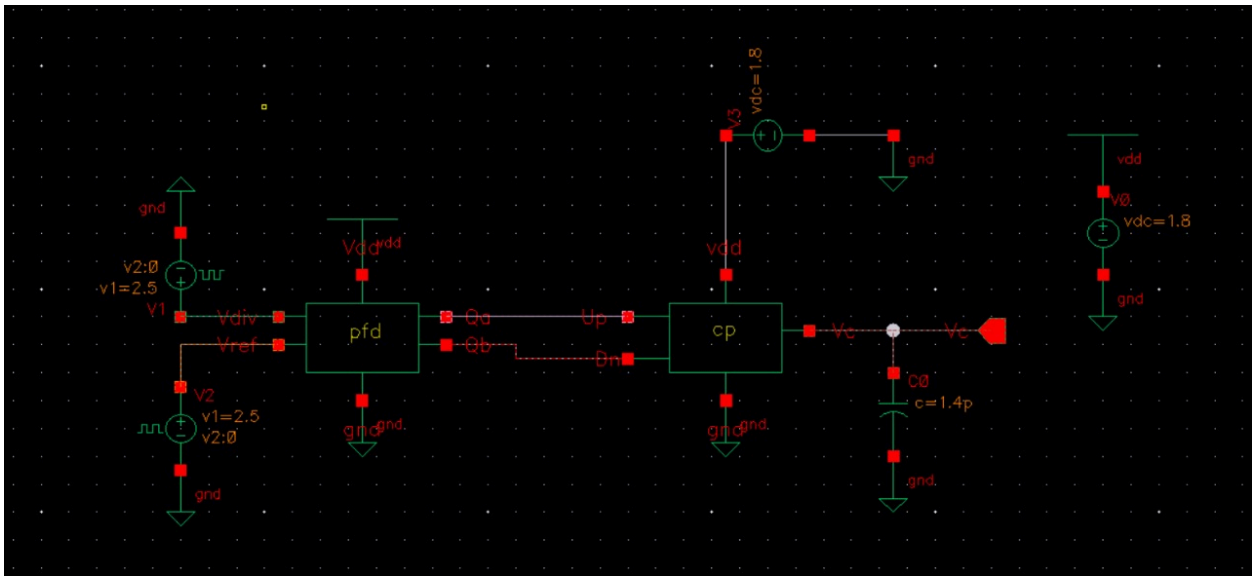


It contains an inverter in between, which is designed as follows:

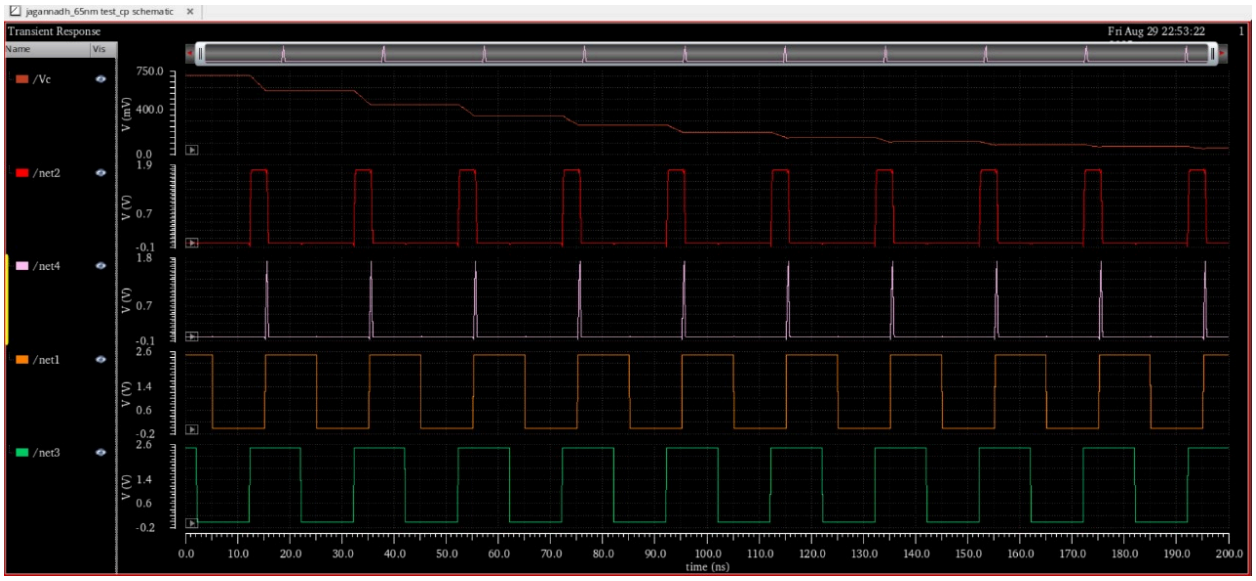


Now, here also, I had taken the same measurements for all the NMOS and the PMOS. The selected NMOS and PMOS in the Cadence software are:
Nch_lvt
Pch_lvt

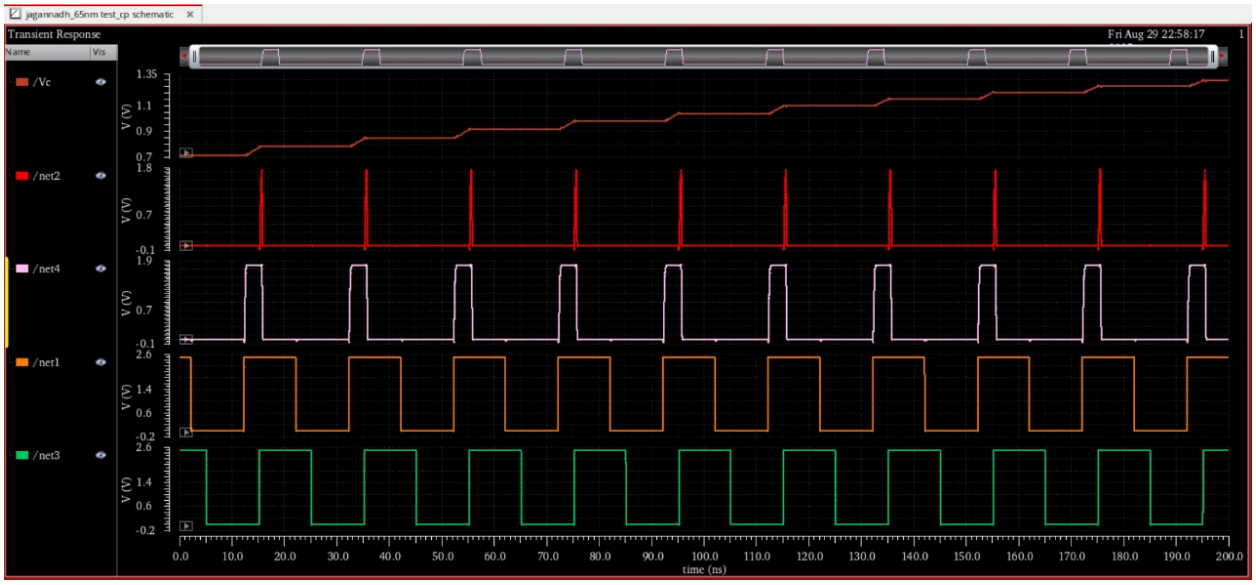
Output Testing plot:



Circuit combining both the PFD and the CP. For testing.
The output plots are as follows:

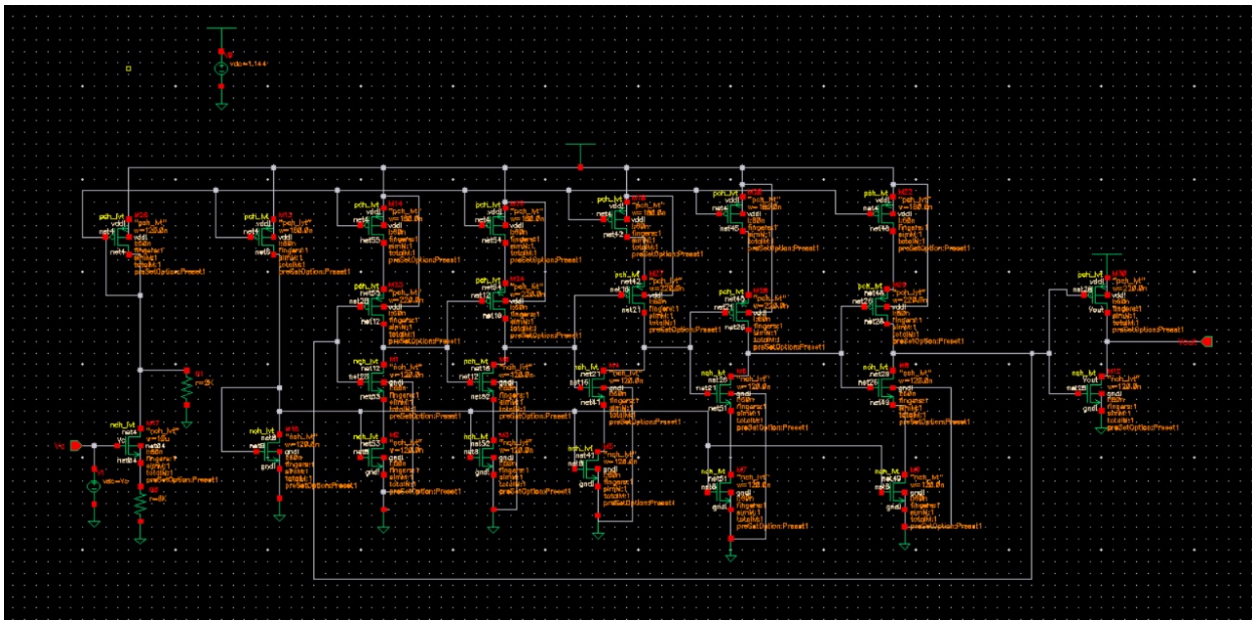


When the voltage is high then the charge pump decreases the value. As expected. When the down is high, the charge pump should increase its value. Which is in the next plot.



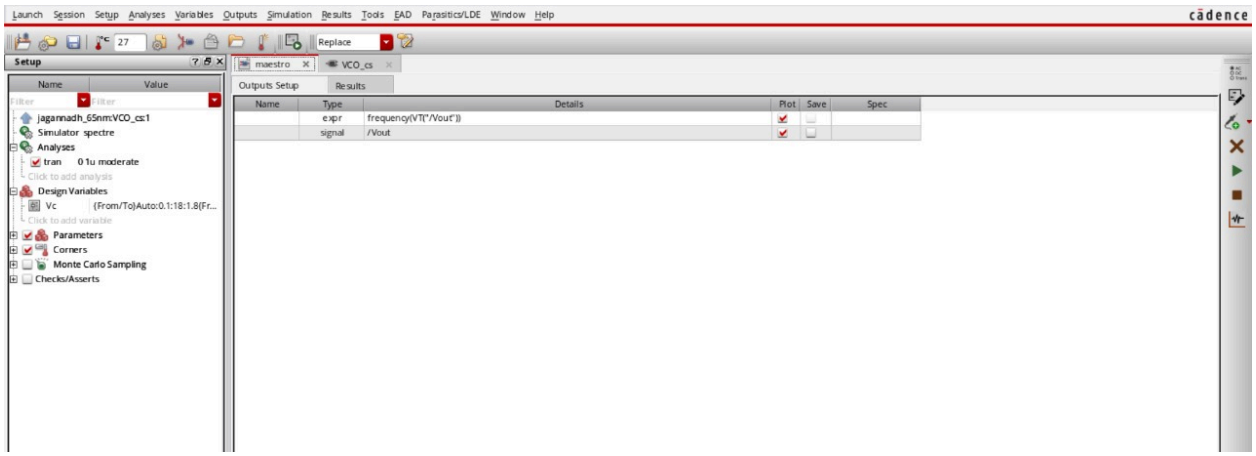
Hence, our charge pump and combined with the PFD are working perfectly.

3. Voltage Controlled Oscillator:

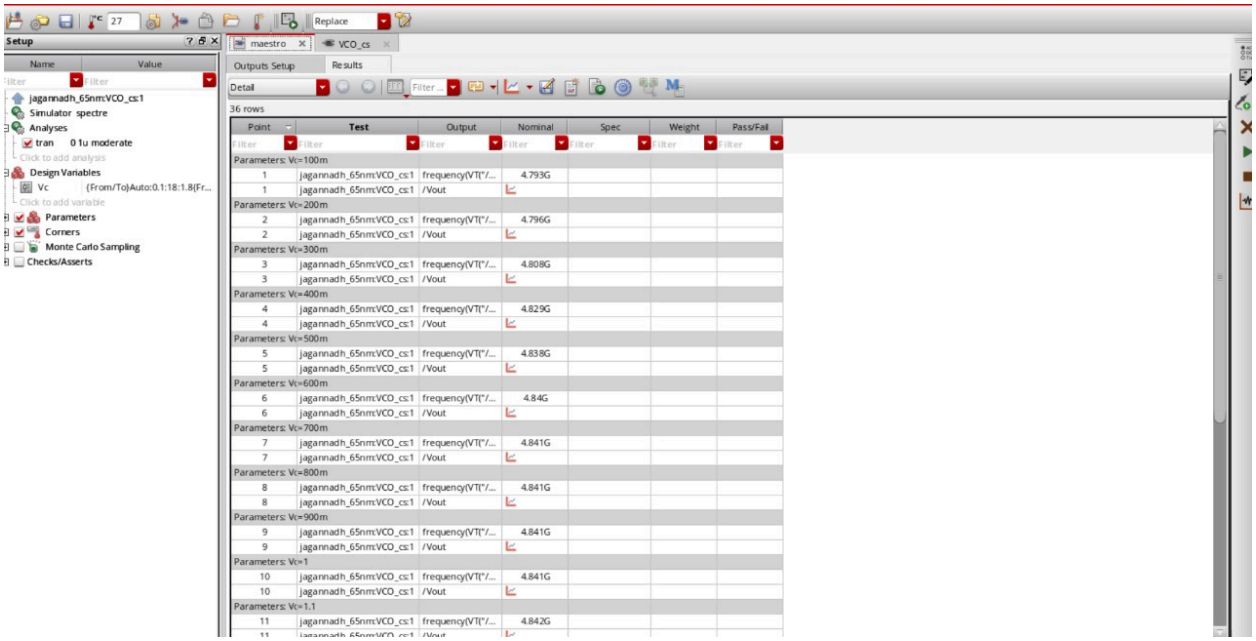


Here, the above circuit is the entire circuit for the VCO. The circuit contains 5 inverters with current mirrors attached to the PMOS as well as the NMOS. At the start, there is an input pin for the voltage control over the frequency we are obtaining from the VCO.

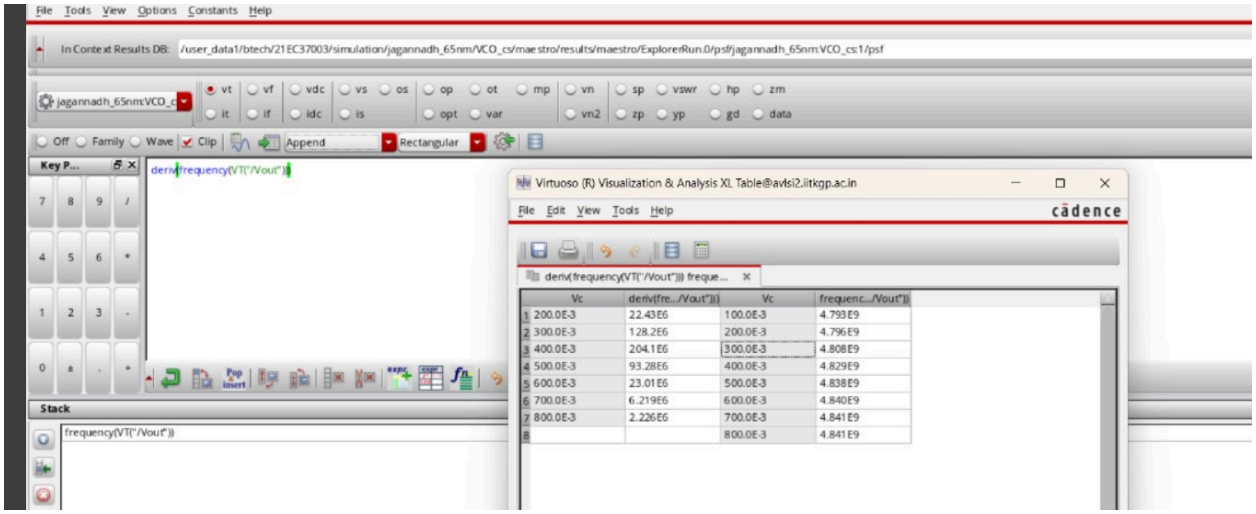
The Mastreo analysis set up for the above circuit is as follows:



The corresponding simulation results are:



Clearly, we can see the frequency we are obtaining is around 4.8 GHz, which is what I am designing.

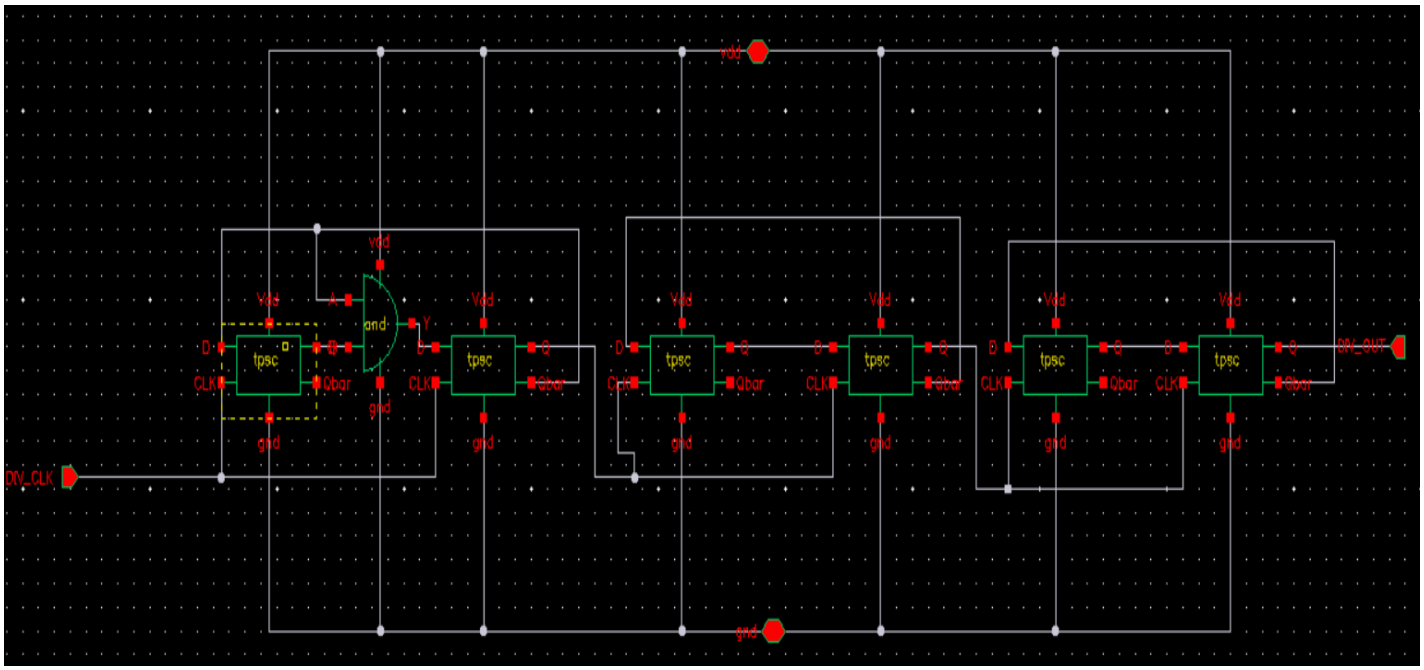


From the calculator in the tools, I had calculated the corresponding KVCO for the next step. Around 300mv, we are getting the frequency equal to 4.,8 and the kvco is also we are obtaining around 128.2E6. This value we are using for the next step.

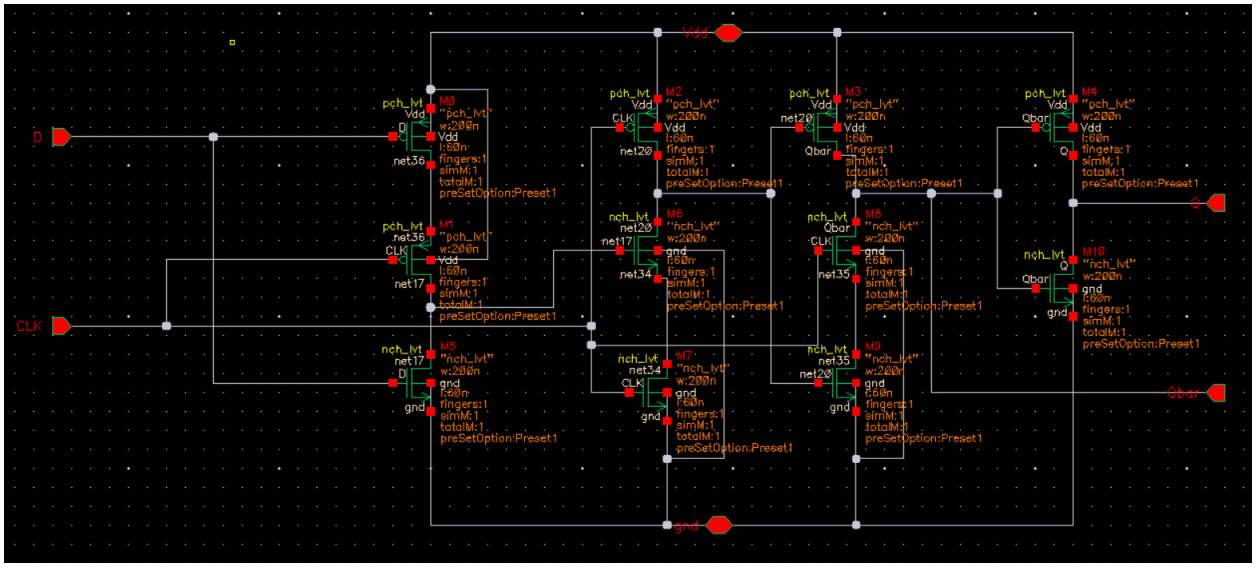
Parameters: Vc=300m			
3	jagannadh_65nm:VCO_cs:1	frequency(VT("/...	4.808G
3	jagannadh_65nm:VCO_cs:1	/Vout	

4. Divider Design:

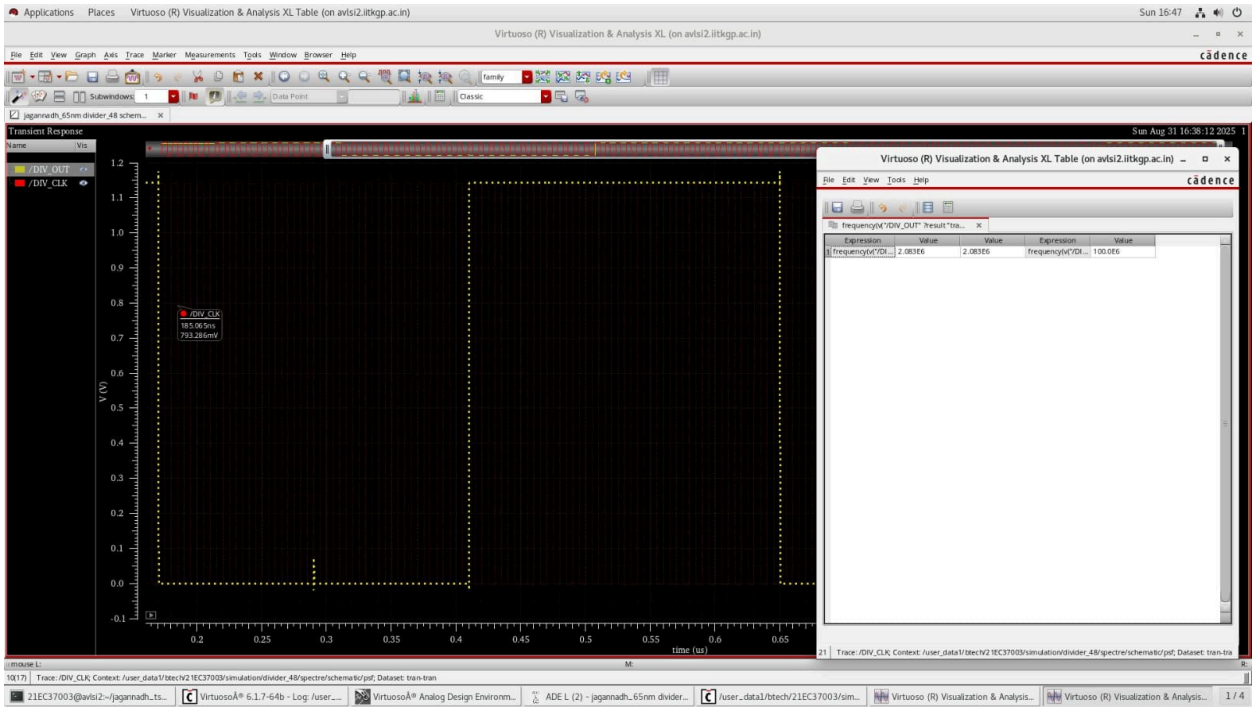
We are having many topologies for the driver design. I had chosen the TPSC divider, an easy and effective divider. I am dividing the input frequency by 48. The corresponding design is as follows:



The above circuit has TPSC, AND blocks used. And it is already designed in the starting portion. The circuit for the TPSC is as follows:

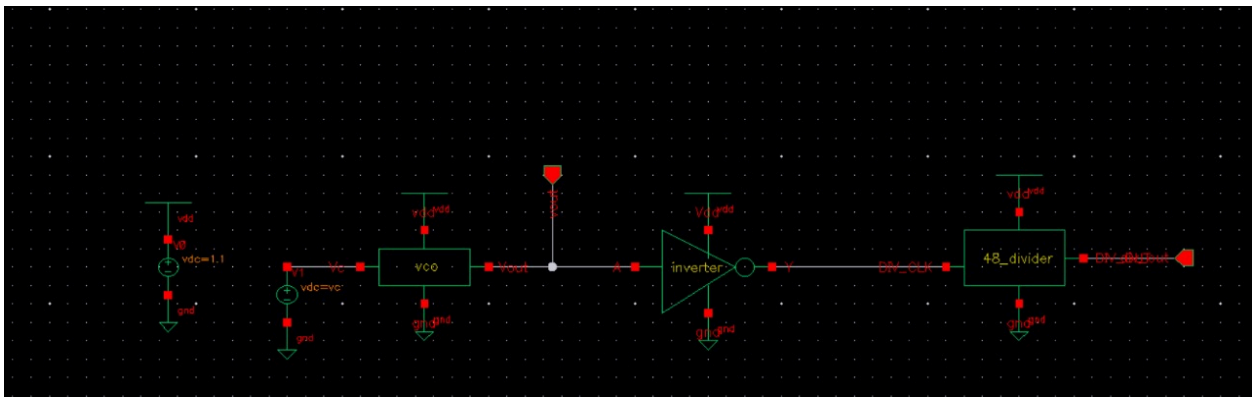


Testing:
Now, for this circuit, we are giving the input signal of high frequency, and we will get the output frequency to be very less.

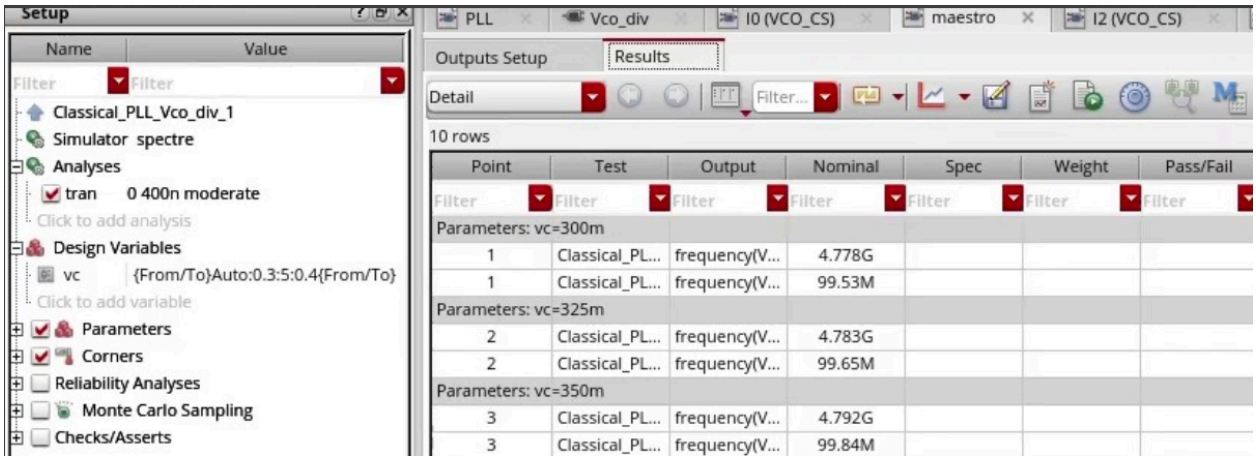


Here, the input signal has having frequency of 100MHz and the output frequency is 2MHz, which is calculated using tools -> calculator.

Hence, our Divider is also working.
Now we need to combine the entire circuit.
Here, before combining, we need to combine the VCO and the divider and check their performance. For that test circuit is as follows:

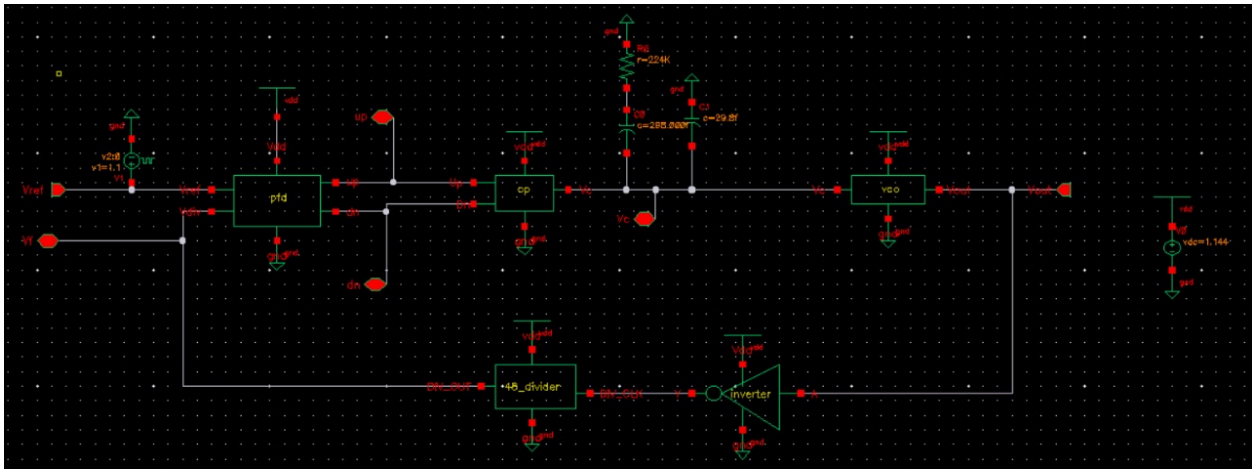


The corresponding maestro simulation is as follows:

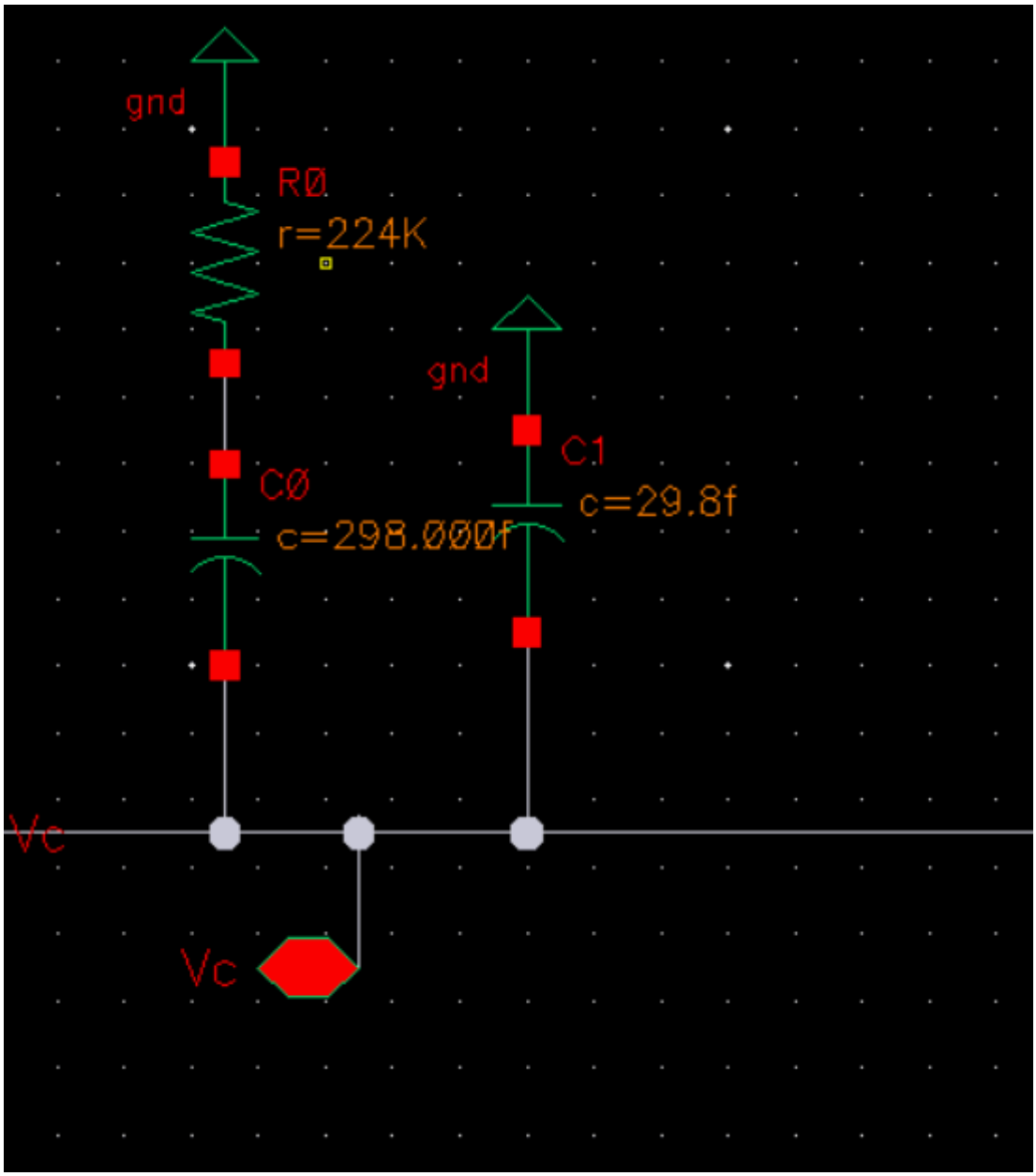


Clearly, we are getting the dividing operation working perfectly, and the VCO is also giving us the frequency close to 4.8 GHz. Hence, working perfectly.

Final Circuit:



Here, as in the above diagram, I had combined all the circuit elements into a single loop.
There are some hand calculations needed for the capacitor and the resistor part.


gnd
R0
r=224K
gnd
C1
c=29.8f
C0
c=298.000f
Vc
Vc

Hand Calculations for this are as given below:

PLL calculations

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Transfer function of type 2 PLL.

From simulation.

$K_{VCO} \rightarrow 128.2\ E6.$

$V_C = 300.e^{-3}$,

Frequency = 4.808 E9.

$\rightarrow \omega_n = \frac{2\pi f_n}{21}$

$C = \frac{R_1}{2}\sqrt{\frac{I_p K_{VCO} C_1}{2\pi M}}$

$\omega_n = \sqrt{\frac{I_p K_{VCO}}{2\pi M C_1}}$

$C_1 = \frac{J_p . K_{VCO}}{2\pi . \omega_n^2 . N}$

$\omega_u = 2.1\omega_n = \frac{\omega_{ref}}{10}$

Given, $I_p = 100\ MA$.

$K_{VCO} = 128.2\ MHz/V$.

ζ, damping factor = 1.

$f_{out} = 4.8\ GHz$, $N = 48$.

$K_{VCO} = 2\pi \times 128.2\ MHz/v$.

$\rightarrow f_s = \frac{f_{out}}{N} = 100MHz$.

$T_s = 1/f_s = 10ns$.

$T_{s/2} = T_s/2 = 5ns$.

$\omega_n = \frac{2\pi f_s}{21} \approx 2.991 \times 10^7 rad/s$.

$= 29.92 MHz$.

$C_1 = \frac{100 \times 10^{-6} \times 2\pi \times 128.2 \times 10^{-6}}{2\pi \times 29.92 \times 10^6 \times 29.92 \times 10^6 \times 10^7 \times 48}$.

$= \frac{128.2}{29.92 \times 10^6 \times 10^7 \times 29.92 \times 48}$.

0.00298×10^{-10}.

$= 0.298 \times 10^{-12}$.

$C_1 = 0.298 PF$.

$C_2 = \frac{0.298PF}{10}$

$= 0.0298PF$.

RT7 :

$$R_1 = 2(\zeta) \times \sqrt{\frac{2\pi N}{I_P \cdot K_{VCO} \cdot C_1}}$$

$$R_1 = 2 \times 1 \times \sqrt{\frac{2\pi \times 48 \times 10^{10}}{100 \times 10^{6} \times 2\pi \times 128 \cdot 2 \times 10^{6} \times 0 \cdot 298 \times 10^{-12}}}$$

$$= 2 \times \sqrt{\frac{48 \times 10^{10}}{128 \cdot 2 \times 0 \cdot 298}}$$

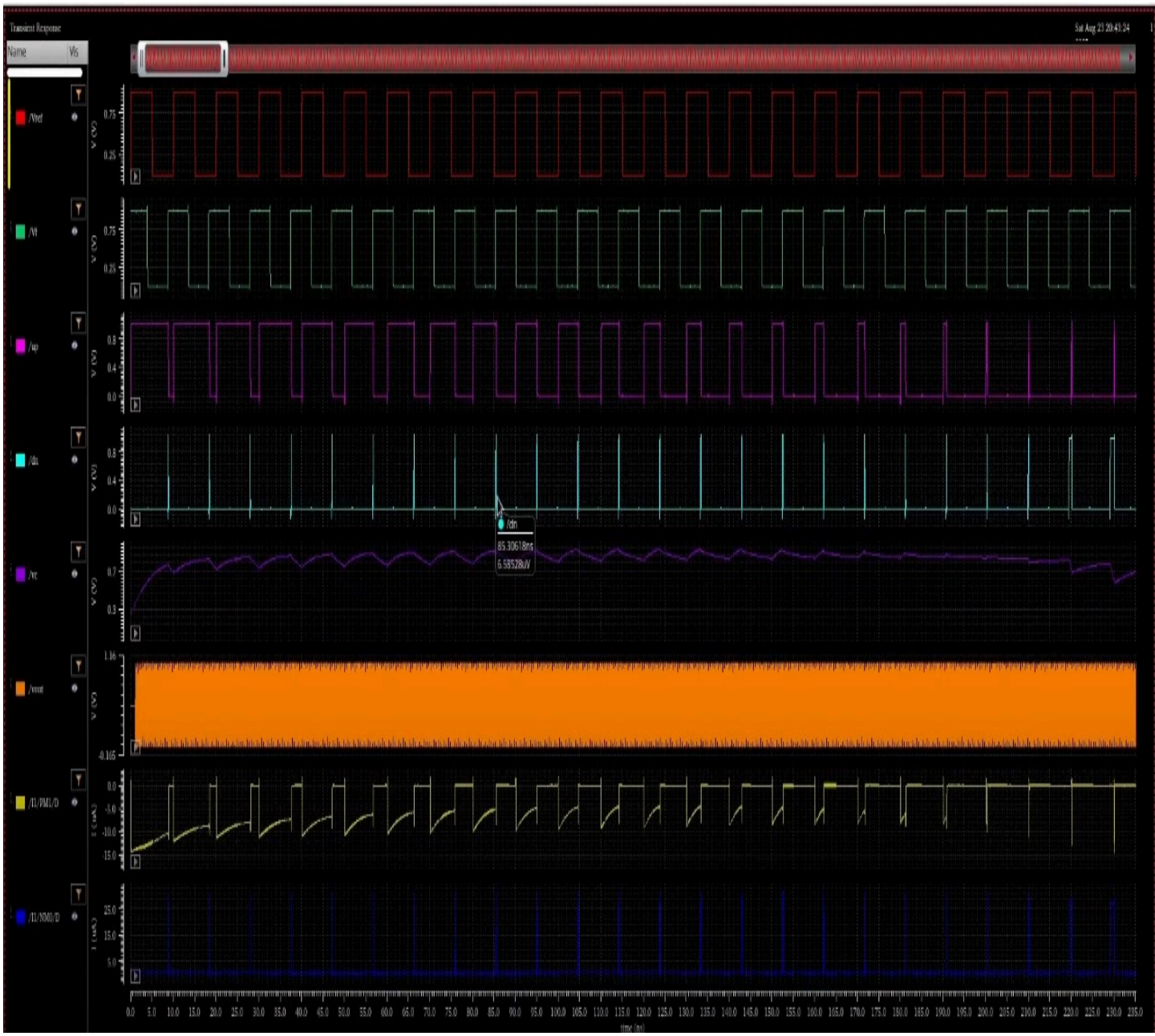
$$= 2 \times \sqrt{1 \cdot 256 \times 10^{5}}$$

$$= \cdot 2 \times 1 \cdot 12 \times 10^{5}$$

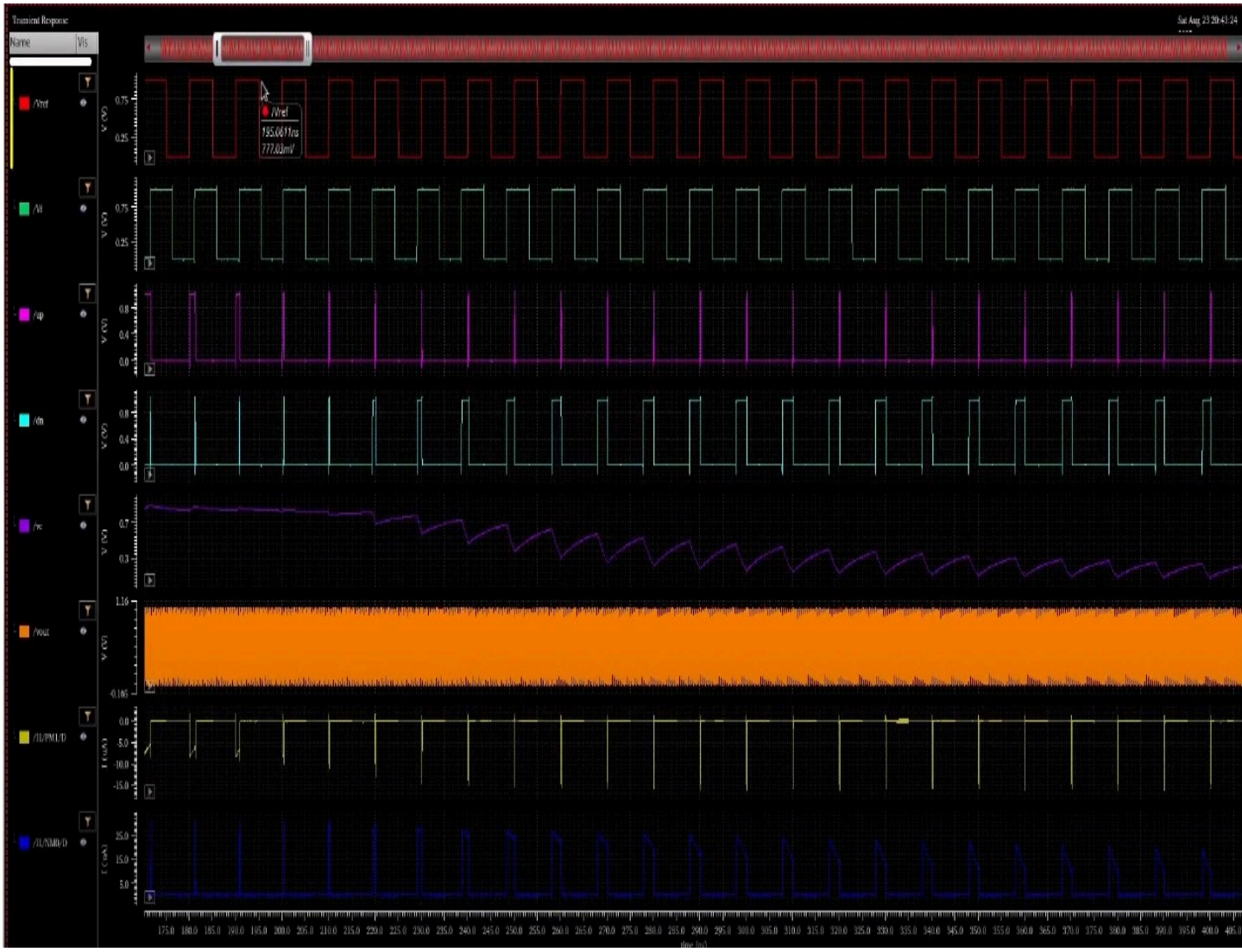
$$= 2 \cdot 24 \times 10^{5}$$

$$R_1 = \boxed{224\ k\Omega}$$

Final Resulting Waveform:

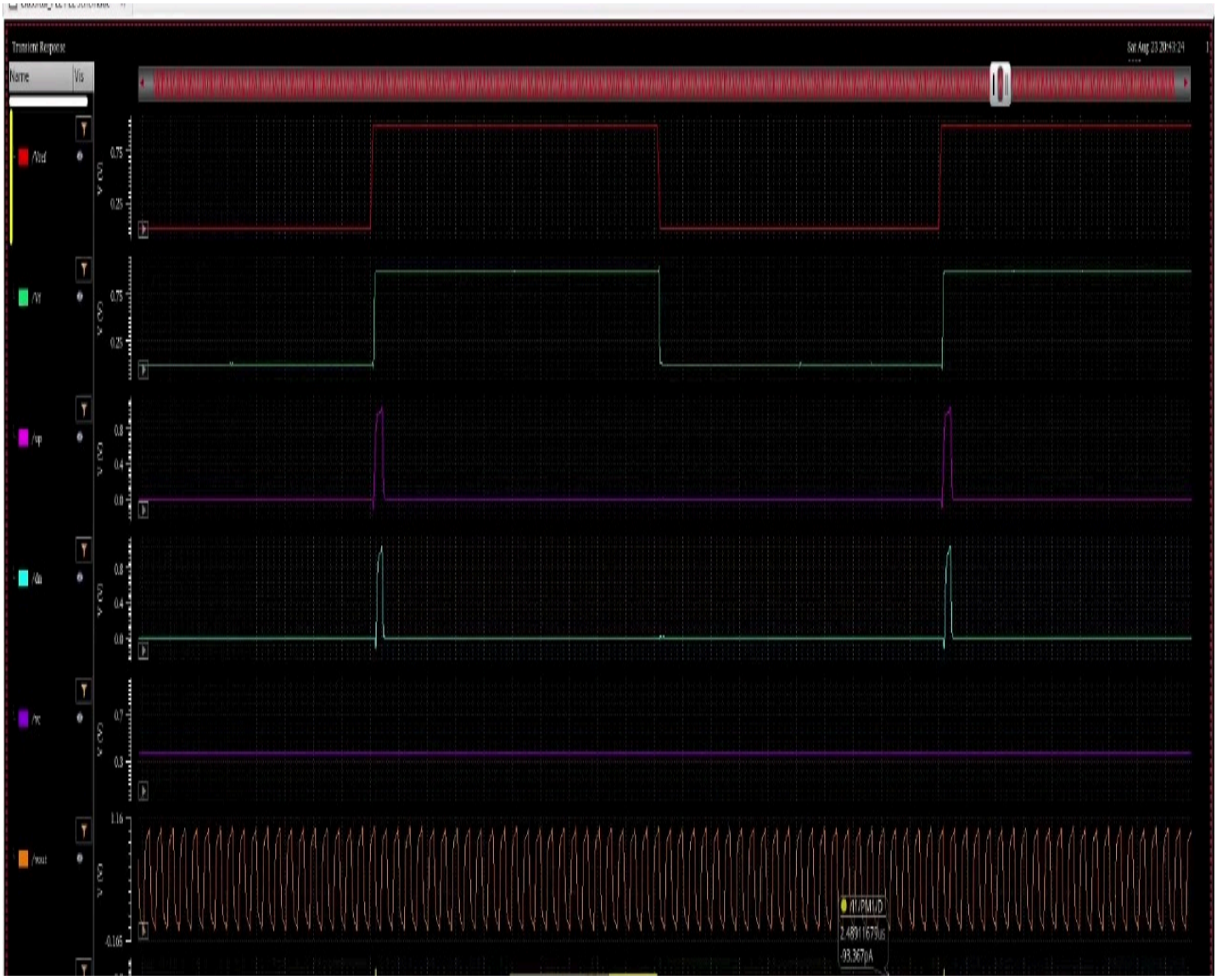


Initially, the up signal is very high, then later it starts decreasing, making the down signal to become slowly increase.

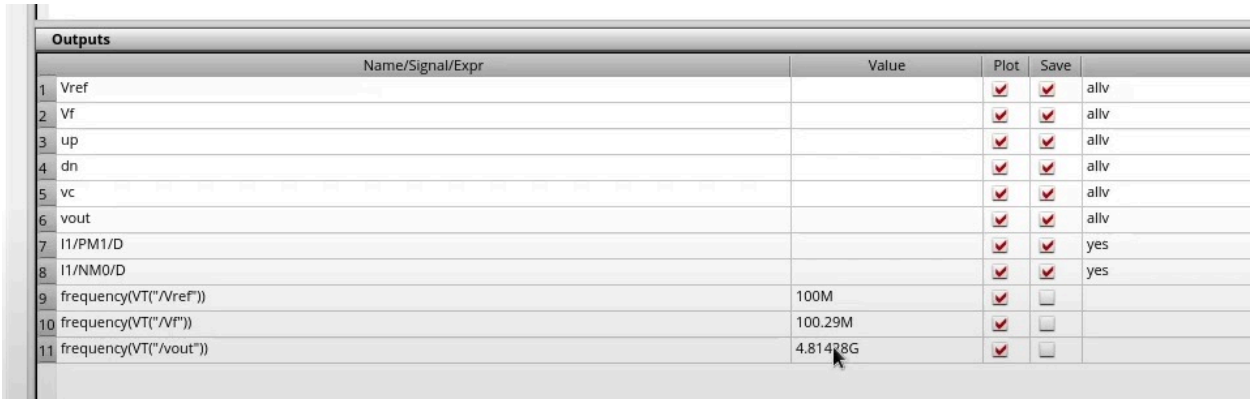


As in the above plot, the down signal is increasing gradually both the down and up signals will be becoming close to 0 leaving a single spike making the frequency set and locked without any changing. Without any lagging or leading.

The almost zero up and down image is given below:



Both the up and down signals are very small. The Vref and Vdiv are almost equal, hence our PLL is working absolutely fine.



Outputs

	Name/Signal/Expr	Value	Plot	Save	
1	Vref		☑	☑	allv
2	Vf		☑	☑	allv
3	up		☑	☑	allv
4	dn		☑	☑	allv
5	vc		☑	☑	allv
6	vout		☑	☑	allv
7	I1/PM1/D		☑	☑	yes
8	I1/NM0/D		☑	☑	yes
9	frequency(VT("/Vref"))	100M	☑	☐	
10	frequency(VT("/Vf"))	100.29M	☑	☐	
11	frequency(VT("/vout"))	4.81428G	☑	☐	

Thank You.

Regards,
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