



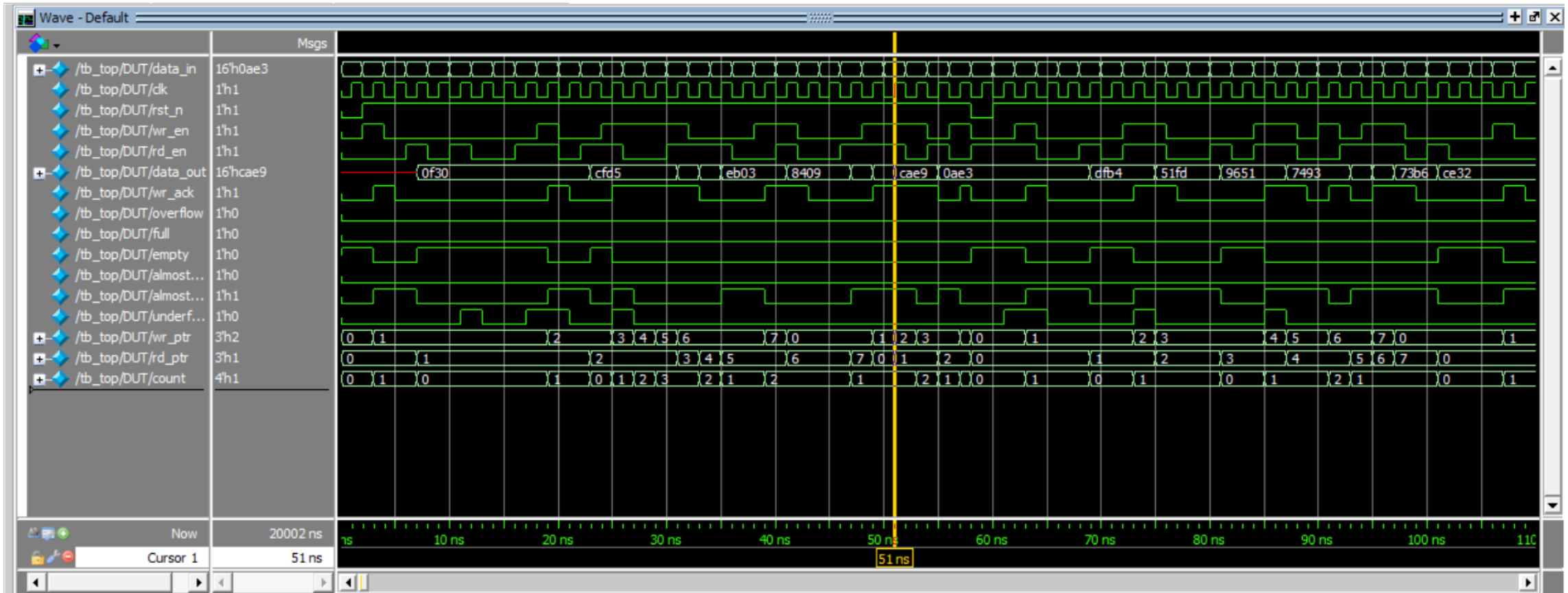
Asynchronous FIFO

complete top-level UVM environment

Verification plan

- Active reset at the first 2 cycle
- read when FIFO full
- Write when FIFO empty
- Write when FIFO not full
- read when FIFO not empty
- Check for Overflow and underflow when FIFO is empty or full
- Check internal signal
- constraint on reset to be most of time on active

Waveform

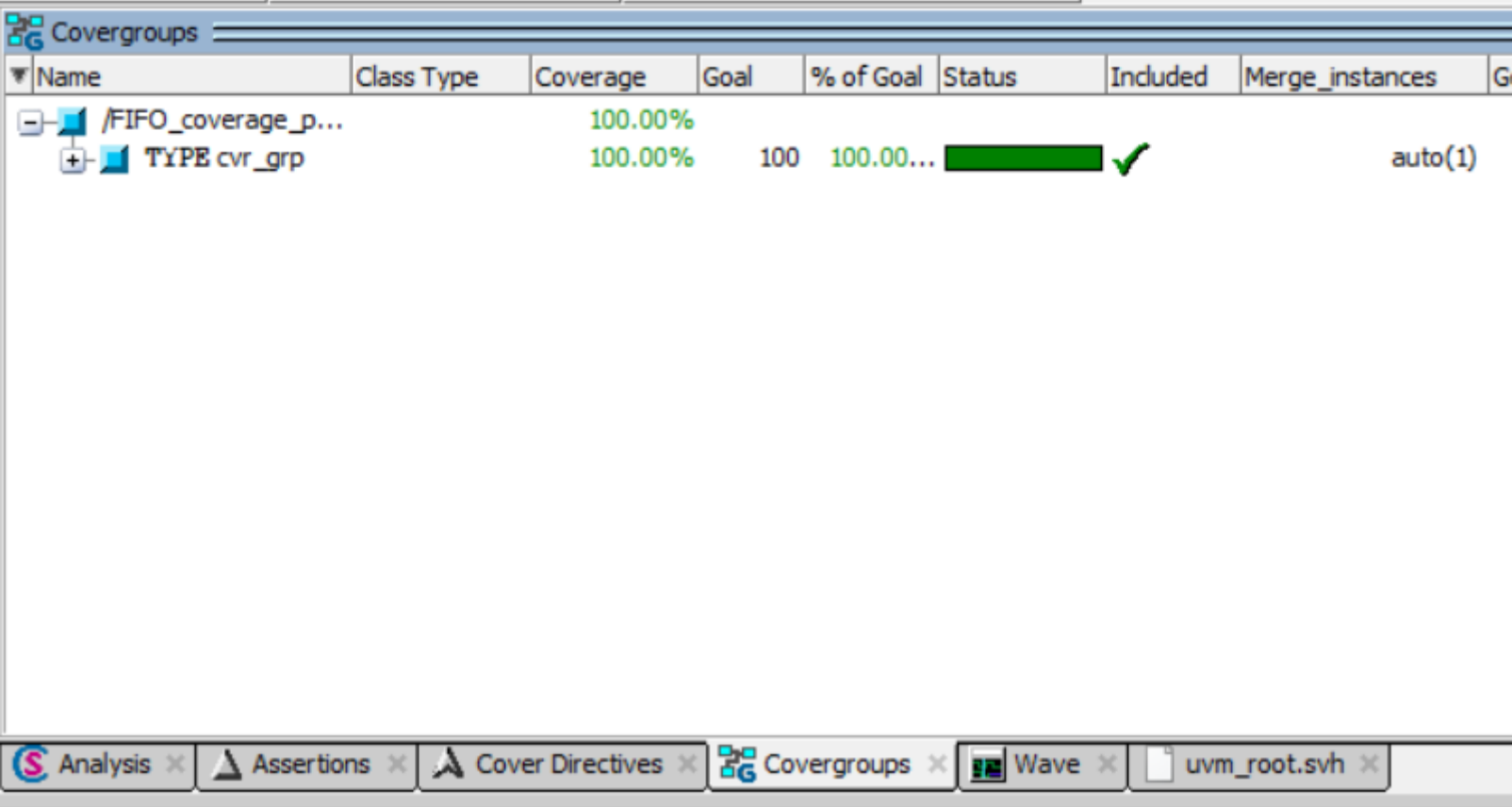


Cover Directive

Cover Directives																		
Name	Cover Type	Design Unit	Design Unit Type	Language	Enabled	Log	Count	AtLeast	Limit	Weight	Cmplt %	Cmplt graph	Included	Memory	Peak Memory	Peak Memory Time	Cumulative Threads	
/tb_top/DUT/full_c...	Concurrent	FIFO	Verilog	SVA	✓	Off	286	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/empt...	Concurrent	FIFO	Verilog	SVA	✓	Off	1504	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/almos...	Concurrent	FIFO	Verilog	SVA	✓	Off	584	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/almos...	Concurrent	FIFO	Verilog	SVA	✓	Off	2117	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/wr_ac...	Concurrent	FIFO	Verilog	SVA	✓	Off	4656	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/overfl...	Concurrent	FIFO	Verilog	SVA	✓	Off	139	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/under...	Concurrent	FIFO	Verilog	SVA	✓	Off	630	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/count...	Concurrent	FIFO	Verilog	SVA	✓	Off	2329	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/count...	Concurrent	FIFO	Verilog	SVA	✓	Off	2061	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/wr_e...	Concurrent	FIFO	Verilog	SVA	✓	Off	4795	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/wr_ful...	Concurrent	FIFO	Verilog	SVA	✓	Off	4963	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/wr_o...	Concurrent	FIFO	Verilog	SVA	✓	Off	5012	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/rd_un...	Concurrent	FIFO	Verilog	SVA	✓	Off	5037	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/wr_w...	Concurrent	FIFO	Verilog	SVA	✓	Off	5012	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/almos...	Concurrent	FIFO	Verilog	SVA	✓	Off	142	1	Unli...	1	100%		✓	0	0	0 ns	0	
/tb_top/DUT/almos...	Concurrent	FIFO	Verilog	SVA	✓	Off	489	1	Unli...	1	100%		✓	0	0	0 ns	0	

Analysis x Assertions x Cover Directives x Covergroups x Wave x uvm_root.svh x

Covergroup



Name	Class Type	Coverage	Goal	% of Goal	Status	Included	Merge_instances	G
/FIFO_coverage_p...		100.00%						
TYPE cvr_grp		100.00%	100	100.00...	<div></div> ✓		auto(1)	

Toggle coverage

Toggle Coverage:				
Enabled Coverage	Bins	Hits	Misses	Coverage
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Toggles	106	106	0	100.00%

Branch coverage

Branch Coverage:				
Enabled Coverage	Bins	Hits	Misses	Coverage
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Branches	27	27	0	100.00%

Statement coverage

Statement Coverage:				
Enabled Coverage	Bins	Hits	Misses	Coverage
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Statements	34	34	0	100.00%

Total coverage by instance

Total Coverage By Instance (filtered view): 100.00%

