Department of Computer Science and Engineering

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Submitted by:
Section: B
Name: Md. Farhad
ID: 20101073

Submitted to:

Shammi Akhtar
Assistant Professor
University of Asia Pacific,UAP

Question :

Find the number of misses for a cache with 16, 1-word blocks given the following sequence of memory block accesses:

0, 8, 0, 6, 8, 25, 13, 9, 8, 0 for each of the following cache configurations

a. direct mapped

b. 2-way, 4-way, 8-way and 16-way set associative (use LRU replacement policy)

c. fully associative

Solution :

a. direct mapped

sequence: **0, 8, 0, 6, 8, 25, 13, 9, 8, 0**

Block address	Cache block	Block address	Cache block
0	0 (= 0 mod 16)	25	9 (= 25 mod 16)
8	8 (= 8 mod 16)	13	13 (= 13 mod 16)
0	0 (= 0 mod 16)	9	9 (= 9 mod 16)
6	6 (= 6 mod 16)	8	8 (= 8 mod 16)
8	8 (= 8 mod 16)	0	0 (= 0 mod 16)

Address of memory block accessed	Hit/ Miss	Contents of cache blocks after reference															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Miss	M[0]															
8	Miss									M[8]							
0	Hit	M[0]															
6	Miss							M[6]									
8	Hit									M[8]							
25	Miss										M[25]						
13	Miss														M[13]		
9	Miss										M[9]						
8	Hit									M[8]							
0	Hit	M[0]															

no of hit = 4
no of miss = 6

b. i)2-way set associative:

Block Set = 16/2= 8

Now, we mod block address by 8

Block address	Cache block	Block address	Cache block
0	0 (= 0 mod 8)	25	1 (= 25 mod 8)
8	0 (= 8 mod 8)	13	5 (= 13 mod 8)
0	0 (= 0 mod 8)	9	1 (= 9 mod 8)
6	6 (= 6 mod 8)	8	0 (= 8 mod 8)
8	0 (= 8 mod 8)	0	0 (= 0 mod 8)

Address of memory block accessed	Hit/ Miss	Contents of cache blocks after reference															
		Set 0		Set 1		Set 2		Set 3		Set 4		Set 5		Set 6		Set 7	
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Miss	M[0]															
8	Miss	**M[0]**	M[8]														
0	Hit	M[0]	**M[8]**														
6	Miss													M[6]			
8	Hit		M[8]														
25	Miss			M[25]													
13	Miss											M[13]					
9	Miss			**M[25]**	M[9]												
8	Hit	**M[0]**	M[8]														
0	Hit	M[0]	**M[8]**														

no of hit = 4
no of miss = 6

ii) 4-way set associative:

Block Set = 16/4= 4

Now, we mod block address by 4

Block address	Cache block	Block address	Cache block
0	0 (= 0 mod 4)	25	1 (= 25 mod 4)
8	0 (= 8 mod 4)	13	1 (= 13 mod4)
0	0 (= 0 mod 4)	9	1 (= 9 mod 4)
6	2 (= 6 mod 4)	8	0 (= 8 mod 4)
8	0 (= 8 mod 4)	0	0 (= 0 mod 4)

Address of memory block accessed	Hit/ Miss	Contents of cache blocks after reference															
		Set 0				Set 1				Set 2				Set 3			
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Miss	M[0]															
8	Miss	**M[0]**	M[8]														
0	Hit	M[0]	**M[8]**														
6	Miss									M[6]							
8	Hit	**M[0]**	M[8]														
25	Miss					M[25]											
13	Miss						M[13]										
9	Miss					**M[25]**	M[13]	M[9]									
8	Hit	**M[0]**	M[8]														
0	Hit	M[0]	**M[8]**														

no of hit = 4

no of miss = 6

ii) 8-way set associative:

Block Set = 16/8= 2

Now, we mod block address by 2

Block address	Cache block	Block address	Cache block
0	0 (= 0 mod 2)	25	1 (= 25 mod 2)
8	0 (= 8 mod 2)	13	1 (= 13 mod 2)
0	0 (= 0 mod 2)	9	1 (= 9 mod 2)
6	0 (= 6 mod 2)	8	0 (= 8 mod 2)
8	0 (= 8 mod 2)	0	0 (= 0 mod 2)

Address of memory block accessed	Hit/ Miss	Contents of cache blocks after reference															
		Set 0								Set 1							
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Miss	M[0]															
8	Miss	**M[0]**	M[8]														
0	Hit	M[0]	**M[8]**														
6	Miss			M[6]													
8	Hit	**M[0]**	M[8]														
25	Miss									M[25]							
13	Miss									**M[25]**	M[13]						
9	Miss									**M[25]**	**M[13]**	M[9]					
8	Hit	**M[0]**	M[8]														
0	Hit	M[0]	**M[8]**														

no of hit = 4

no of miss = 6

iv) 16-way set associative:

Block Set = 16/16= 1

Now, we mod block address by 1

Block address	Cache block	Block address	Cache block
0	0 (= 0 mod 1)	25	1 (= 25 mod 1)
8	0 (= 8 mod 1)	13	1 (= 13 mod 1)
0	0 (= 0 mod 1)	9	1 (= 9 mod 1)
6	2 (= 6 mod 1)	8	0 (= 8 mod 1)
8	0 (= 8 mod 1)	0	0 (= 0 mod 1)

Address of memory block accessed	Hit/ Miss	Set 0															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Miss	**M[0]**															
8	Miss	M[0]	**M[8]**														
0	Hit	**M[0]**	M[8]														
6	Miss	M[0]	M[8]	**M[6]**													
8	Hit	M[0]	**M[8]**	M[6]													
25	Miss	M[0]	M[8]	M[6]	**M[25]**												
13	Miss	M[0]	M[8]	M[6]	M[25]	**M[13]**											
9	Miss	M[0]	M[8]	M[6]	M[25]	M[13]	**M[9]**										
8	Hit	M[0]	**M[8]**	M[6]	M[25]	M[13]	M[9]										
0	Hit	**M[0]**	M[8]	M[6]	M[25]	M[13]	M[9]										

no of hit = 4

no of miss = 6

c. fully associative :

Address of memory block accessed	Hit/ Miss	Blocks															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Miss	**M[0]**															
8	Miss	M[0]	**M[8]**														
0	Hit	**M[0]**	M[8]														
6	Miss	M[0]	M[8]	**M[6]**													
8	Hit	M[0]	**M[8]**	M[6]													
25	Miss	M[0]	M[8]	M[6]	**M[25]**												
13	Miss	M[0]	M[8]	M[6]	M[25]	**M[13]**											
9	Miss	M[0]	M[8]	M[6]	M[25]	M[13]	**M[9]**										
8	Hit	M[0]	**M[8]**	M[6]	M[25]	M[13]	M[9]										
0	Hit	**M[0]**	M[8]	M[6]	M[25]	M[13]	M[9]										

no of hit = 4

no of miss = 6