University of Asia Pacific (UAP)

Department of Computer Science & Engineering

Program: B.Sc. in Computer Science and Engineering
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Course Code : CSE 317

Course Title : Computer Architecture

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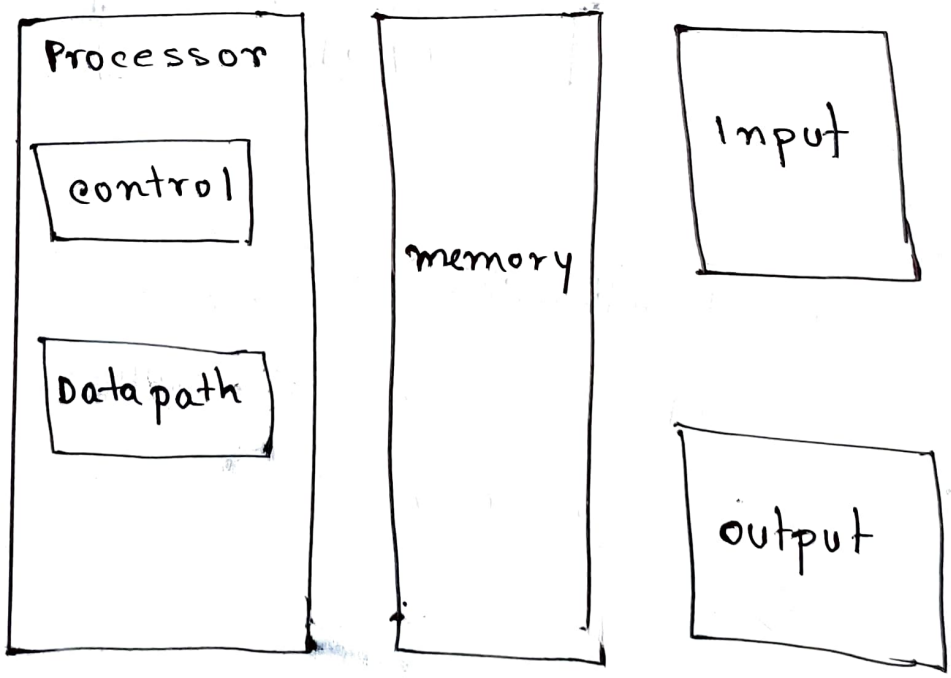
Ans to the qus no. 1 (a)

There are 5 classic component of a computer.

1. Input
2. output
3. Memory
4. Datapath
5. control.



fig, Basic component of a computer.

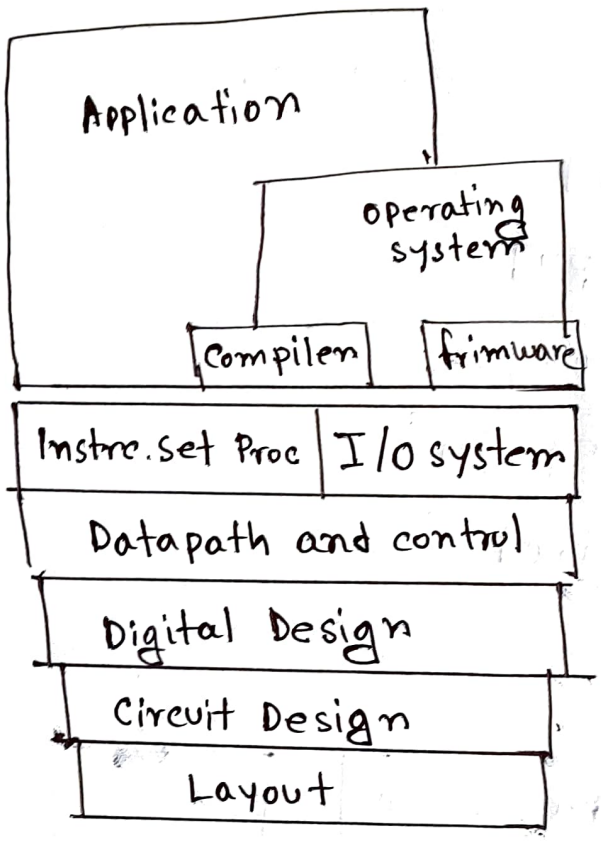


Fig. Relationship among Instruction set, software and Hardware of a computer.

Ans to the qus no. 1(b)

1. Response time: The time between the start and completion of a task.

2. Throughput: The total amount of work in a given time.

3. Relative Performence: relative performence is the total excution of two program.

4. Measing performence: Time is the measure of computer performence. The computer performs the same amount work in the least time.

clock cycle: A clock cycle is a sigle period of an oscillating clock signal.

ex. multiplication, addition is a sequence of cycle.

Ans to the qus no. 1(e)

Clock cycles For:

class A = 3

class B = 2

class C = 4

Instruction:

class A = 5
class B = 2
class C = 3

} 1st code

class A = 6
class B = 4
class C = 2

} 2nd code

Now, CPU clock cycle (1st code) $= \sum_{i=1}^{h} (CPI \times C_i)$

$= (3 \times 5) + (2 \times 2) + (4 \times 3)$

$= 31$ cycle.

CPU clock cycle = (3×6) + (2×4) + (1×2)

(2nd code) = 34 cycles.

$$CPI\ (1st\ code) = \frac{\text{clock cycle}}{\text{total instructions}}$$

$$= \frac{31}{10}$$

$$= 3.1$$

$$CPI\ (2nd\ code) = \frac{34}{12} = 2.83$$

So, 2nd code seq. will be faster, Because it's CPI is less, So, performence will be better.

$$\therefore n = \frac{3.1}{2.83} = 1.1$$

So, 2nd code sequence will faster by 1.1 times.

Ans to the qus no. 3 (a)

Last digit of ID = 4

m * (mx) [5 Bit Multiplexer]

$m = \{4 \bmod 6\} + 2$

$= 4 + 2$

$= 6$

$mx = -4$

So, $6 \times (-4)$

$m = 00110$

$m' = 11001$

$+1$

$\therefore -m = 11010$

Result = -29

$4 = 00100$

11011 (1's com

$+1$

$\therefore mx = 11100$

$-4 = 11100$

$24 = 000011000$

111101001111

$+1$

$-24 = 111101000$

Iteration	steps	Mn	P	Extra Bit
0	initialization	00110	00000	111000
1	1. $P_0 P_{0-1} = 00$ 1.(a) NOP 2. $\overrightarrow{P}$	00110	00000	011100
2	1. $P_0 P_{0-1} = 00$ 1 (a) NOP 2. $\overrightarrow{P}$	00110	00000	001110
3	1. $P_0 P_{0-1} = 10$ 1 (a) $P(L) = P_L - Mn$ 2. $\overrightarrow{P}$	00110	11010	001110
4.	1. $P_0 P_{0-1} = 11$ 1.(a) NOP 2. $\overrightarrow{P}$	00110	11110	100011
5.	1. $P_0 P_{0-1} = 11$ 1 (a) NOP 2. $\overrightarrow{P}$		11 111 ↓ Result	01000 1 ↓ Extra Bit

Ans to the qus no. 2 (a)

Instruction class of MIPS architure are 3 types.

(i) R type → Register reference Ins.

(ii) I type → Memory reference Ins.

(iii) J type → Jump Instruction.

(i) R type: Arthicmatic operatieons are R type instruction.

MIPS code: add $0, $S1, $S2

C code: A = B + C

A → S0, B → S1, C → S2

I Type % load, store, Addi, Subi, are I type instruction.

code: A[5] = b + A[6]
S_0 S_1 S_1

MIPS code: lw $to 40($s0)
add $to, $s1, $to
sw $to, 32($s0)

~~Jum~~ J type:

op code	Address

In MIPS arthmetic we use 3 operadands for simplifcation hardware design

Ans to the qus no. 2(b)

My ID: 18101094

i = 94

A[94] = C + A[99]

/ / /

S_0 S_1 S_6

① lw $to, 76($S0)

② Add $to, $S1, $to ;

③ sw, $to, 356 ($S0);

Lets assume $S_0 = 17$, $S_1 = 18$, $to = 19$

lw = 14, sw = 15

Add = 30

①

14	17	19	376

= | 001110 | 10001 | 10011 | 0000000101111000 |

② | 000000 | 10010 | 10011 | 10011 | 00000 | 011110 |

(3)

15	12	19	356

=

001111	10001	10011	0000001011 00100

Ans to the qus no. 3(b)

ver. 1 muliplication	ver 2 muliplication	ver 3 muliplcation
64 Bit ALU	32 Bit ALU	32 Bit ALU
64 Bit wasted	32 bit wasted	no bit wasted
Multiplicand 64 Bit	Multiplicad 32 bit	Mutiplicand 32 bit
Multiplier 32 bit	Multiplier 32 bit	Multiplier 32 bit
Multtiplein On anothe register	Muliplier Another resistor.	For my half part of prodod resiston