

VLSI Design Technology

Lab 1: Design a CMOS inverter.

Objective:

- 1) Library creation.
- 2) Cell View creation.
- 3) Schematic Design.
- 4) Symbol creation.

Lab 2: Design NAND and NOR gates.

Objective:

- 1) Library creation.
- 2) Cell View creation.
- 3) Schematic Design.
- 4) Symbol creation.
- 5) Finding operating region.
- 6) DC and Transient analysis.

Lab 3: Characterization of a MOSFET. (Ref: Razavi: Sections 2.1 and 2.2)

Objective:

- 1) To simulate the voltage-current relationships of a MOSFET in Cadence platform.
- 2) To perform DC analysis.
- 3) To perform Parametric analysis (also use calculator tool). Determine λ (Channel length modulation coefficient).
- 4) To perform step 3 by changing W/L of the MOSFET. Determine λ at $V_{GS}=0.7$ V and $V_{GS}=1.8$ V. explain the difference between step 3 & 4.
- 5) To find out the square root of I_d and from this estimate V_{th} . (Hint. Use linear extrapolation)
- 6) To determine g_m (Transconductance) at $V_{GS} = 1$ V. Compare to the value on the plot.
- 7) To observe the body effect.
- 8) To observe relation of Threshold voltage with body effect.

Lab 4: Design a NMOS with gate voltage 3V and Drain is connected to a 5V source through 200k resistance. Aspect ratio=10/2.

Objective:

- 1) To find operating region.

- 2) To calculate ID, VDS, and estimate the small-signal resistance looking into the drain of the MOSFET.
- 3) Compare your simulation result with hand calculation.

Lab 5: Full custom design of PMOS and NMOS devices.**Objective:**

- 1) To open Virtuoso Layout Suite.
- 2) To draw different types of layers.
- 3) To generate layout from schematic.

Lab 6: Full custom design of a NAND gate.**Objective:**

- 1) To design schematic view.
- 2) To perform DC and Transient and Parametric analysis.
- 3) To find Gain and Bandwidth.
- 4) To generate layout from schematic.
- 5) To check LVS and DRC.

Lab 7: Calculate the DC and AC voltages and currents for the circuit seen in Fig. 1. Verify your answers with AC analysis simulation by Cadence system.**Objective:**

- 1) To find operating region.
- 2) To do AC analysis and DC analysis.
- 3) Compare your simulation result with hand calculation.

Lab 8: Calculate the Transition Frequency (ft) of a 10/2 NMOS.**Objective:**

- 1) To find Transition Frequency (ft).
- 2) To find Transition Frequency (ft) when NMOS is multiplied by 10 and compare 1) & 2)
- 3) Verify your hand calculations using simulations by Cadence system.

Lab 9: For the circuits seen in Fig. 3, estimate both the output voltage at room temperature and how it will change with temperature. Use the short-channel CMOS process.



Fig. 01: Circuit for Lab 10.

Objective:

- 1) To find output voltage at room temperature and by varying temperature.
- 2) Verify your answer with Cadence simulation.

Lab 10: Design a current Mirror circuit.

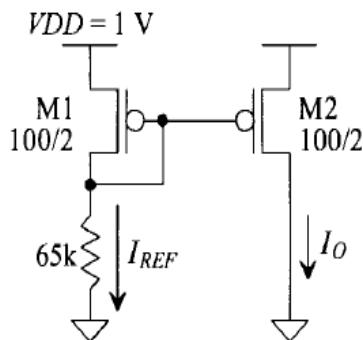


Fig.01

Objective:

- 1) To design schematic.
- 2) To find voltage and current of each branch.
- 3) To observe voltage and current of each branch by changing width and length of devices.
- 4) Verify your answer with Cadence simulation.
- 5) To estimate the temperature behavior of the gate voltage of M1 in Fig. 01.

Lab 11: Design an R-2R DAC.

Objective:

- 1) To design schematic view.
- 2) To create symbol.
- 3) To perform transient analysis.
- 4) To create layout from schematic.
- 5) To check and clean LVS, DRC.
- 6) To extract RC.

VLSI Design Technology

General Notes:

Fist to perform all the labs we need to install below tools properly:

- I. IC615
- II. Assura
- III. MMSIM
- IV. Incisive Enterprise Simulator

Now

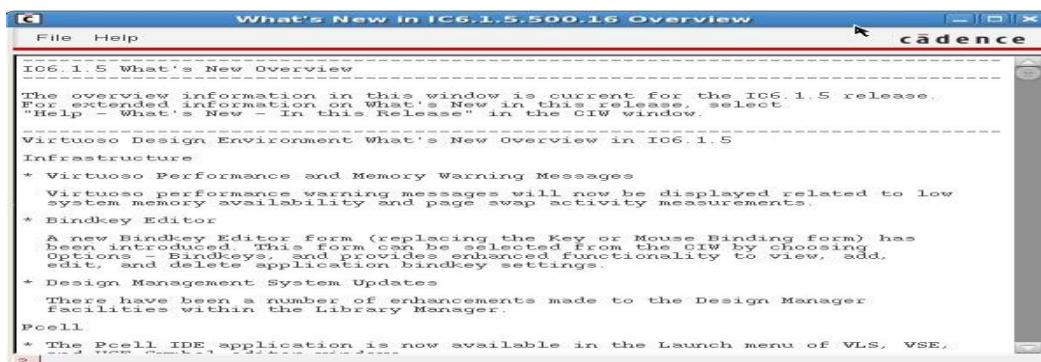
- 1) To start, Log in to your workstation using the username and password.
- 2) Open terminal and go to the directory where **cshrc** file is located.
e.g. **cd /home/license/**
- 3) In the terminal window, type **csh** at the command prompt to invoke the C shell.
csh
- 4) Source the **cshrc** file.
source cshrc
- 5) Go to the working directory.
e.g. **# cd /home/tajjaj/work**
- 6) Type **virtuoso &** command in terminal.
virtuoso &

It will start the Cadence Design Framework II environment from this directory because it contains **cds.lib** file, which is the local initialization file. The library search paths are defined in this file.



This window called CIW (Command Interpreter Window). Keep opened CIW window for the labs.

- 7) If the “What’s New ...” window appears, close it with the **File → Close** command.



Lab 1: Design a CMOS inverter.

Objective:

- 1) Library creation.
- 2) Cell View creation.
- 3) Schematic Design.
- 4) Symbol creation.

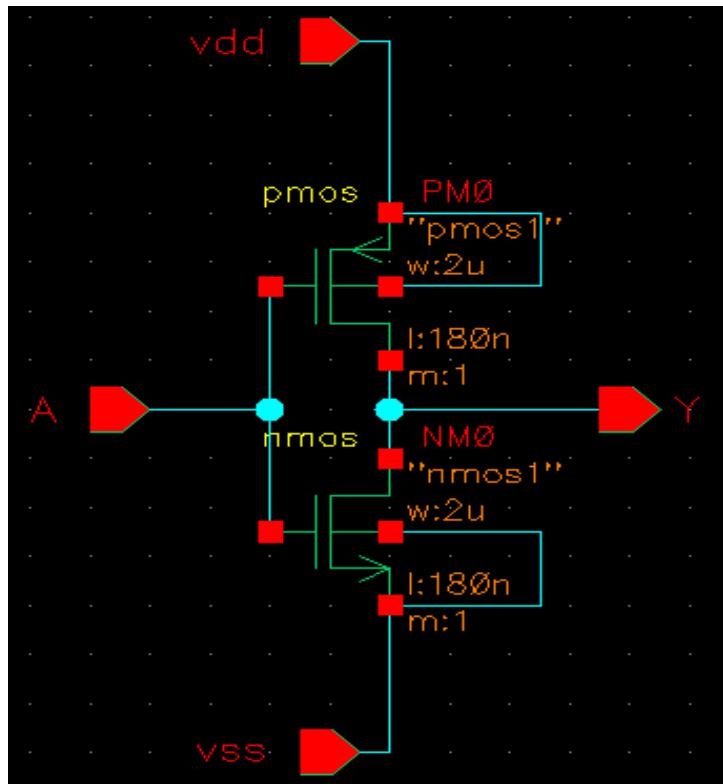


Fig: Schematic view of an Inverter

1) Library creation.

Below steps explain the creation of a new library “**myDesignLib**” and we will use the same throughout this course for building various cells that we going to create in the next labs. Execute **Tools – Library Manager** in the **CIW (Command Interpreter Window)** or Virtuoso window to open Library Manager.

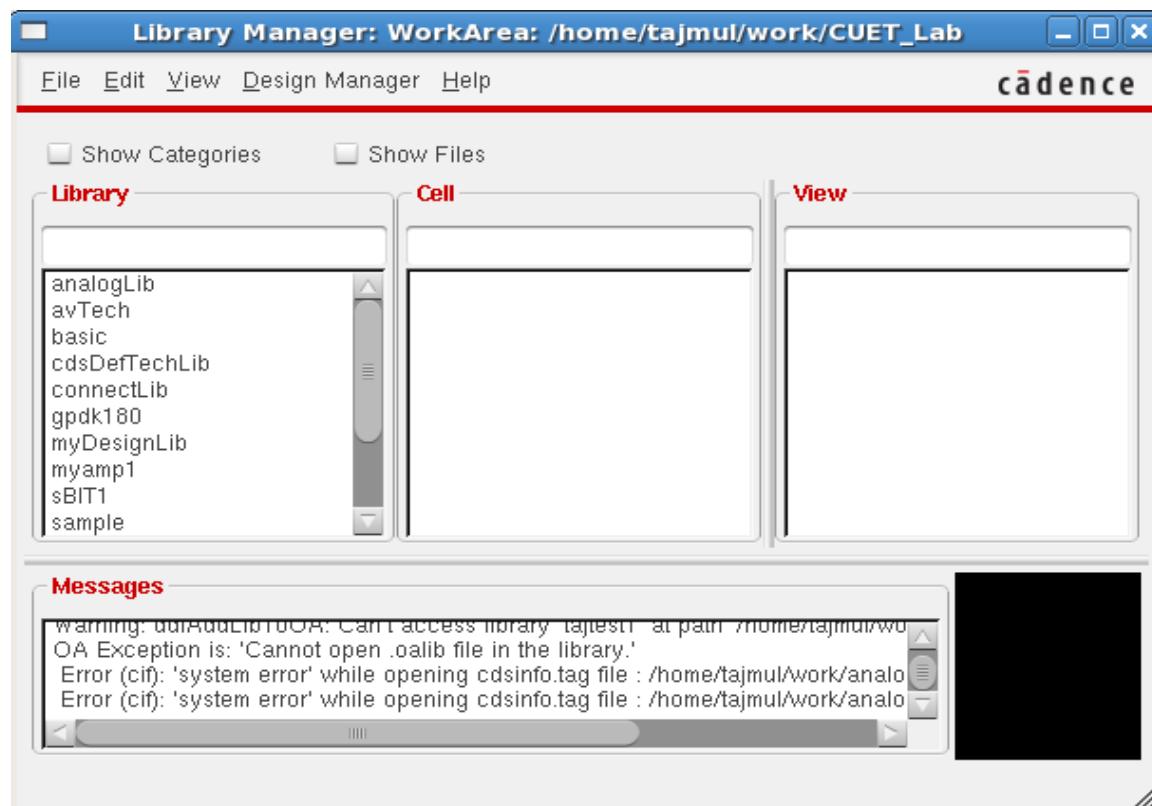
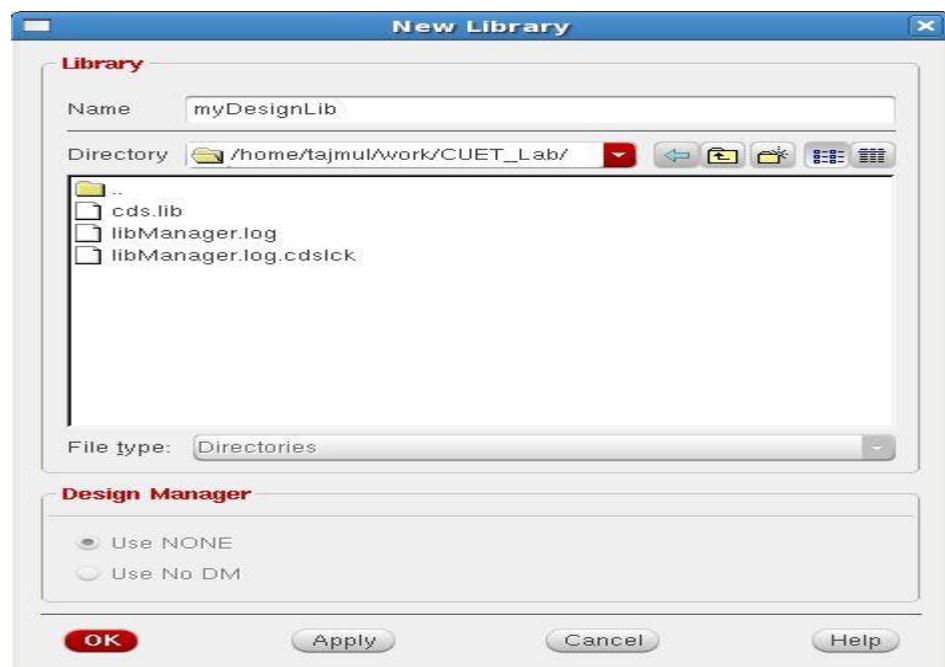


Fig: Library Manager

Creating a New library:

- I. In the Library Manager, execute **File - New – Library**. The new library form appears.
- II. In the “New Library” form, type “**myDesignLib**” in the Name section.



- III. Fig: New Library window In the field of Directory section, verify that the path to the library is set to the current working directory (e.g. here working directory path is **/home/tajmul/work/CUET_Lab**) and click **OK**.
- IV. In the next “Technology File for New library” form pops up, select option **Attach to an existing techfile** and click **OK**.



Fig: Technology File for New library

- V. Then “Attach Design Library to Technology File” form pops up, select **gpdk180** from the cyclic field and click **OK**.

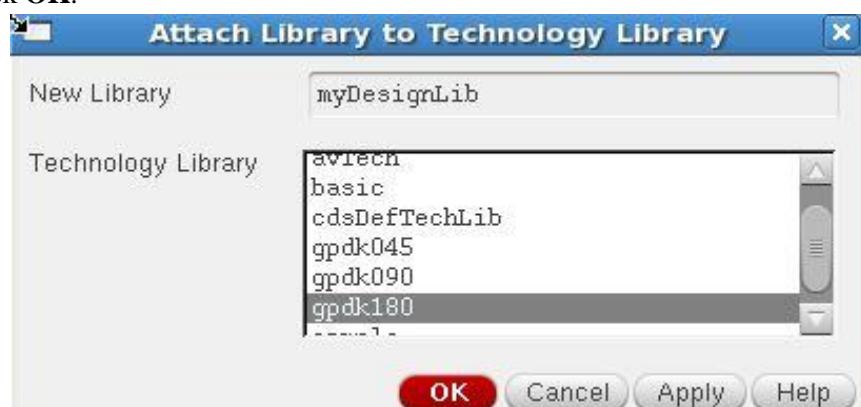


Fig: Attach Design Library to Technology File

- VI. After creating a new library we can verify it from the library manager.
- VII. If you right click on the “**myDesignLib**” and select properties, you will find that **gpdk180** library is attached as techlib to “**myDesignLib**”.

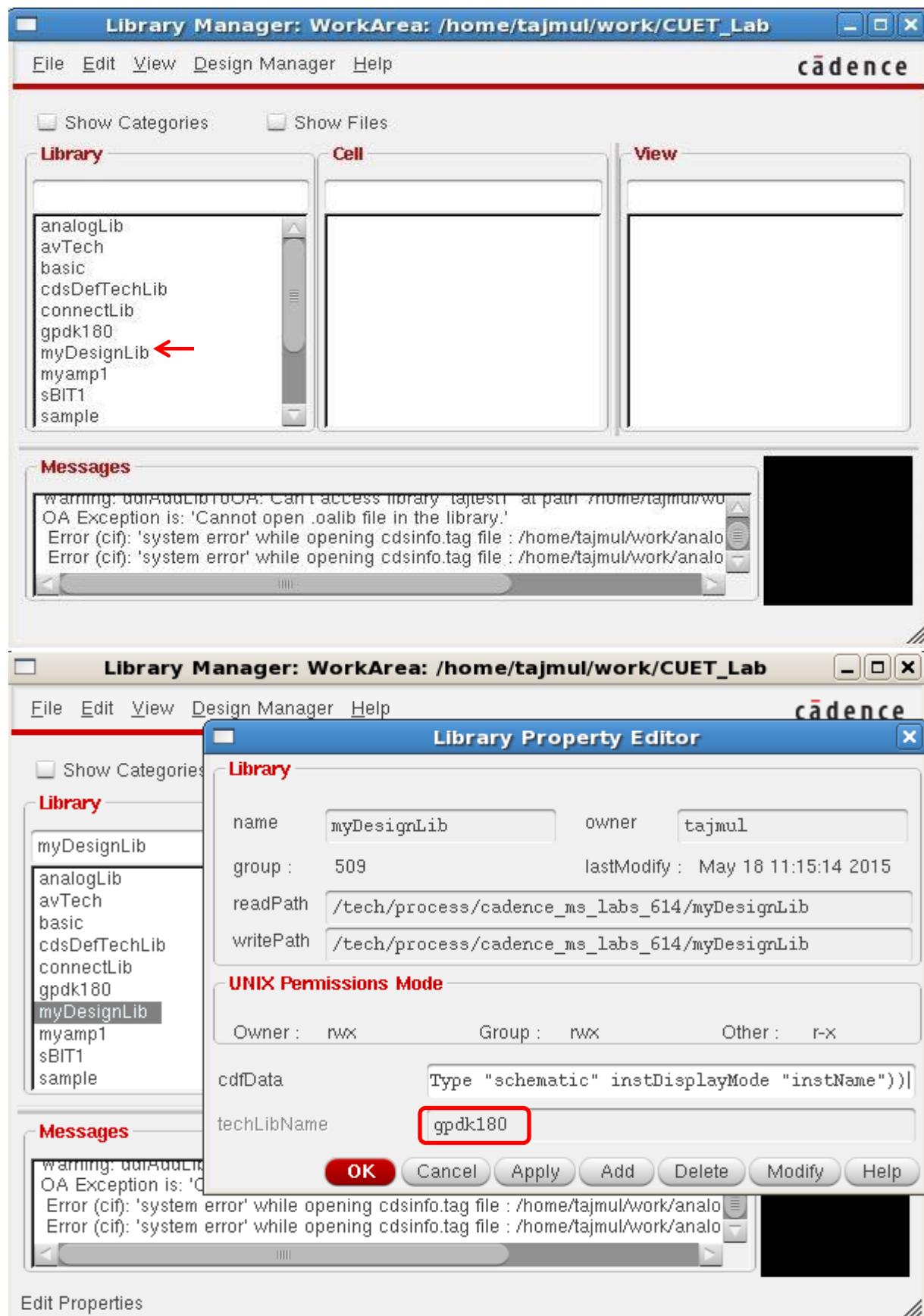
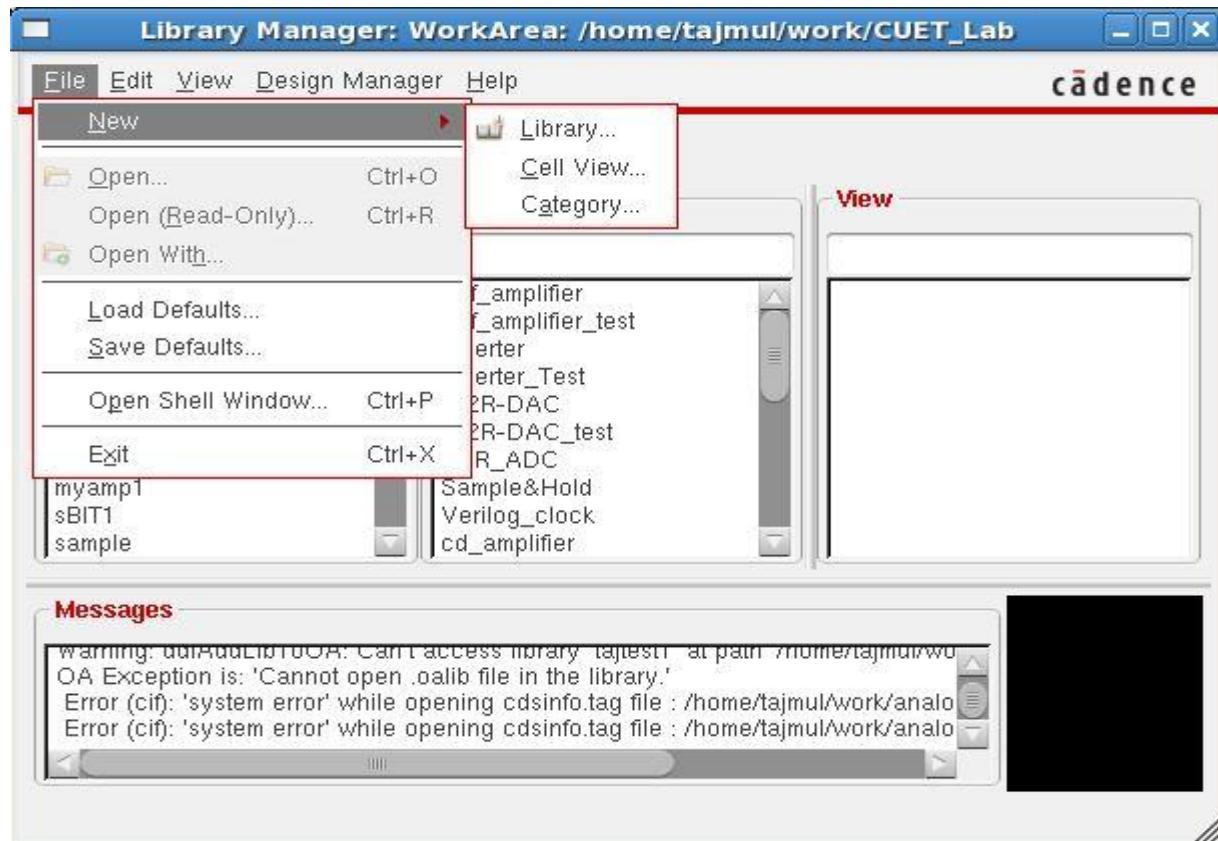


Fig: Library Property

2) Cell View creation:

In this section we will learn how to create a new cell view in the new “**myDesignLib**” library.

- In the CIW or Library manager, execute **File** → **New** → **Cellview**.



- A **New file** form pops up. Set up the **New file** form as follows:

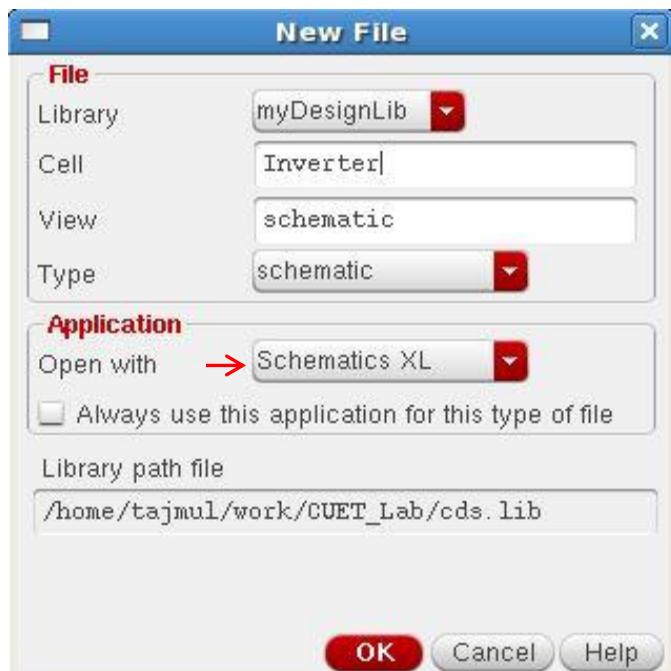


Fig: New File

- III. In **Open with** option under the **Application** select it as **Schematic XL**.
Do not edit the **Library path file** and the one above might be different from the path shown in your form.
- IV. Click **OK** when done the above settings. A blank schematic window for the Inverter design appears.

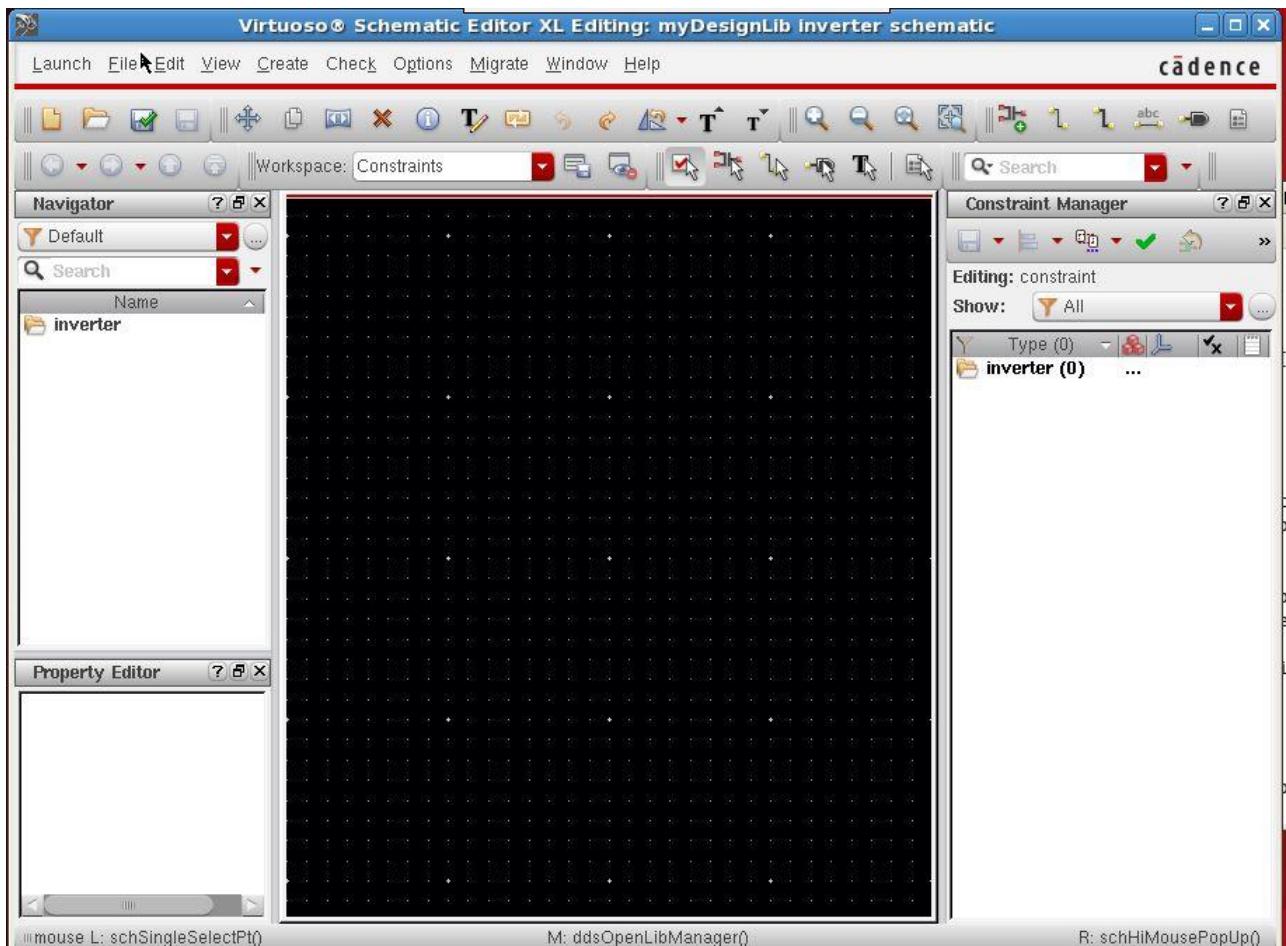


Fig: Virtuoso Schematic Editor

- V. Click on **Check and Save** Icon It will save our cell.

3) Schematic Design.

- I. In the Inverter schematic black window click the **Instance** fixed menu to display the Add Instance form.

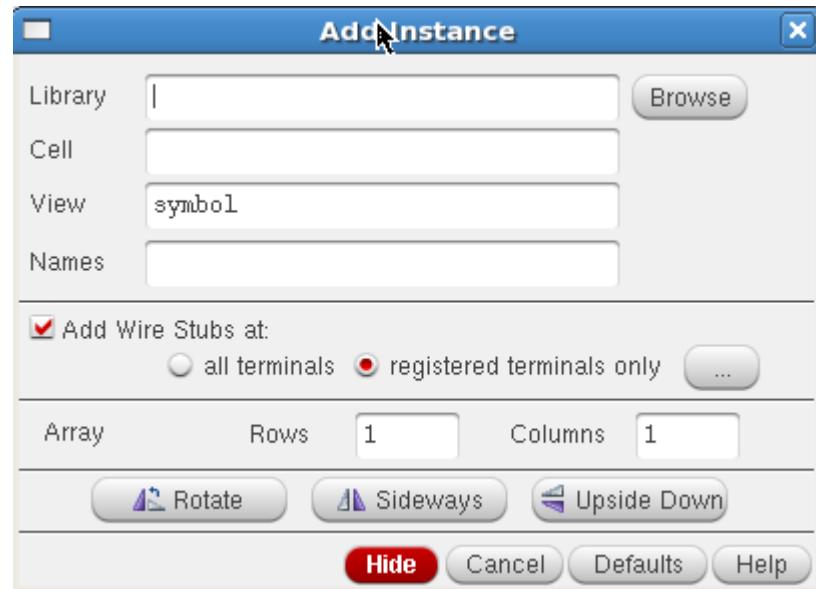


Fig: Add Instance form

Tip: We can also execute **Create — Instance** or press **i**.

- II. Click on the **Browse** button. This opens up a **Library browser** from which we can select components and the **symbol** view .

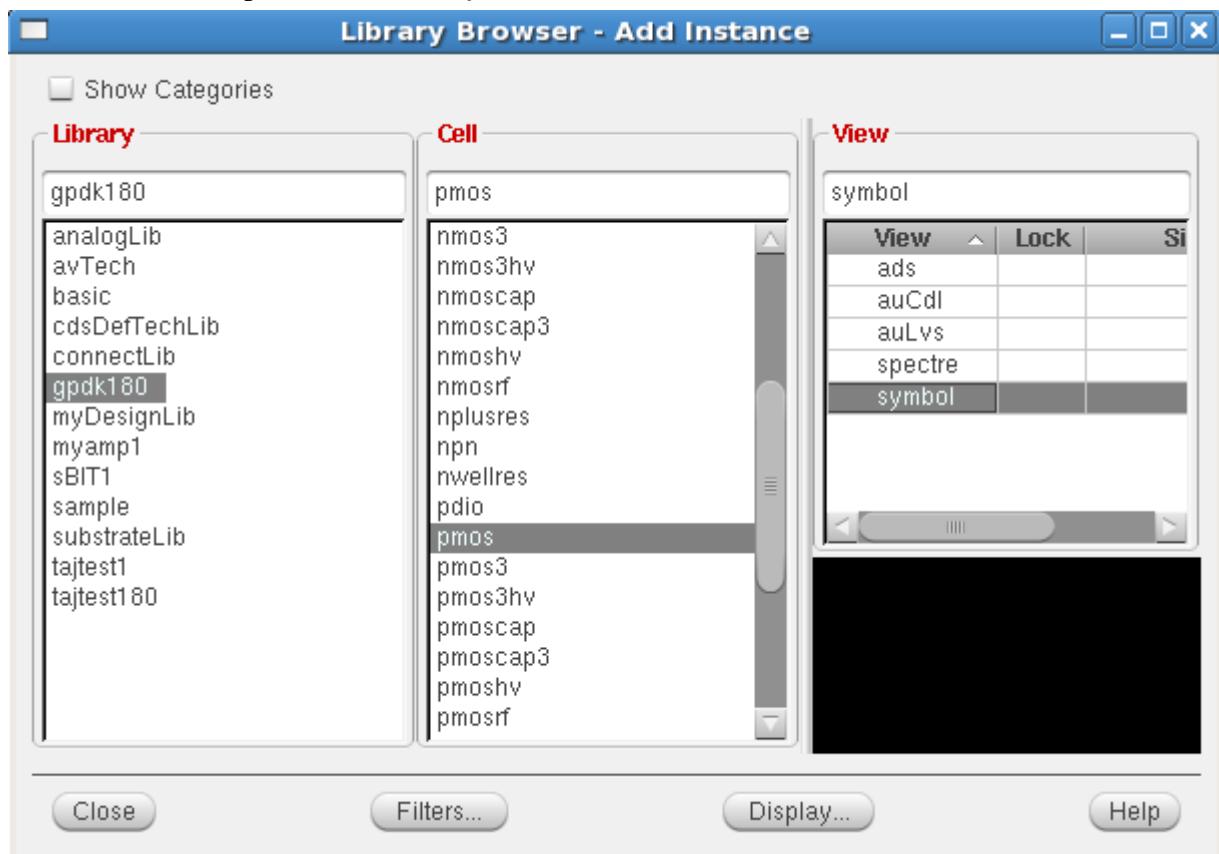
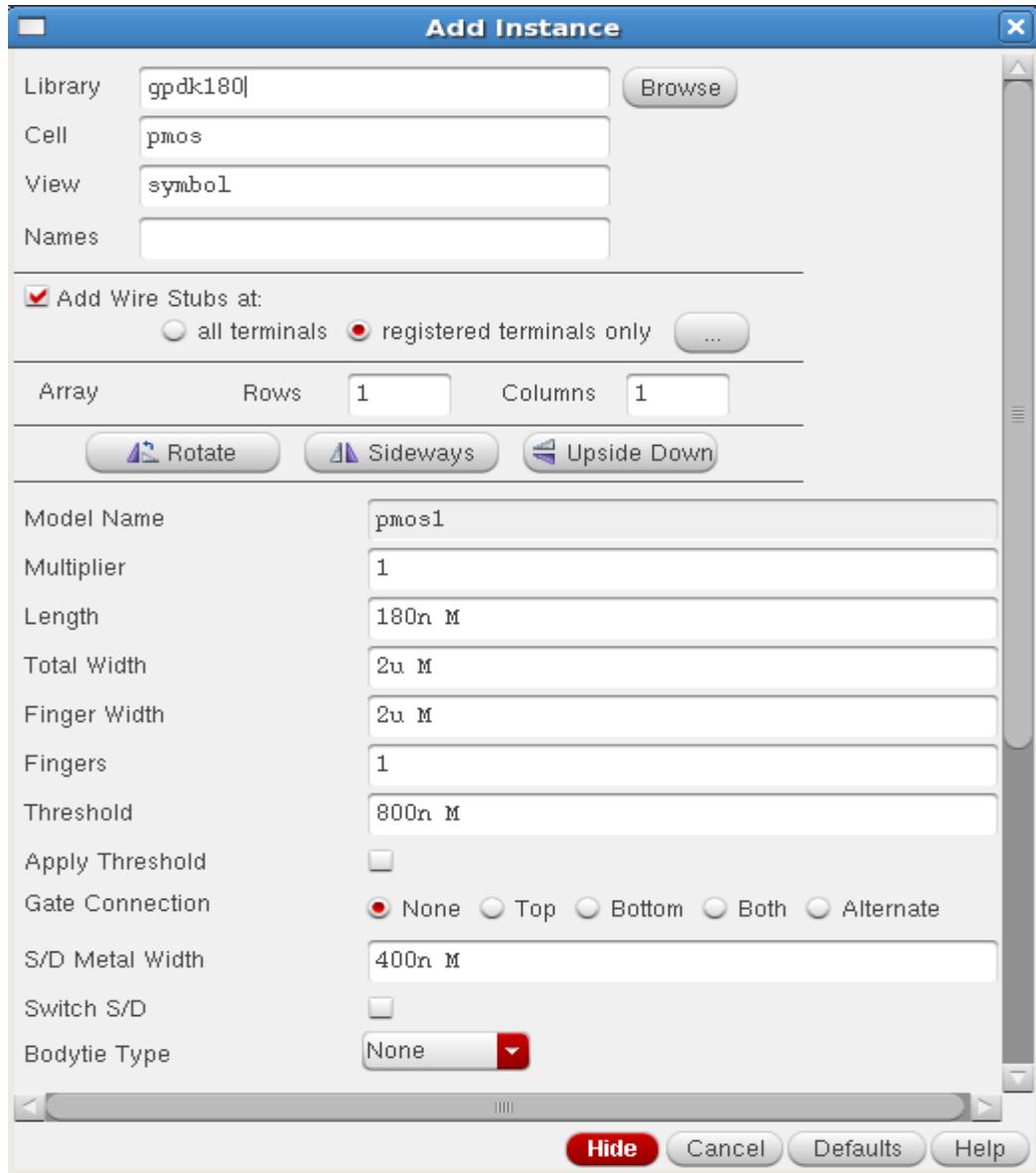


Fig: Library Browser form

- III. We will update the Library Name, Cell Name, and the property values given in the table on the next page as you place each component.



- IV. After we complete the Add Instance form, move our cursor to the schematic window and click **left** of mouse to place a component.
 V. This is a table of components for building the Inverter schematic.

Library name	Cell Name	Properties/Comments
gpd़k180	pmos	For M0: Model name = pmos1, W= 4u, L=180n
gpd़k180	nmos	For M1: Model name = nmos1, W= 2u, L=180n

If we place a component with the wrong parameter values, use the **Edit—Properties—Objects** command to change the parameters. Use the **Edit—Move** command if you place components in the wrong location.



We can rotate components at the time we place, or use the **Edit—Rotate** command after they are placed.

- VI. After entering components, click **Cancel** in the Add Instance form or press **Esc** with your cursor in the schematic window.

VII. Adding pins to Schematic:

- Click the Pin fixed menu icon in the schematic window. The Add pin form appears.

Tip: We can also execute Create — Pin or press p.

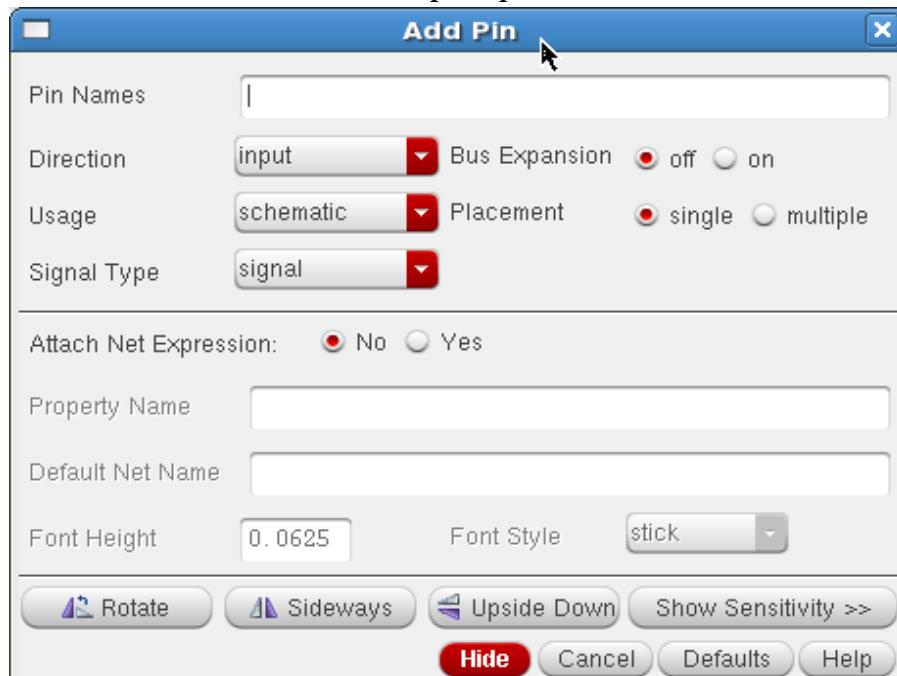


Fig: Add pin form

- Type the following in the Add pin form in the exact order leaving space between the pin names.

Pin Name	Direction
A	Input
Y	Output
Vdd	Input
Vss	Input

Make sure that the direction field is set to **input/output/inputOutput** when placing the **input/output/inout** pins respectively and the Usage field is set to schematic.

- Select **Cancel** from the Add – pin form after placing the pins.
In the schematic window, execute Window—Fit or press the f bindkey.

VIII. Adding Wires to a Schematic:

Add wires to connect components and pins in the design.

- Click the Wire (narrow) icon in the schematic window.

We can also press the **w** key, or execute **Create — Wire (narrow)**.

2. In the schematic window, click on a pin of one of our components as the first point for our wiring. A diamond shape appears over the starting point of this wire.
3. Follow the prompts at the bottom of the design window and click left on the destination point for our wire. A wire is routed between the source and destination points.
4. Complete the wiring as shown in figure and when done wiring press ESC key in the schematic window to cancel wiring.

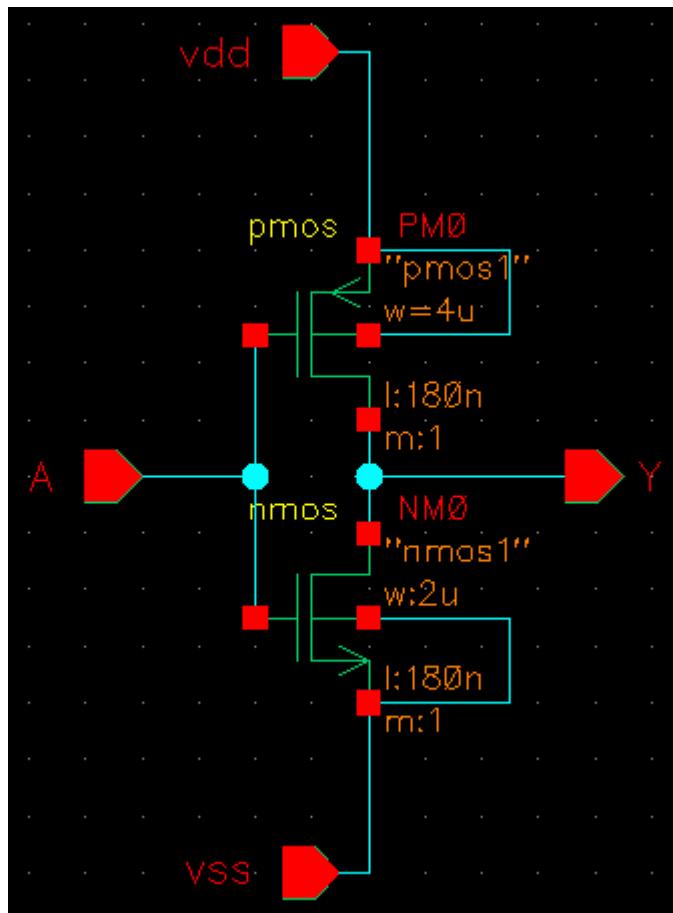


Fig: Inverter schematic view

5. Click the Check and Save icon in the schematic editor window.
6. Observe the CIW output area for any errors.
7. Now if you check our Library “**myDesignLib**” in **Library Manager**, we will see the inverter is saved as Schematic view.

4) Symbol creation:

In this section, we will create a symbol for your inverter design so we can place it in a test circuit for simulation. A symbol view is extremely important step in the design process. The symbol view must exist for the schematic to be used in a hierarchy. In addition, the symbol has attached properties that facilitate the simulation and the design of the circuit.

- I. In the Inverter schematic window, execute **Create — Cellview— From Cellview**.
 The **Cellview From Cellview** form appears. With the Edit Options function active, you can control the appearance of the symbol to generate.



Fig: Cellview From Cellview form

- II. Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is set to **symbol**, with the **Tool/Data Type** set as **SchematicSymbol**.
 III. Click **OK** in the **Cellview From Cellview** form. The Symbol Generation Form appears.

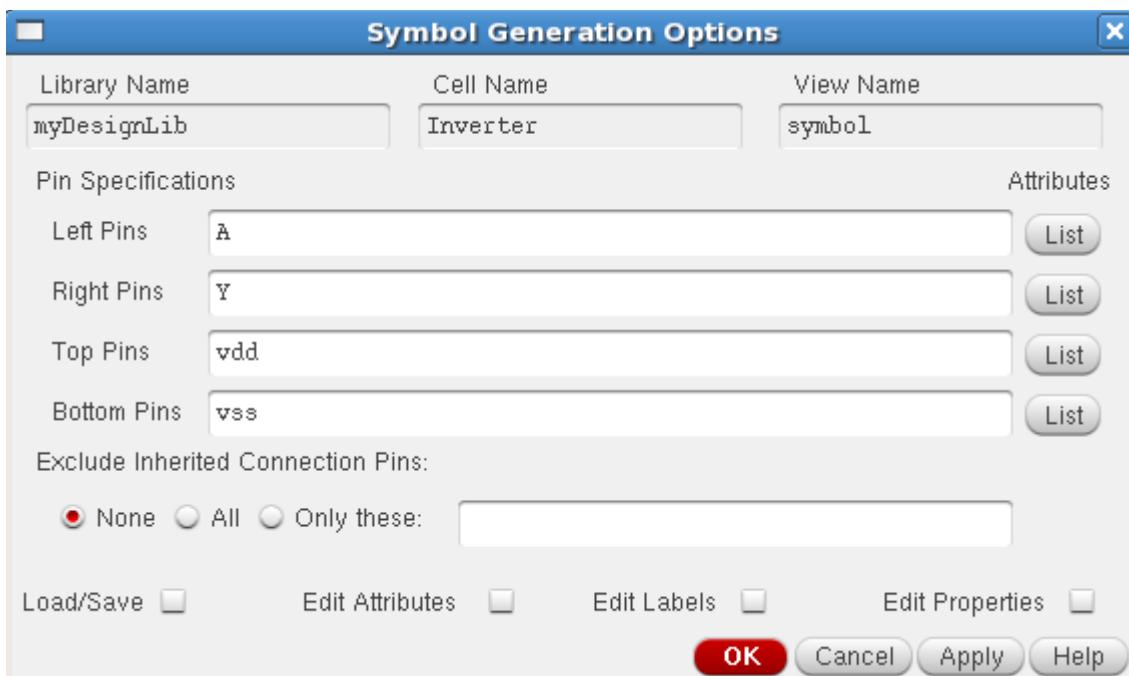
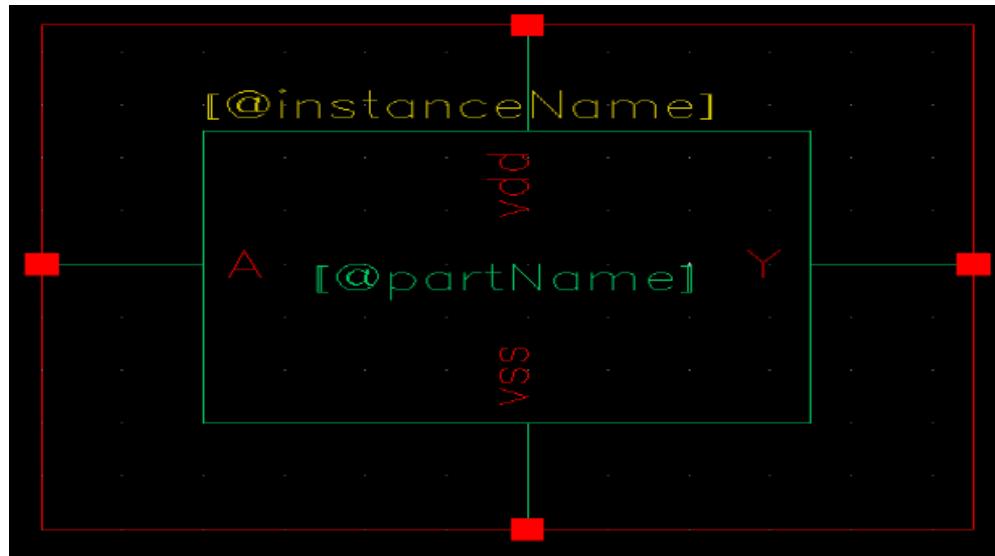
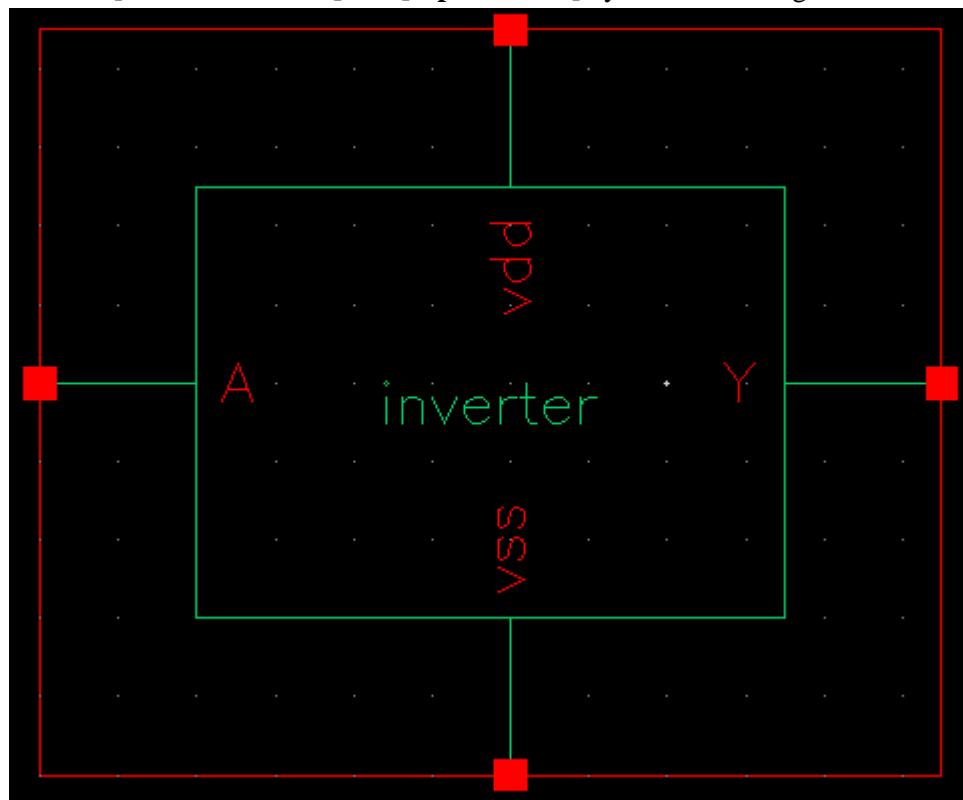


Fig: Symbol Generation Options

- IV. Modify the Pin Specifications as above:
- V. Click **OK** in the Symbol Generation Options form.
- VI. A new window displays an automatically created Inverter symbol as shown here



- VII. We can edit the **[@instance Name]** and **[@part Name]** by double clicking on it.



VIII. Editing the Symbol:

In this section we will modify the inverter symbol to look like a Inverter gate symbol.



1. Move the cursor over the automatically generated symbol, until the green rectangle is highlighted, click **left** to select it.
2. Click **Delete** icon in the symbol window, similarly select the red rectangle and delete that.
3. Execute **Create – Shape – polygon**, and draw a shape similar to triangle.
4. After creating the triangle press **ESC** key.
5. Execute **Create – Shape – Circle** to make a circle at the end of triangle.
6. We can move the pin names according to the location by using **M** key.
7. Execute **Create — Selection Box**. In the Add Selection Box form, click **Automatic**. A new red selection box is automatically added.
8. After creating symbol, click on the *save* icon  in the symbol editor window to save the symbol. In the symbol editor, execute **File — Close** to close the symbol view window.

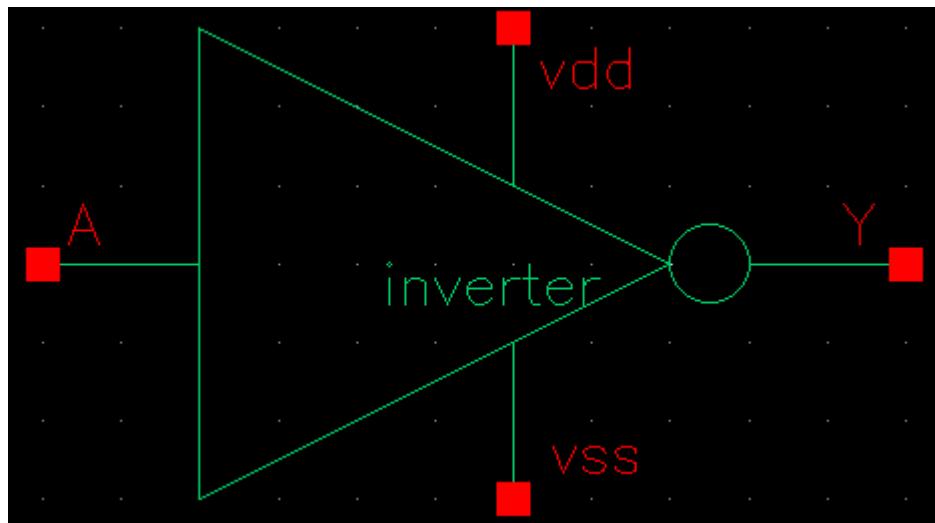


Fig: Inverter Symbol

9. Now if we check our Library “**myDesignLib**” in **Library Manager**, we will see the inverter is saved as Symbol view.

End of Lab 1

Lab 2: Design NAND and NOR gates.

Objective:

- 7) Library creation.
- 8) Cell View creation.
- 9) Schematic Design.
- 10) Symbol creation.
- 11) Finding operating region.
- 12) DC and Transient analysis.

1. Library Creation:

I. From CIW (Command Interpreter Window) Click - **tools > library manager**. A new window “Library Manager” is open. From library manager window click- **file > new > library**.

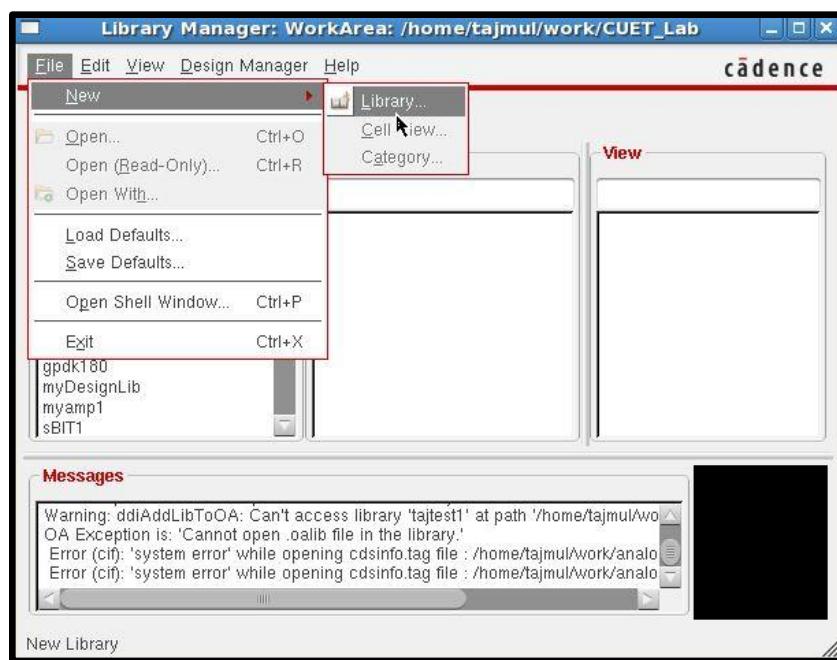


Fig. 01: Library manager library

II. A new window “New Library” is open. Here write the library **name** and click **ok**. Here library name **myDesignLib** is used.

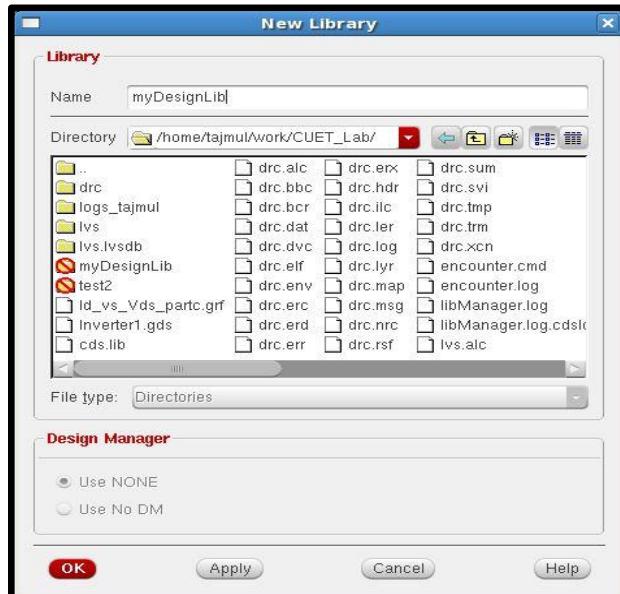


Fig. 02: New Library window

III. A “Technology File for new Library file” window is open. Where you select technology file. Select **Attach to an existing library. Click **ok**.**



Fig. 03: Technology File for New Library window

IV. “Attach Library to Technology Library” window is open. Here **gpdk180 is used. Click **ok**.**



Fig. 04: Attach Library to Technology Library

V. Now in library manager, new library **myDesignLib is open.**

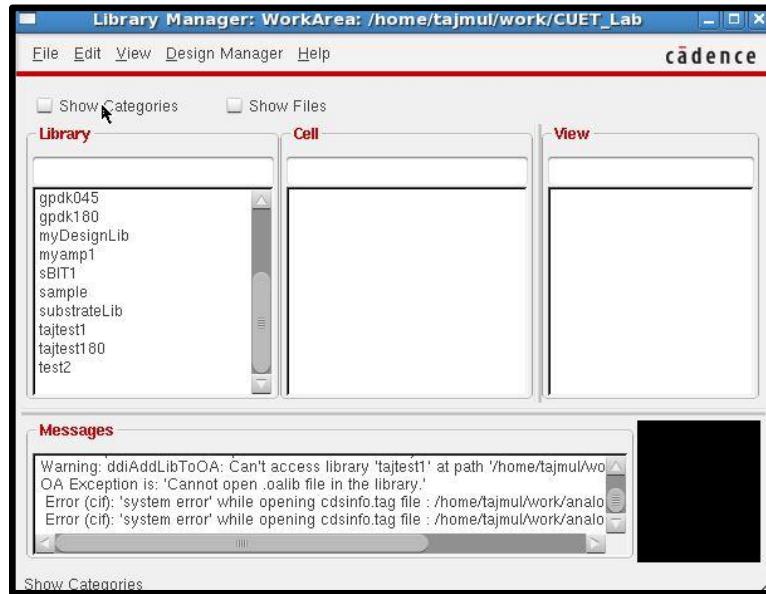


Fig. 05: New library in Library Manager

2. Cell View Creation:

I. From library manager window select your library here myDesignLib and click – **File > new> cell view**.

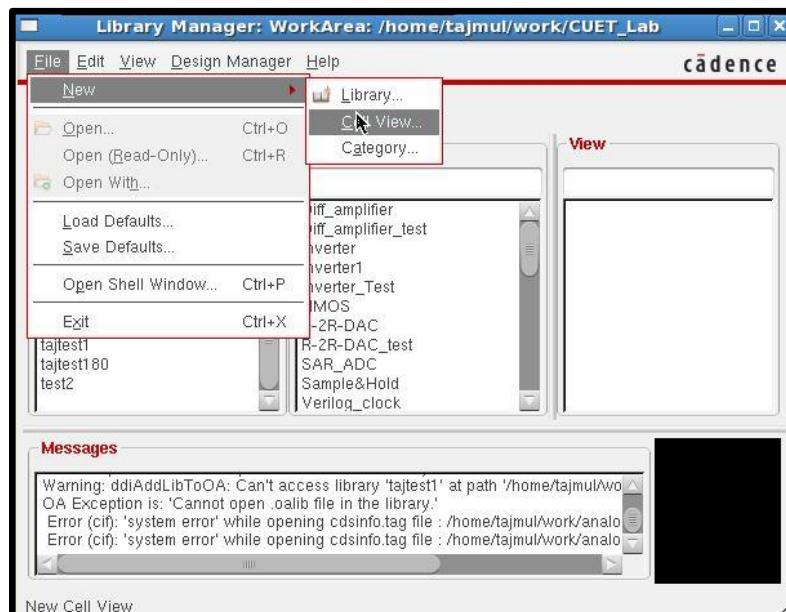


Fig. 06: Library Manager window

II. A window “**New file**” is open. Here write **cell name** and select **type >schematic**, **Open with > Schematic XL**. Click **ok**.

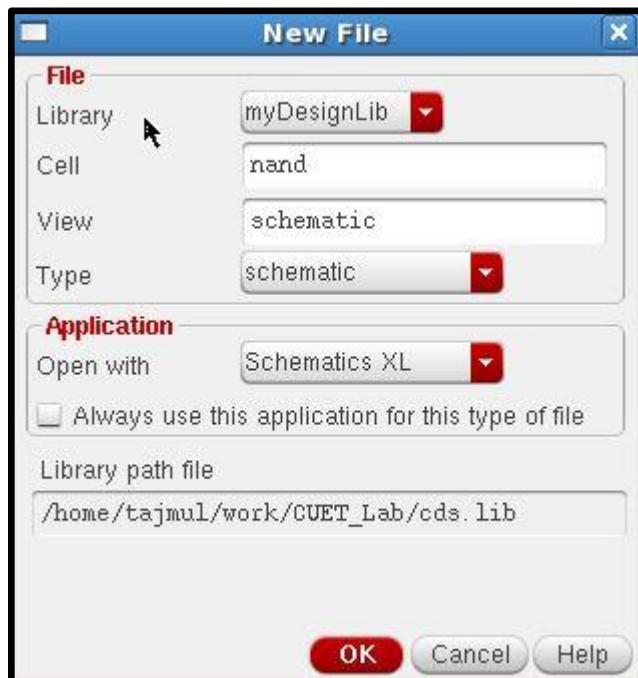


Fig. 07: New file window

III. A new cell **nand** is saved under myDesignLib library.

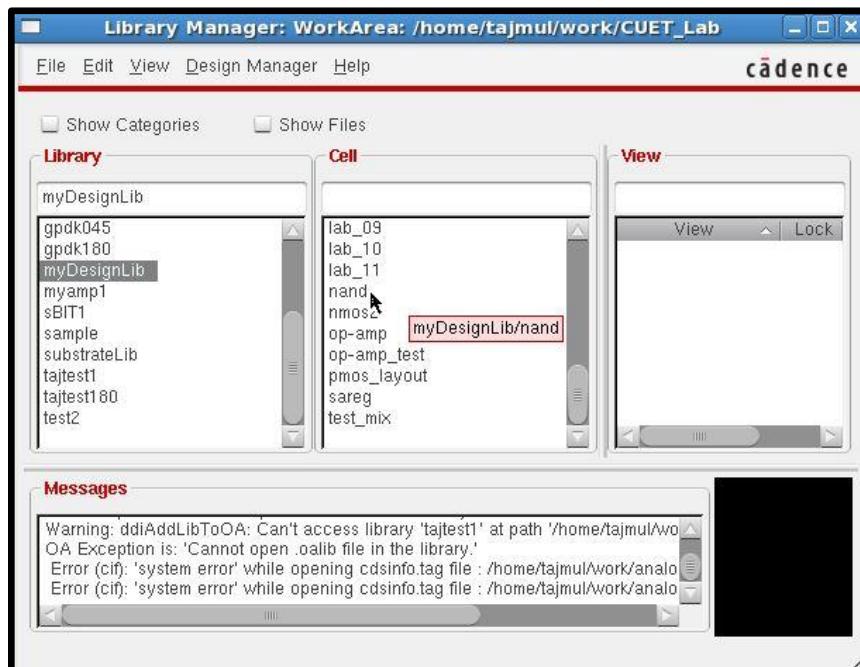


Fig. 08: A new cell nand in myDesignLib library

3. Schematic Design:

The schematic diagram of NAND gate is given below –

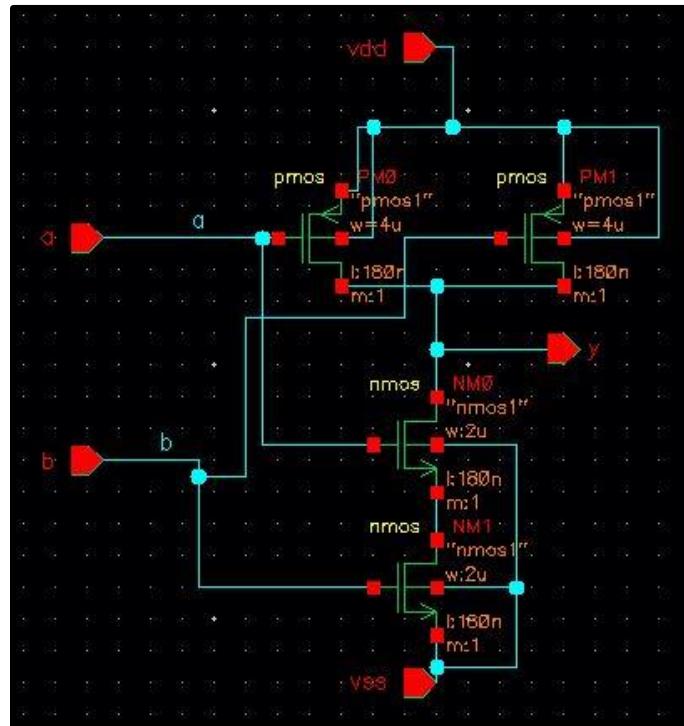


Fig.09: Schematic diagram of NAND gate

4. Symbol creation:

I. In the NAND schematic window, click - Create — Cellview— From Cellview.

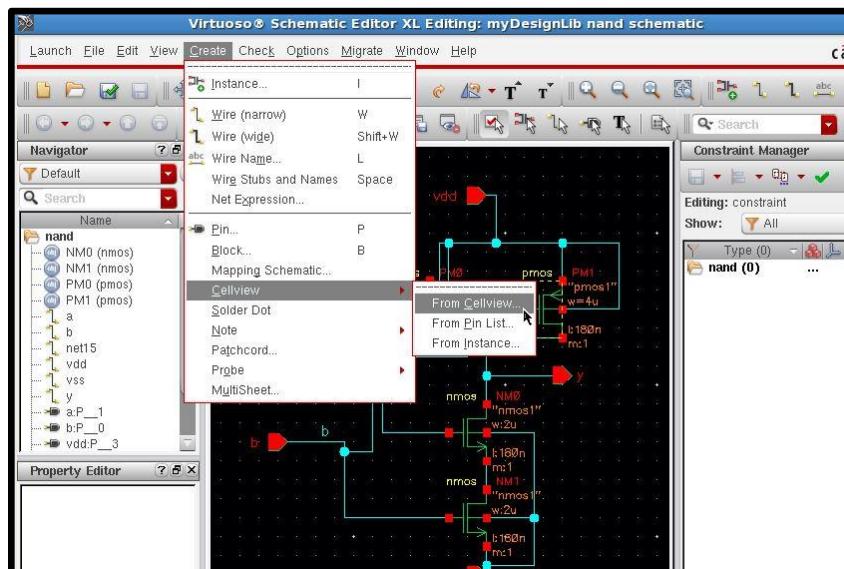


Fig. 10: Virtuoso schematic editor

II. A window **Cellview From Cellview** appears. With the Edit Options function active, you can control the appearance of the symbol to generate. Verify that the **From View Name** field is set to **schematic**, and the **To View Name** field is set to **symbol**, with the **Tool/Data Type** set as **SchematicSymbol**. Click **OK** in the **Cellview From Cellview** form.



Fig. 11: Cellview From Cellview window

III. The “**Symbol Generation Options**” window appears. Modify the **Pin Specifications**. Click - **OK** in the Symbol Generation Options form.

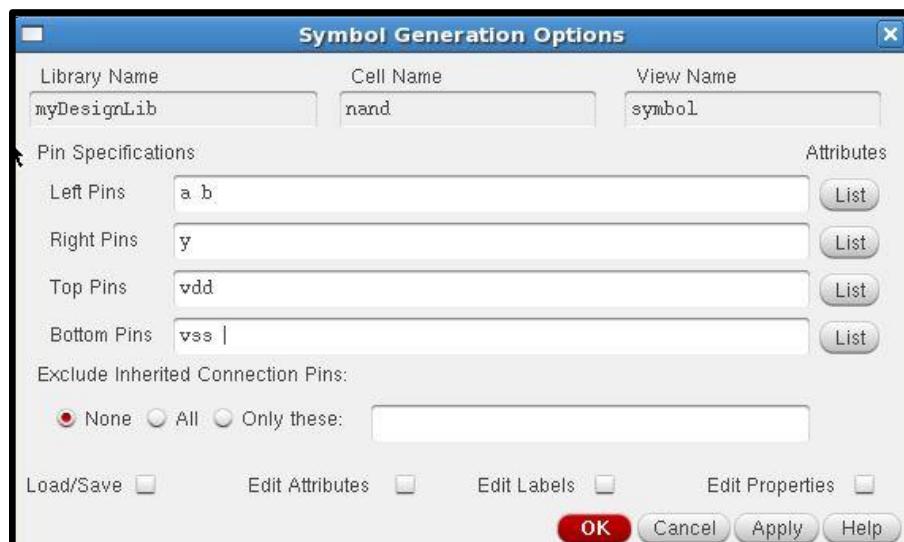


Fig. 12: Symbol Generation Options

IV. A new window displays an automatically created NAND symbol as shown here.

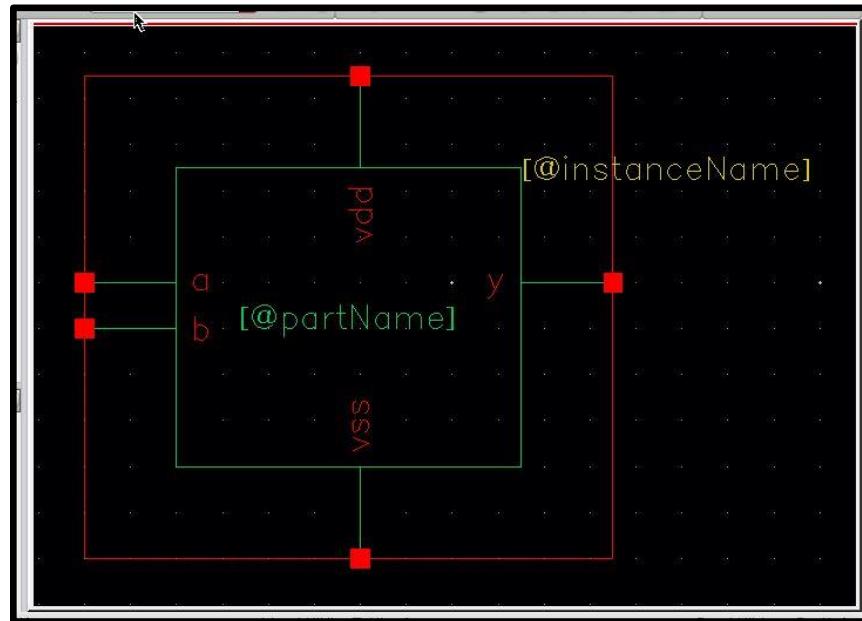


Fig. 13: NAND symbol

V. Move the cursor over the automatically generated symbol, until the green rectangle is highlighted, click **left** to select it. Click **Delete** icon in the symbol window, similarly select the red rectangle and delete that.

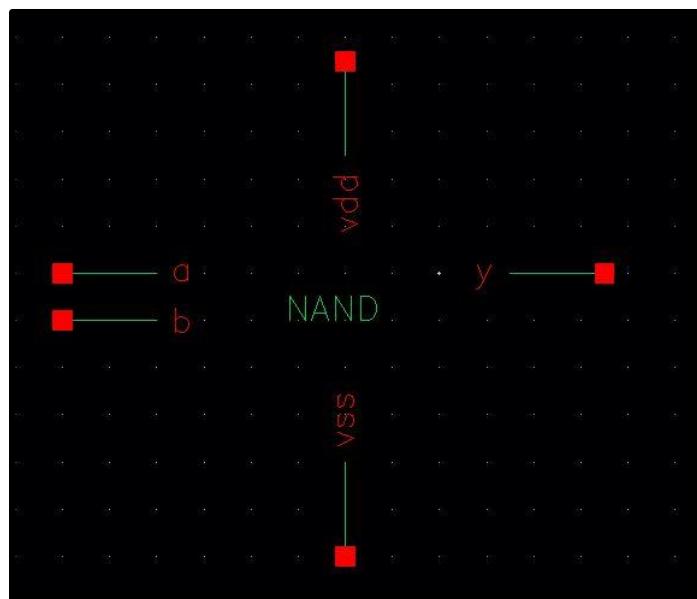


Fig. 14: The green and red rectangles are deleted

VI. **Editing the Symbol:** In this section we will modify the NAND gate symbol to look like a NAND gate symbol



Fig. 15: Editing symbol using these tools

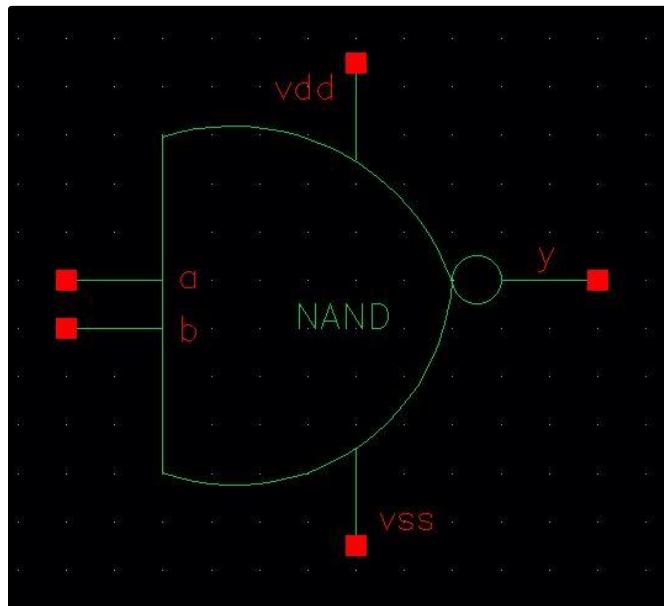


Fig. 16: Final NAND symbol

5. Finding operating region:

- I. Draw the schematic diagram:** In the previous schematic diagram use vdc as VDD, a and b. Check and Save the schematic.

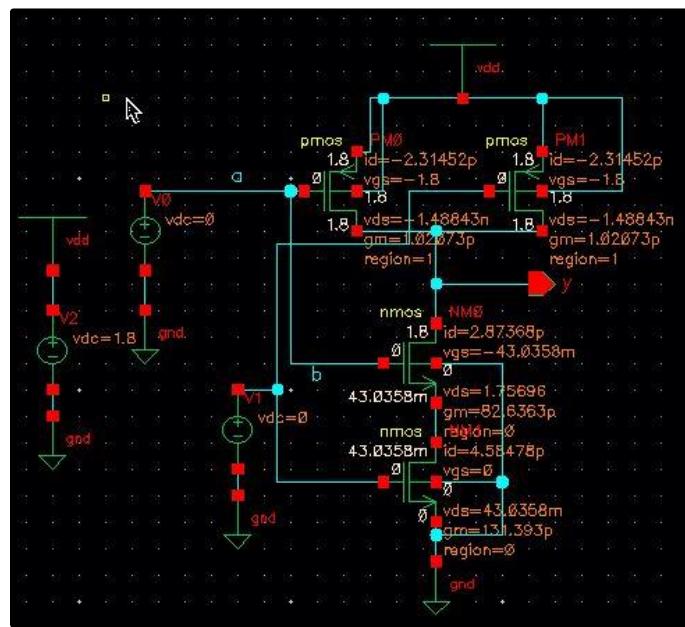


Fig. 17: Schematic diagram

- II. From the schematic diagram click – launch > ADE L. A “Virtuoso Analog Design Environment” window is open.**

In this window click – **Analyses > Choose** or just click on icon  . A “Choosing Analyses..” window is open.

In this window select **dc, Save DC Operating Point**. Click –**ok**.

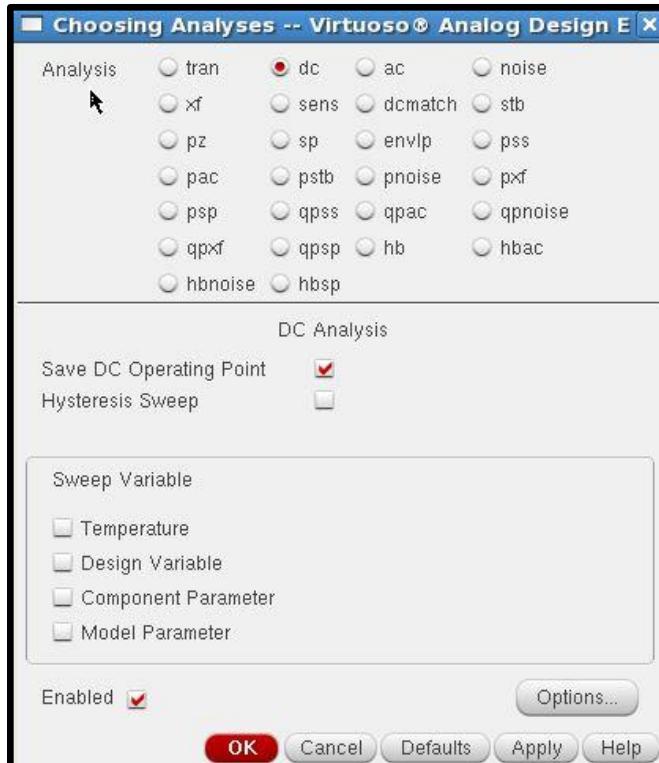


Fig. 18: Choosing Analysis window

III. In the virtuoso analog design environment window analysis type is saved. **Run** the simulation.

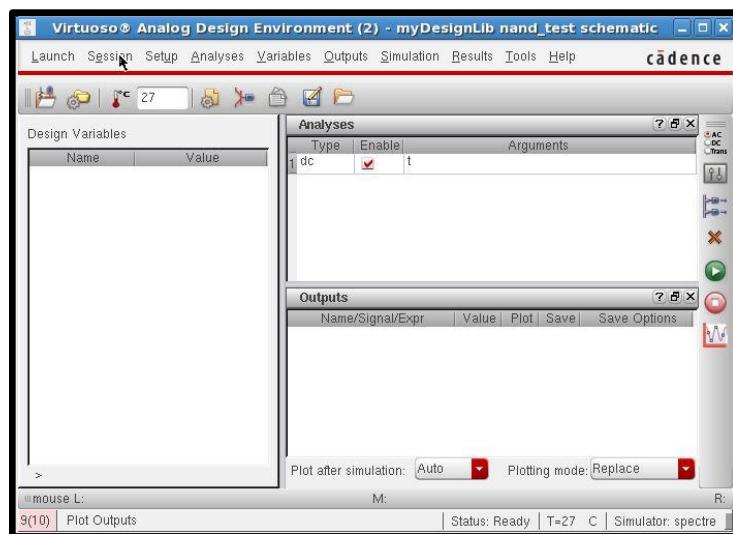


Fig. 19: Virtuoso analog design environment window

IV. From the Schematic window click – Edit > Component Display.

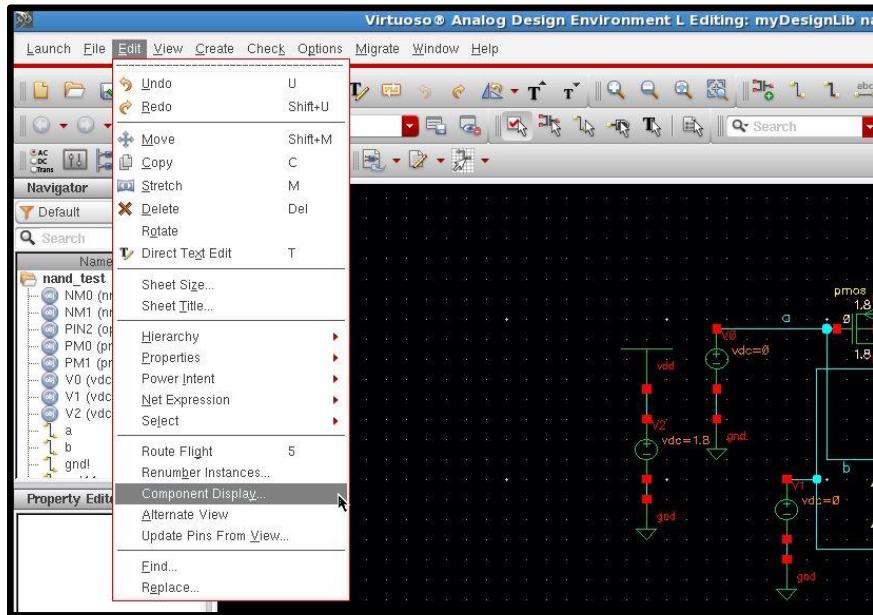


Fig. 20: Schematic window

V. An “Edit Component Display Options” window is open.

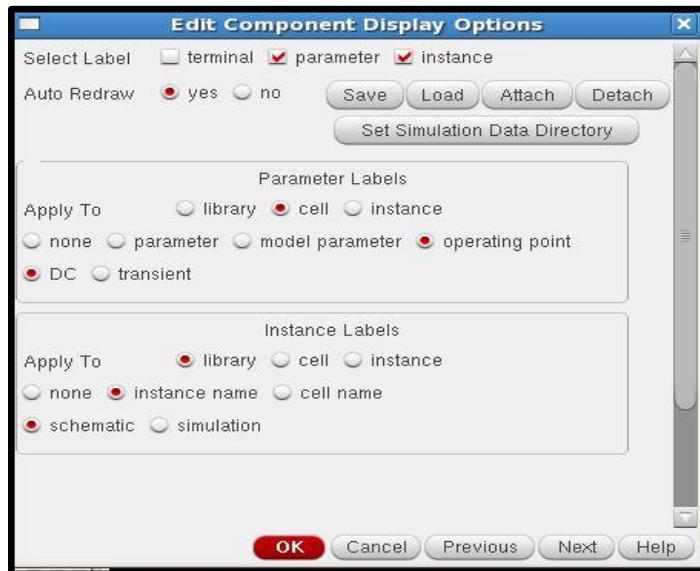


Fig. 21: Edit component display options window

VI. Select a MOSFET from schematic. “Edit Component PM1 Display” is open. In this window select the **display value only. Do it for every MOSFET.**

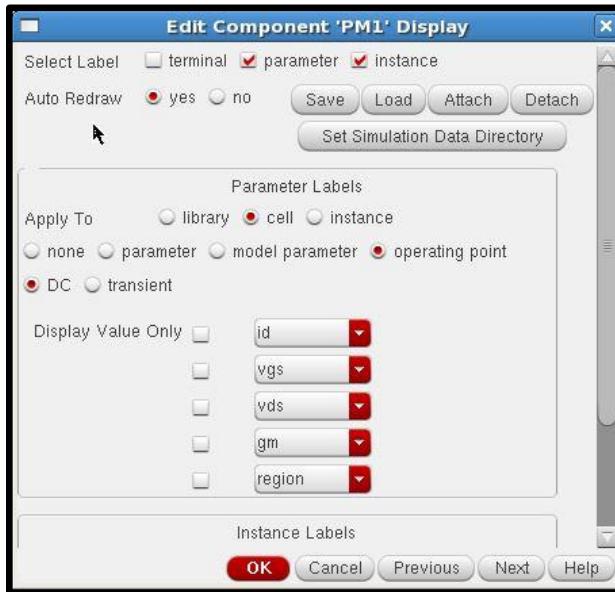


Fig. 22: Edit component display for different MOSFET

VII. Finally see the dc operating point of all MOSFET in the schematic window.

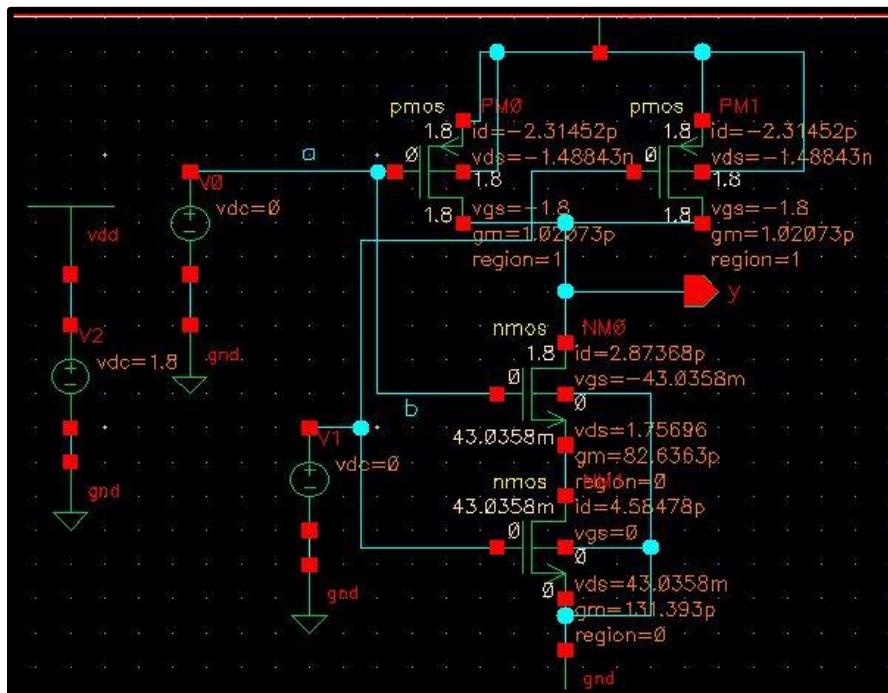


Fig. 23: Operating points of MOSFETs

6. DC and Transient analysis:

I. For the DC and transient analysis two vpulse are connected in a and b. A vdc is connected in vdd. Vpulse are taken from analoglib library.

The properties of vpulse are given below-

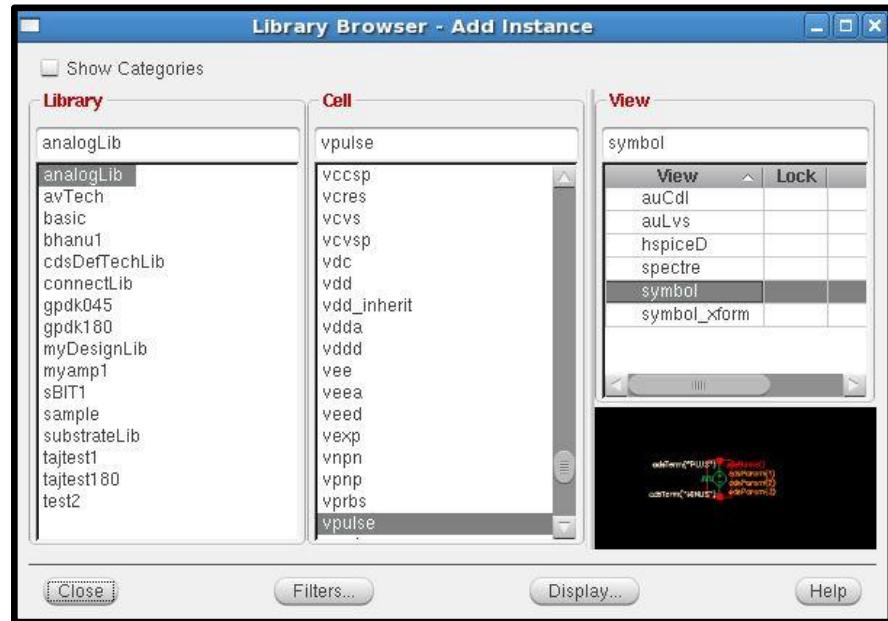


Fig. 24: Vpulse are taken from analoglib library



Fig. 25: Properties of vpulse for input a

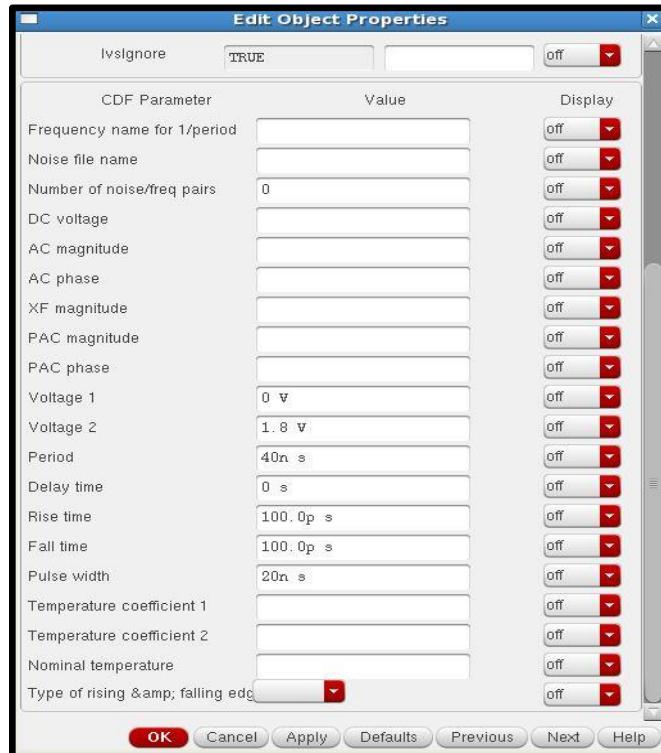


Fig. 26: Properties of vpulse for input b

II. Check and Save the schematic. From the schematic diagram click – **launch > ADE L**. A “**Virtuoso Analog Design Environment**” window is open. In this window click – **Analyses >**

Choose or just click on icon . A “**Choosing Analyses..**” window is open. For transient analysis select **tran**. **Stop time = 200ns**. Select **moderate**. Click – **ok**.

In the virtuoso analog design environment window click – **Outputs > Setup** or just click on icon .

A “**Setting Outputs..**” window is open. In this window click on **From Schematic** and select a, b and y wires from the schematic diagram.

In the virtuoso Analog Design Environment window selected wires and Analyses type are saved.

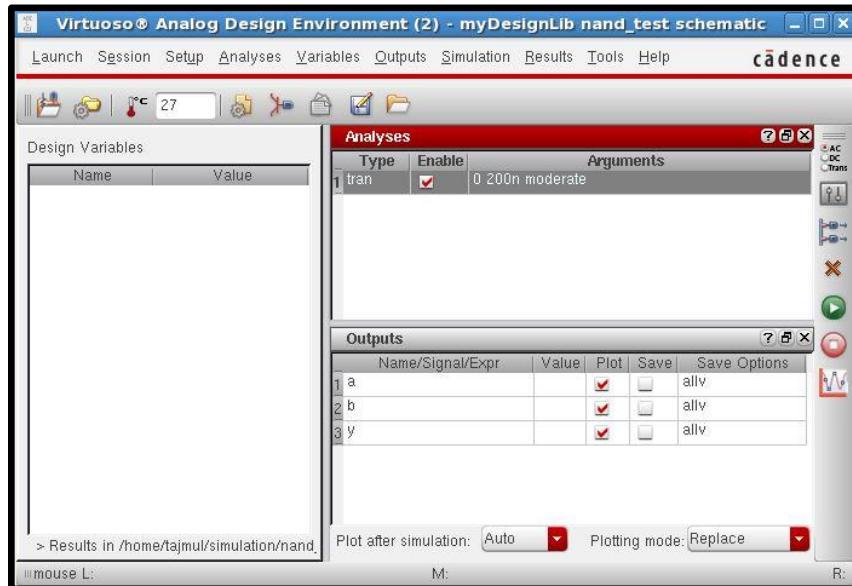


Fig. 27: Virtuoso analog design environment window

III. Run the simulation and see the transient response of NAND gate.

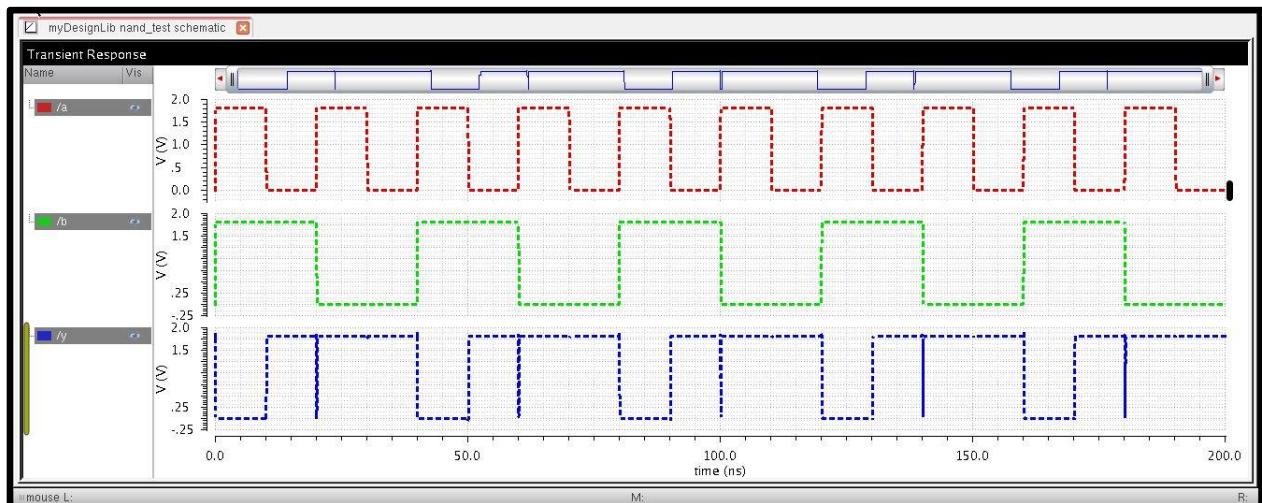


Fig. 28: Transient response of NAND gate

IV. In this window click – **Analyses > Choose** or just click on icon . A “Choosing Analyses..” window is open. In this window select **dc**, **Save DC Operating Point**, **Component Parameter**. In the choosing analyses window Click – **Select component**. From the schematic window select the **varying source V0**. A “select component parameter” window is open. In this window select – **DC Voltage** and click – **ok**.

In the choosing analyses window write the sweep range – **Start = 0, Stop = 1.8**.

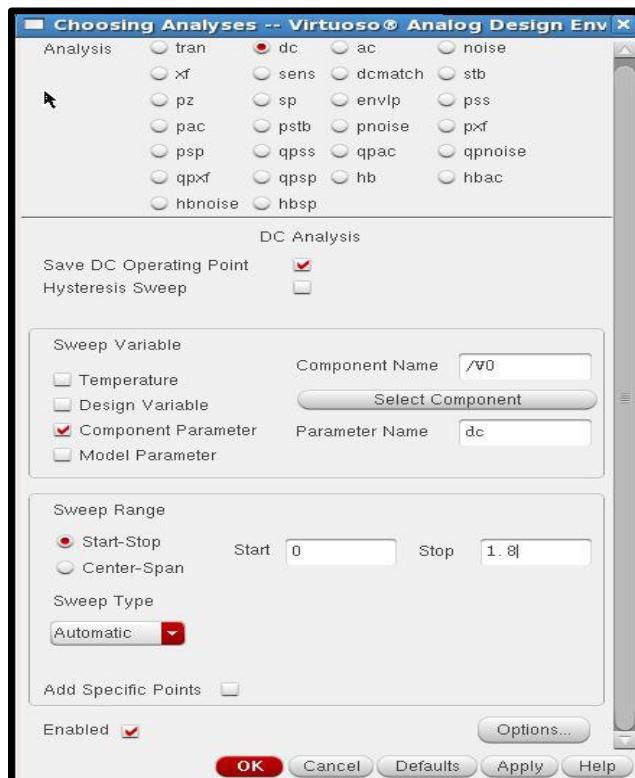


Fig. 29: Choosing analysis.. window

V. In the virtuoso Analog Design Environment window Analyses type dc is saved. Unselect the analyses type tran.

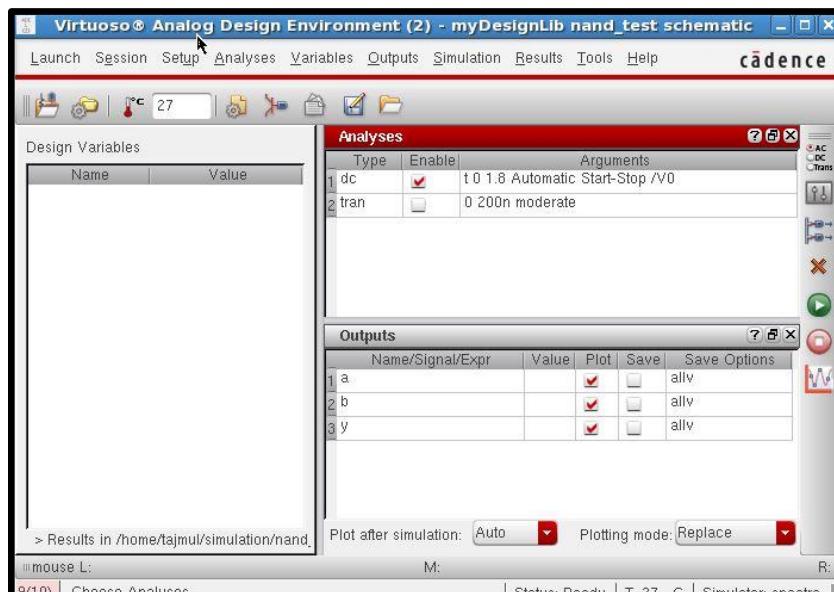


Fig. 30: Virtuoso analog design environment window

VI. Run the simulation and see the DC response of NAND gate.

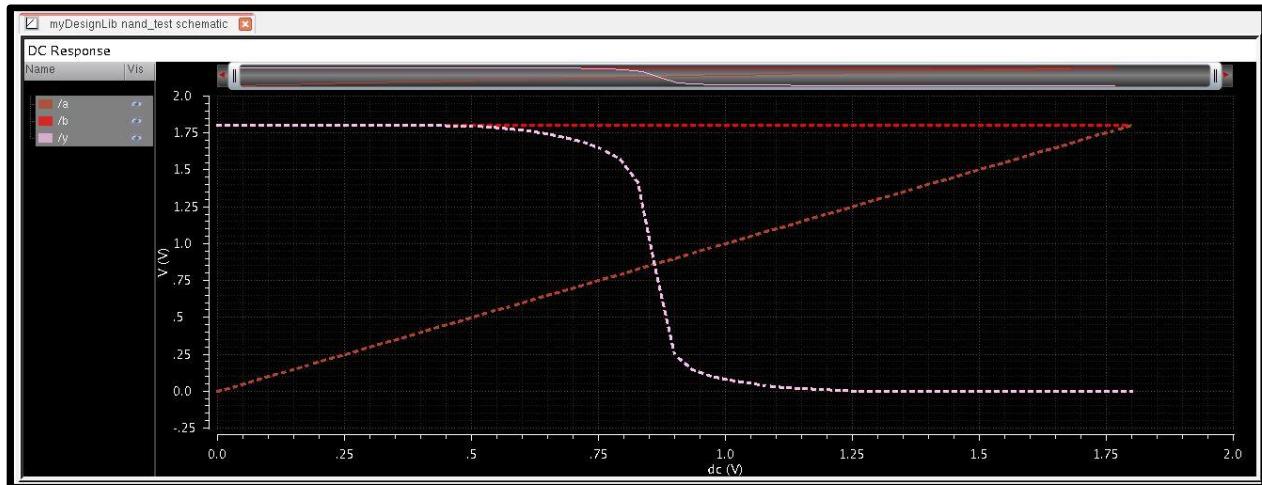


Fig. 31: DC response of NAND gate

Lab Summary:

In this lab you learn how to –

- Library creation.
- Cell View creation.
- Schematic Design.
- Symbol creation.
- Finding operating region.
- DC and Transient analysis.

We can Use same technique for NOR gate.

End of Lab 2

Lab 3: Characterization of a MOSFET. (Ref: Razavi: Sections 2.1 and 2.2)

Objective:

- 9) To simulate the voltage-current relationships of a MOSFET in Cadence platform.
- 10) To perform DC analysis.
- 11) To perform Parametric analysis (also use calculator tool). Determine λ (Channel length modulation coefficient).
- 12) To perform step 3 by changing W/L of the MOSFET. Determine λ at $V_{GS}=0.7$ V and $V_{GS}=1.8$ V. explain the difference between step 3 & 4.
- 13) To find out the square root of I_d and from this estimate V_{th} . (Hint. Use linear extrapolation)
- 14) To determine g_m (Transconductance) at $V_{GS} = 1$ V. Compare to the value on the plot.
- 15) To observe the body effect.
- 16) To observe relation of Threshold voltage with body effect.

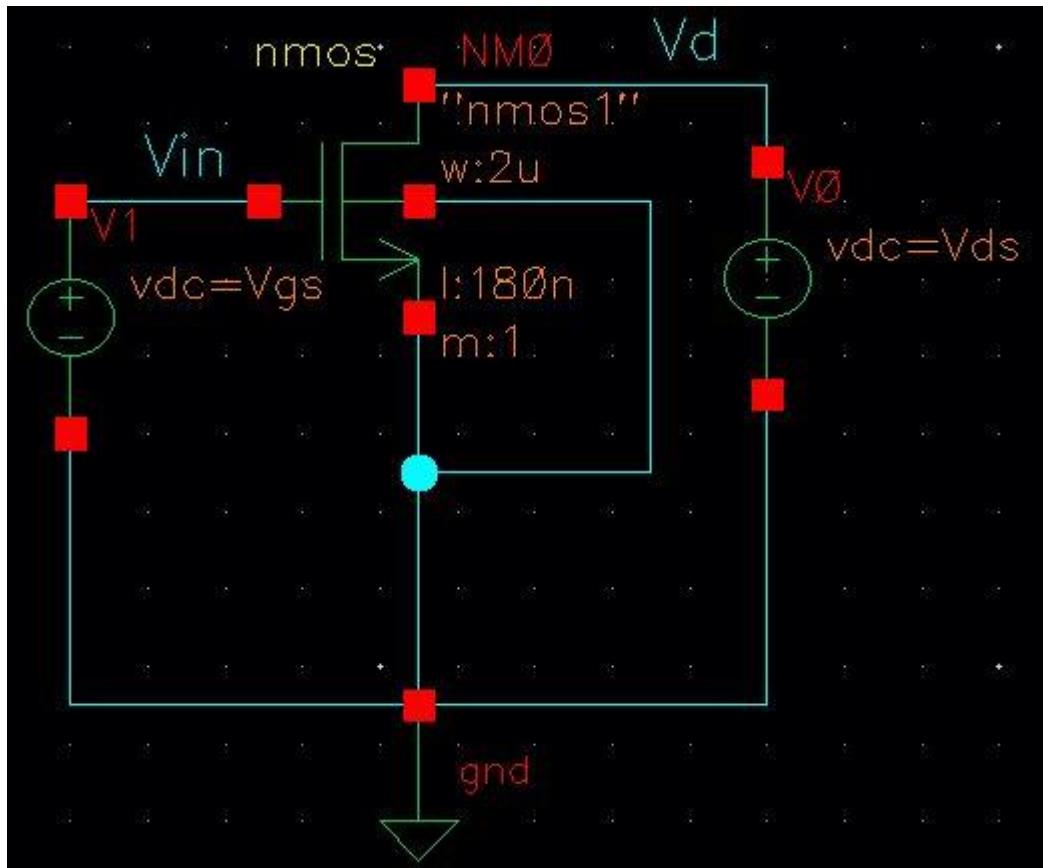
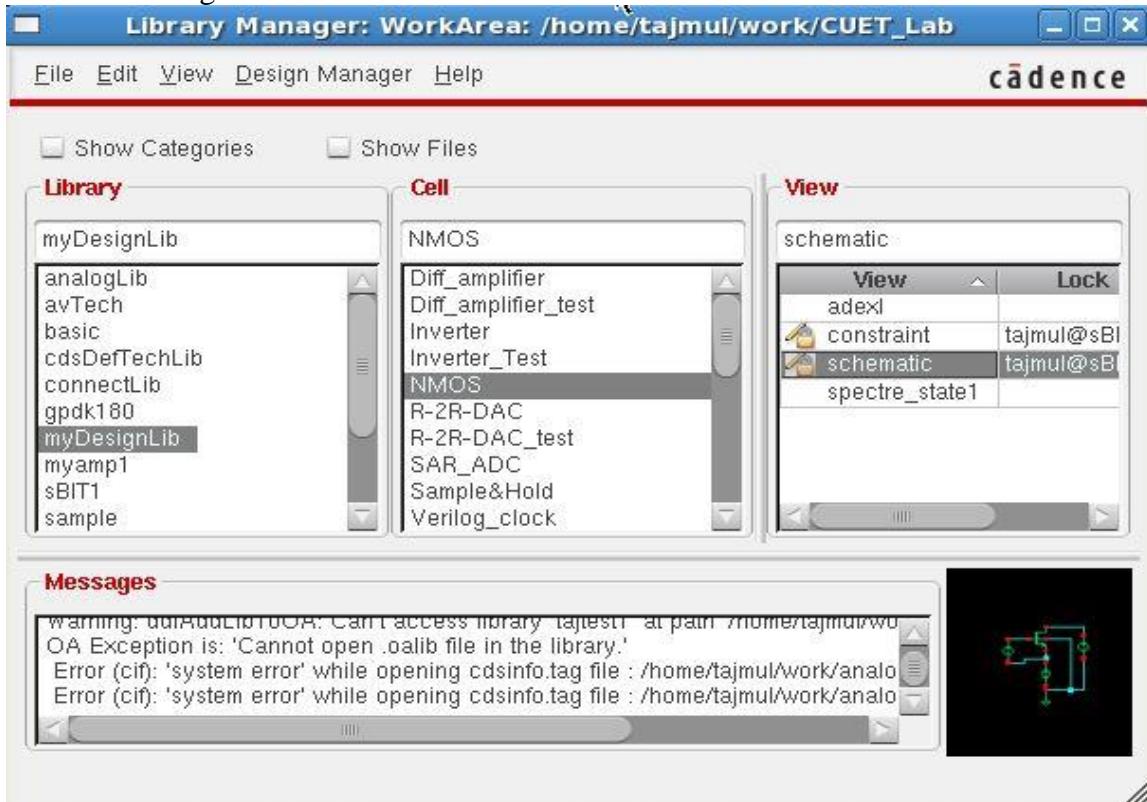


Fig 1: A NMOS test circuit.

In this lab we will simulate the voltage-current relationships of a NMOS transistor in Cadence and estimate some process parameters using the simulation results. Finally the body effect and its relation to the threshold voltage will be simulated.

- I. First start Cadence virtuoso platform and select our library “**myDesignLib**”. Create a new cell (say: NMOS) within this library and draw the schematic shown in above Figure. This schematic will be used to simulate the relationship between Vgs, Vds, and Id for a single NMOS transistor.



- II. The DC voltage of the two sources is set to the variable names Vgs and Vds. Later, we will sweep these variables.

III. The transistor has length=180um and width=2um. Check and Save the design.

IV. To build this test circuit we need below items:

Library name	Cellview name	Properties
MyDesignLib	NMOS	Symbol
analogLib	Vdc (as input signal)	Voltage = Vgs (as variable)
analogLib	Vdc (Drain to Source)	Voltage = Vds (as variable)
analogLib	gnd	

- V. Add the above components using **Create — Instance** or by pressing **I** or VI. Wire your schematic.
 VII. Click **Create — Wire Name** or press **L** to name the input (Vin) and Drain Voltage (Vd) wires as in the Fig 1.
 VIII. Click on the **Check and Save** icon to save the design.

1) To simulate the voltage-current relationships of a MOSFET in Cadence platform

In this section, we will run the simulation for Nmos and plot the DC characteristics and we will do Parametric Analysis after the initial simulation.

I. Starting the Simulation Environment

In the Nmos schematic window, execute **Launch – ADE L**. The **Virtuoso Analog Design Environment (ADE)** simulation window appears.

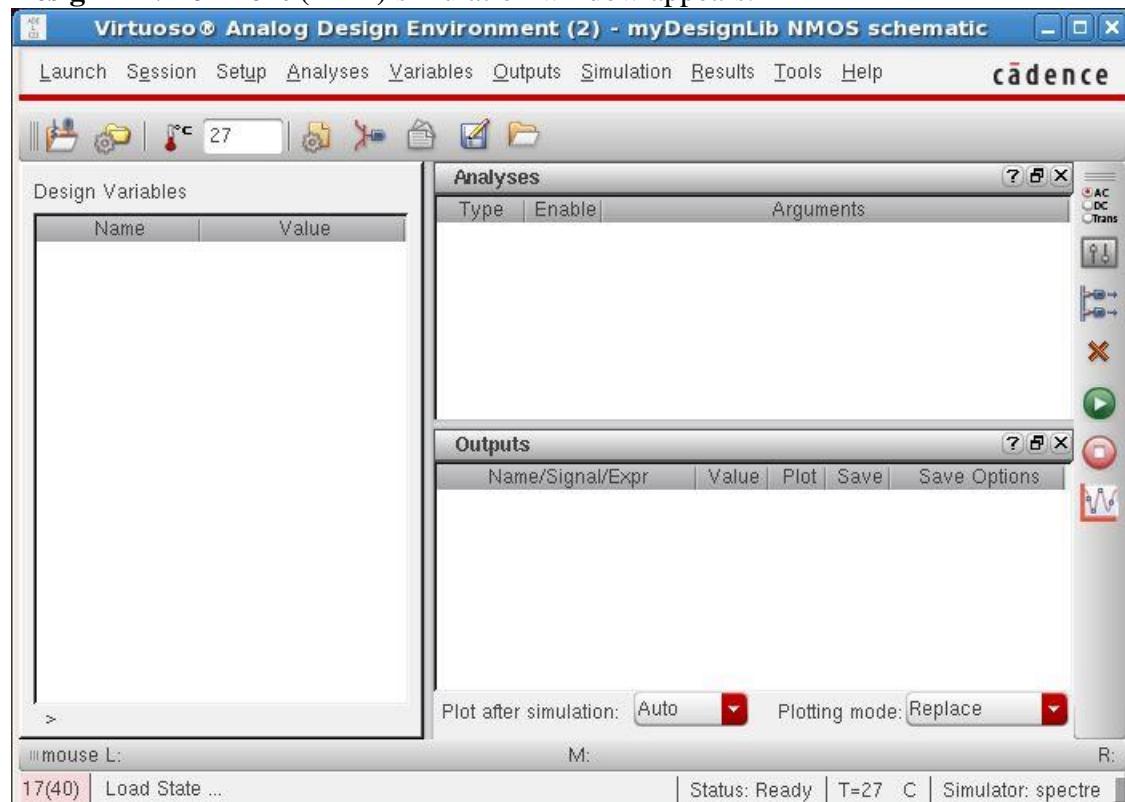
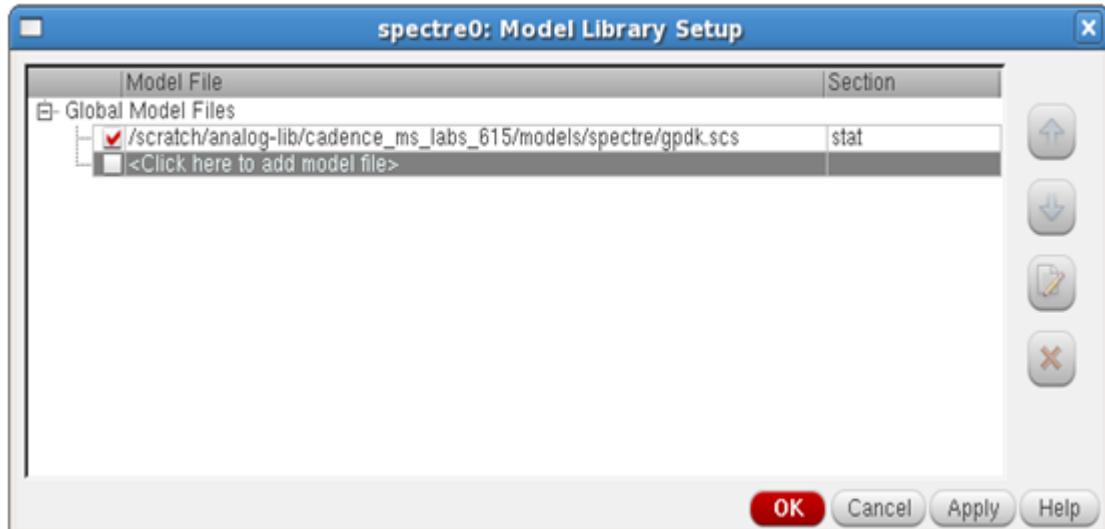


Fig: Virtuoso ADE form

- II. Set the environment to use the **Spectre®** tool, a high speed, highly accurate analog simulator. Use this simulator with the Nmos test design, which is made-up of analog components.
- III. In the simulation window (ADE), execute **Setup— Simulator/Directory/Host**.
- IV. In the Choosing Simulator form, set the Simulator field to **Spectre** (Not spectreS) and click **OK**.
- V. The Model Library file contains the model files that describe the nmos and pmos devices during simulation.
- In the simulation window (ADE L), execute **Setup - Model Libraries**.
- VI. The Model Library Setup form appears. Click the **browse** button to add **gdk.scs** if not added by default as shown in the **Model Library Setup** form. Remember to select the section type as **stat** in front of the gdk.scs file.
- VII. The Model Library Setup window should looks like the figure below.



- VIII. To view the model file, highlight the expression in the **Model Files** field and Click **Edit File.**
- IX. To complete the Model Library Setup, move the cursor and click **OK**.
- X. **Choosing Analysis:**
This section demonstrates how to view and select the different types of analysis to complete the circuit when running the simulation.
- XI. In the Simulation window (ADE), execute **Analysis - Choose Analysis** or click the **Choose Analysis** icon.
- XII. The Choosing Analysis form appears. This is a dynamic form, the bottom of the form changes based on the selection above.

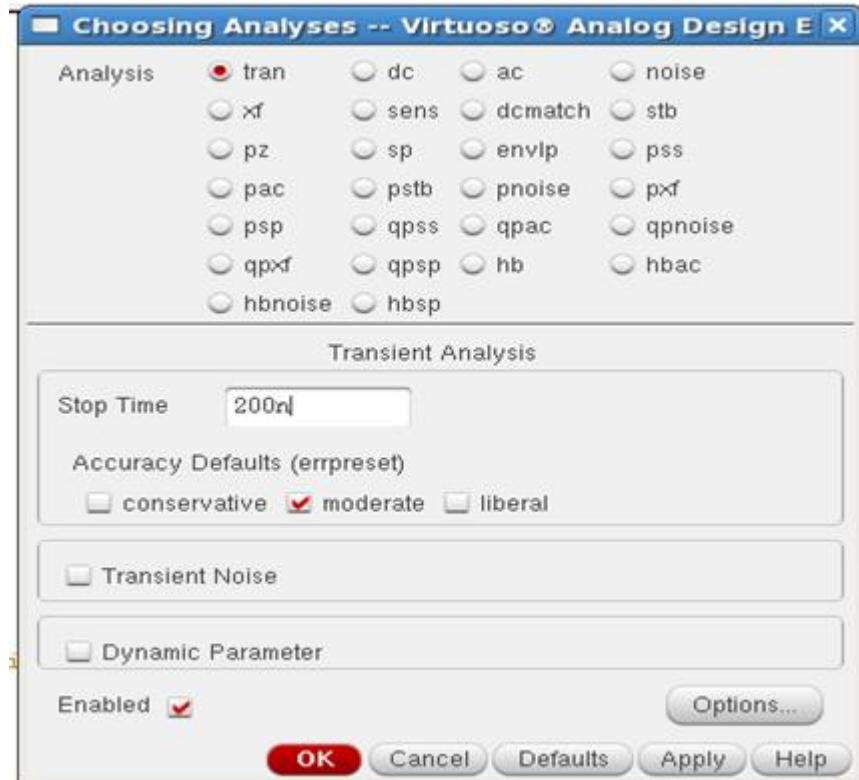
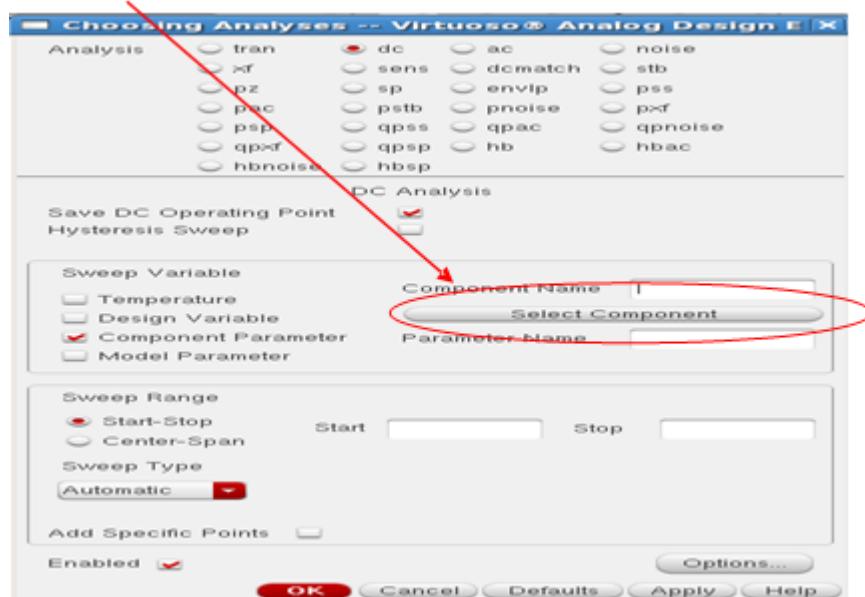


Fig 2: Choose Analysis form

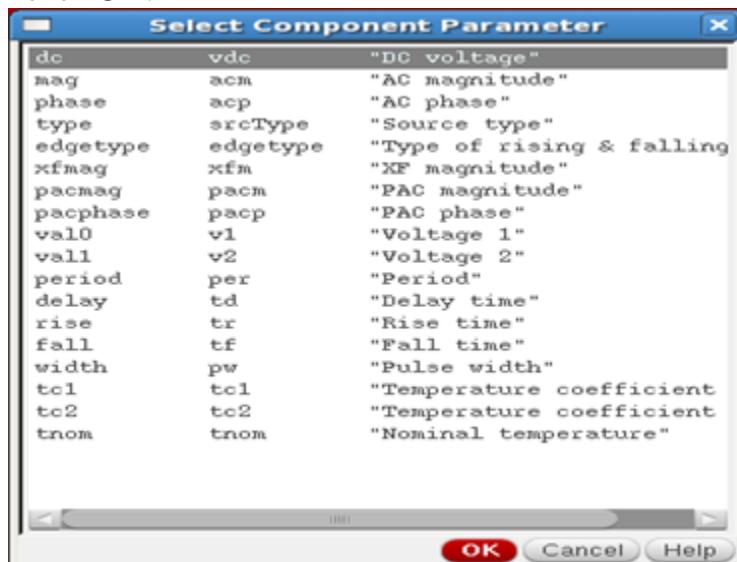
2) To perform DC analysis:

I. To set up for DC Analysis:

- In the Analysis section, select dc.\
- In the DC Analysis section, turn on **Save DC Operating Point**.
- Turn on the Component Parameter.
- Click the **Select Component**, Which takes we to the schematic window.



- e) Select input signal **V0 source (Vds)** in the test schematic window.
- f) Select **DC Voltage** in the ‘Select Component Parameter’ window and click **OK**.



- g) In the analysis form, enter **start** and **stop** voltages as **0** to **2** respectively.
- h) Check the enable button and then click **Apply**.

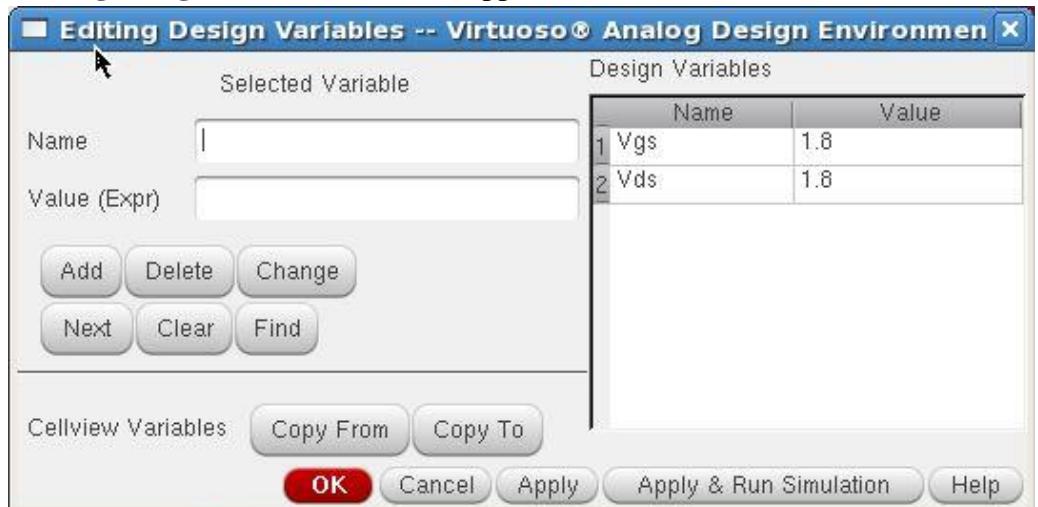


- i) Click **OK** in the Choosing Analysis Form.

II. Setting Design Variables:

Set the values of any design variables in the circuit before simulating. Otherwise, the simulation will not run.

- a) Here The DC voltage of the two sources is set to the variable names Vgs and Vds. Later, we will sweep these variables.
- b) In the Simulation window, execute **Variables – Edit variables** or click the **Edit Variables icon** present in the **ADE L** window. The **Editing Design Variables** window appears

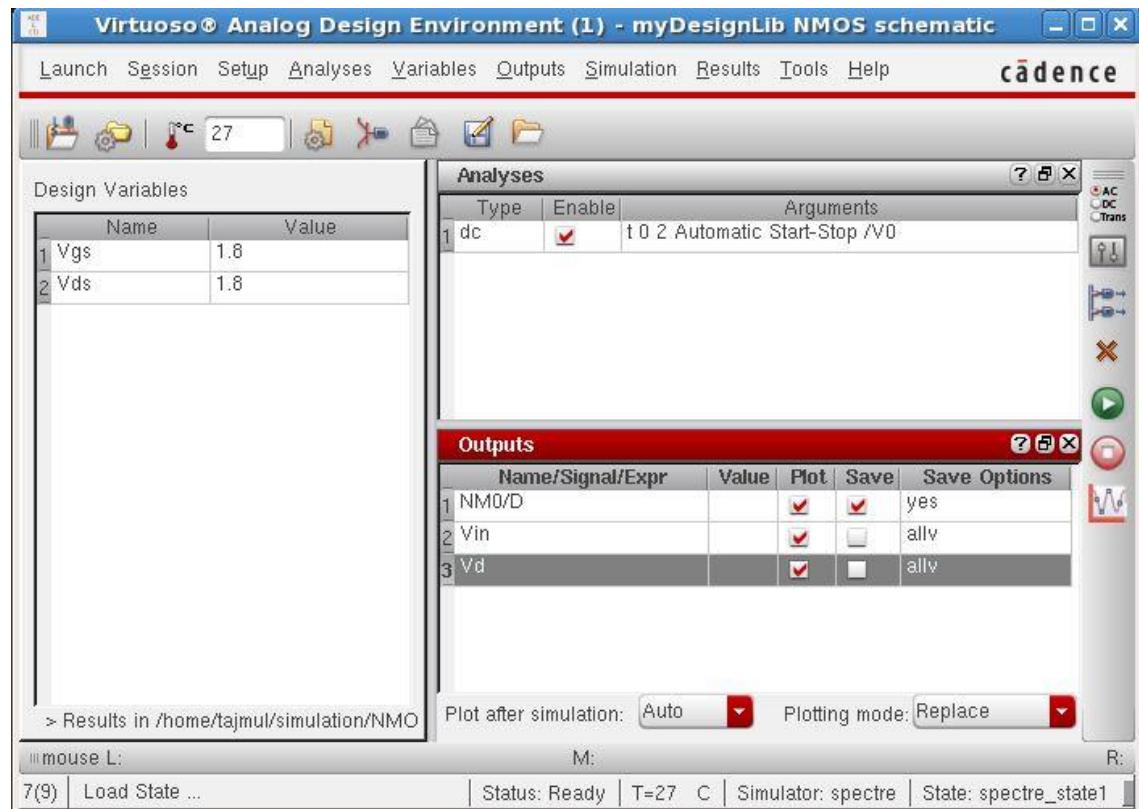


- c) Click **Copy From** at the bottom of the window. The design is scanned and all variables found in the design are listed. In a few moments, the **Vgs and Vds** variable appears in the Table of Design variables section.
- d) Set the value of the Vgs and Vds variable: With the Vgs and Vds variable highlighted in the Table of Design Variables, click on the variable name Vgs and Vds and enter the following:

Value (Expr)	1.8
--------------	-----

- e) Click **Change** and notice the update in the Table of Design Variables, Click **OK** to exit.

- III. Execute **Outputs – To be plotted – Select on Schematic** in the simulation window.
- IV. Follow the prompt at the bottom of the schematic window, Click on output node of Nmos drain NMO/D; input net of **Vds** of the Nmos. Press **Esc** with the cursor in the schematic after selecting it.
- V. After setting the DC analysis and also the signals for wave plotting, the ADE L window will look like the figure below;



- VI. Now execute **Simulation – Netlist and Run** in the simulation window to start the Simulation or the **Netlist and Run** icon present in the ADE L window, this will create the netlist as well as run the simulation.
- VII. When simulation finishes, the DC plots automatically will be popped up along with log file.
- VIII. The output “NMO/D” should now appear in the Outputs waveform window.

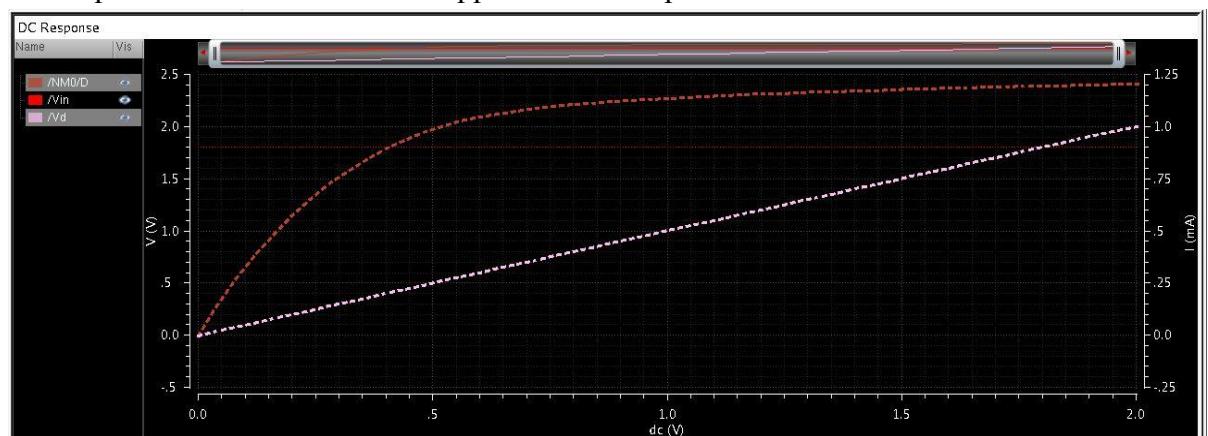


Fig 3: Id vs Vds (DC response)

- IX. Click on the **Split Current Strip** icon to separate the wave plots.

3) To perform Parametric analysis. Determine λ (Channel length modulation coefficient).

Now for Parametric analysis we will enter Vgs for the variable name, sweep it from 0 to 1.8 V using 6 total steps.

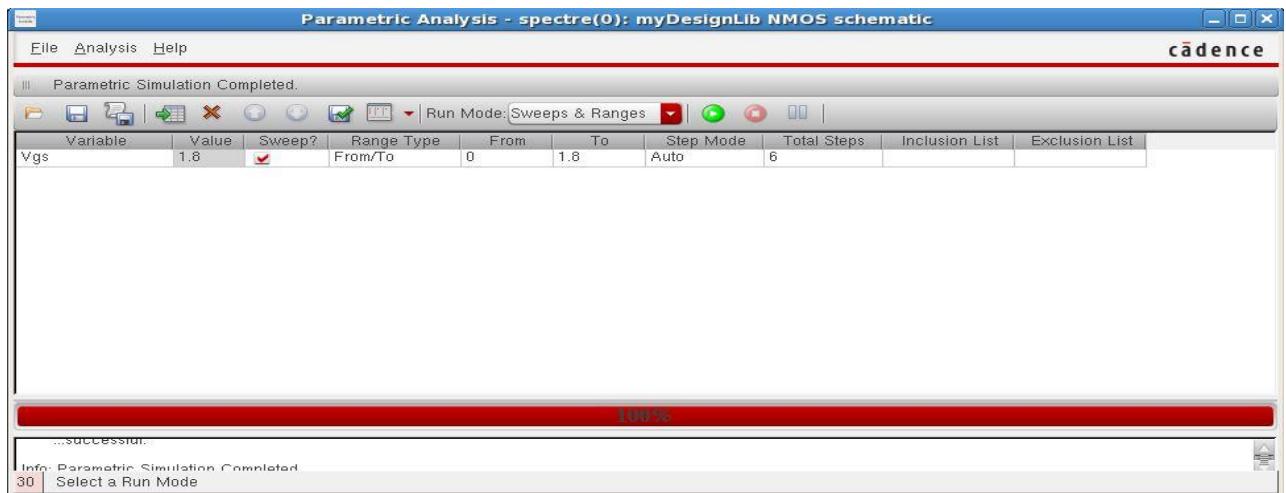
- I. In the Simulation window, execute **Tools—Parametric Analysis**. The Parametric Analysis form appears.
- II. In the **Parametric Analysis** window, double click on the **Add Variable** field. Then an option for selecting the variable appears. This option leads to a selection window with a list of all variables in the design that you can sweep. This list includes the variables that appear in the Design Variables section of the Simulation window.
- III. In the selection window, click on Vgs, the Variable Name field for Sweep in the Parametric Analysis form is set to Vgs.
- IV. Change the **Range Type**, **Step Mode** and **Total Steps** fields in the Parametric Analysis form as shown below:

Range Type: **From/To** From → **0** To → **1.8**

Step Control: **Auto**

Total Steps: **6**

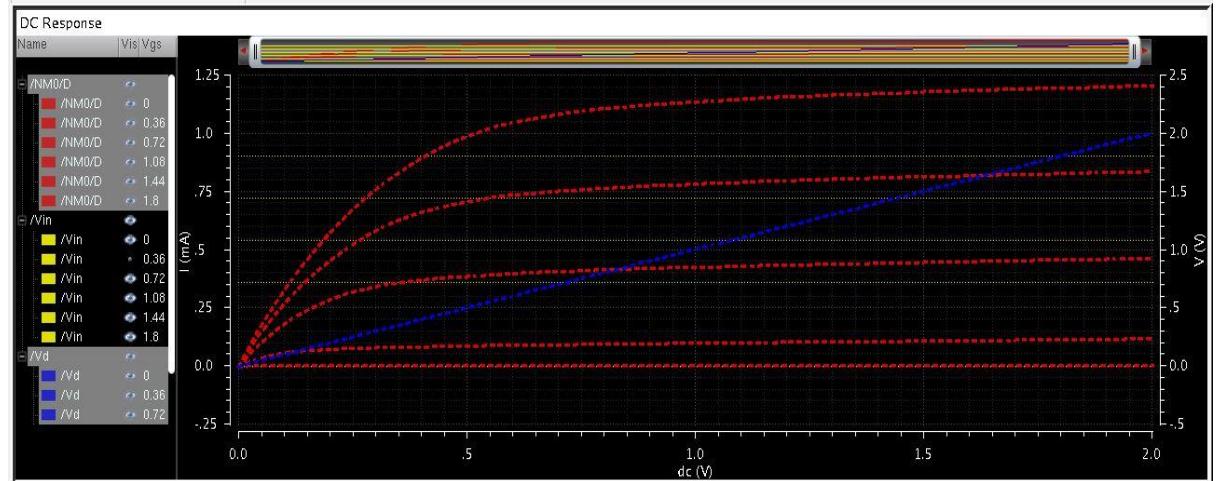
These numbers vary the value of the **Vgs** of the nmos between 0V and 1.8V at six evenly spaced intervals.



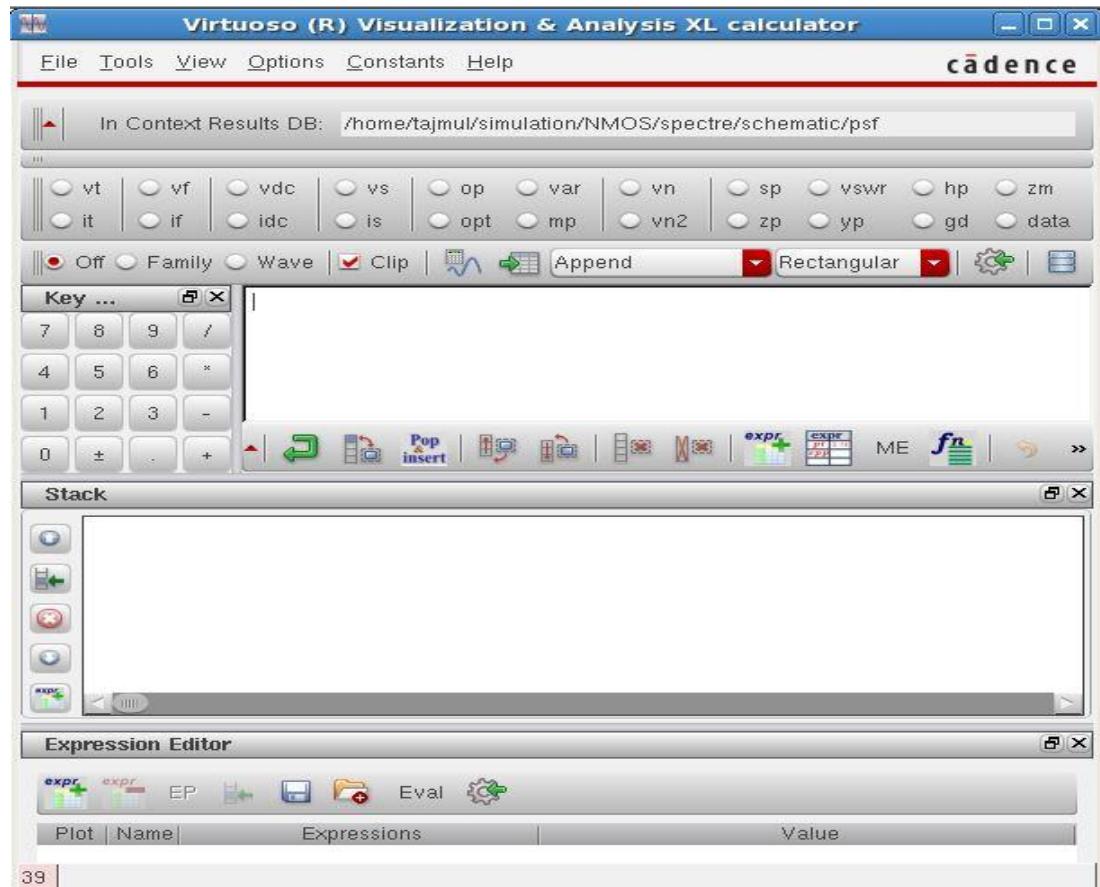
- V. Execute **Analysis—Start Selected** or click the **Run Selected Sweeps** icon in the **Parametric Analysis** window.

The **Parametric Analysis** window displays the number of runs remaining in the analysis and the current value of the swept variable(s). Look in the upper left corner

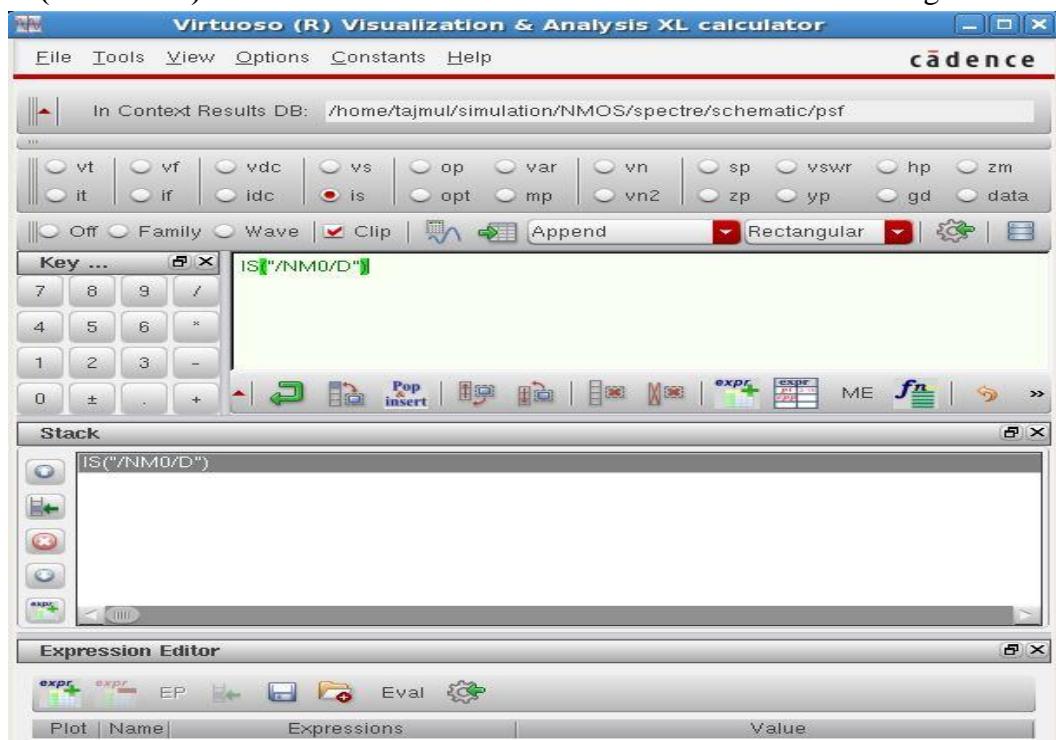
of the window. Once the runs are completed the **wave scan** window comes up with the plots for different runs.



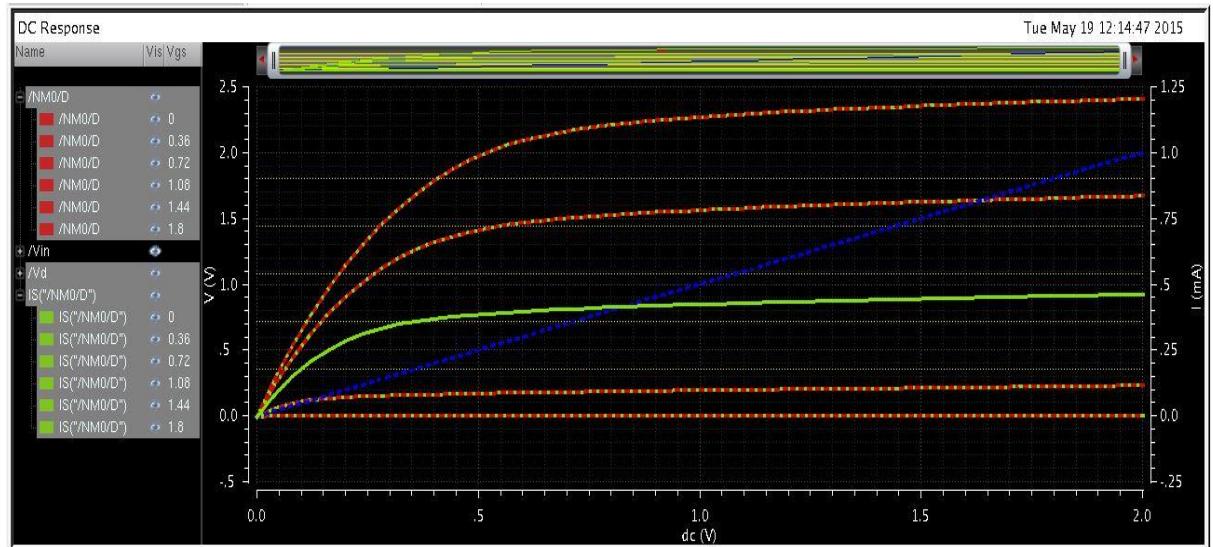
- VI. We will view the output using the Calculator tool. The calculator is a very powerful tool; it gives the user the ability to customize the plots and apply built in functions to data.
- VII. To run calculator go to **Tools > Calculator** from waveform window.
- VIII. To plot the current-voltage characteristics of this transistor, click on the *is* button on the calculator. It will take us to schematic window.



- IX. Then click on the drain terminal of the Nmos in the schematic. So we will get IS("NM0/D") in the calculator window. Now it will look like below figure:

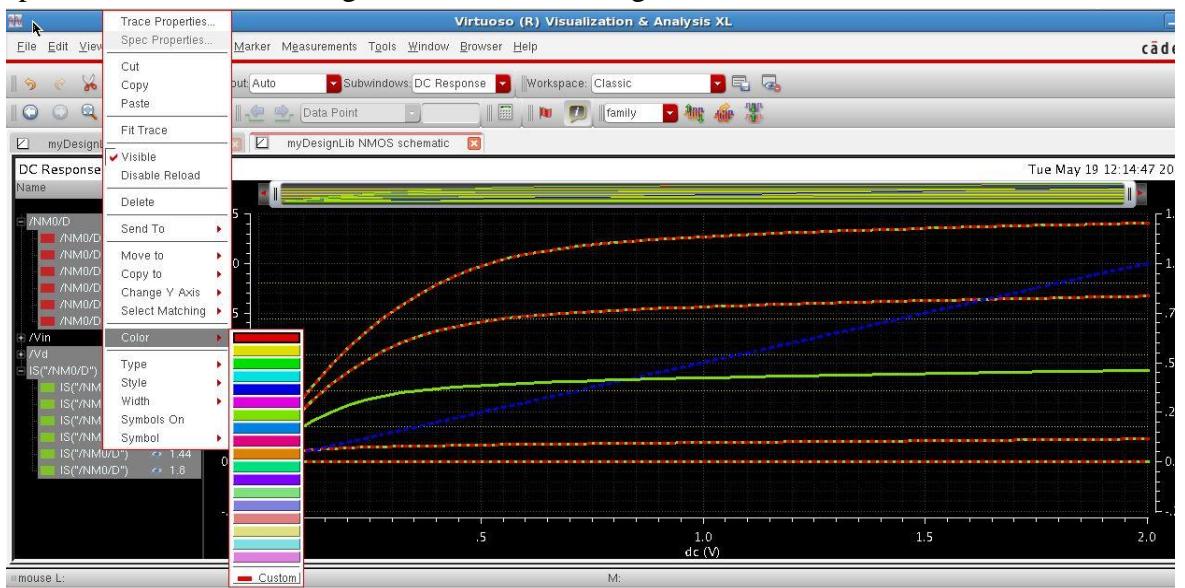


- X. Push the plot button in the calculator. Id vs. vds for different values of vgs should appear in a new window.



- XI. Print this and hand it in.

- XII. We can change the color of waves. To change color we first have to select the specific wave then click right of mouse and change the color as we want.

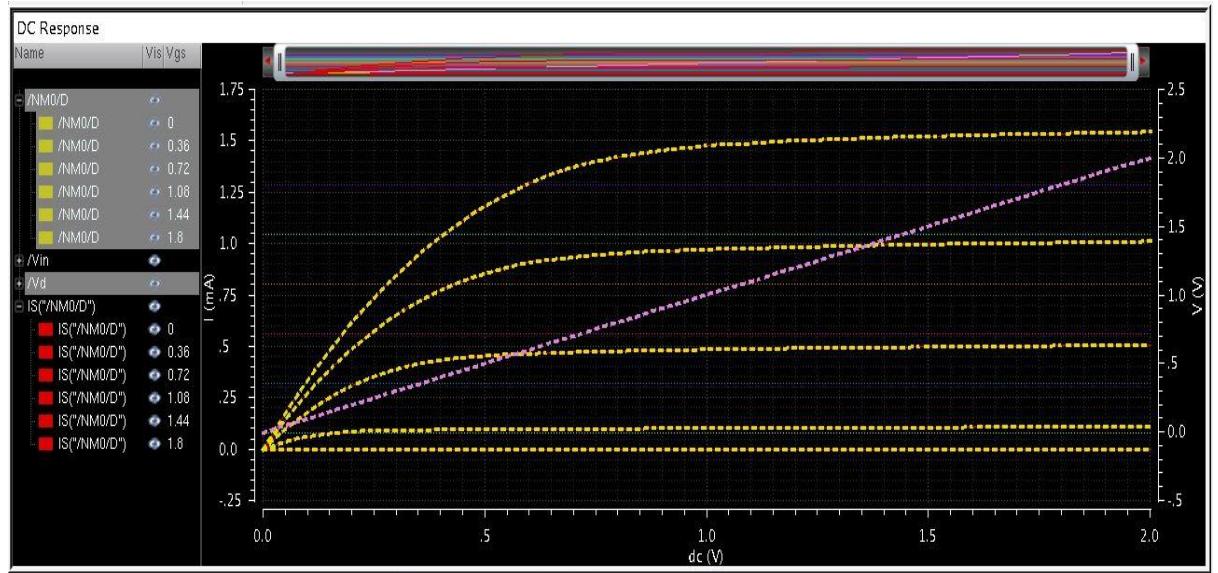


$$I_D = \frac{KP_n}{2} \frac{W}{L} (V_{GS} - V_{THN})^2 [1 + \lambda (V_{DS} - V_{DS,sat})] = I_{D,sat} [1 + \lambda (V_{DS} - V_{DS,sat})]$$

For, $V_{DS} > V_{DS,sat} = V_{GS} - V_{THN}$ and $V_{GS} > V_{THN}$

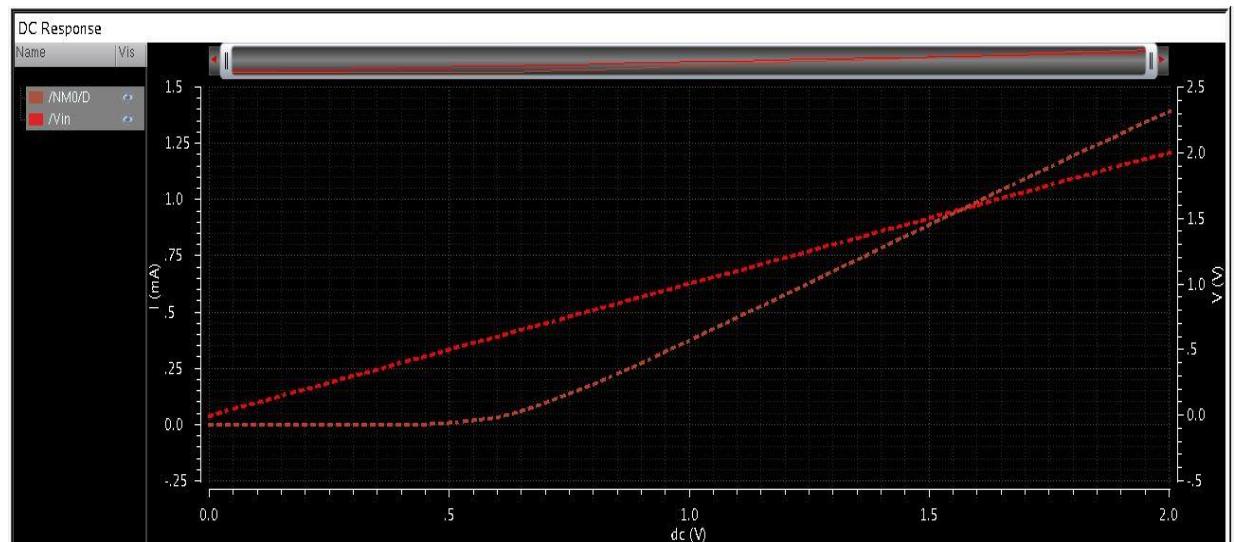
4) To perform step 3 by changing W/L of the MOSFET and explain the difference:

- Change the width of the transistor to 4 um and the length to 360 nm. Plot the Id vs. Vds curve for Vgs from 0 to 1.8 V in 6 steps (like in part 3).
- Determine λ at VGS=0.72 V and VGS=1.8 V. explain the difference between step 3 & 4.



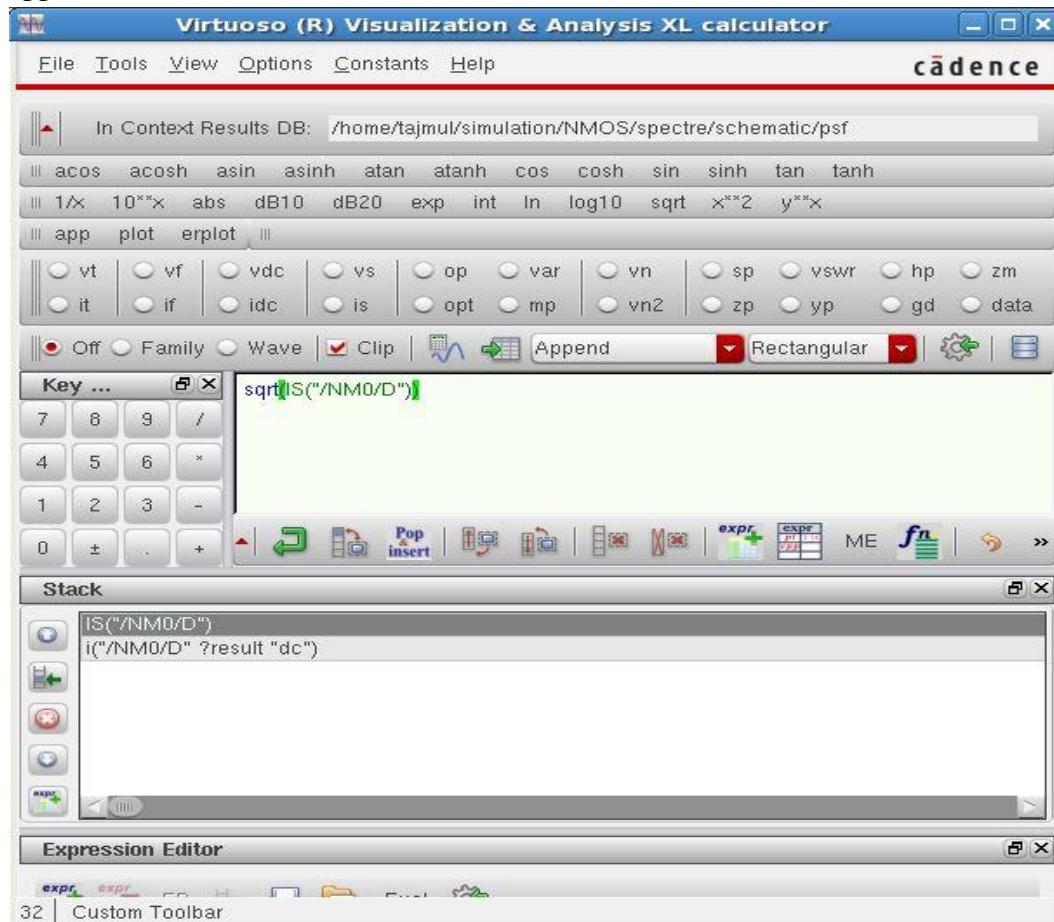
5) To find out the square root of Id and from this estimate Vth:

- I. Now, we will plot Id vs. Vgs for a fixed value of Vds.
- II. Change the size of the transistor back to its original size ($L=180$ nm, width=2 um).
- III. Set up a new dc analysis by following the process done in step 2, sweeping Vgs from 0 to 2. An automatic sweep type will work fine here.
- IV. If you remember, we already set the Vds Design Variable to 1.8 V at the beginning of this lab. So, if this variable is not swept, it will remain at 1.8 V for this simulation.
- V. Now, Click on Netlist and Run, and plot Id using the calculator, as we did in Part 3.
- VI. We should now obtain the Id vs. Vgs curve with Vds at 1.8 V.

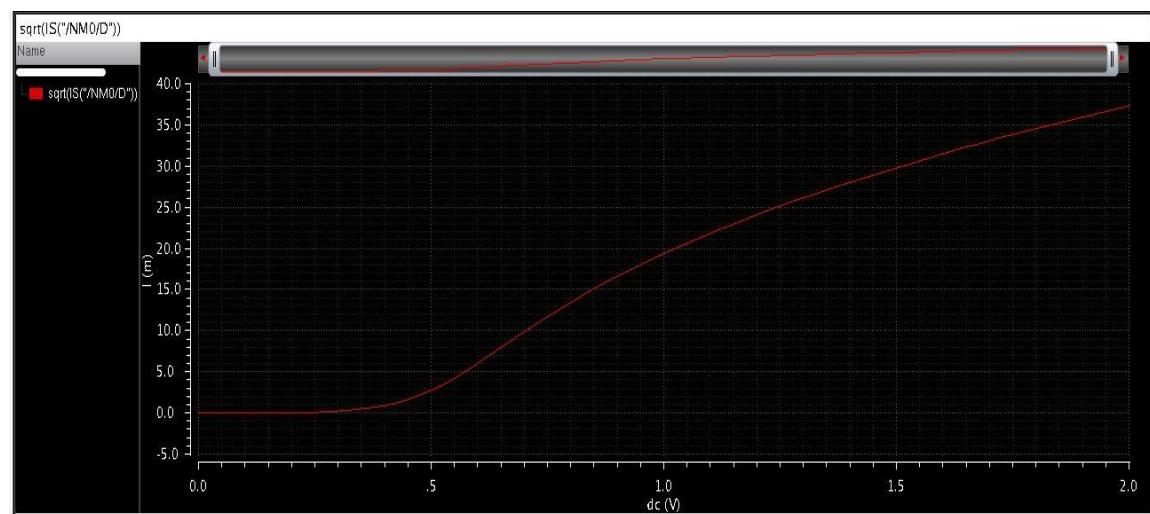


- VII. We would also like to plot the square root (sqrt) of Id. Using this plot we can estimate the threshold voltage Vth for this transistor.
- VIII. Go back to the calculator and the expression **IS("NM0/D")** should still appear in the window.

- IX. We want to take the sqrt of this, so press the *sqrt* button on the calculator. The button pressed on the calculator operates on the expression that is already displayed (The calculator uses Reverse Polish Notation). Now, $\text{sqrt}(\text{IS}("/\text{NM0/D}")$) should appear in the window.



- X. Push the *erplot* button. This will erase all previous plots and plot the expression in a new window.



- XI. Print this curve and hand it in. Using this curve estimate the value for Vth. (Hint. Use linear extrapolation)

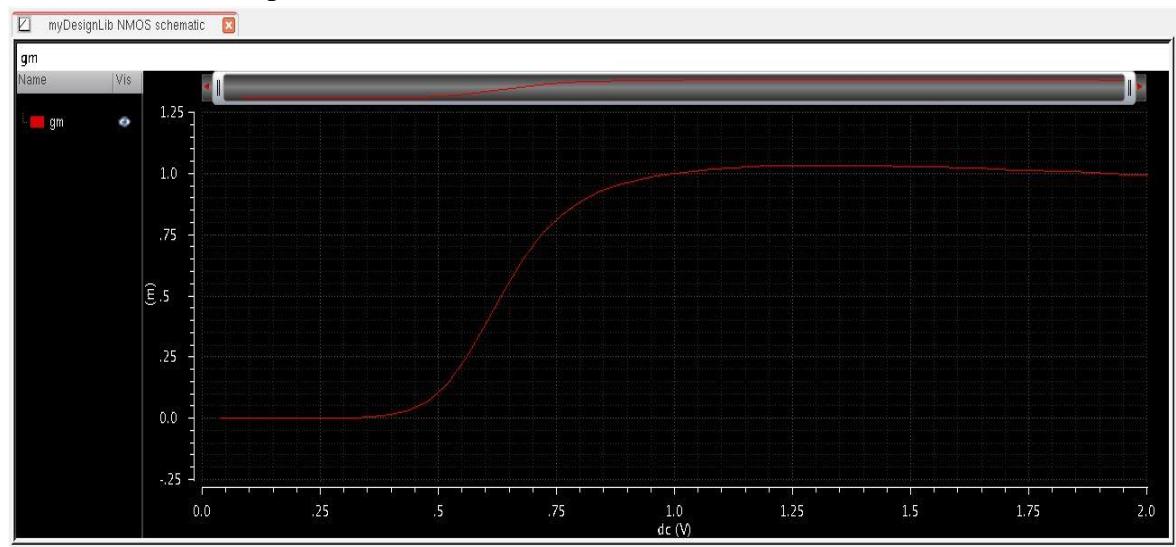
6) To determine gm (Transconductance) at Vgs = 1 V. Compare to the value on the plot:

Let's see how gm varies with Vgs.

- I. In the calculator, make sure IS("NM0/D") is displayed as the current expression.
- II. We would like to take the derivative of this curve to find how gm varies with Vgs.
- III. Go to the Special Functions button on the calculator, and then click on the *deriv* button.



- IV. The new expression should be **deriv(IS("NM0/D"))**.
- V. Plot this waveform, print, and hand in.



- VI. Using the equations from text book (Razavi), determine gm at Vgs = 1 V. Compare to the value on the plot.

7) To observe the body effect:

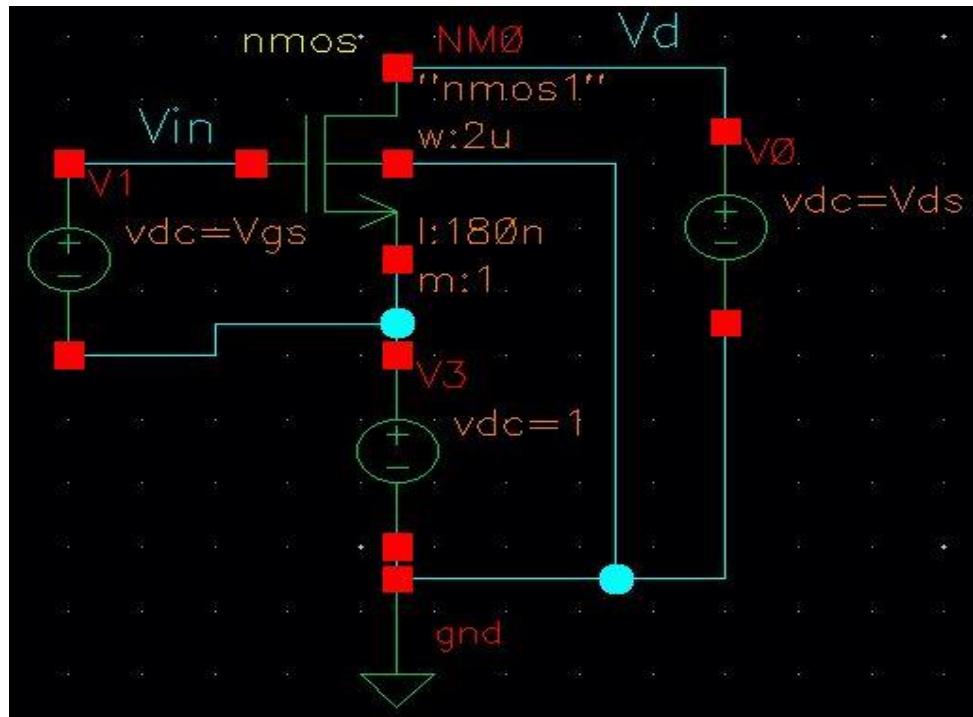
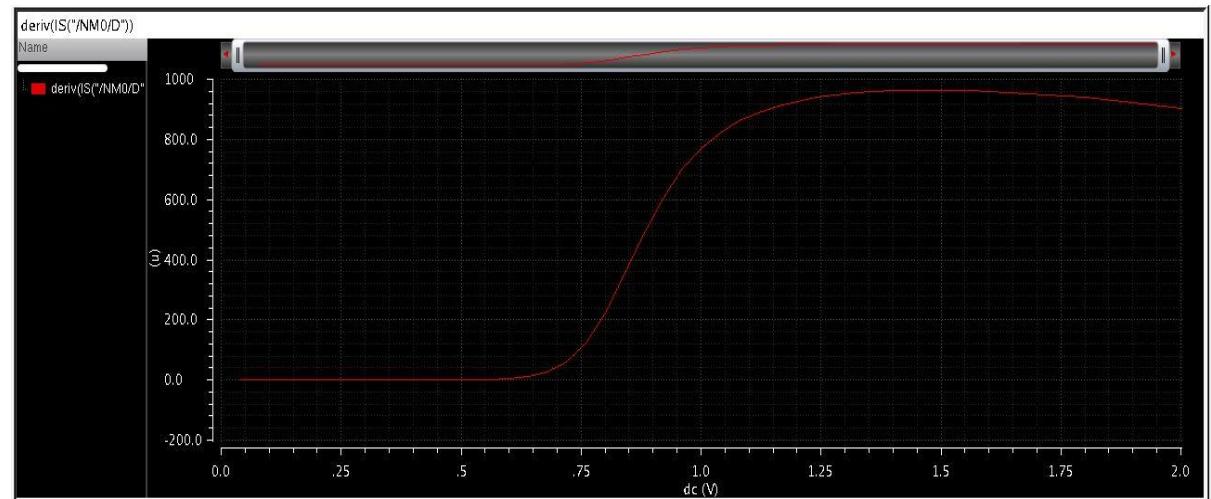


Fig 4:

Finally, we would like to see how the body effect changes V_{th} .

- I. Add a 1 V dc voltage source from the source of the transistor to ground as shown in the above figure.
- II. Now there is a difference in potential between source and bulk.
- III. The negative terminal of the V_{gs} voltage source should now be connected to the source of the transistor, instead of ground.
- IV. Repeat part 6 with this new circuit. Determine V_{th} from the plot.



- V. Explain the how the body effect has changed V_{th} .

End of Lab 3

Lab 4: Design a NMOS with gate voltage 3V and Drain is connected to a 5V source through 200k resistance. Aspect ratio=10/2.

Objective:

- 4) To find operating region.
- 5) To calculate ID, VDS, and estimate the small-signal resistance looking into the drain of the MOSFET.
- 6) Compare your simulation result with hand calculation.

1. Drawing Schematic:

An **nmos** is taken from **gpd़k180** library and two **vdc** are taken from **analoglib** library.

DC Voltage, **V0 = 3V**

DC Voltage, **V1= 5V**

A **resistance** is taken from **gpd़k180** library. Total resistance, **R0 = 200k**. The properties of R0 is given below-

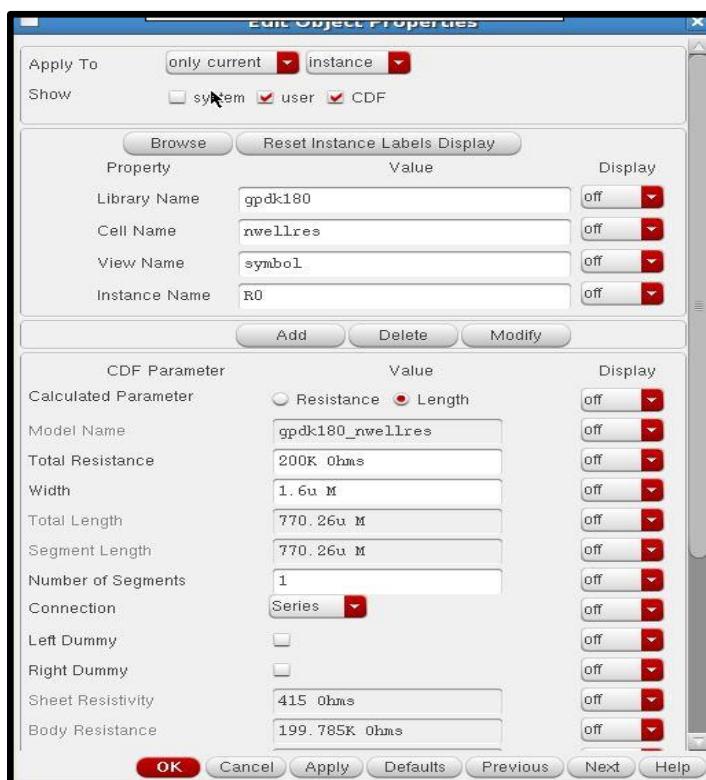


Fig. 01: Properties of resistance

The final schematic diagram is given below-

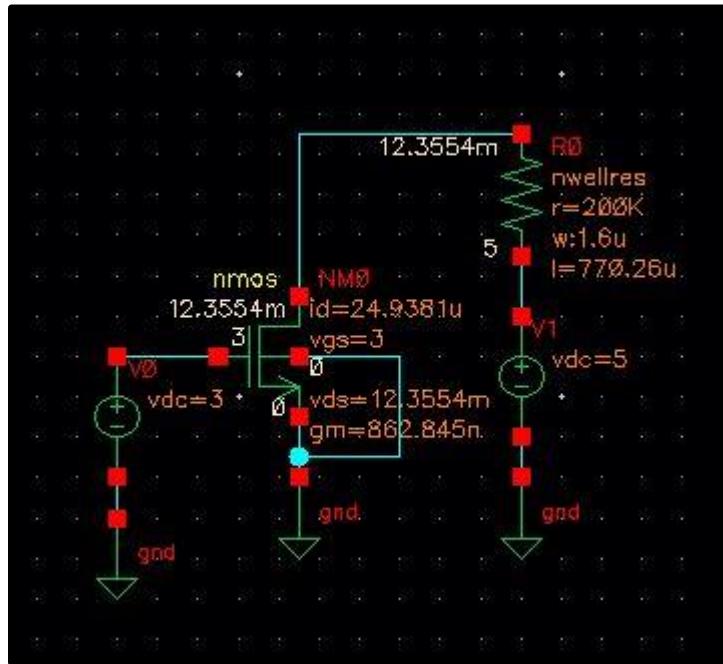


Fig. 02: Schematic Diagram

Now Check and Save the Schematic

2. DC Analysis:

- I. From the schematic window click – **Launch > ADE L**. A “Virtuoso Analog Design Environment” window is open. In this window click icon  . A “Choosing Analyses..” window is open. In this window select – **dc, Save DC Operating Point**. Click – **ok**

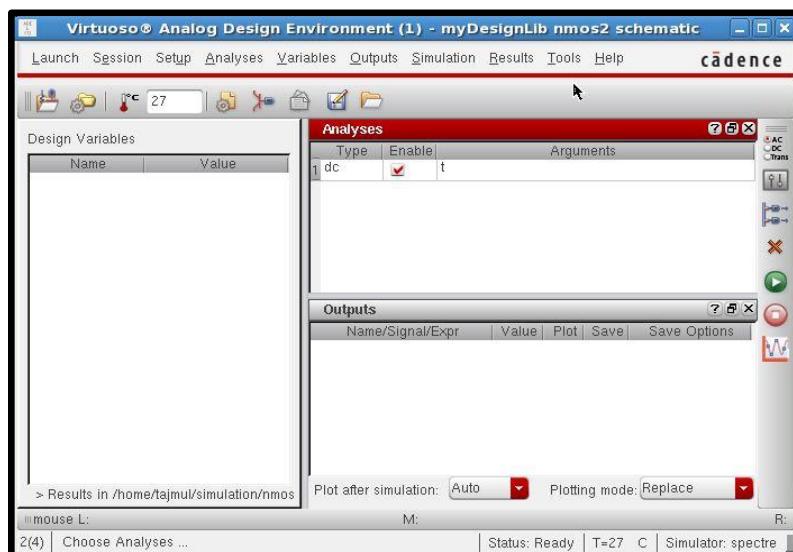


Fig. 03: Virtuoso Analog Design Environment window

II. In the virtuoso analog design environment window click icon  to run the simulation.

III. In the virtuoso analog design environment window click – **Results > Print > DC Operating Points.**

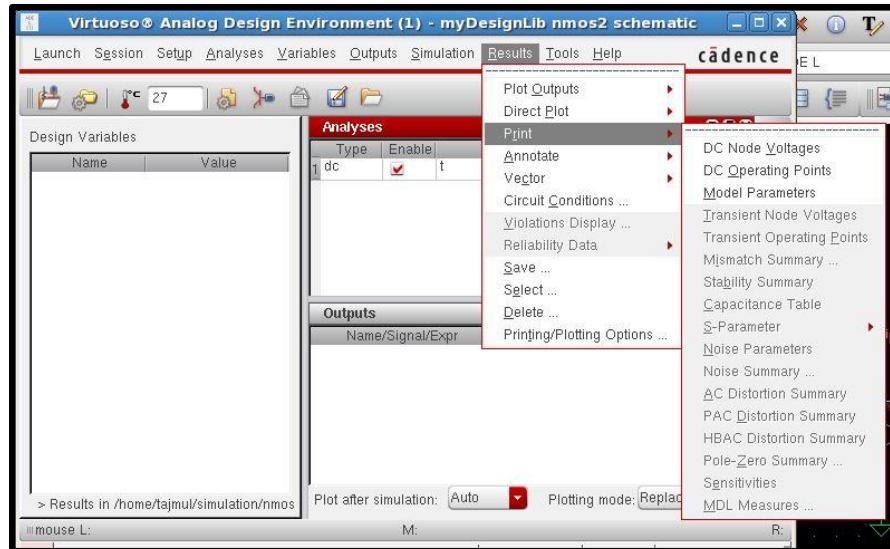


Fig. 04: Virtuoso Analog Design Environment window

IV. A “Result Display Window” is open.

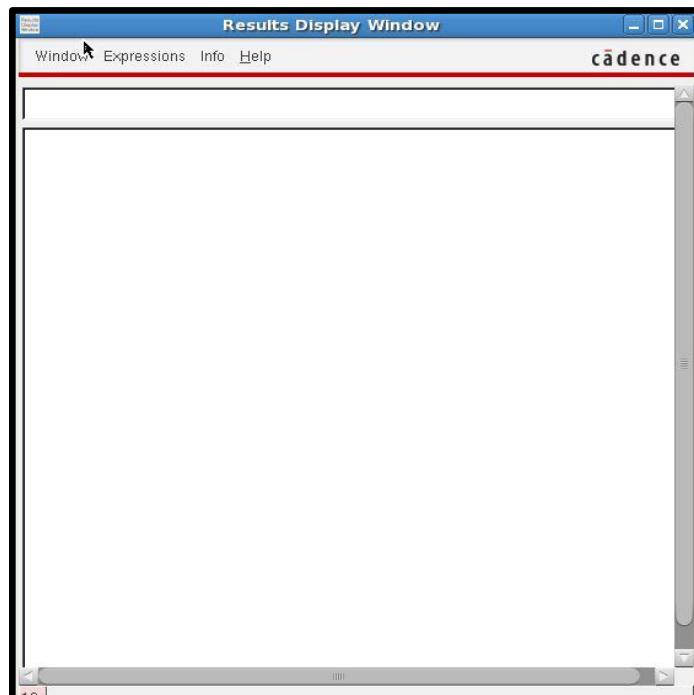


Fig. 05: Results Display Window

V. From the schematic window select the NMOS and in the result display window see the result. Region is 1 that means linear region. You can also see the Id and Vds in the result display window.

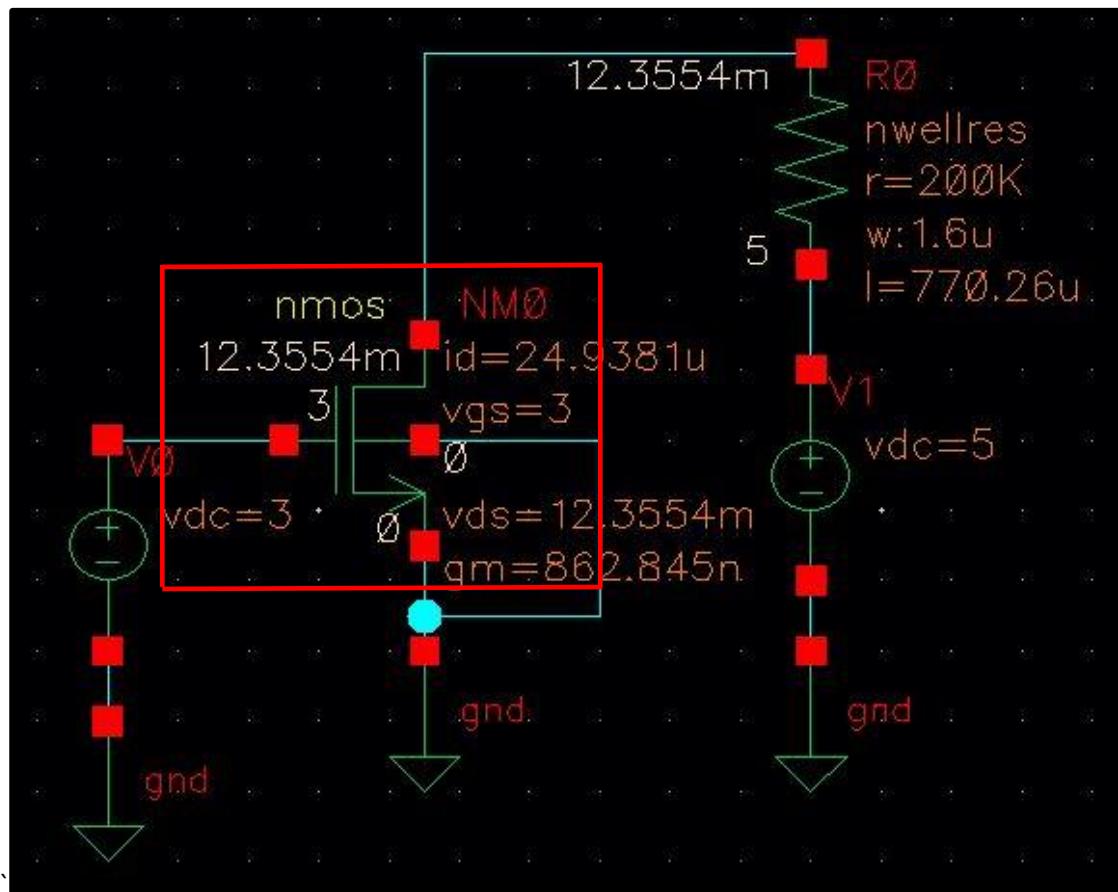


Fig. 06: Select component from the schematic window

Results Display Window	
Window	Expressions
Info	Help
pwr	308.121m
qb	-3.19029f
qbd	-27.9811a
qbi	-3.01729f
qbs	-42.8654z
qd	-8.28691f
mdi	-6.31923f
qg	19.8799f
qqi	15.7634f
qinv	3.82041m
qsi	-6.42688f
qsro	-8.40267f
region	1
reversed	0
ron	495.445
rout	496.985
self_gain	428.822u
type	0
vbs	0
vdb	12.3555m
vds	12.3555m
vdsat	1.26182
vdss	1.26182
vearly	12.3939m
vfbeff	-973.464m
vgb	3
vgd	2.98764
vgs	3
vgsteff	2.49395
vgt	2.49397
vsat_marg	-1.24946
vsb	-0
vth	506.029m

Fig. 07: Component details in the results display window

Lab Summary:

In this lab you learn how to –

- I. Find operating region
- II. Calculate ID, VDS, and estimate the small-signal resistance looking into the drain of the MOSFET.

End of Lab 4

Lab 5: Full custom design of PMOS and NMOS devices.

Objective:

- 4) To open Virtuoso Layout Suite.
- 5) To draw different types of layers.
- 6) To generate layout from schematic.

1. Open Virtuoso Layout Suite:

I. From library manager window select your library here **myDesignLib** and click – **File > new> cell view.**

A window “New file” is open. Here write **cell** name and select **type >layout, Open with > Layout XL.** Click **ok.**

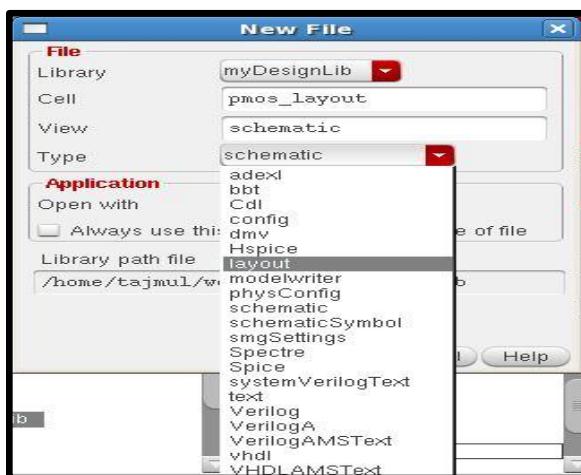


Fig. 01: New file window

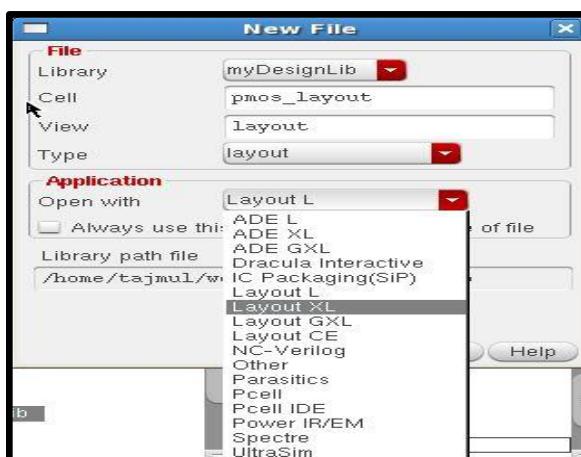


Fig. 02: New file window

II. An “ Update Connectivity Reference” window is open. Click –ok.

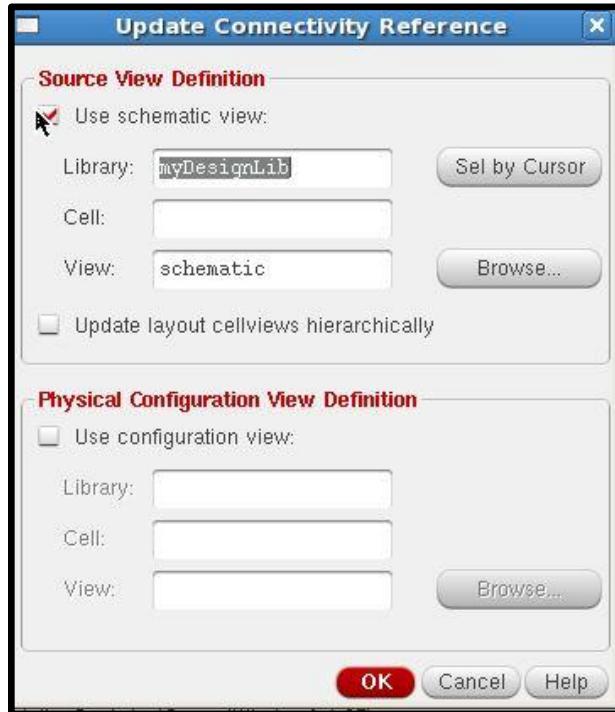


Fig. 03: Update Connectivity Reference

III. A “ Virtuoso Layout Suite XL Editing..” window is open.

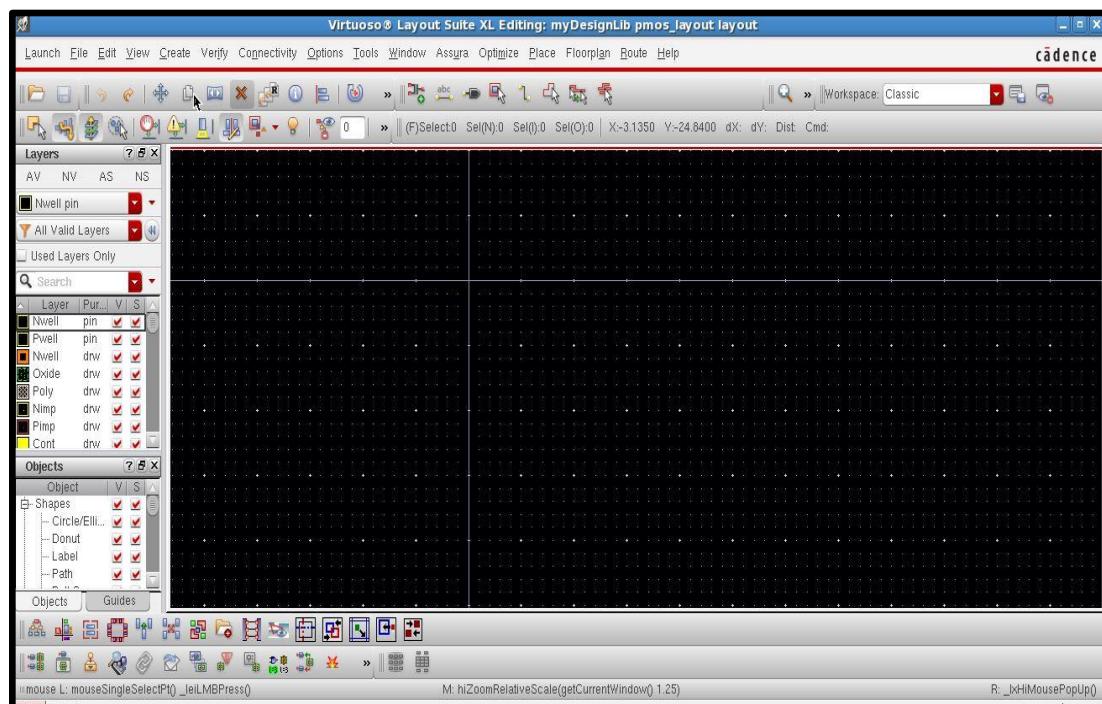


Fig. 04: Virtuoso Layout Suite XL Editing.. window

2. Drawing Different Types of Layers:

I. In the left side of the Virtuoso Layout Suite XL window.. contains different type of metal.

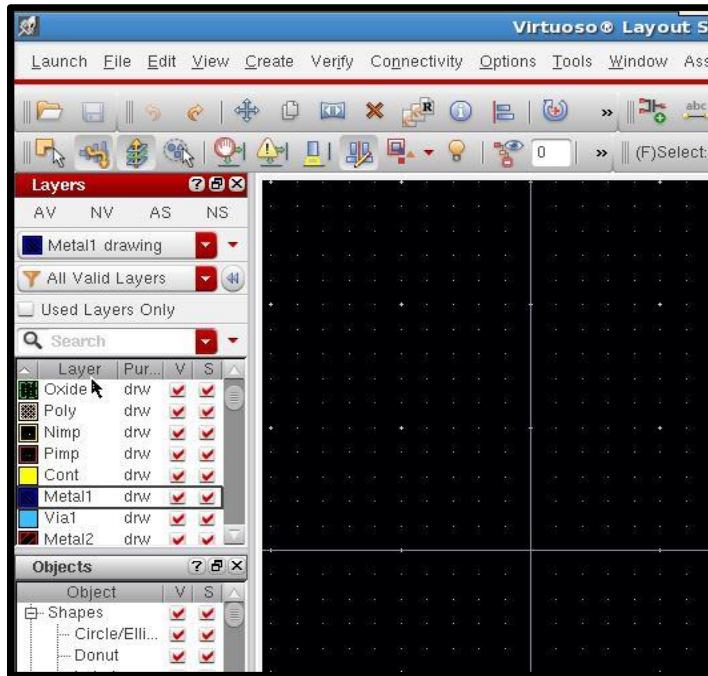


Fig. 05: Different type of metal in Virtuoso Layout Suite XL window

II. To draw a **rectangular layer**, select any one metal. Here, metal 1 is selected. Now click - or **press r** in keyboard. Now you can draw a rectangular layer.

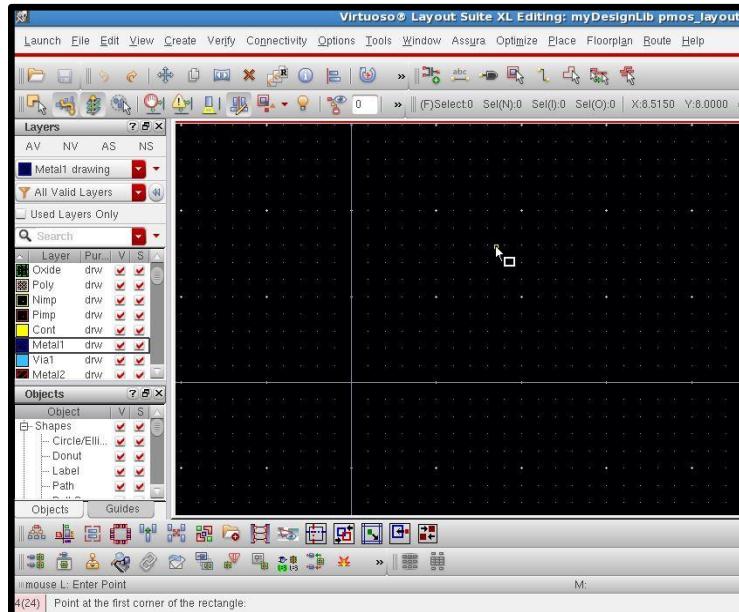


Fig. 06: select metal

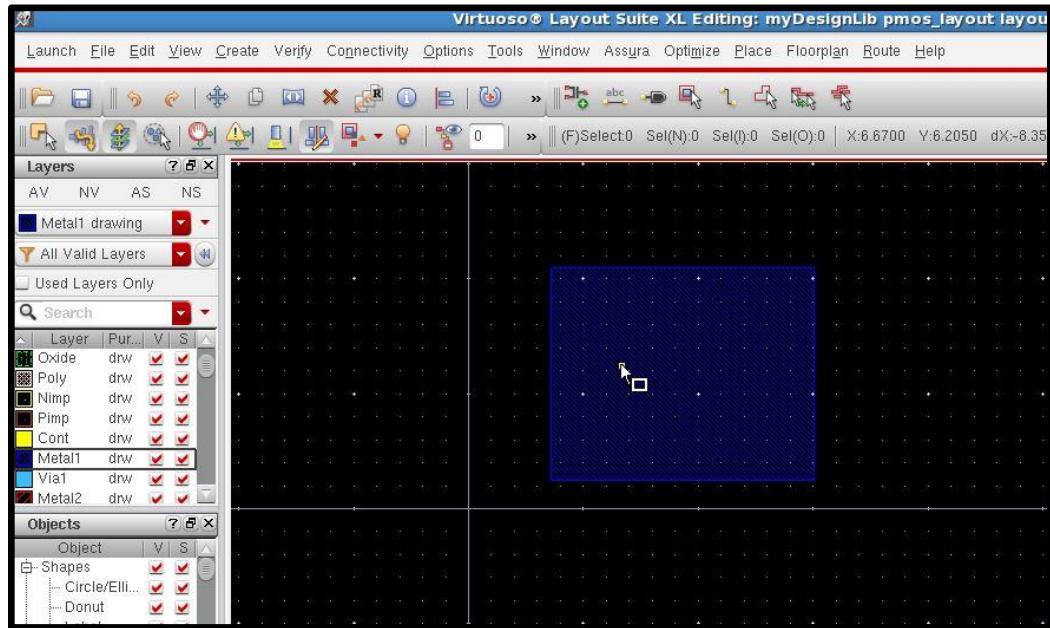


Fig. 07: Drawing rectangular layer



III. To draw a path, select a metal layer. Here metal 1 is selected. Now click - or press **p** in keyboard. At the beginning of the path press one click and at the end just two click.

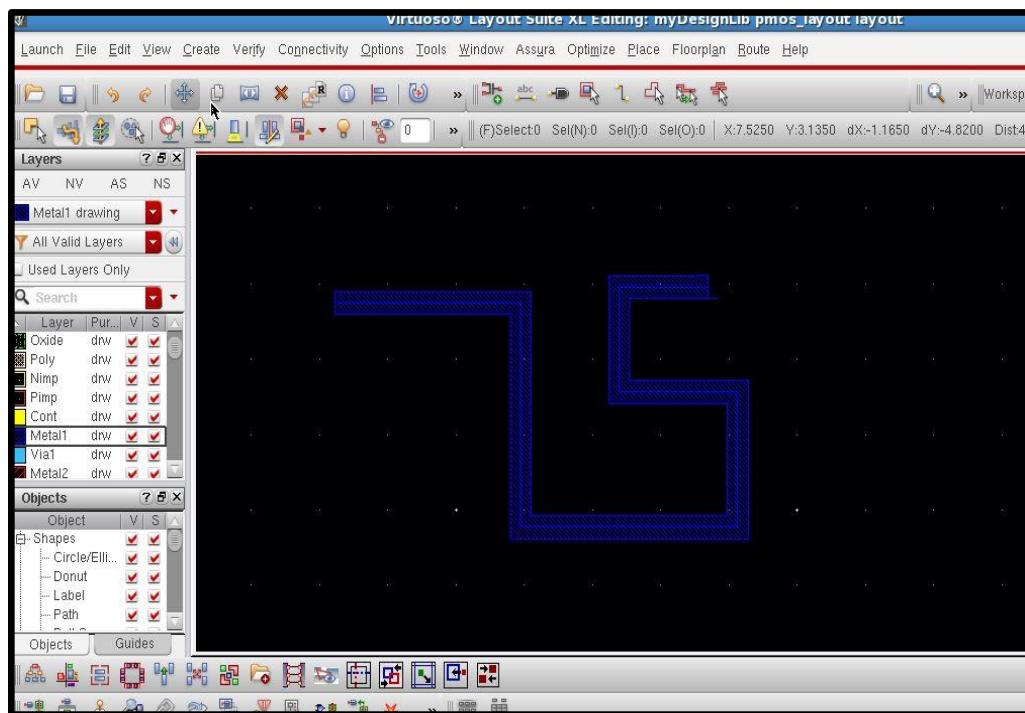


Fig. 08: Drawing a path

3. Drawing Layout of a PMOS:

I. As this black window is a p-substrate so we have to draw an **n-well**. Select n-well from the metal layer and a rectangular layer.

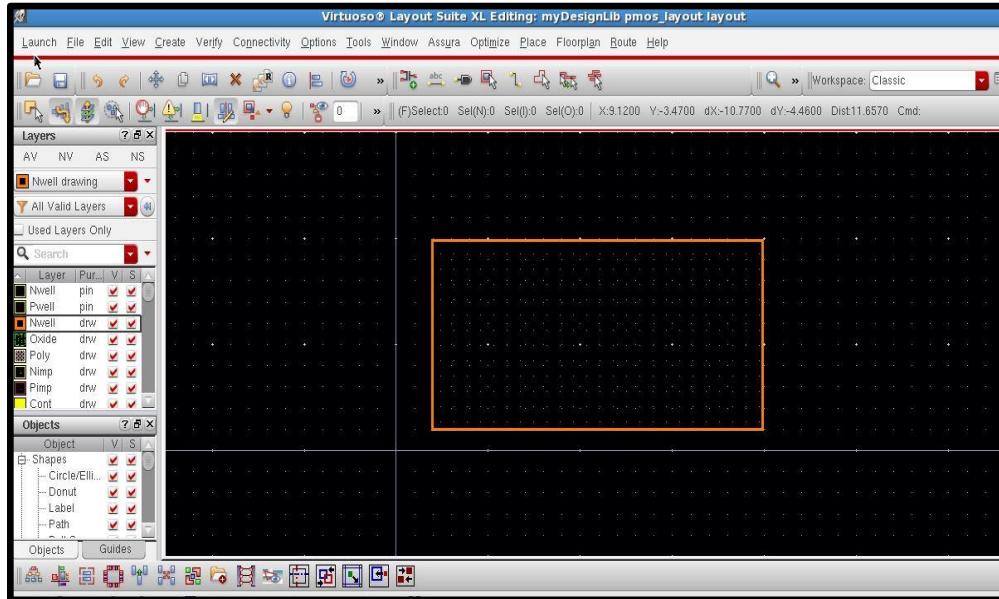


Fig. 09: Drawing n-well layer

II. Now draw two layer **poly** and **pimp**.

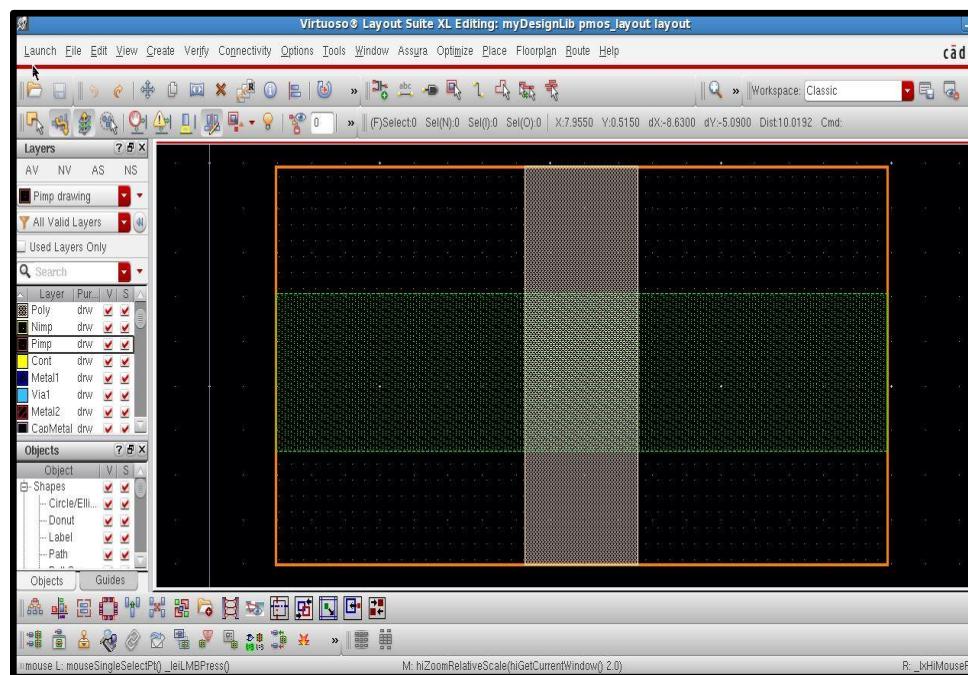


Fig. 10: Drawing poly and pimp

III. Select **cont** from metal layer and draw two contacts on pimp layer.

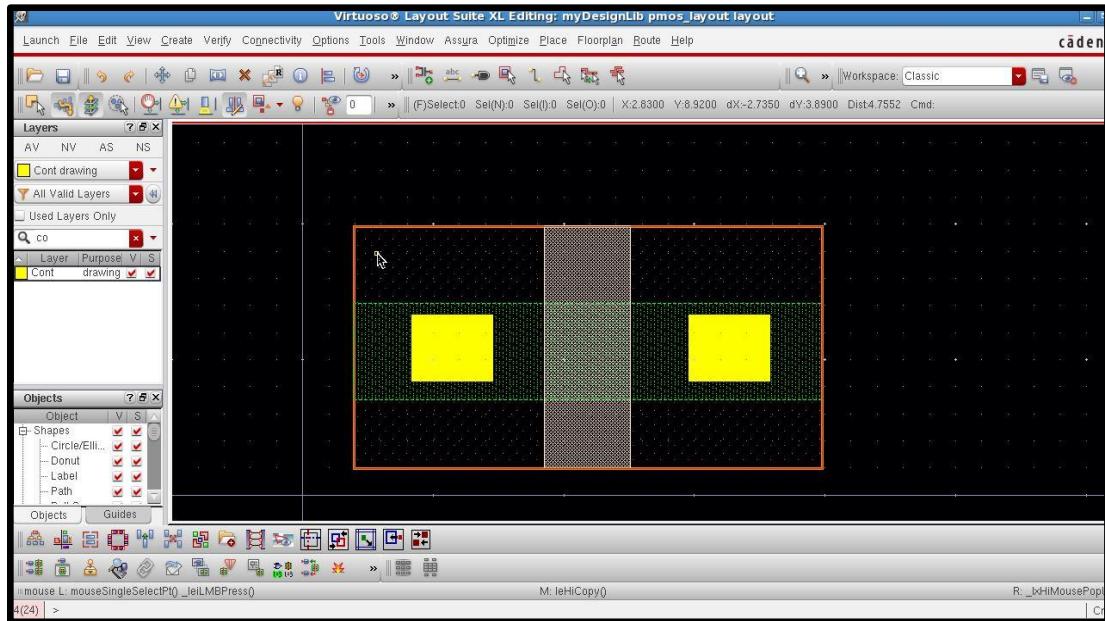


Fig. 11: Drawing contact on pimp layer

IV. Now draw two **metal 1** layer over the two contacts. Finally you get the layout of a PMOS.

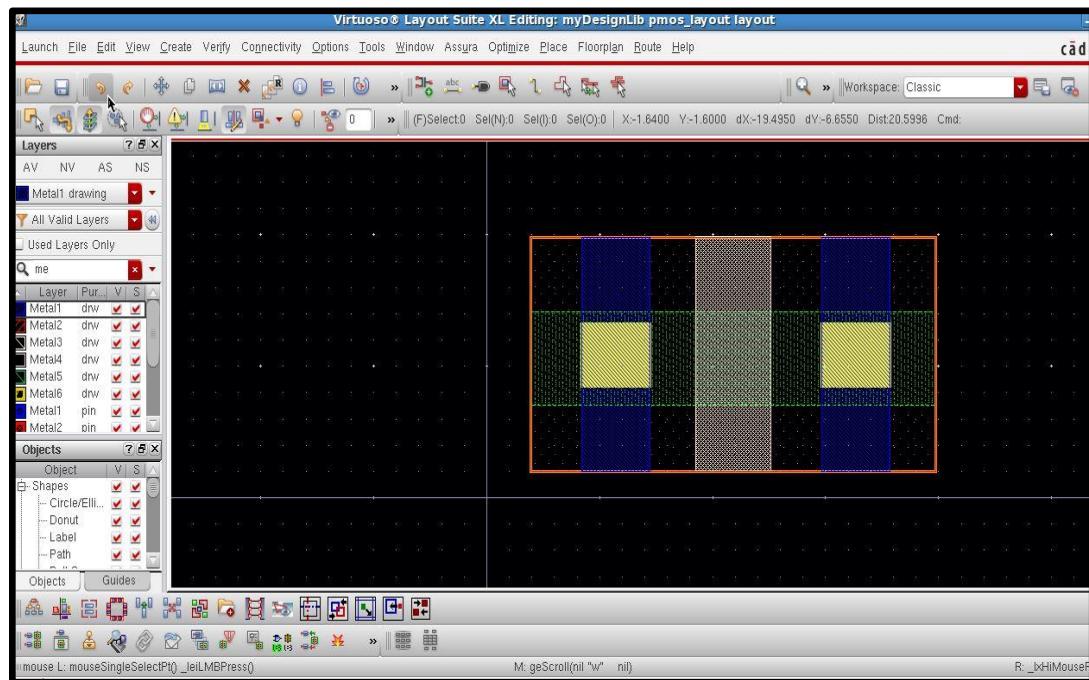


Fig. 12: Layout of PMOS

V. If we zoom in a contact we can see the layer of it.

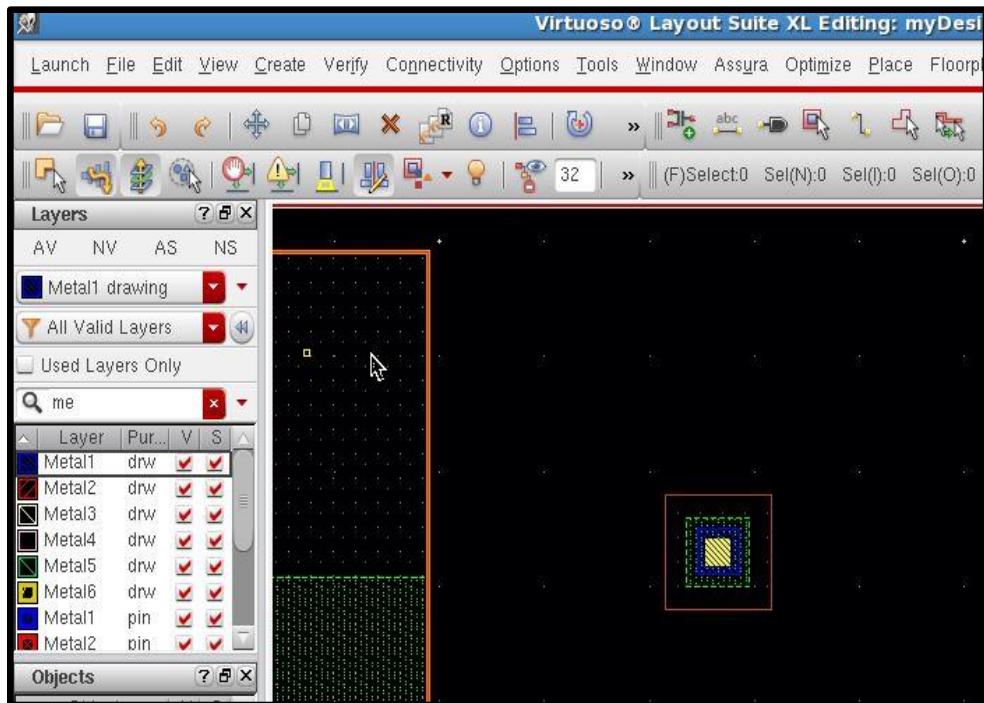


Fig. 13: Different layers of a contact

Lab Summary:

In this lab you learn how to-

- I. Open Virtuoso Layout Suite
- II. Draw different types of layers.
- III. Generate layout from schematic

End of Lab 5

Lab 6: Full custom design of a NAND gate.

Objective:

- 6) To design schematic view.
- 7) To perform DC and Transient and Parametric analysis.
- 8) To find Gain and Bandwidth.
- 9) To generate layout from schematic.
- 10) To check LVS and DRC.

1. Design Schematic View:

In this schematic design, Two NMOS and two PMOS are taken from gpdk180 library. Two input pin a, b and one output pin y are used. The schematic diagram of an NAND gate is given below-

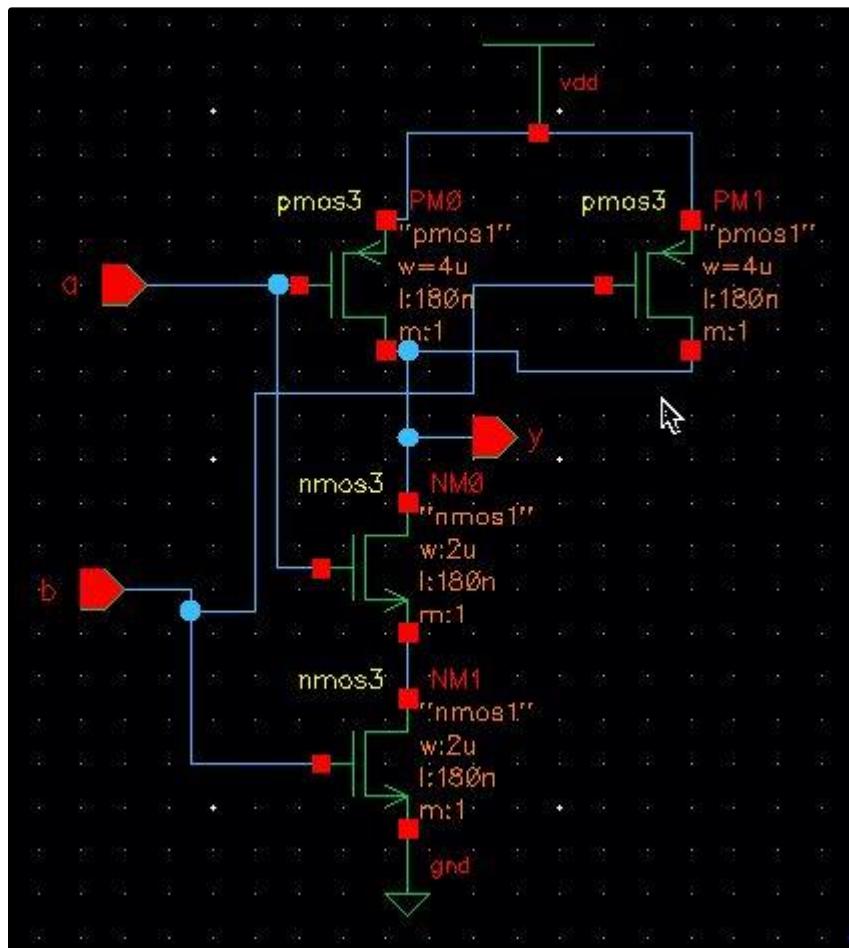


Fig. 01: Schematic diagram of an NAND gate

2. DC and Transient and Parametric Analysis:

A. DC and Transient Analysis:

I. For the DC and transient analysis two vpulse are connected in a and b. A vdc is connected in vdd.

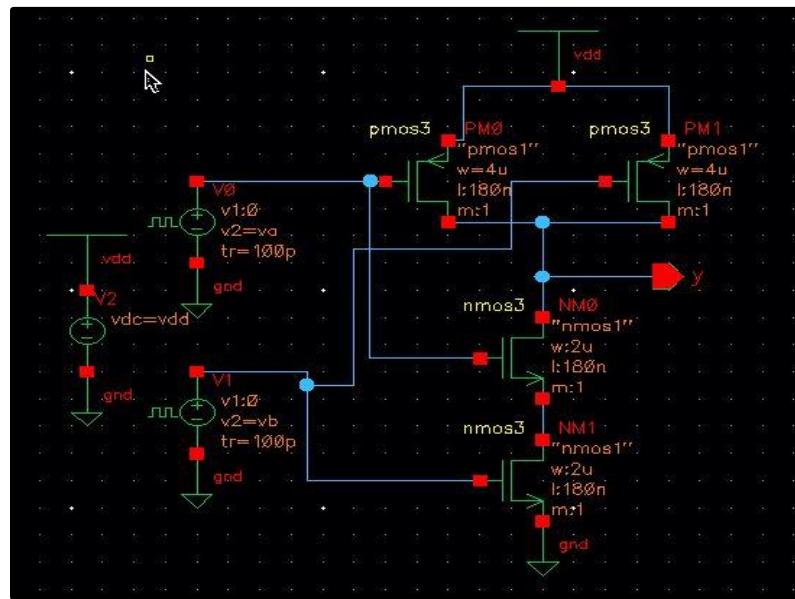


Fig. 02: Schematic diagram for dc and transient analysis

II. Check and Save the schematic.

III. From the schematic diagram click – **launch > ADE L**. A “ **Virtuoso Analog Design Environment**” window is open.

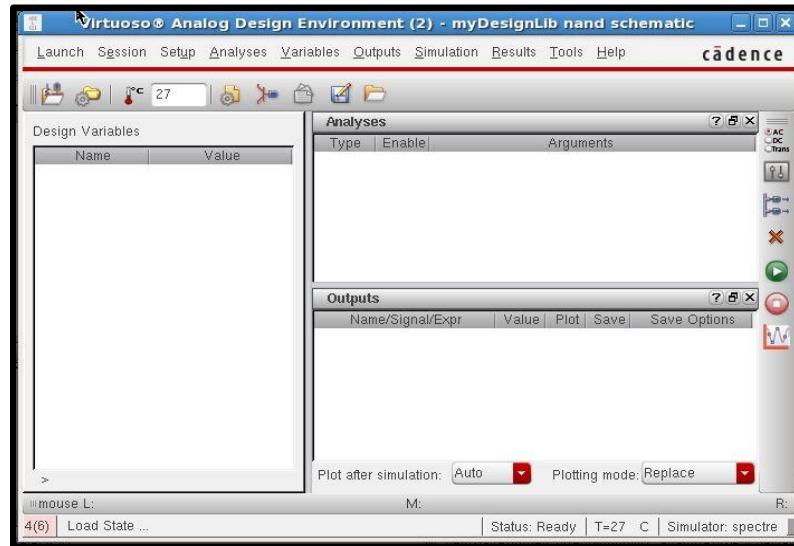


Fig. 03: Virtuoso Analog Design environment window

IV. In this window click – **Analyses > Choose** or just click on icon . A “Choosing Analyses..” window is open.

In this window select **dc, Save DC Operating Point, Component Parameter**.

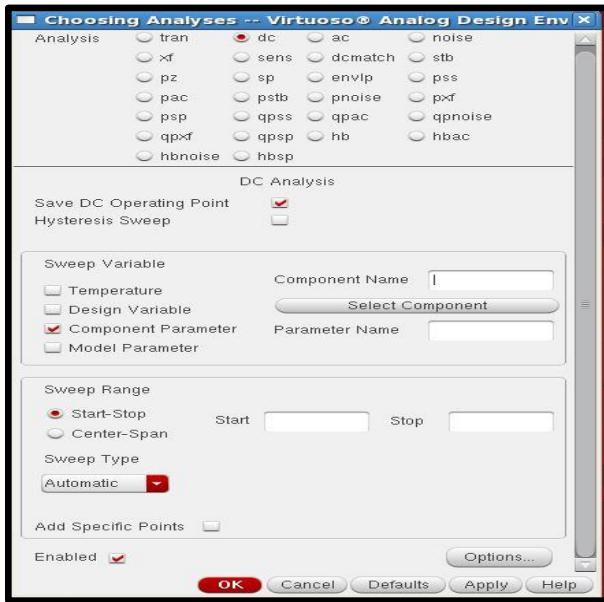


Fig. 04: Choosing Analysis.. window

V. In the choosing analyses window Click – **Select component**. From the schematic window select the **varying source V0**. A “select component parameter” window is open. In this window select – **DC Voltage** and click – **ok**.

In the choosing analyses window write the sweep range – **Start = 0, Stop = 2**.

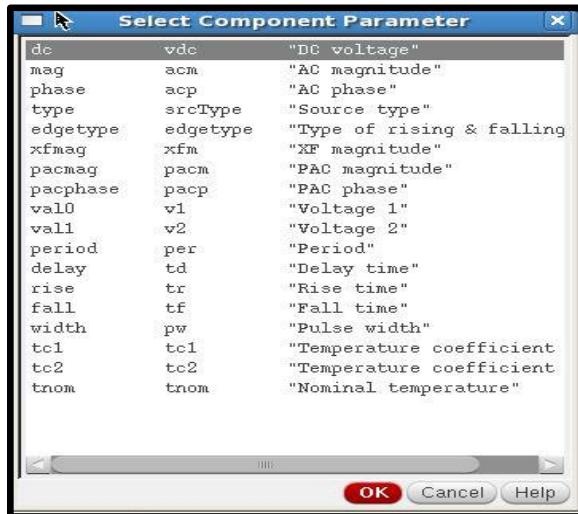


Fig. 05: Select Component Parameter window

VI. For transient analyses click in virtuoso analog design environment window. Then the “Choosing Analysis..” window is open. For transient analysis select **tran**. **Stop time = 200ns**. Select **moderate**. Click – **ok**.

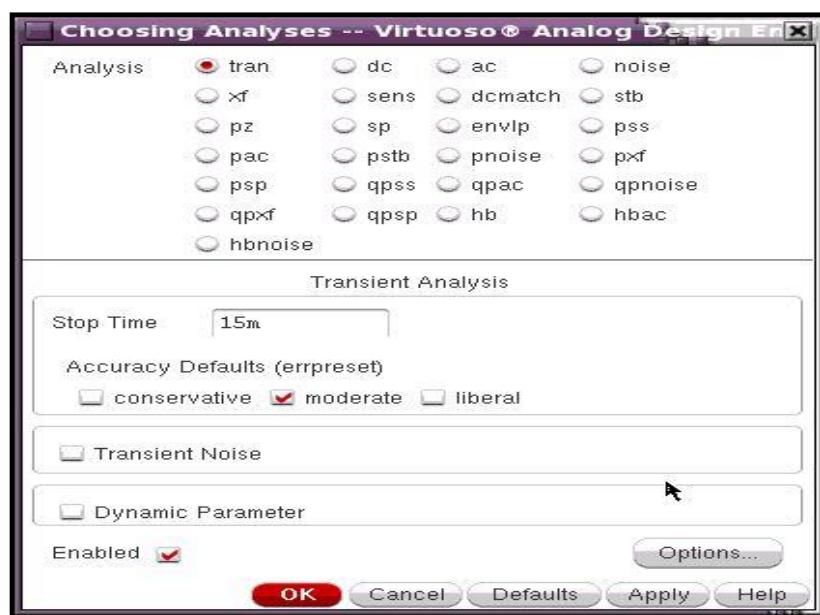


Fig. 06: Choosing Analyses window

VII. Two analyses type transient and dc are saved in the virtuoso analog design environment window.

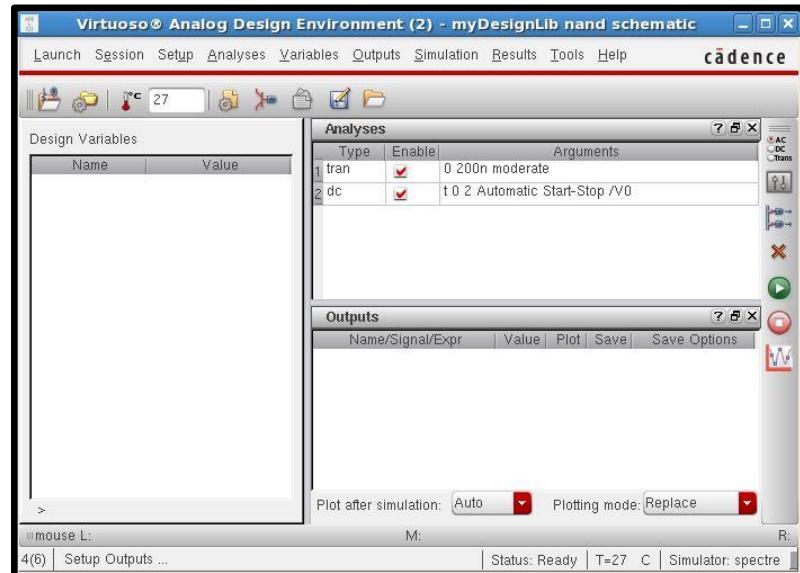


Fig. 07: Analyses types are saved in virtuoso analog design environment window

VIII. In the virtuoso analog design environment window click – **Outputs > Setup** or just click on  icon. A “**Setting Outputs..**” window is open

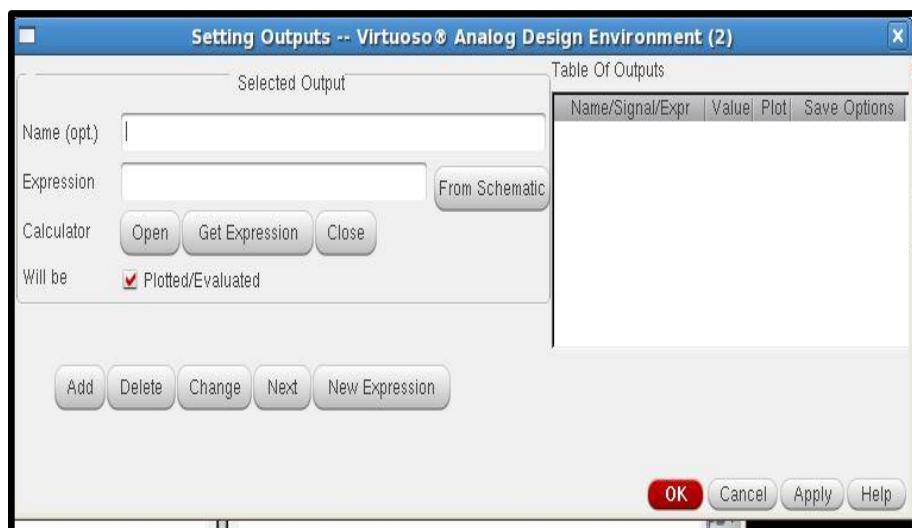


Fig. 08: Setting Outputs.. window

IX. Press 1, “**Add Wire Name**” window is open. In this window write the wire name and click – **Hide**. Do this for three wires **a**, **b** and **y**.



Fig. 09: Add wire name window

X. In the setting output window three wires are saved.

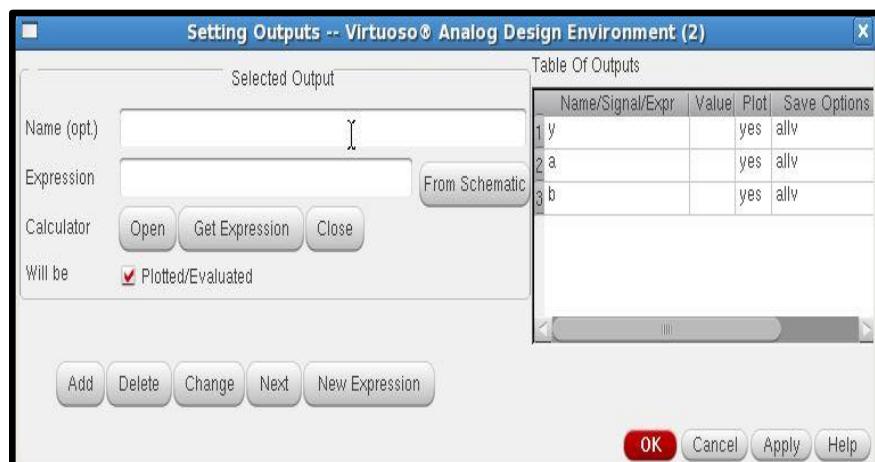


Fig. 10: Setting outputs .. window

XI. In the virtuoso Analog Design Environment window selected wires are saved.

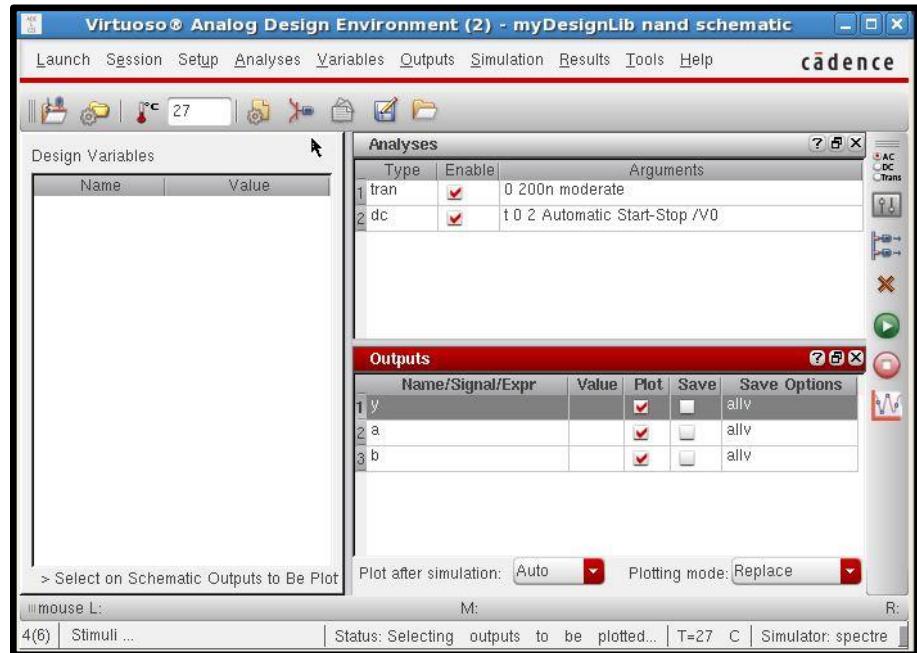


Fig. 11: Virtuoso Analog Design Environment window

XII. From the virtuoso analog design environment window click - . An “Editing Design Variables..” window is open.

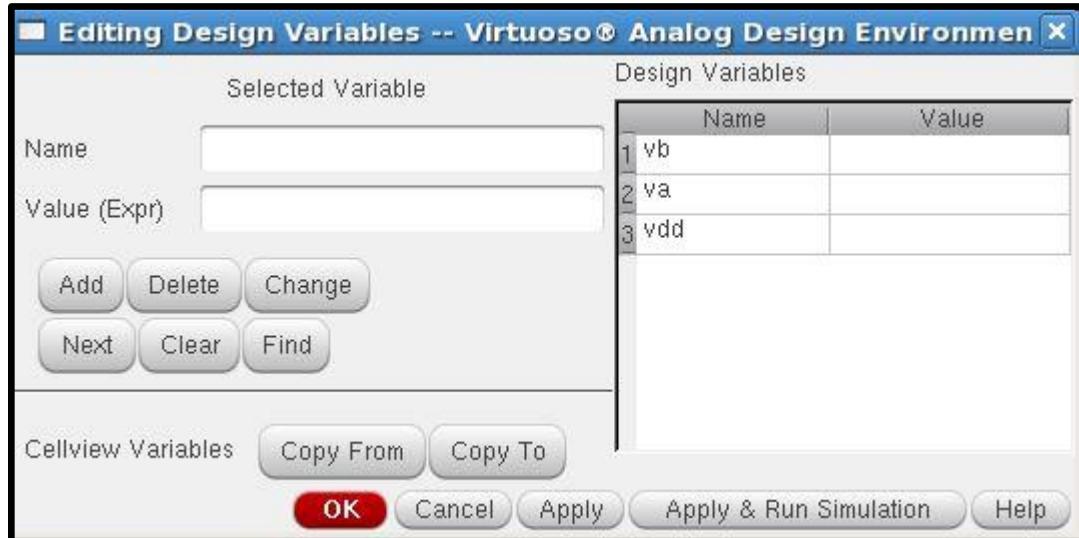


Fig. 12: Editing Design Variables.. window

XIII. In this window select **design variable** and write the value(Expr). Do this for vb, va and vdd.

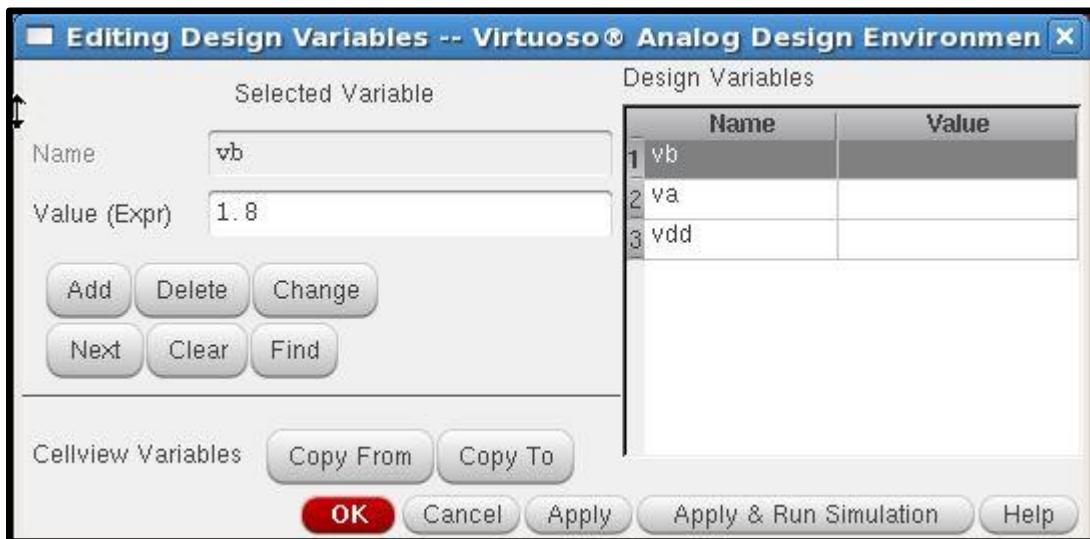


Fig. 13: select the design variables

XIV. Now see in the virtuoso analog design environment window design variables are saved.

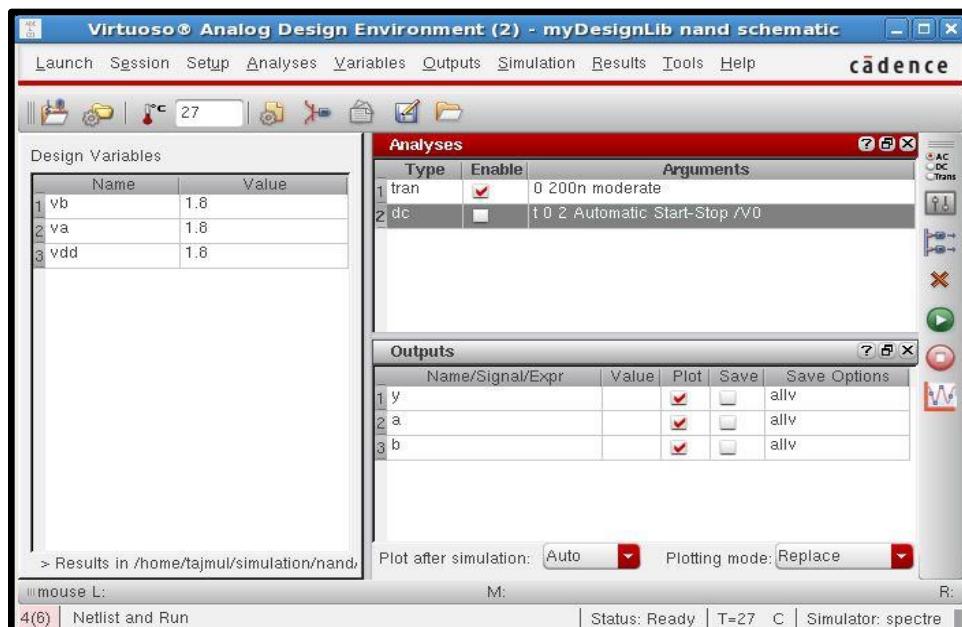


Fig. 14: Virtuoso analog design environment window

XV. Now run the simulation.

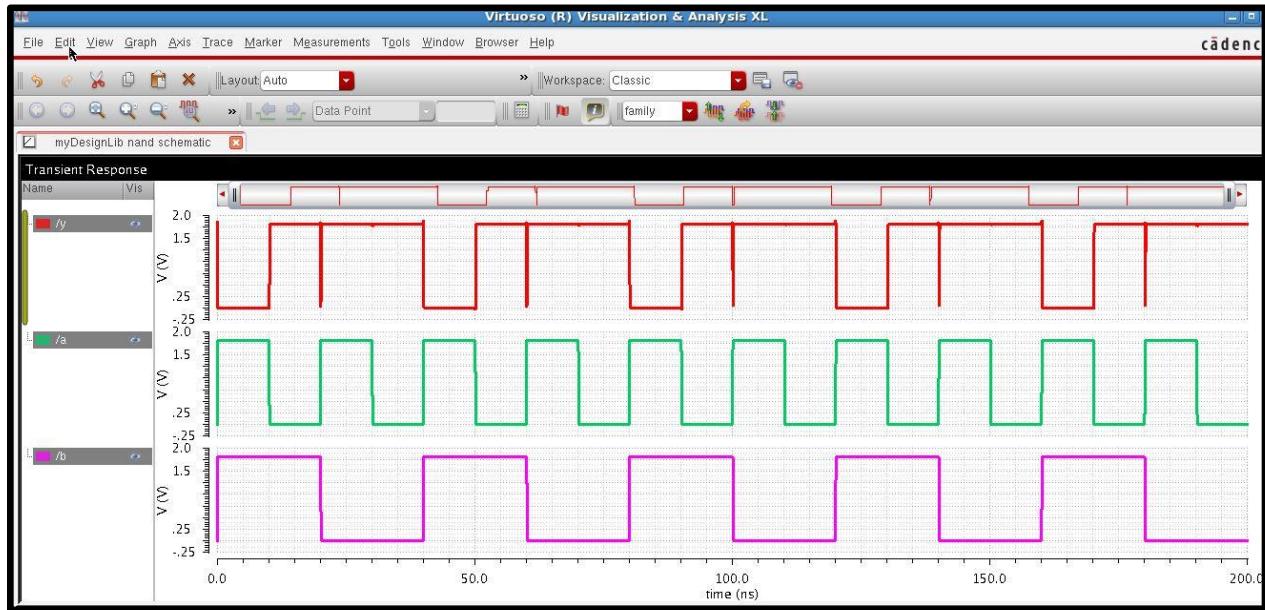


Fig. 15: Transient analyses

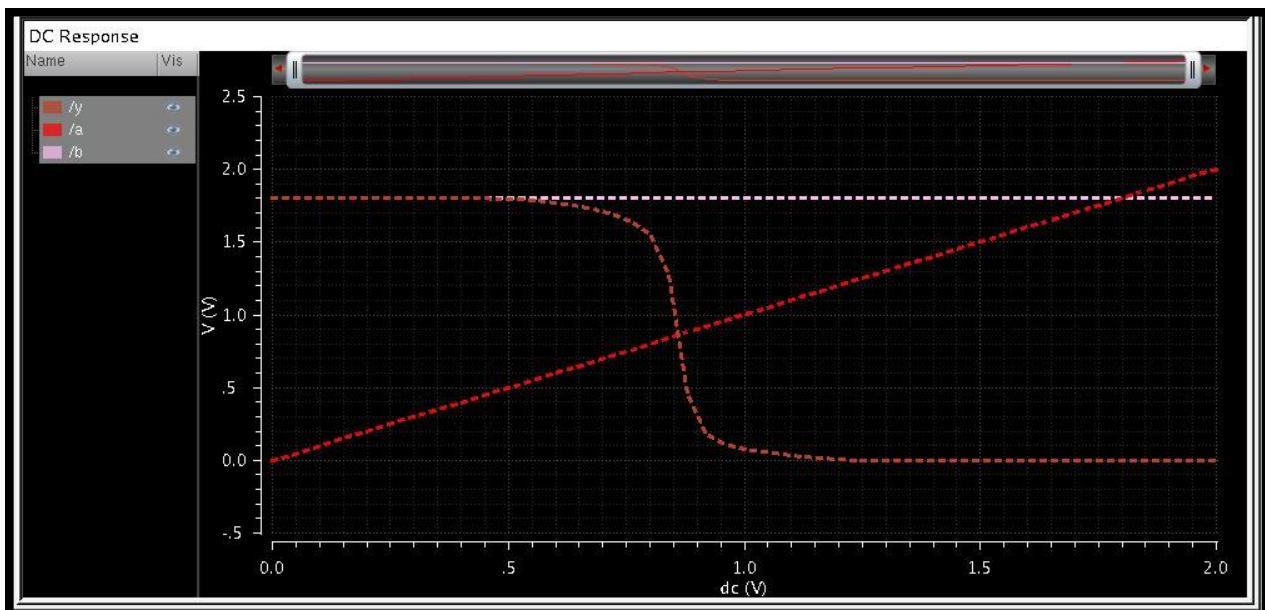


Fig. 16: DC analyses

B. Parametric Analysis:

- From the Virtuoso Analog Design Environment window click – Tools > Parametric Analysis.

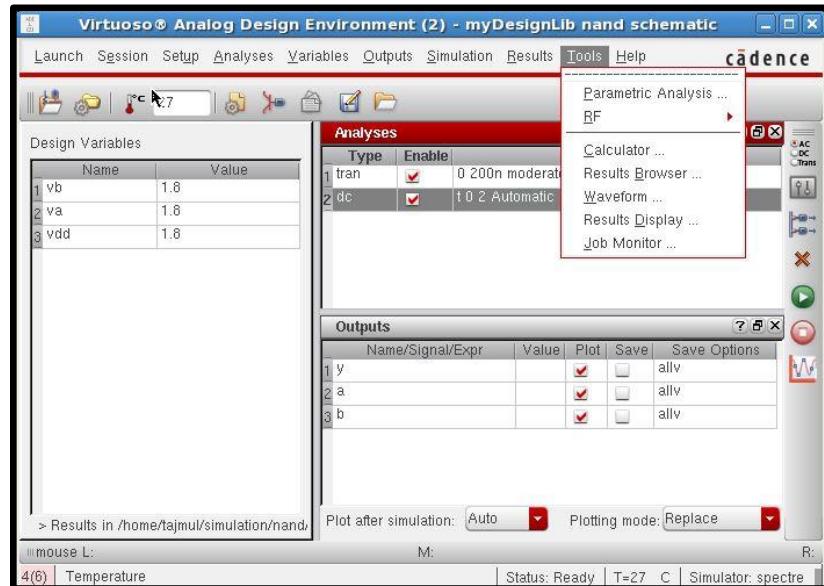


Fig. 17: Virtuoso Analog Design Environment window

II. A “Parametric Analysis..” window is open.

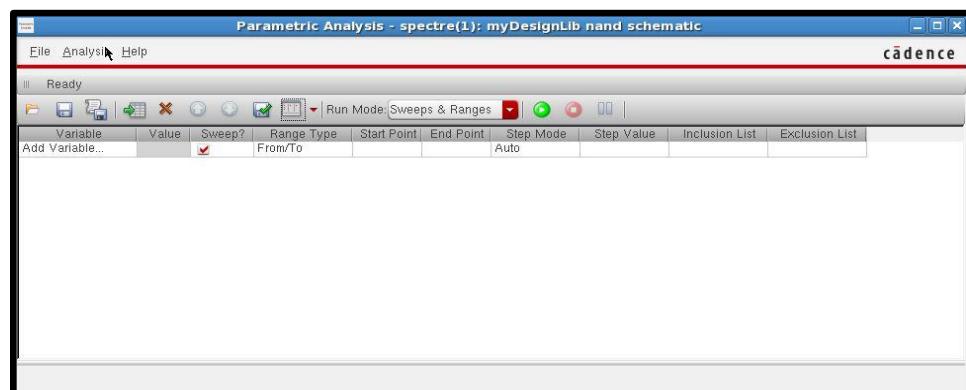


Fig. 18: Parametric Analysis window

III. In this window select - Variable. Write Value, Start Point, End Point and Step Value.



Fig. 19: Parametric Analysis window

IV. Click -  and see the parametric analysis.

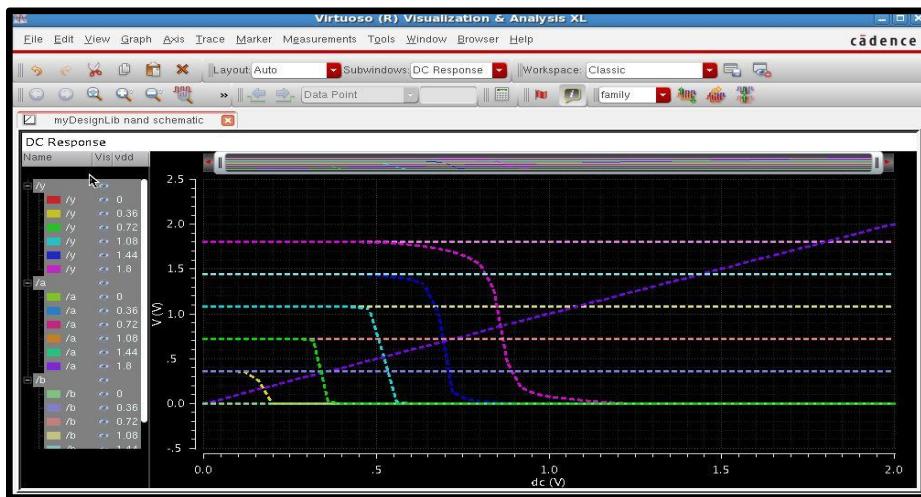


Fig. 20: Parametric analysis

3. Gain and Bandwidth:

A. Gain:

- I. In the virtuoso analog design environment window click – **Analyses > Choose** or just click on icon . A “Choosing Analyses..” window is open. In this widow select – **ac**, write the Sweep Range: **Start = 0** and **Stop = 1G**.

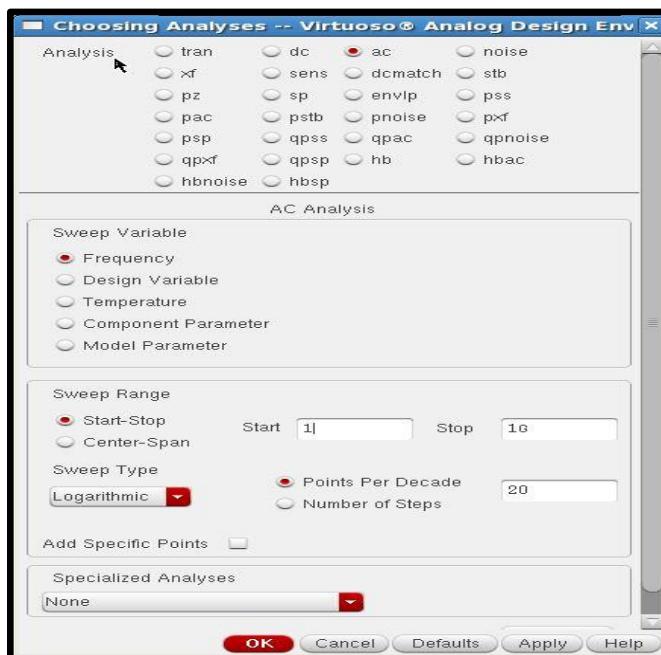


Fig. 21: Choosing Analyses window for ac analysis

- II. Now from the virtuoso analog design environment window **run** the simulation.

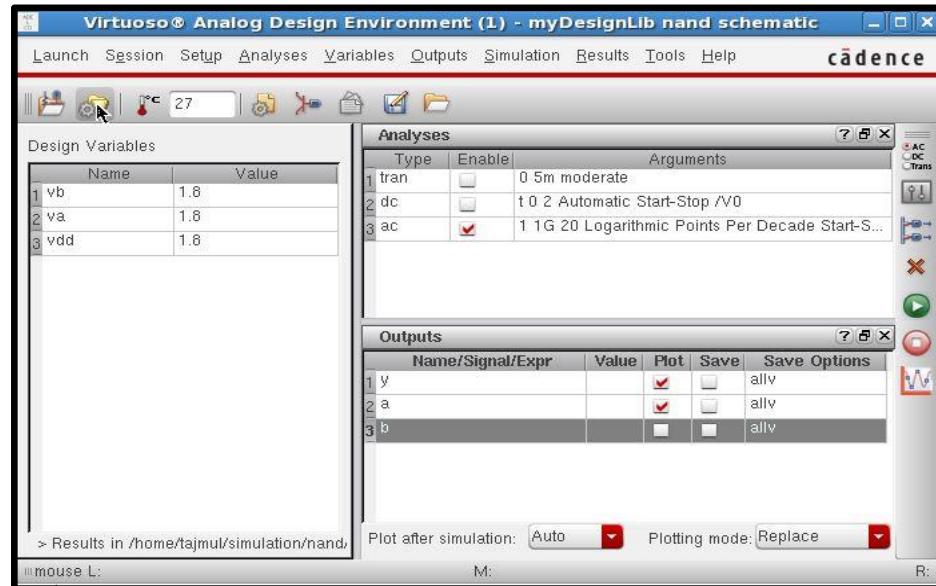


Fig. 22: Run simulation from virtuoso analog design environment window

III. Now from virtuoso analog design environment window click – **Results>Direct Plot> AC dB20.**

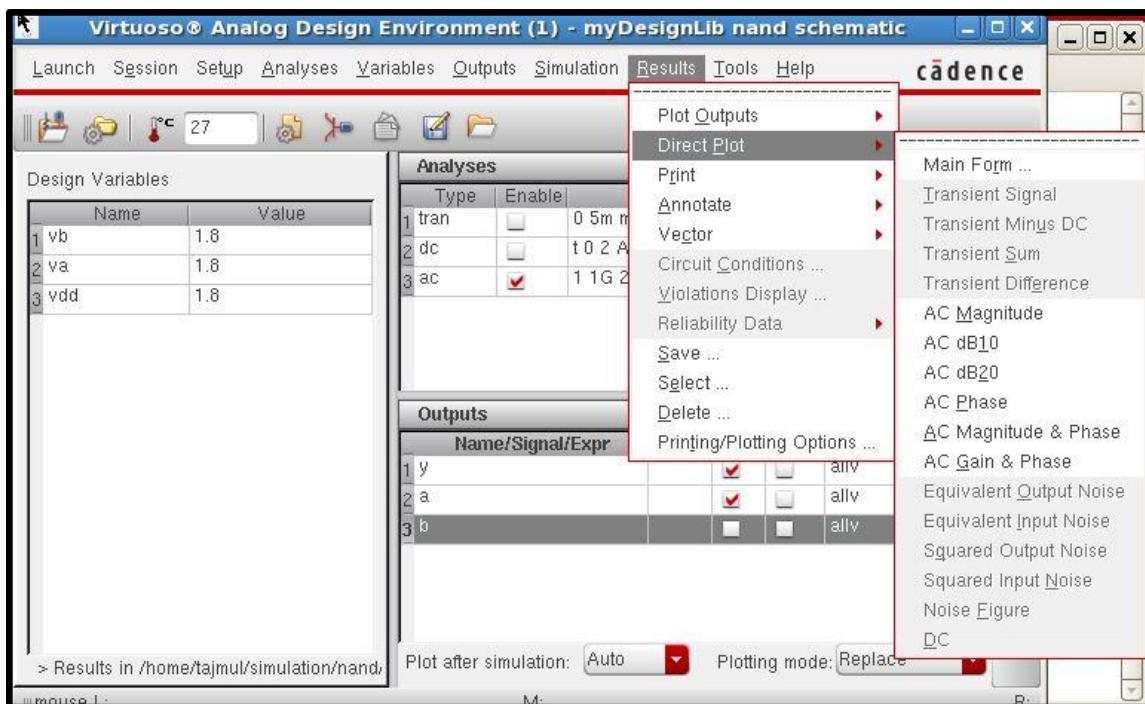


Fig. 23: Virtuoso analog design environment window

IV. Now from the schematic diagram select wire y.

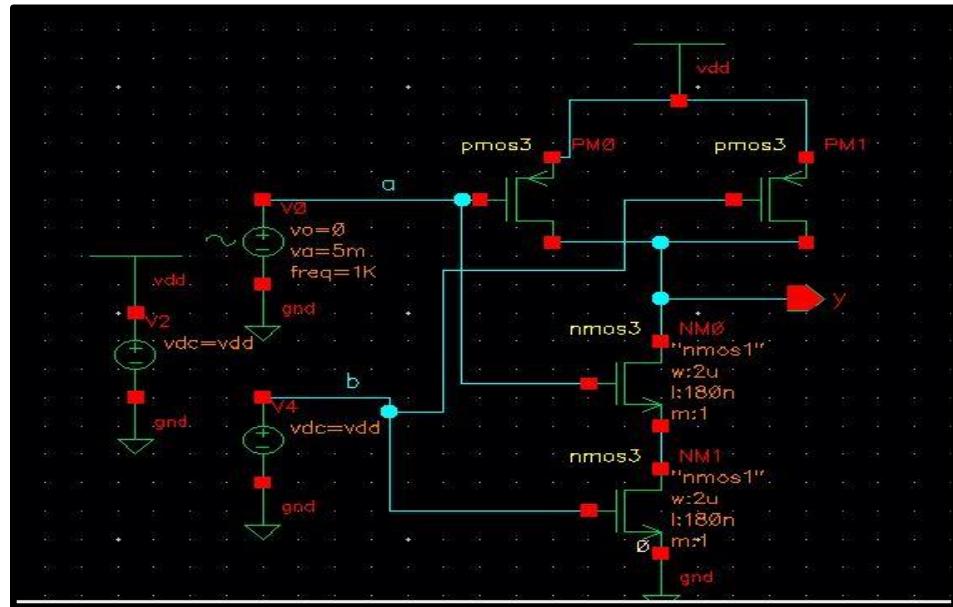


Fig. 24: Select wire y from the schematic

V. Now see the waveform of gain.

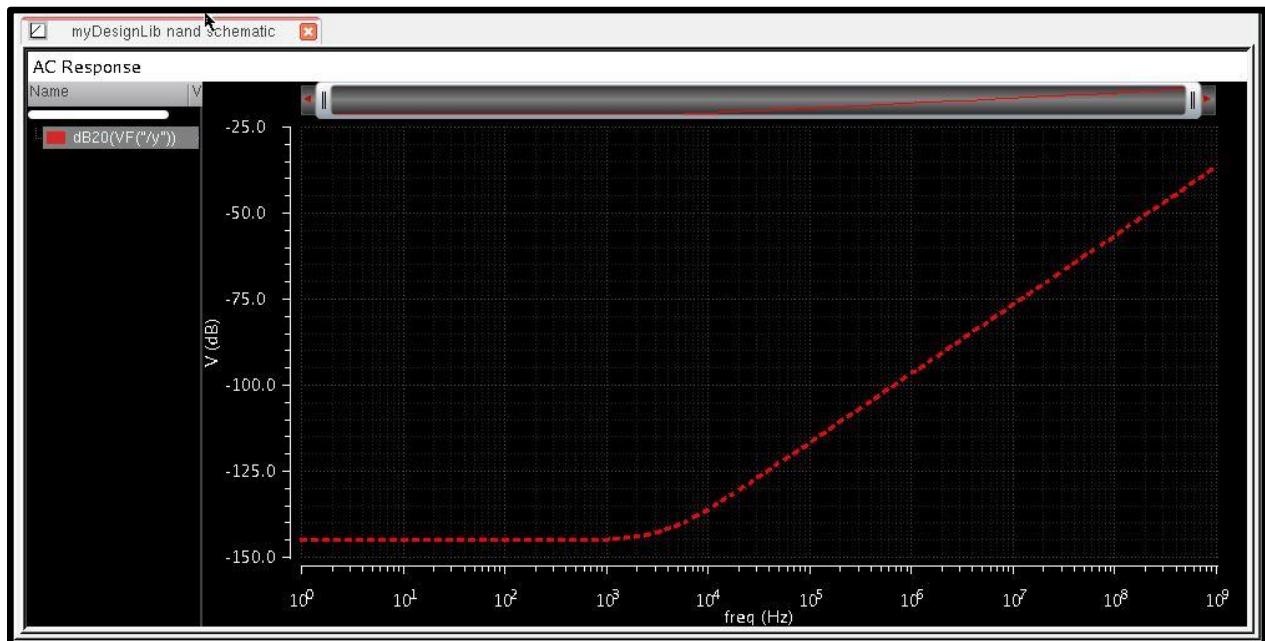


Fig. 25: Gain of NAND gate

B. Bandwidth:

- I. From the Virtuoso Visualization & Analysis XL window click - for calculator. A “**Virtuoso Visualization & Analysis XL calculator**” window is open.

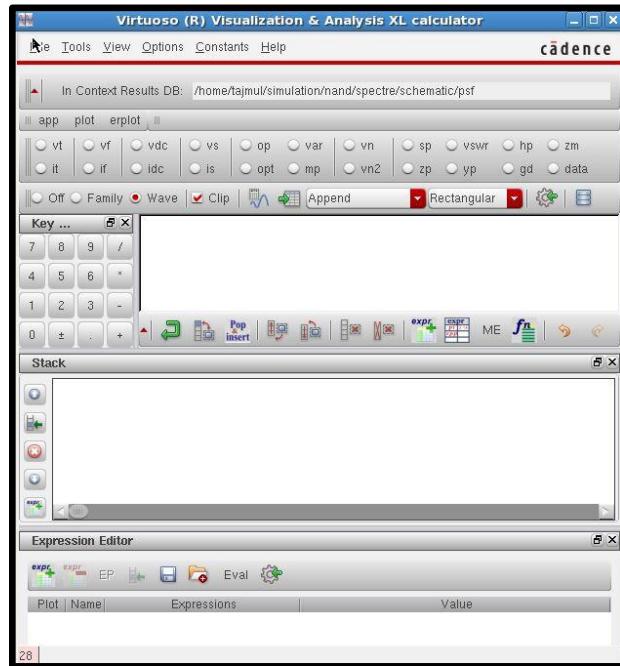


Fig. 26: Virtuoso Visualization & Analysis XL calculator window

II. Select the waveform of gain. Then find out the bandwidth of the signal.

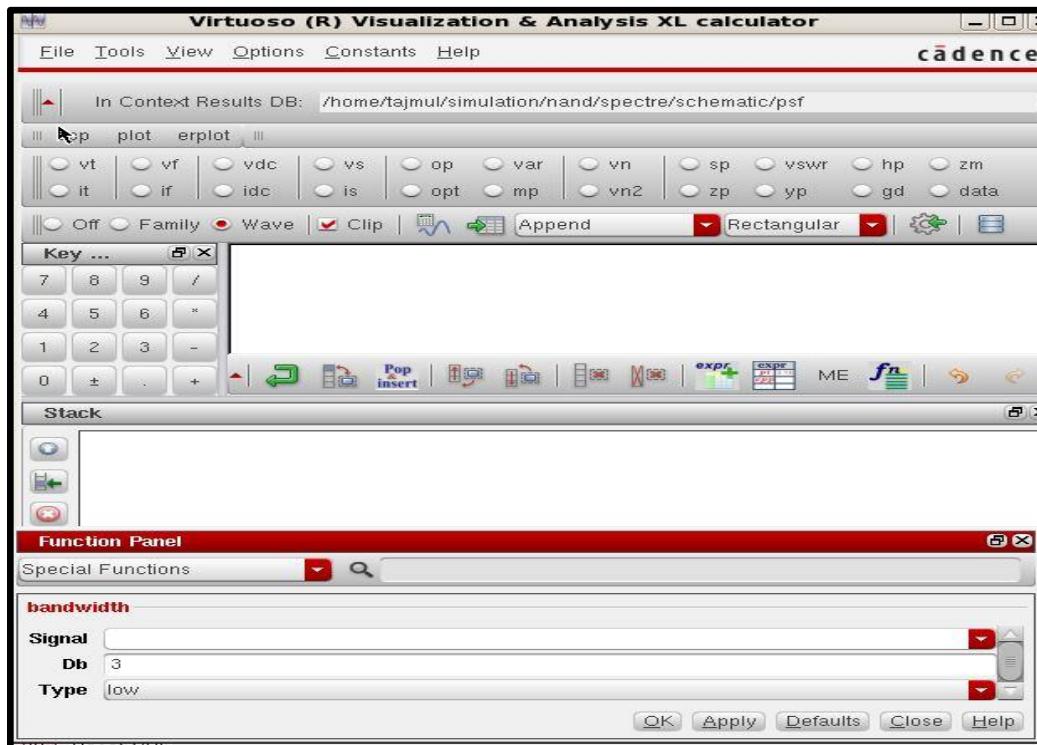


Fig. 27: Function panel

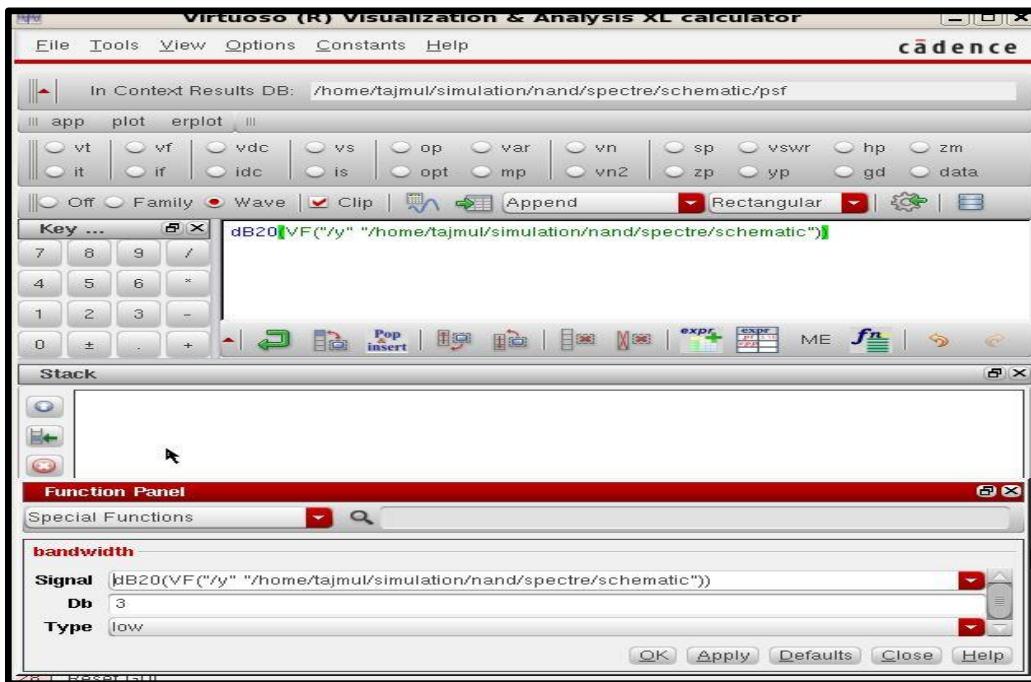


Fig. 28: select the signal of gain

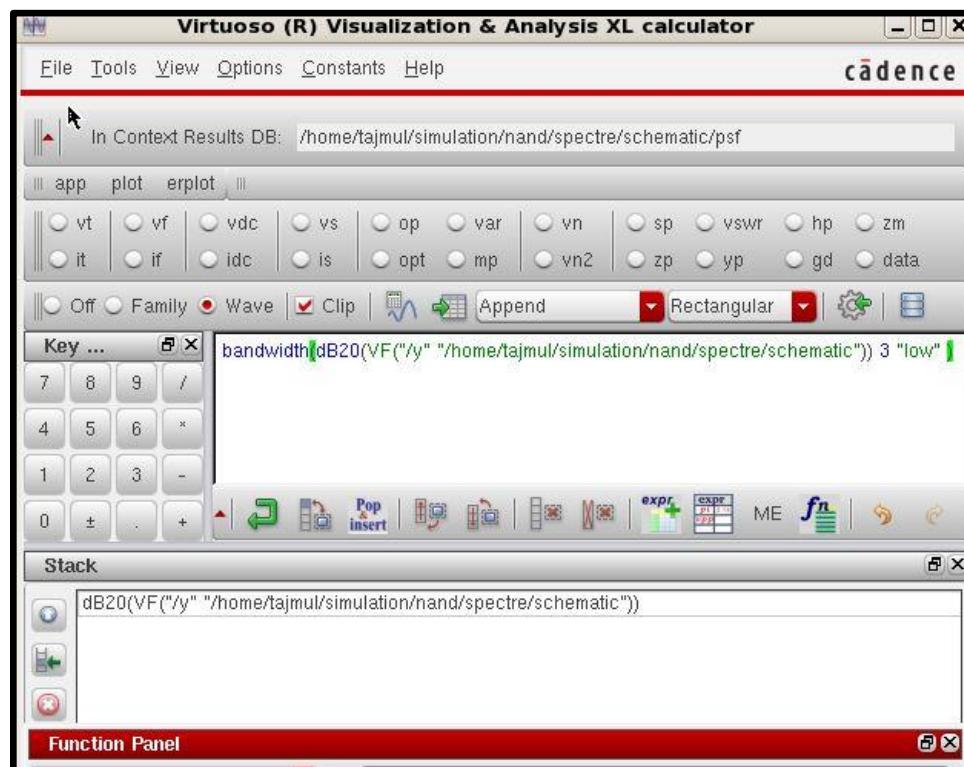


Fig. 29: bandwidth of gain signal

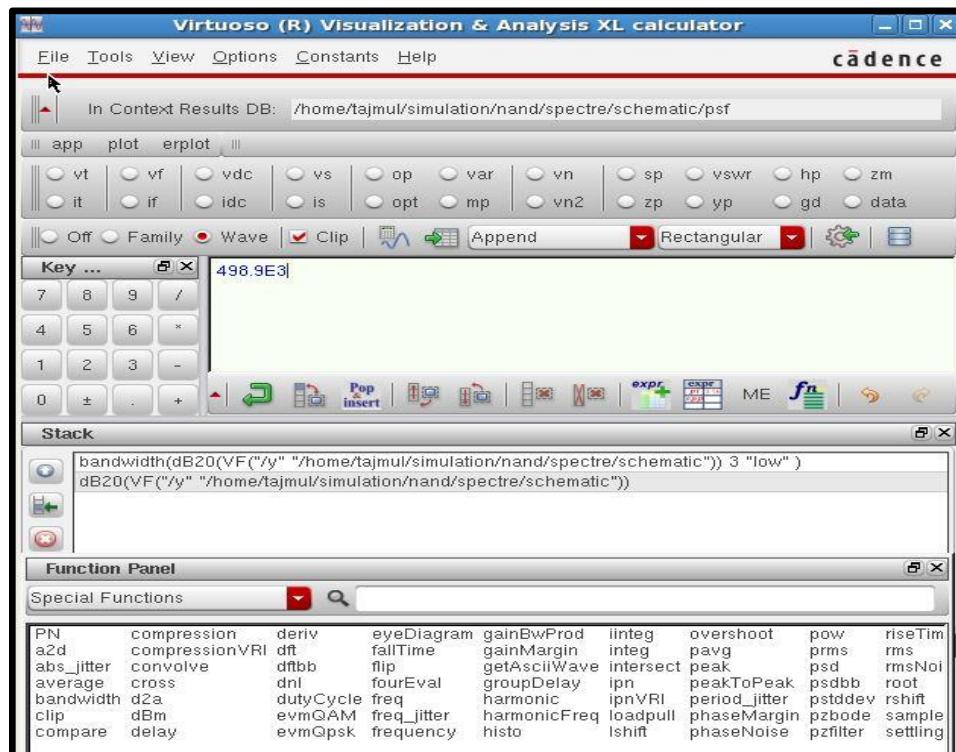


Fig. 30: result of bandwidth

4. Generate Layout from Schematic:

- I. The schematic diagram for layout is given below. It should not contain any source.

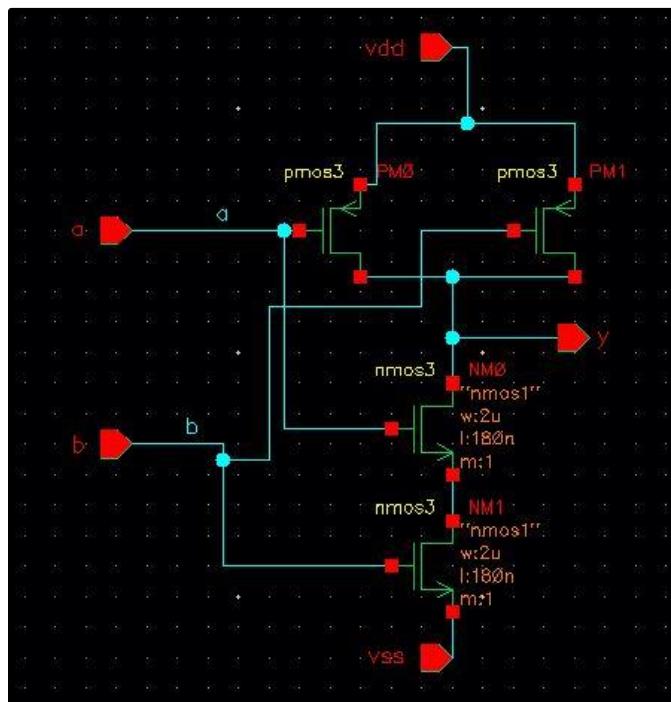


Fig. 31: Schematic diagram for layout

II. From the schematic window click – **Launch > Layout XL.**

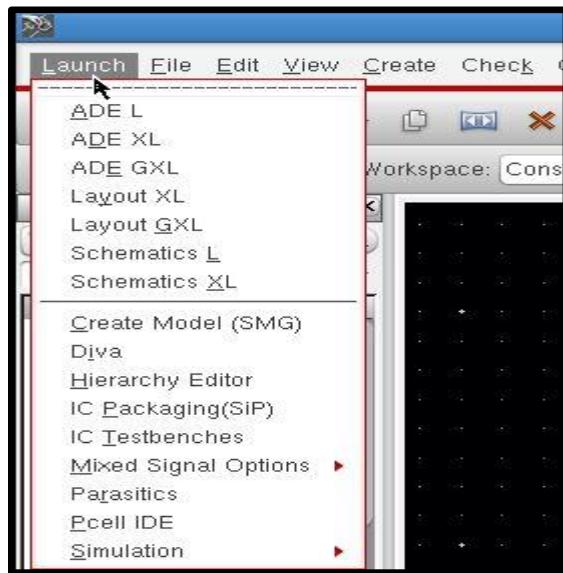


Fig. 32: Schematic window

III. A “Startup Option” window is open. Select – **Create New** and **Automatic**. Click – **ok**.



Fig. 33: Startup Option window

IV. A “Virtuoso Layout Suite XL Editing..” window is open.

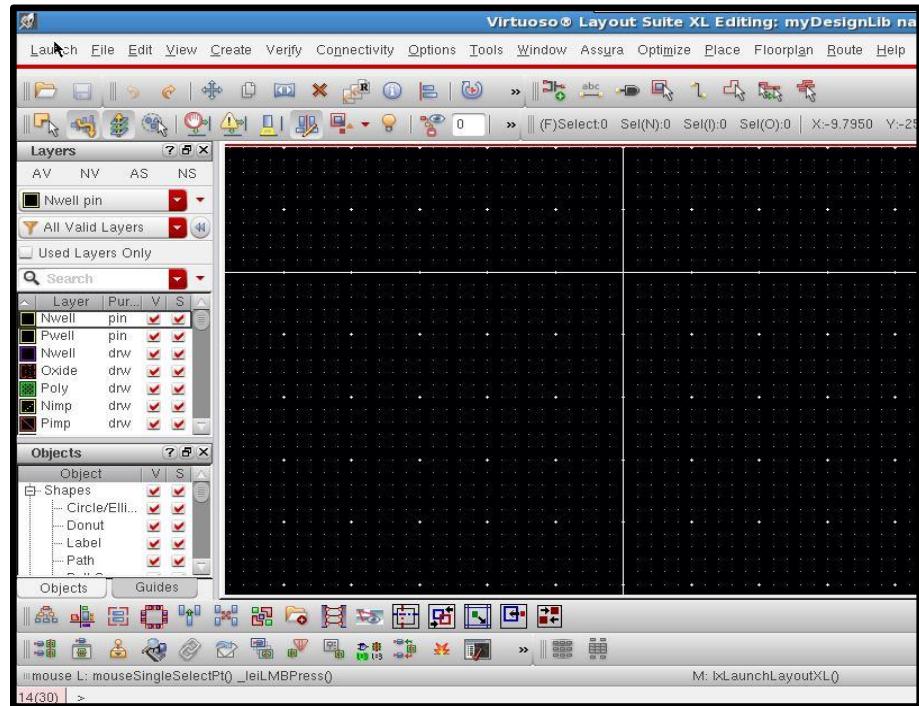


Fig. 34: Virtuoso Layout Suite XL Editing widow

V. From this window Click – Connectivity > Generate > All From Source.

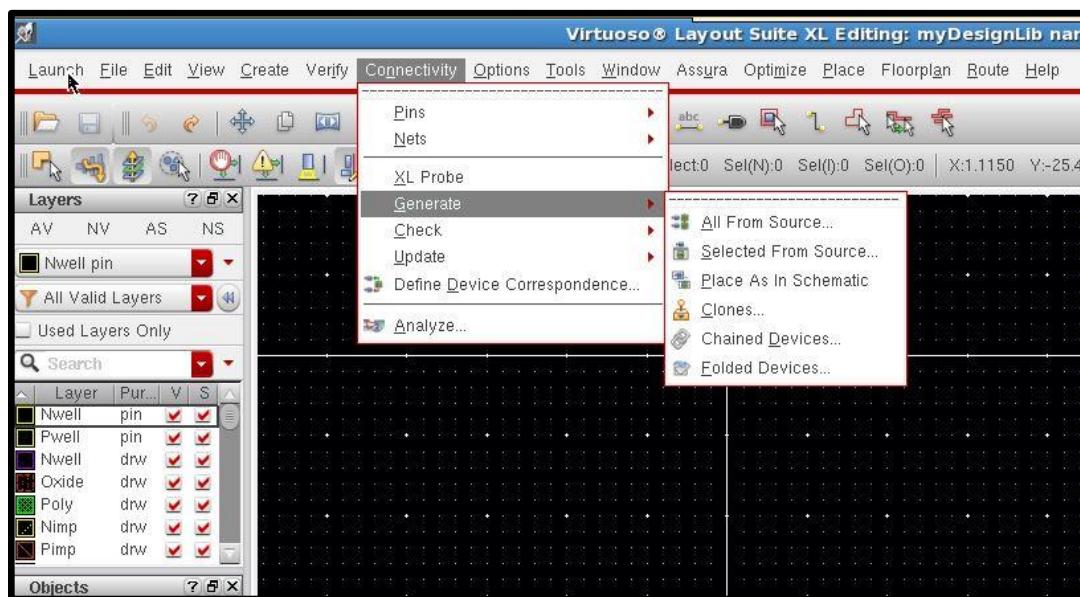


Fig. 35: Virtuoso Layout Suite XL Editing widow

VI. The layout of NAND gate is given below-

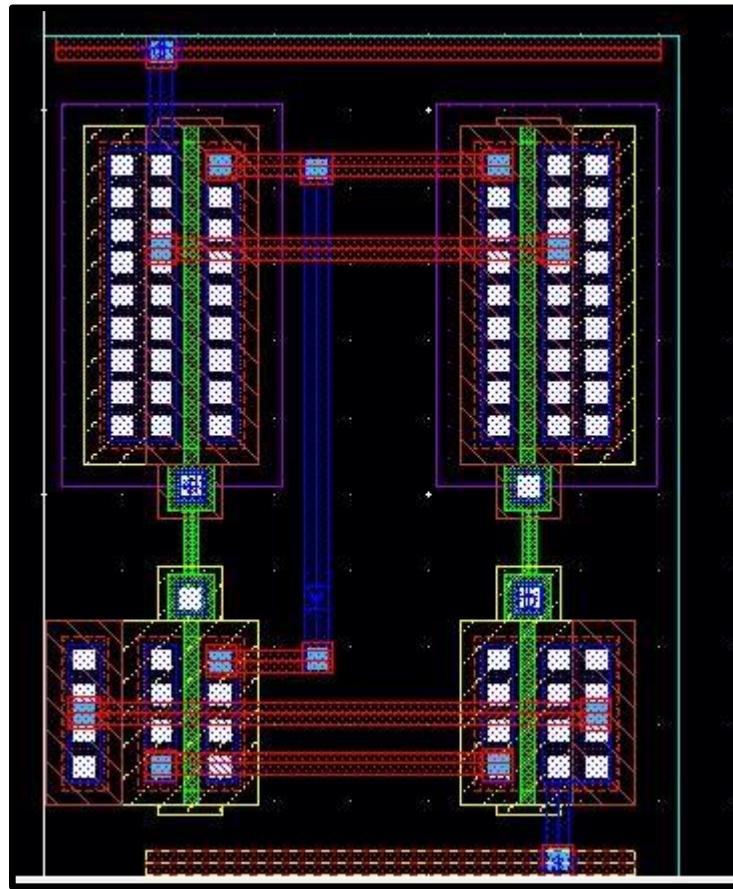


Fig. 36: Layout of NAND gate

5. Check LVS and DRC:

A. DRC Check:

- I. From the Virtuoso Layout Site XL Editing window click – **Pvs> Run DRC**.

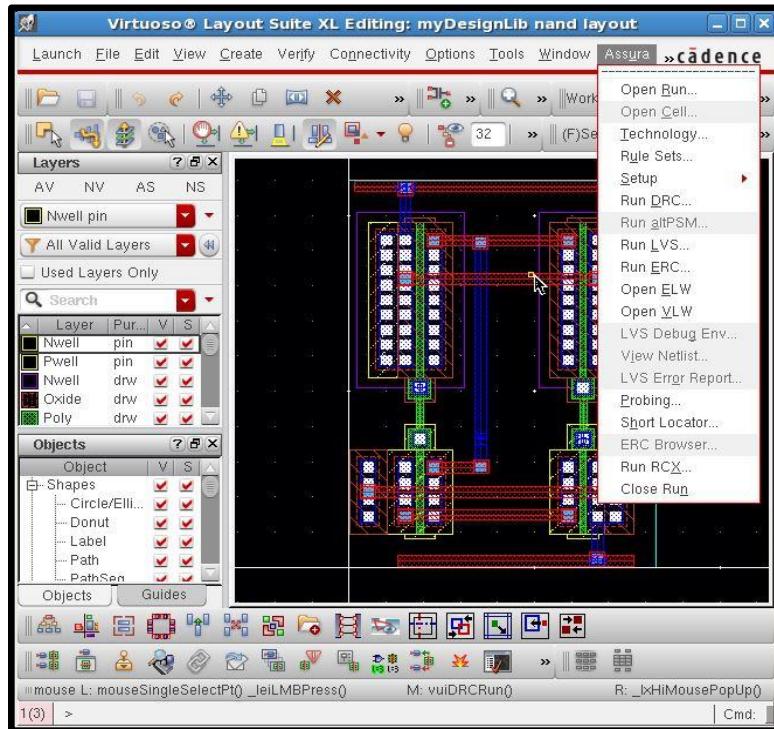


Fig. 37: Virtuoso Layout Suite XL Editing widow

II. “Run Assura DRC” window is open. Here write **Run Name, **Run Directory** and **Rules File**. Click – **ok**.**

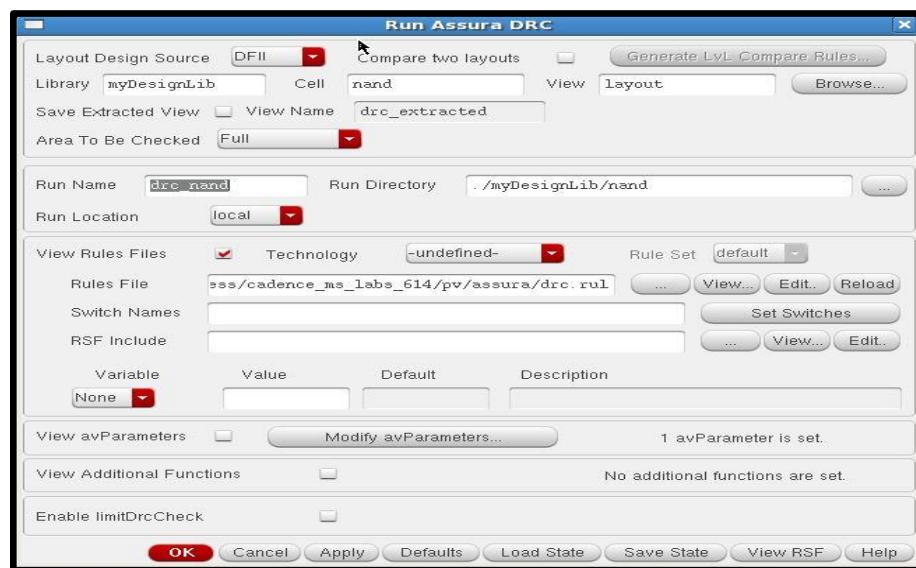


Fig. 38: Run Assura DRC



Fig. 39: No DRC errors

B. LVS Check:

- I. From the Virtuoso Layout Site XL Editing window click – **Assura> Run LVS**.
- II. “Run Assura LVS” window is open. Here write **Run Name, Run Directory and Extract Rules and Compare Rules**. Click – **ok**.

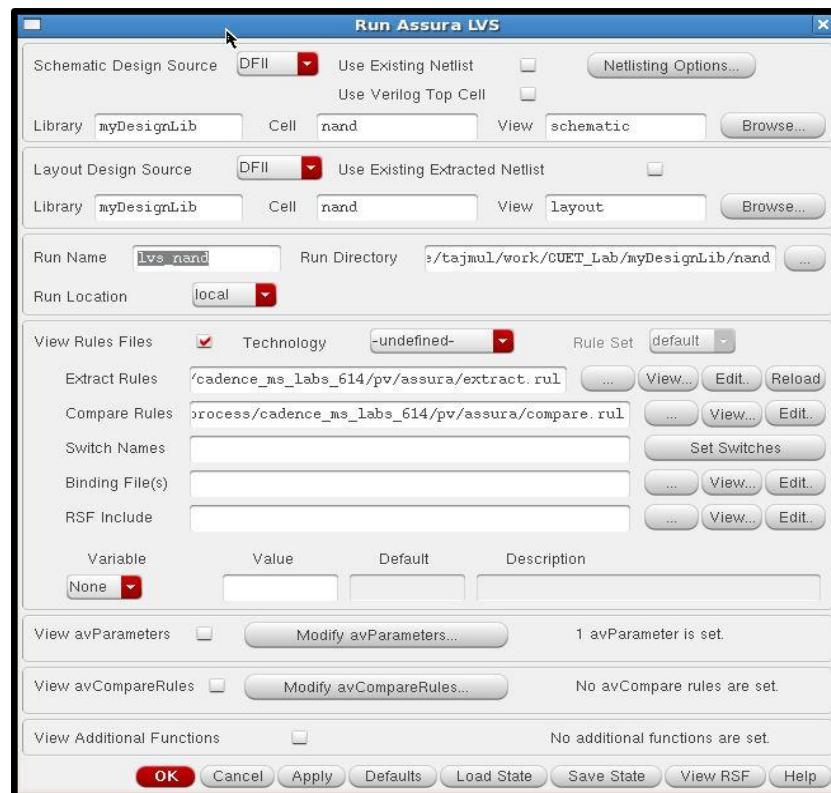


Fig. 40: Run Assura LVS window

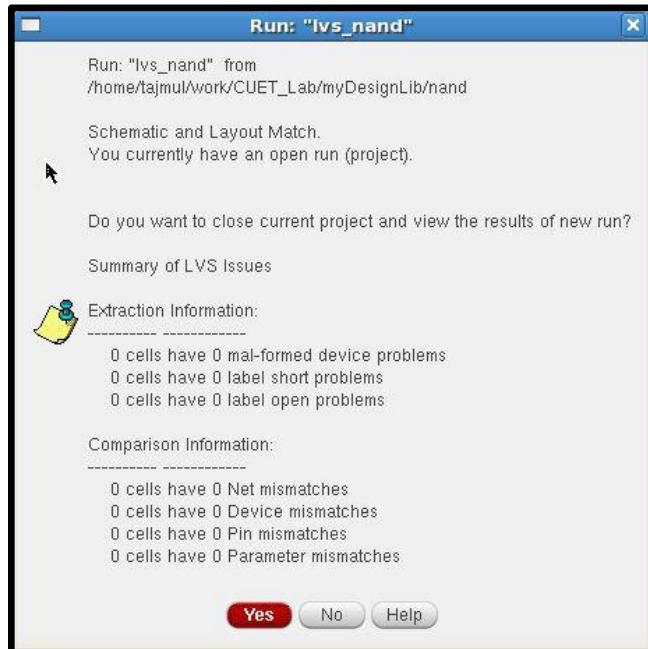


Fig. 41: No LVS errors

Lab Summary:

In this lab you learn how to –

- I. Design schematic view
- II. Perform DC and Transient and Parametric analysis
- III. Find Gain and Bandwidth.
- IV. Generate layout from schematic
- V. Check LVS and DRC.

End of Lab 6

Lab 7: Calculate the DC and AC voltages and currents for the circuit seen in Fig. 1. Verify your answers with AC analysis simulation by Cadence system.

Objective:

- 4) To find operating region.
- 5) To do AC analysis and DC analysis.
- 6) Compare your simulation result with hand calculation.

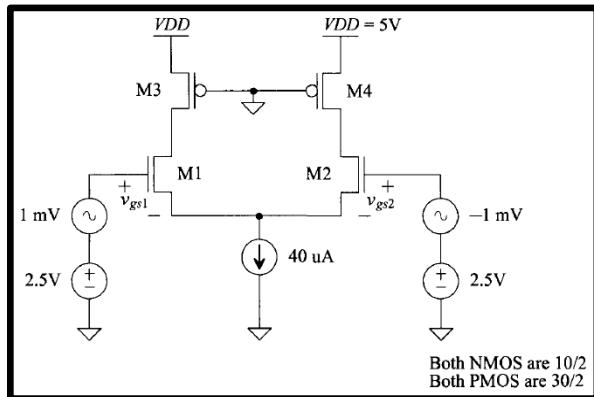


Fig. 1: Circuit for Lab 7

1. Operating Region:

I. Draw the schematic diagram and **Check and Save** the schematic.

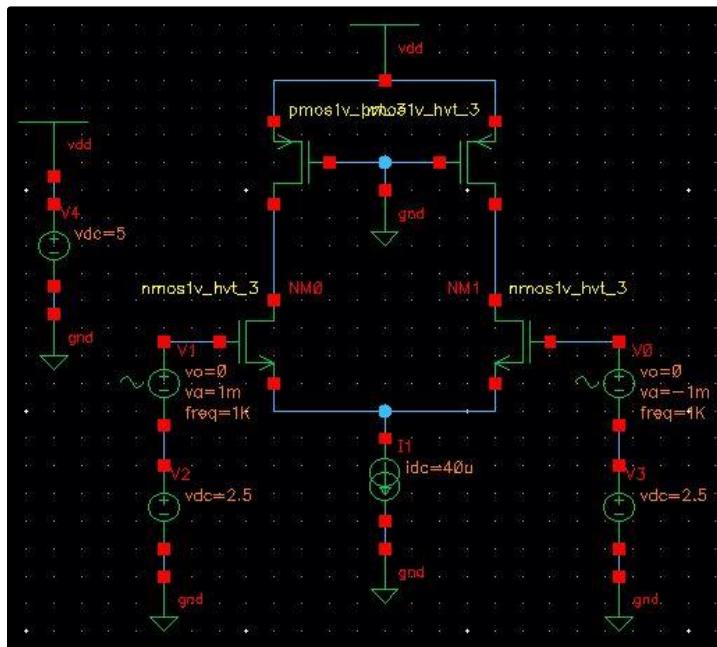


Fig. 02: Schematic diagram

II. From the schematic diagram click – **launch > ADE L**. A “**Virtuoso Analog Design Environment**” window is open.

In this window click – **Analyses > Choose** or just click on icon . A “**Choosing Analyses..**” window is open.

In this window select **dc, Save DC Operating Point**. Click –**ok**.

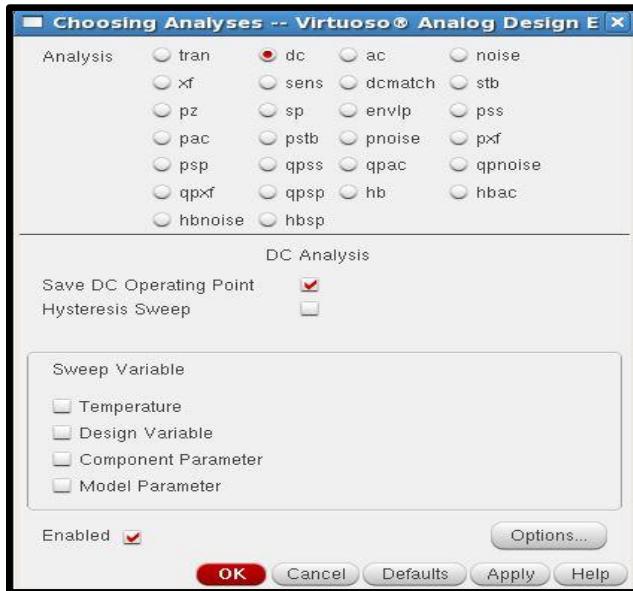


Fig. 03: Choosing analysis window

III. In the virtuoso analog design environment window analysis type is saved. **Run** the simulation.

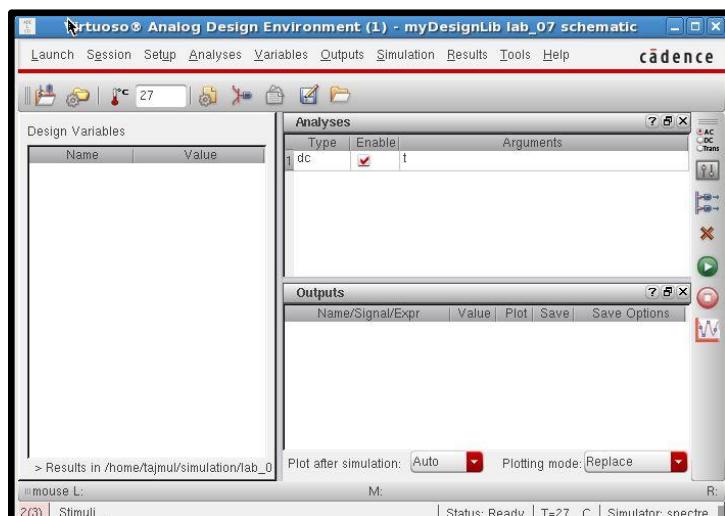


Fig. 04: Virtuoso Analog Design Environment window

IV. From the Schematic window click – **Edit > Component Display**.

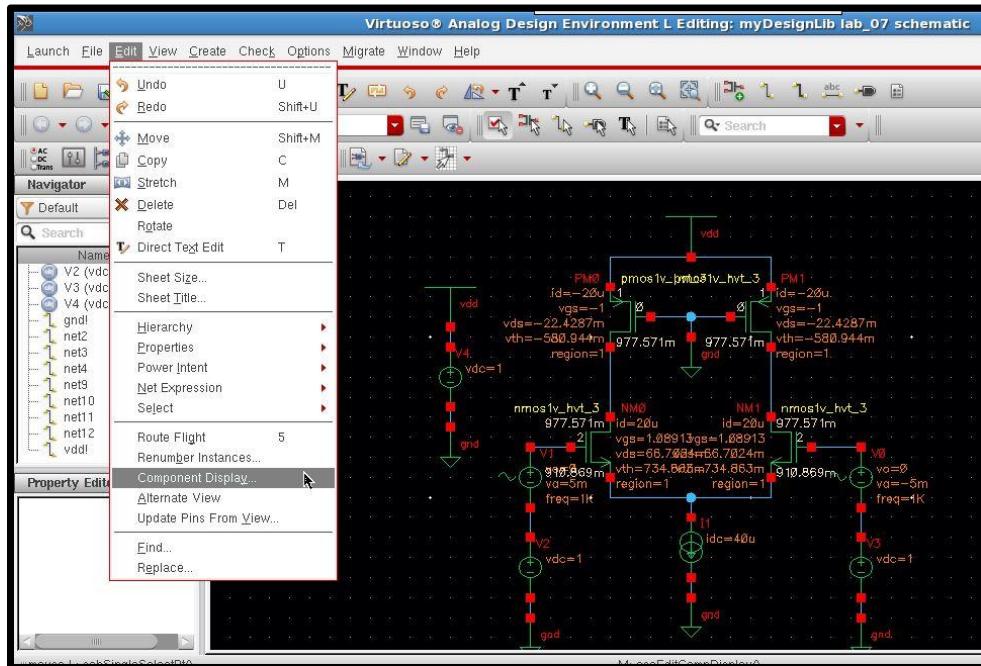


Fig. 05: Schematic window

V. An “Edit Component Display Options” window is open.

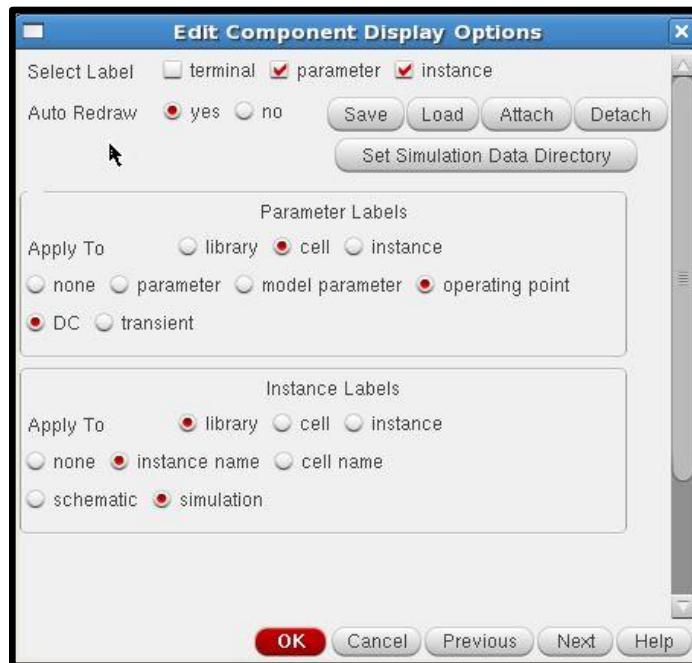


Fig. 06: Edit component display options window

VI. Select a MOSFET from schematic. “Edit Component PM1 Display” is open. In this window select the **display value only**. Do it for every MOSFET.

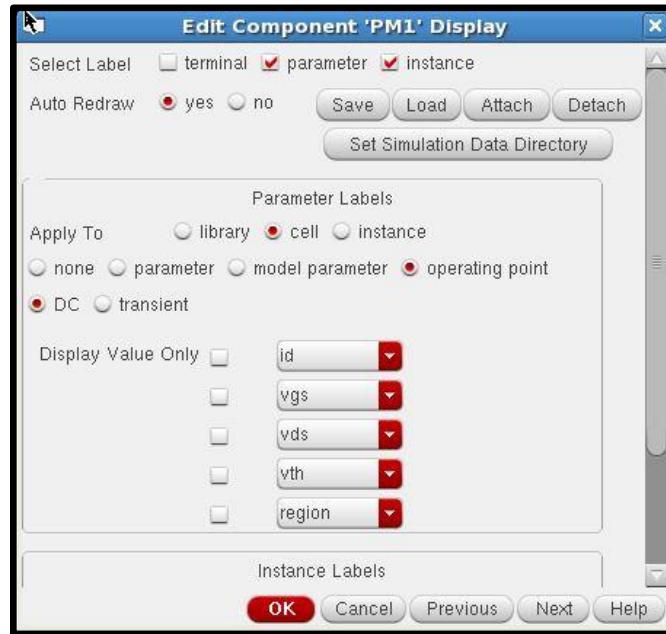


Fig. 07: Edit component display for different MOSFET

VII. Finally see the dc operating point of all MOSFET in the schematic window.

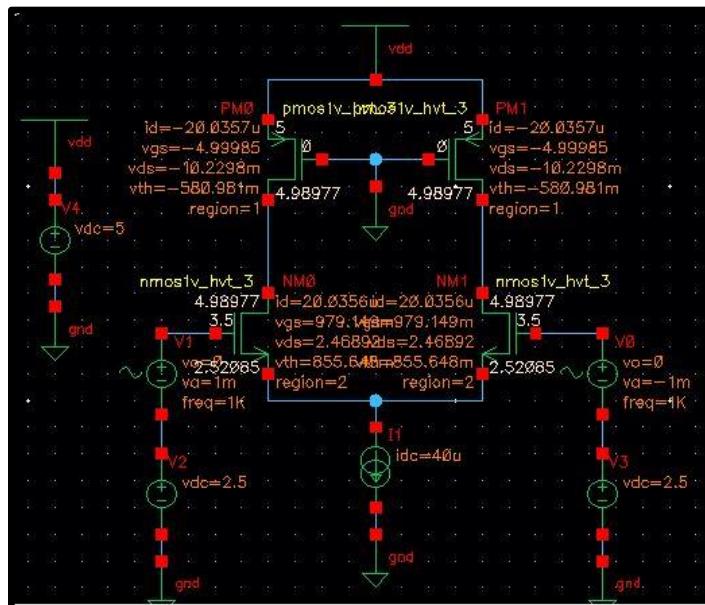


Fig. 08: Operating points of MOSFETs

Another Process:

I. From virtuoso analog design environment click – **Results > Print > DC Operating Points**.

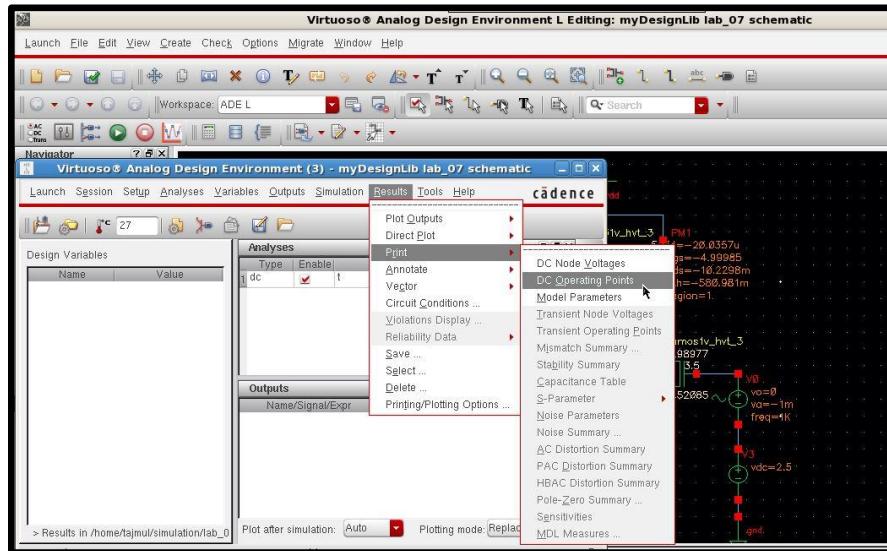


Fig. 09: Virtuoso analog design environment window

II. A “Result Display Window” is open. Now click any component from the schematic and see the dc operating points in result display window.

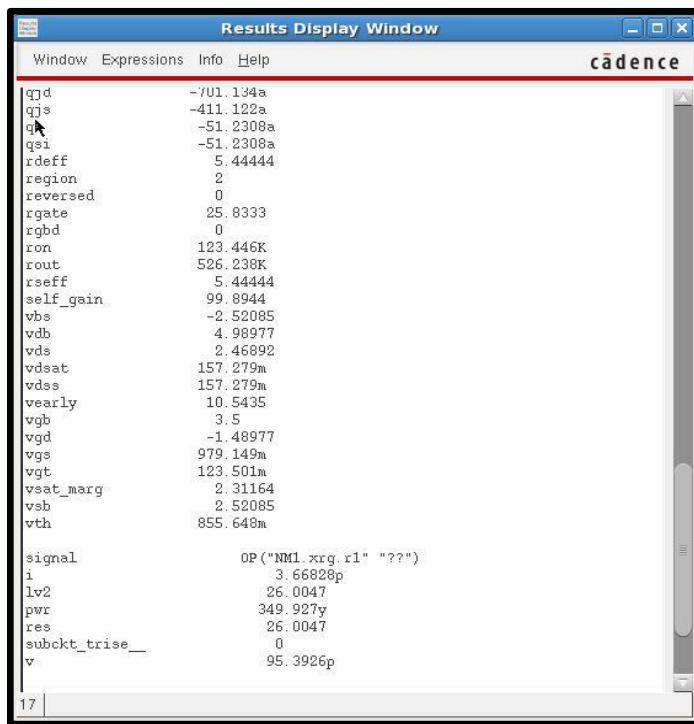


Fig. 10: Results display window

2. AC analysis and DC analysis

DC analysis:

For DC analysis inputs are only DC.

Please follow the previous process to find out the operating points.

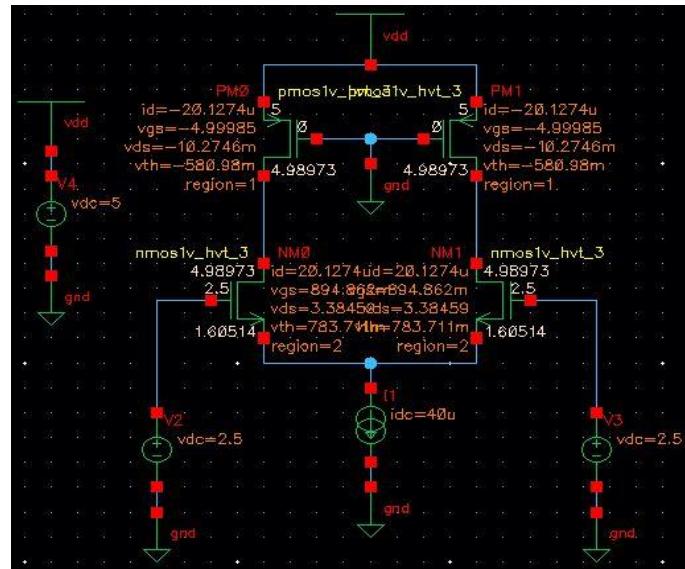


Fig. 11: Operating points for DC analysis

AC analysis:

For AC analysis inputs are only AC. Flow the previous process to find out the operating points.

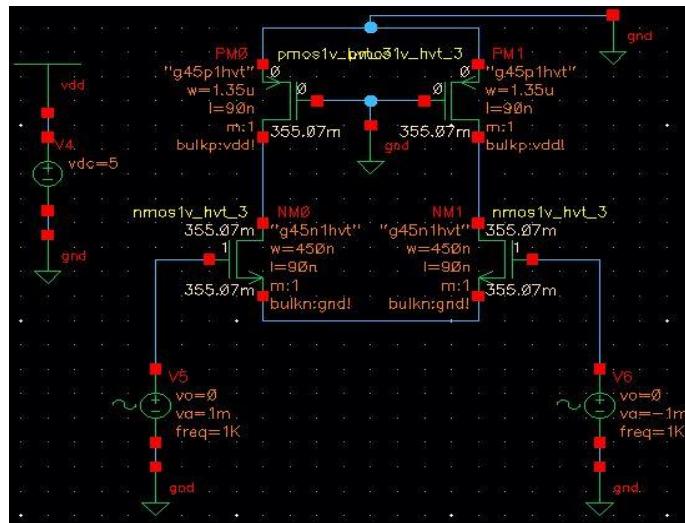


Fig. 12: Operating points for AC analysis

Lab Summary:

In this lab you learn how to –

- I. Find operating region
- II. Do AC analysis and DC analysis

End of Lab 7

Lab 8: Calculate the Transition Frequency (ft) of a 10/2 NMOS.

Objective:

- 4) To find Transition Frequency (ft).
- 5) To find Transition Frequency (ft) when NMOS is multiplied by 10 and compare 1) & 2)
- 6) Verify your hand calculations using simulations by Cadence system.

1. Transition Frequency when 10/2 NMOS:

I. Drawing Schematic:

For NMOS, Width = 450 nm

Length = 90 nm

DC voltage of V1 = 1V

DC voltage of V2 = 1V

The final schematic Diagram is given below-

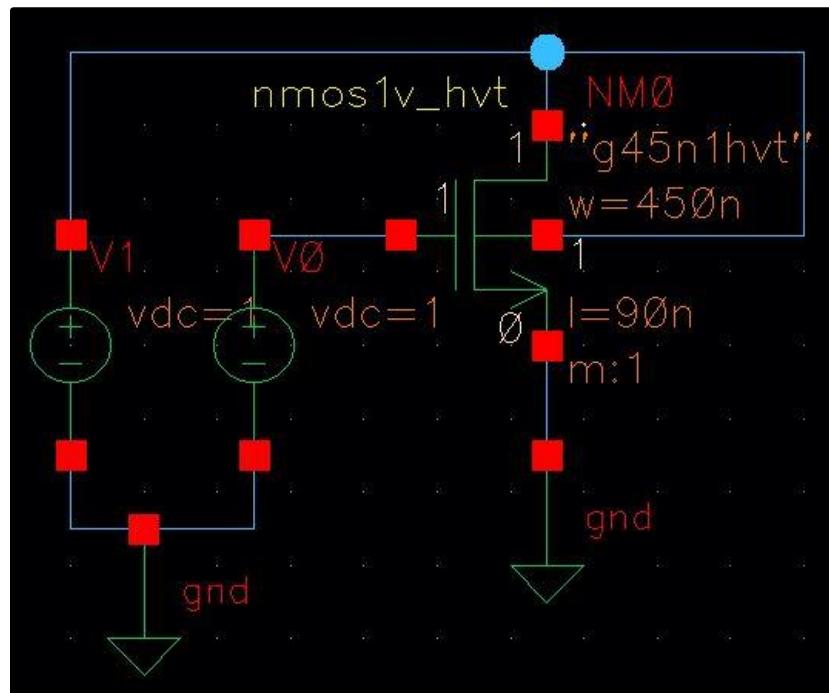


Fig. 01: Schematic diagram for 10/2 NMOS

Check and Save the schematic.

II. DC operating Point:

- A.** From the schematic diagram click – **launch > ADE L**. A “**Virtuoso Analog Design Environment**” window is open.

In this window click – **Analyses > Choose** or just click on icon . A “**Choosing Analyses..**” window is open.

In this window select **dc, Save DC Operating Point**. Click –**ok**.

In the virtuoso analog design environment window analysis type is saved. **Run** the simulation.

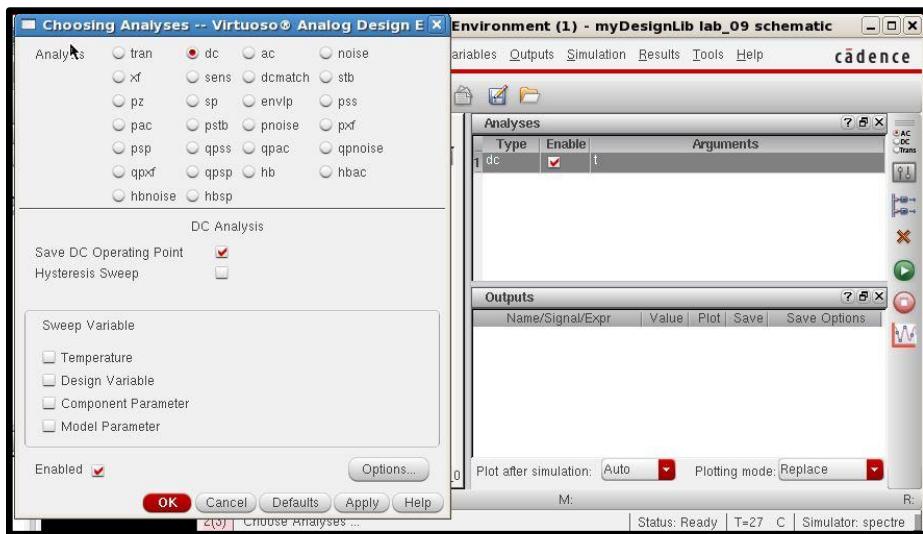


Fig. 02: Choosing analysis and virtuoso analog design environment window

- B.** From virtuoso analog design environment click – **Results > Print > DC Operating Points**.

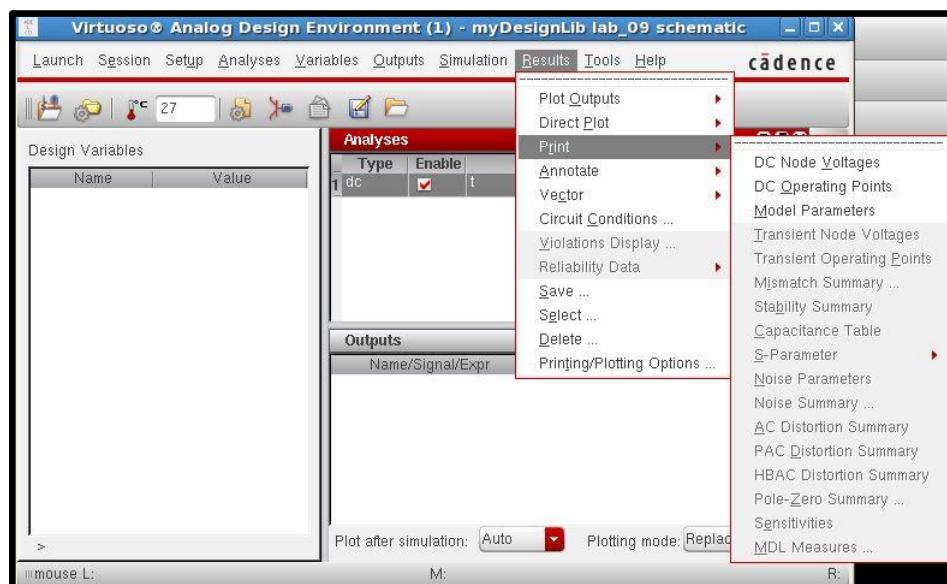


Fig. 03: Virtuoso analog design environment window

C. A “Result Display Window” is open. Now click on NMOS from the schematic and see the dc operating points in result display window.

Results Display Window	
Window	Expressions
cgdbo	449.561a
cge	-514.824a
cgsbo	-450.165a
cjd	233.963a
cjs	370.255a
covlgb	0
covlgd	63.9839a
covlgs	64.6586a
csb	-629.092z
csd	-3.91661a
csg	-411.96a
css	416.506a
fug	93.4716
gbd	1.00002p
gbs	246.679m
gds	33.9883u
gm	339.576u
gmb	0
gmb_s	0
gmoverid	2.41055
ibe	6.38014m
ibulk	6.38014m
id	140.871u
idb	-766.976a
ide	140.871u
ids	140.871u
igb	140.851z
igbacc	140.851z
igbinv	36.5969z
igcd	1.11248p
igcs	1.52567p
igid	601.024z
igidt	2.73577p
ige	2.73577p
igidl	0
sc	

Fig. 04: Operating points of NMOS in results display window

Transition Frequency, $f_T = g_m / (2\pi C_{GS})$

2. Transition Frequency when NMOS is multiplied by 10:

I. Drawing Schematic:

For NMOS, Width = 4.5 μm

Length = 900 nm

All other components are same as before.

The schematic diagram is given below-

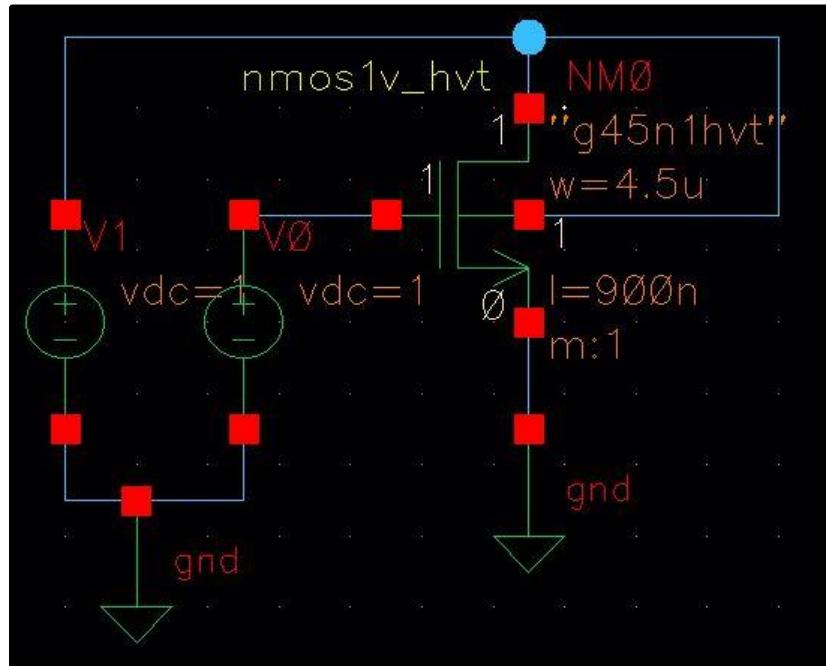


Fig. 05: Schematic diagram when NMOS is multiplied by 10

II. DC operating Point:

Please follow the previous process of DC operating points.

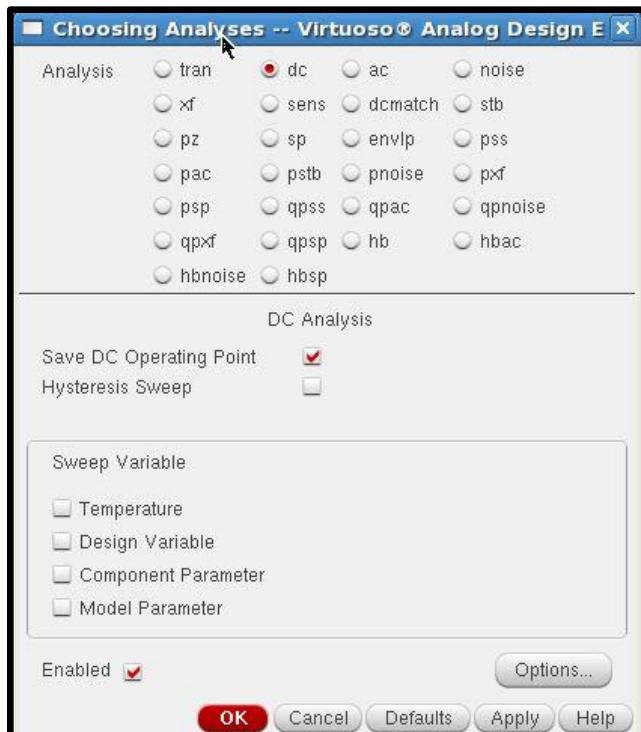


Fig. 06: Choosing analysis window for dc analysis

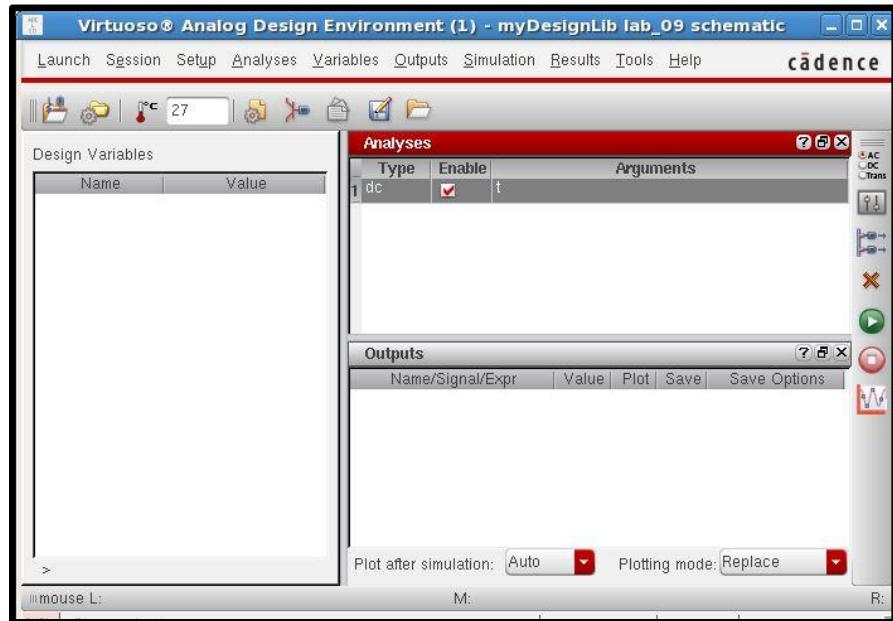


Fig. 07: Virtuoso analog design environment window

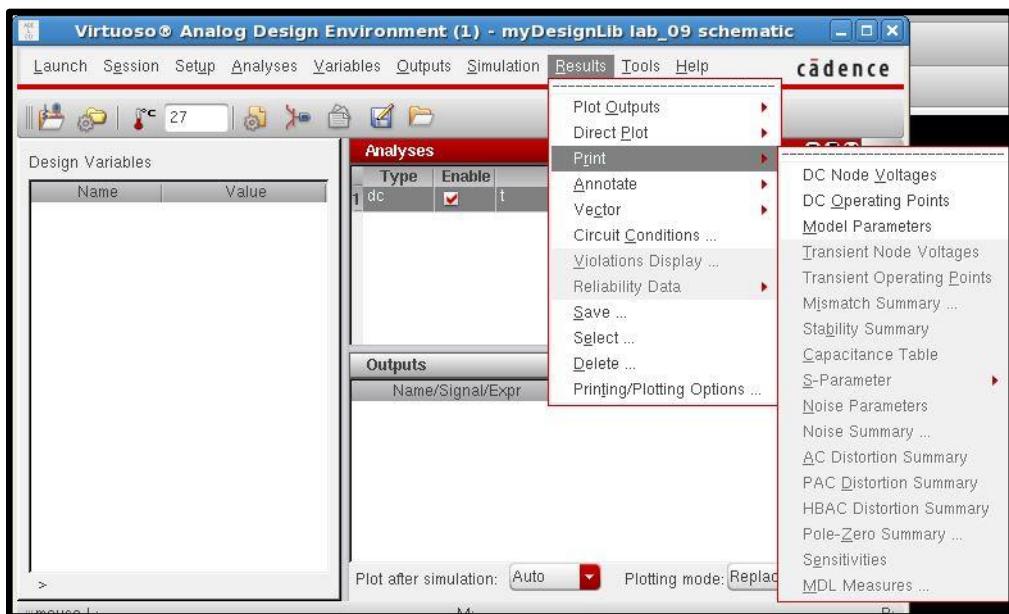


Fig. 08: Virtuoso analog design environment window

Results Display Window	
Window	Expressions
cdb	1.02439a
cdd	702.68a
cddbo	62.8547a
cdg	-695.965a
cdgbo	-56.1398a
cds	-7.73928a
cdsbo	-7.73928a
cgb	507.856a
cgd	-603.755a
cgdbo	36.0706a
cgg	49.1385f
cggbo	47.8521f
cgs	-49.0426f
cgsbo	-48.3961f
cjd	2.23574f
cjs	3.62105f
covlgb	0
covlgd	639.825a
covlgs	646.589a
csb	-384.015a
csd	-81.8925a
csq	-36.7353f
css	37.2012f
fug	8.90392G
gbd	1.00015p
gbs	386.635m
gds	508.505u
gm	2.74906m
gmb	157.954u
gnbs	157.954u
gnoverid	3.59852
ibe	34.1569m
ibulk	34.1569m
id	763.941u
idb	-415.985a
27	

Fig. 09: Operating points in results display window

Now calculate the transition frequency from results display window and compare it with the previous result.

Lab Summary:

In this lab you learn how to –

- I. Find Transition Frequency
- II. Find Transition Frequency when NMOS is multiplied by 10

End of Lab 8

Lab 09: For the circuits seen in Fig. 3, estimate both the output voltage at room temperature and how it will change with temperature. Use the short-channel CMOS process.



Fig. 01: Circuit for Lab 10.

Objective:

- 3) To find output voltage at room temperature and by varying temperature.
- 4) Verify your answer with Cadence simulation.

1. Output Voltage at Room Temperature and by Varying Temperature for NMOS:

I. Drawing Schematic:

The schematic diagram is given below-

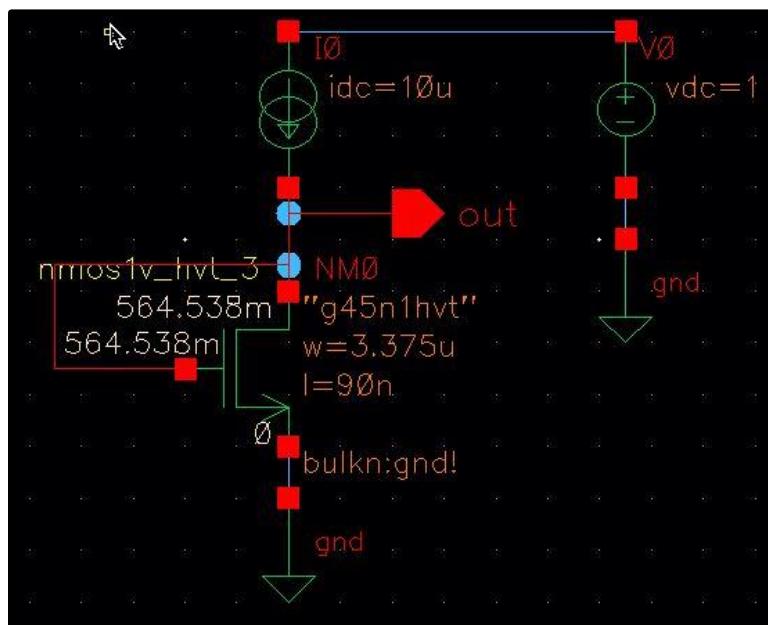


Fig 02: Schematic Diagram

II. DC analysis:

Please follow the DC analysis process of lab 6.

For this lab in choosing analysis window select **dc**, **Save DC Operating Point**.

Select Sweep Variable – **Temperature** and Sweep Range – **Start = -45** and **Stop = 200**.

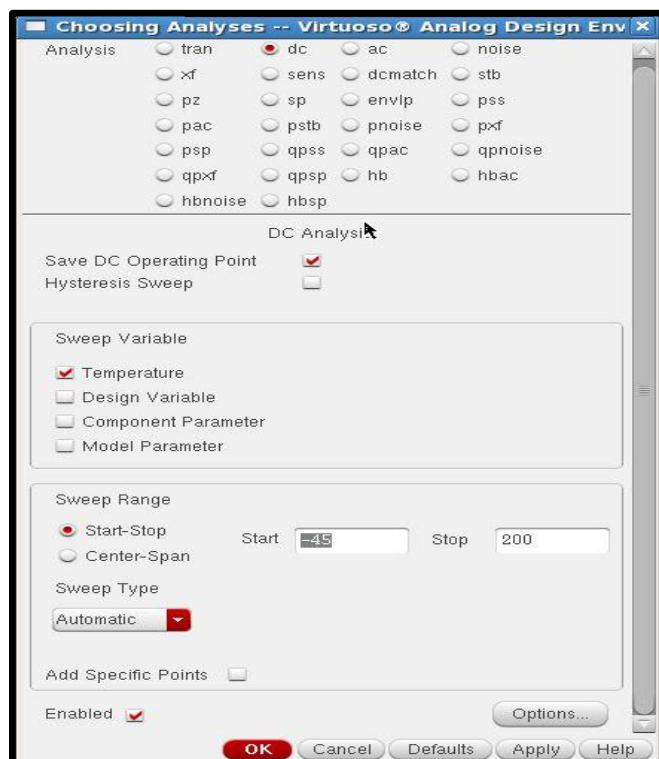


Fig. 03: Choosing analysis window

Now see the output voltage with varying temperature.

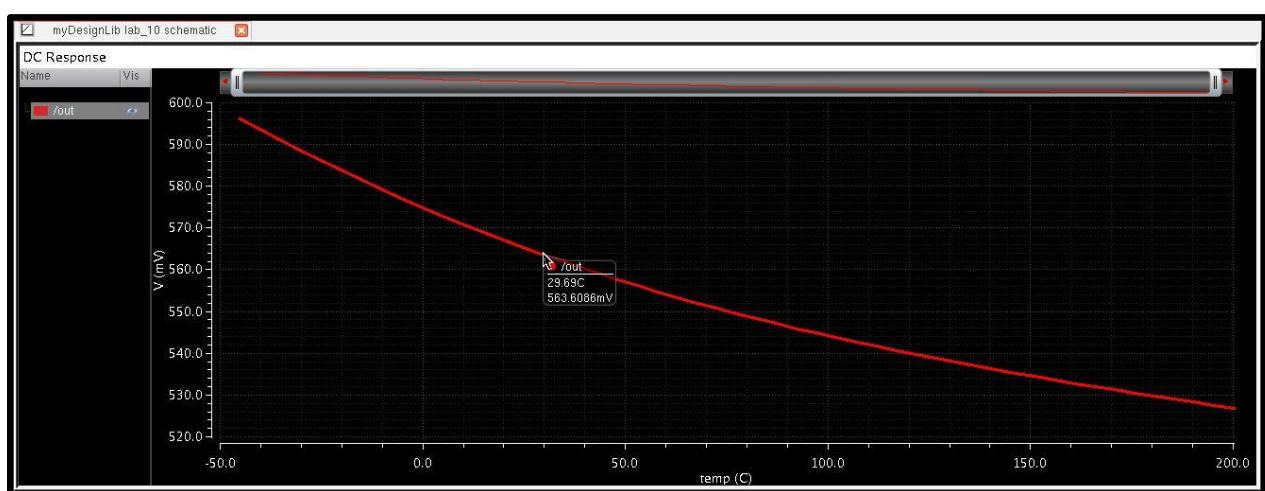


Fig. 04: Output voltage with temperature

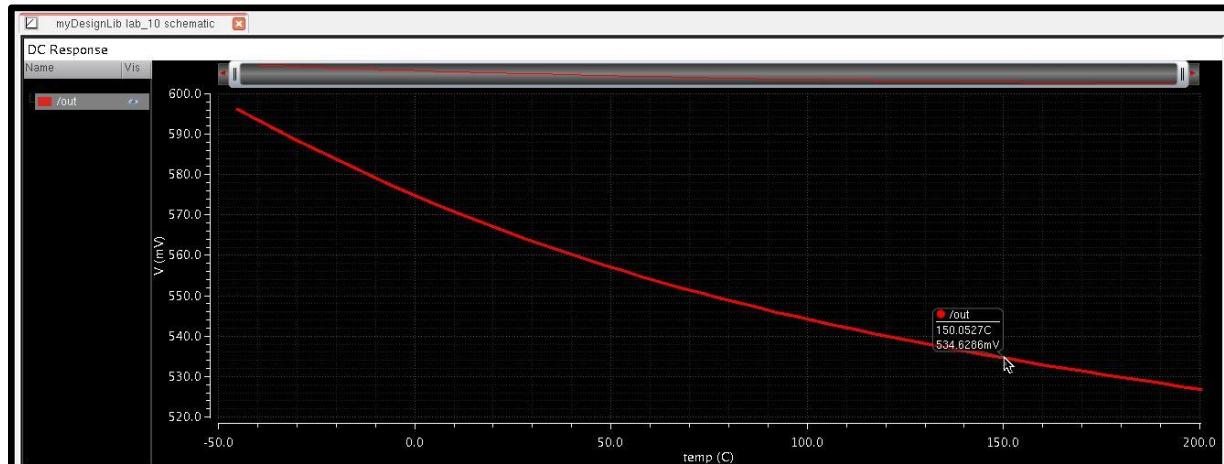


Fig. 05: Output voltage with temperature

At 29.69°C , output voltage = 563.6086mV

At 150.0527°C , output voltage = 534.6286mV

So, **output voltage is decreased, when temperature is increasing.**

2. Output Voltage at Room Temperature and by Varying Temperature for PMOS:

I. Drawing Schematic:

The schematic diagram is given below-

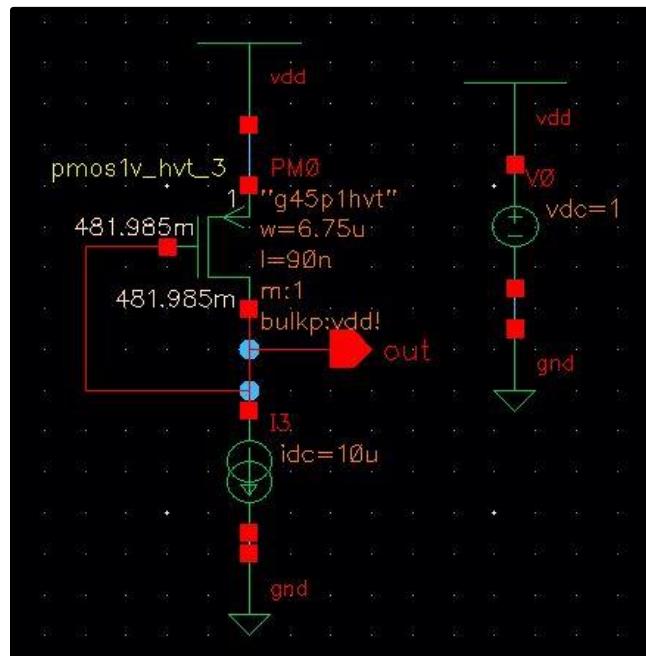


Fig. 06: Schematic diagram

II. DC analysis:

Please follow the previous DC analysis process.

Now see the output voltage with varying temperature.

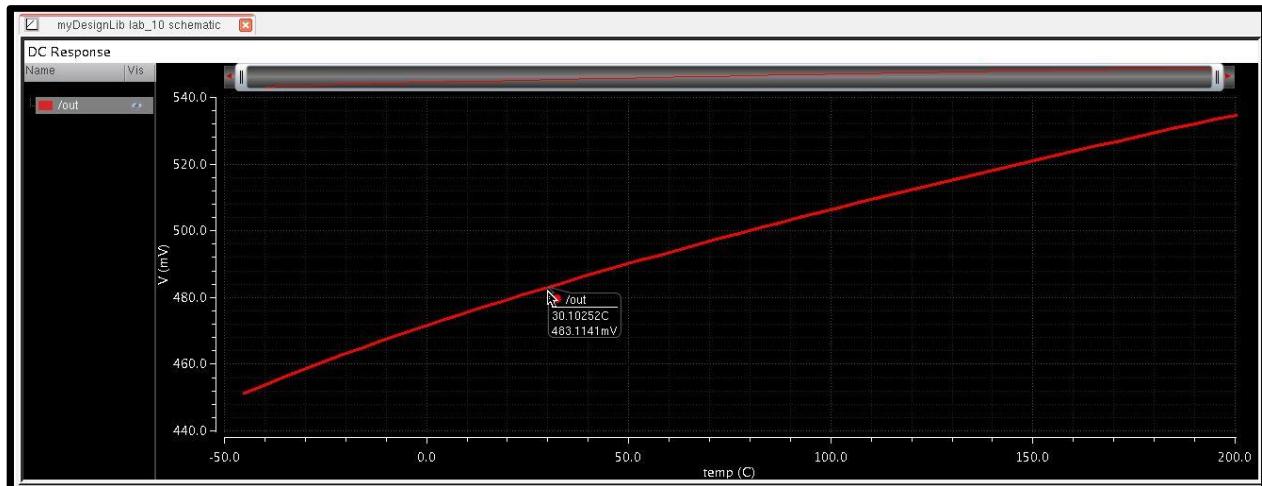


Fig. 07: Output voltage with temperature

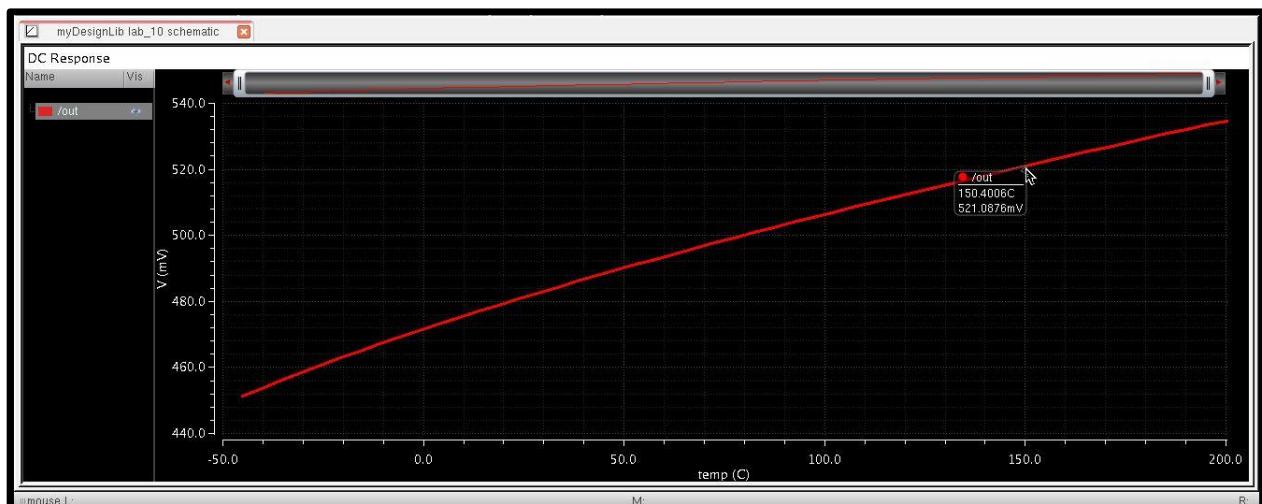


Fig. 08: Output voltage with temperature

At 30.10252°C, output voltage = 483.1141mV

At 150.4006°C, output voltage = 521.0876mV

So, **output voltage is increased, when temperature is increasing.**

Lab Summary:

In this lab you learn how to –

- I. Find output voltage at room temperature and by varying temperature

End of Lab 9

Lab 10: Design a current Mirror circuit.

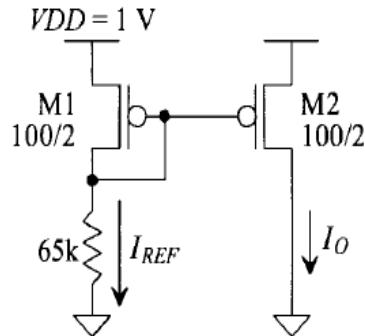


Fig.01

Objective:

- 6) To design schematic.
- 7) To find voltage and current of each branch.
- 8) To observe voltage and current of each branch by changing width and length of devices.
- 9) Verify your answer with Cadence simulation.
- 10) To estimate the temperature behavior of the gate voltage of M1 in Fig. 01.

1. Drawing Schematic:

The schematic diagram is given below-

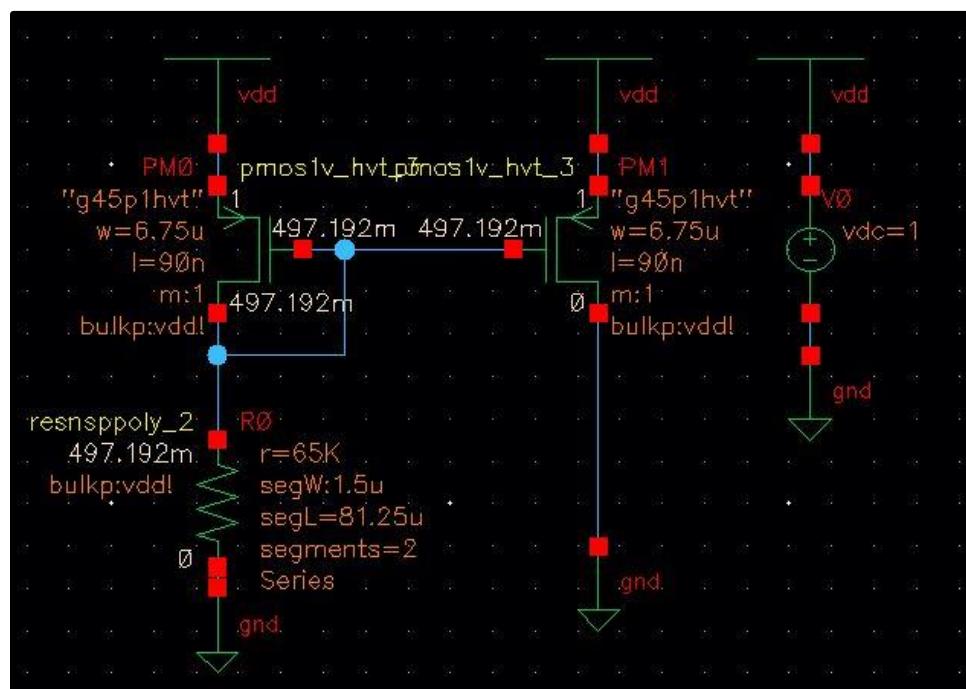


Fig. 02: Schematic diagram

2. Observe Voltage and Current of each branch:

I. Observe Current of each branch:

Please follow the dc analysis process of lab 6.

To see the output select drain node of both PMOS.

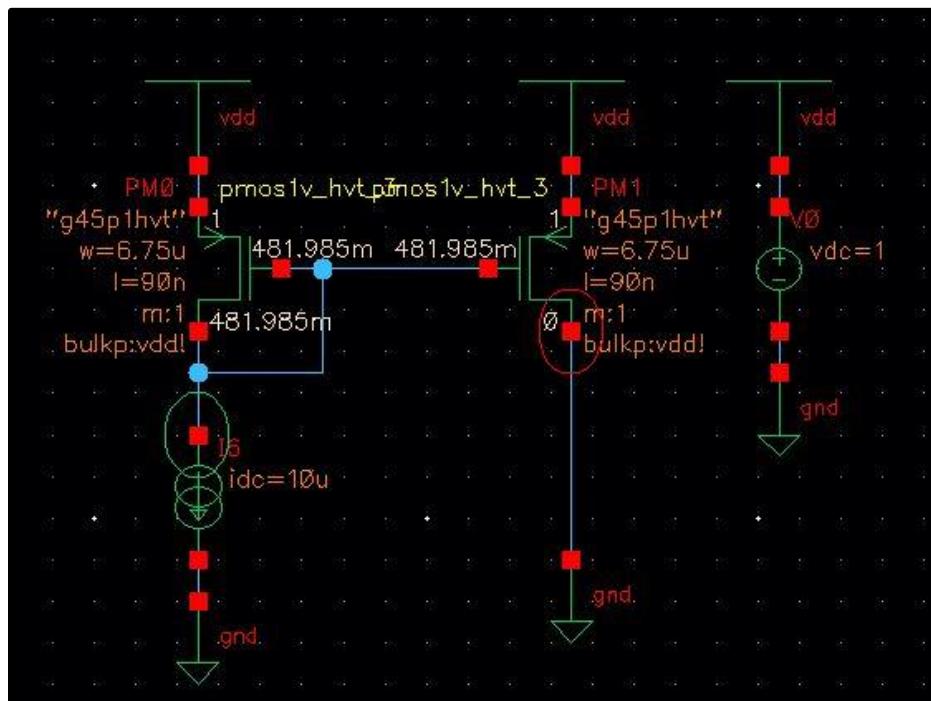


Fig. 03: Select drain node of both PMOS

Now see the current of each branch.

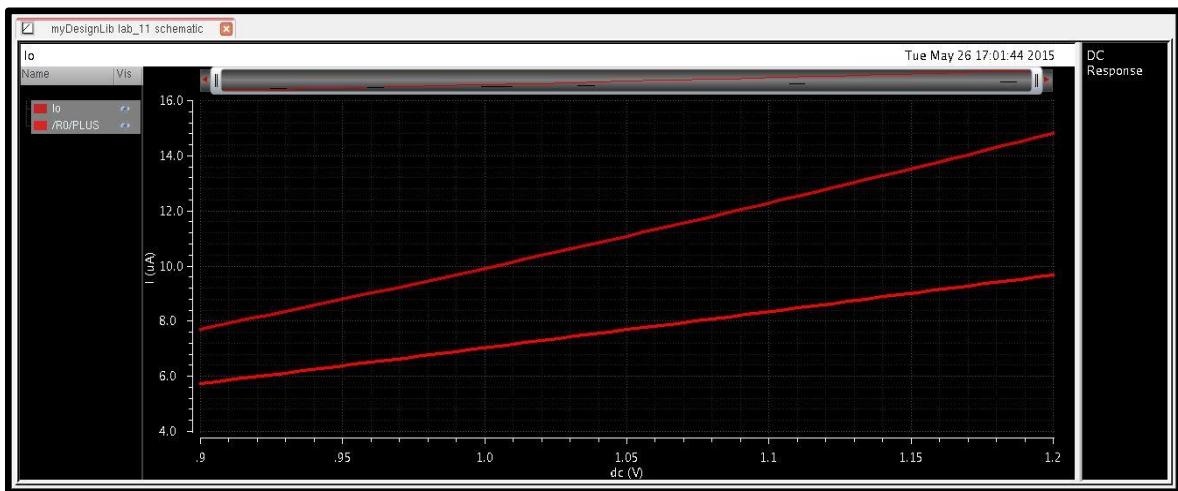


Fig. 04: Current of each branch

II. Observe Voltage of each branch:

Please follow the process of lab 4 to find out the operating point.

Now see the voltage of each branch.

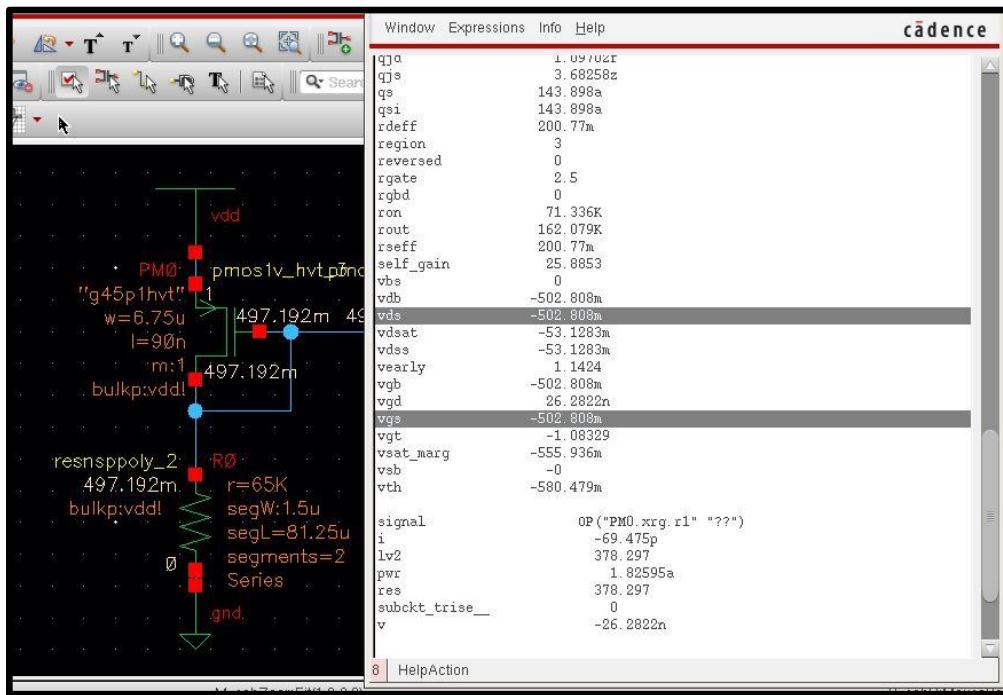


Fig. 05: Voltage of PM0

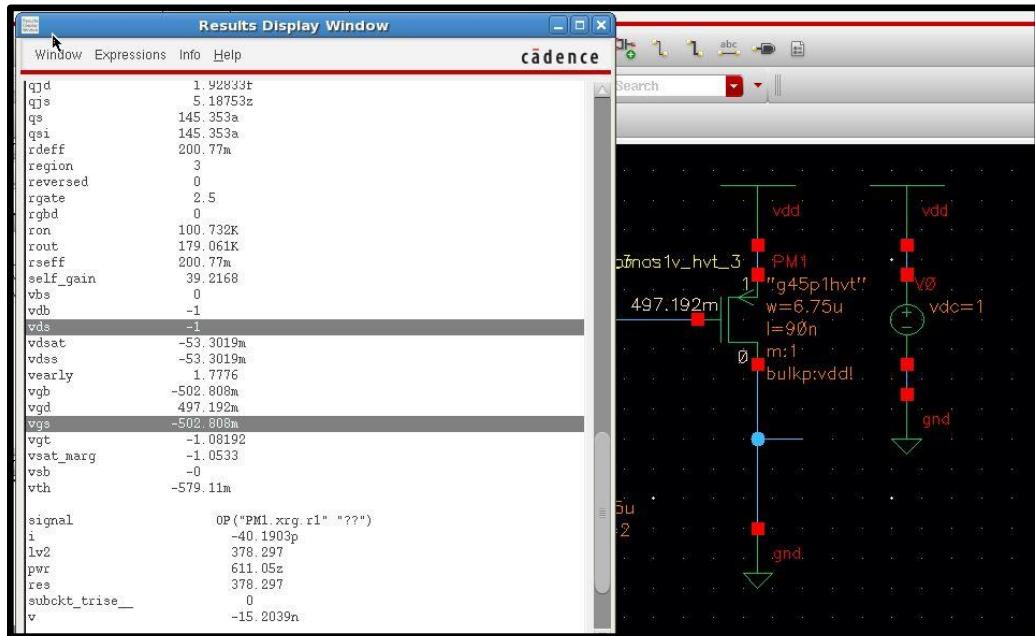


Fig. 06: Voltage of PM1

3. Observe Voltage and Current of each branch by changing width and length of devices:

Now change the width and length of PM0 and PM1 in previous schematic.

*Follow the previous process of **Observe Voltage and Current of each branch**.*

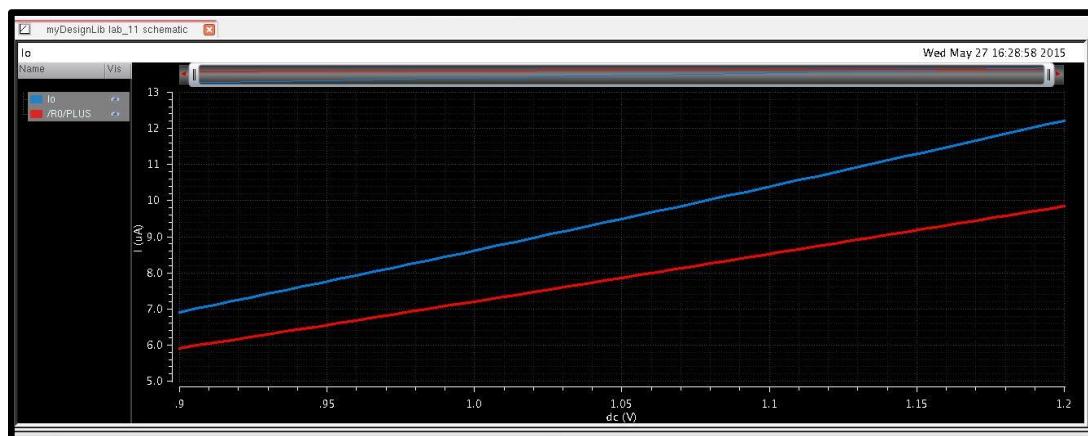


Fig. 07: Current of each branch

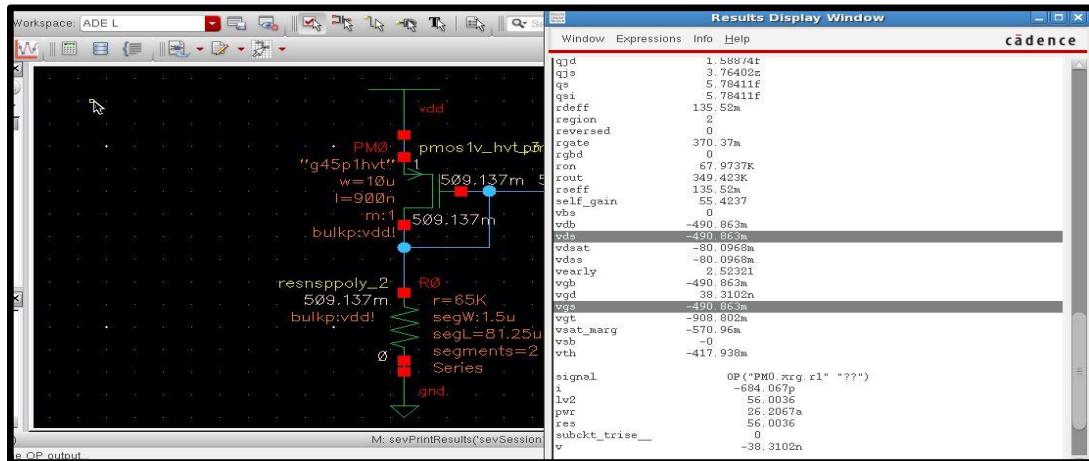


Fig. 08: Voltage of PM0

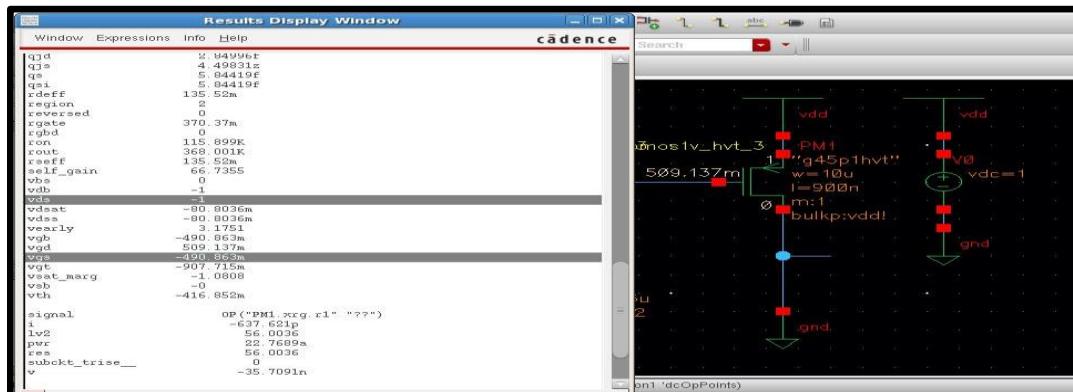


Fig. 09: Voltage of PM1

4. Estimate the Temperature Behavior of the Gate Voltage of M1:

Follow the DC analysis process of lab 6.

For this lab in choosing analysis window select dc, Save DC Operating Point.

Select Sweep Variable – Temperature and Sweep Range – Start = -45 and Stop = 125.

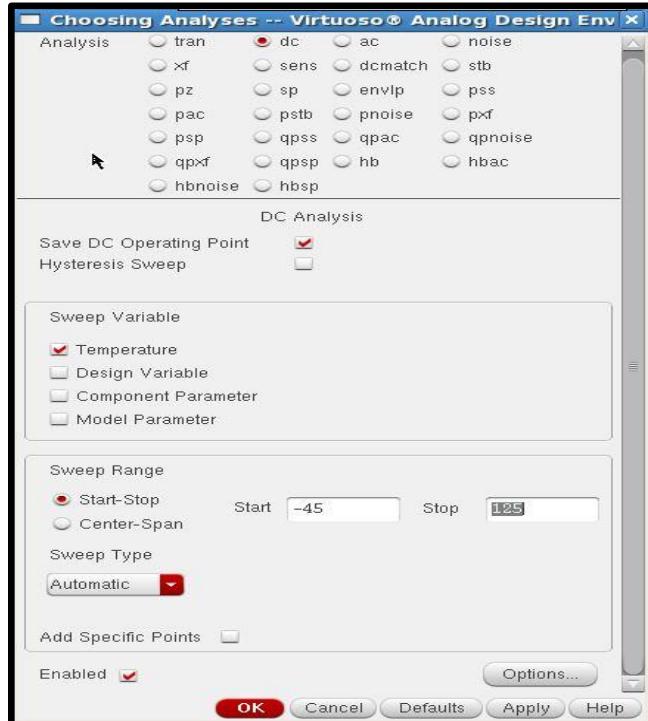


Fig. 10: Choosing analysis window

Now see the gate voltage of M1 varying temperature.

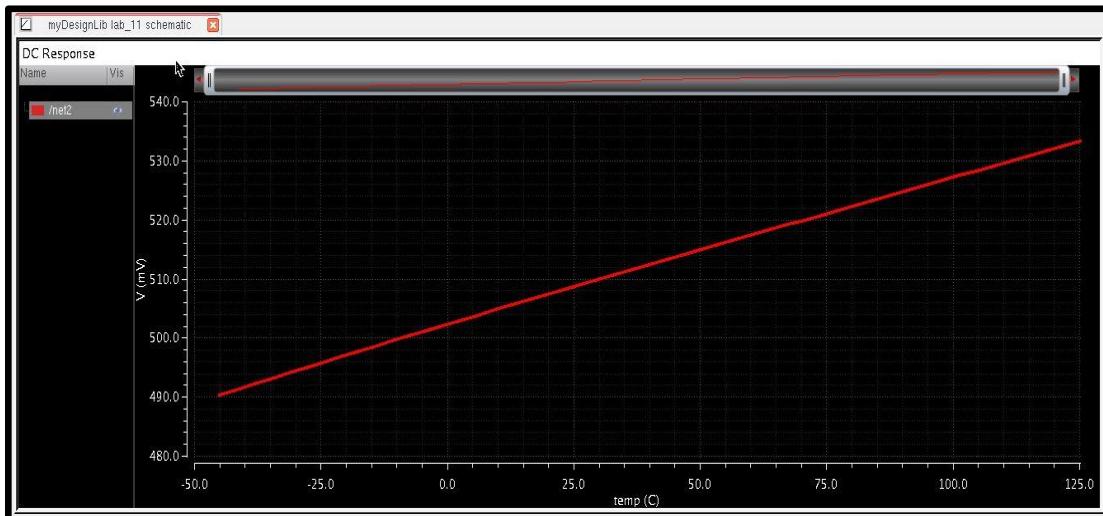


Fig. 11: Gate voltage of M1 with temperature

Lab Summary:

In this lab you learn how to –

- I. Design schematic
- II. Find voltage and current of each branch
- III. Observe voltage and current of each branch by changing width and length of devices
- IV. Estimate the temperature behavior of the gate voltage

End of Lab 10