If you are using lab pc, the IP Address is: 192.168.26.1

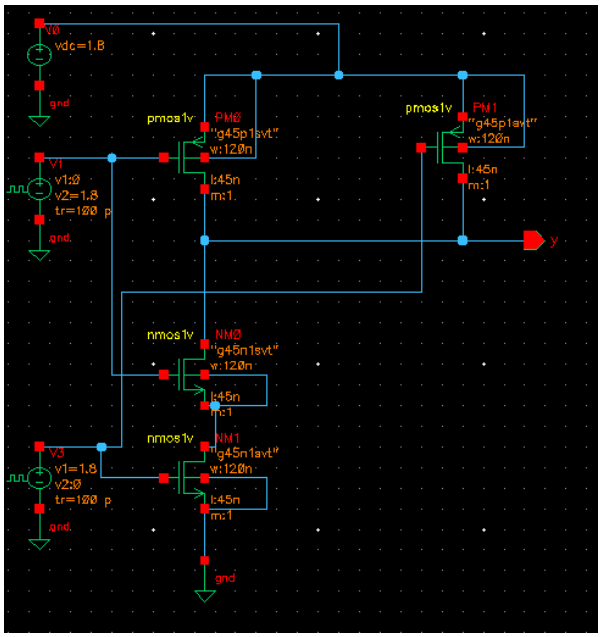
If you are logging in from your personal pc, install Putty and Xming.

Use the IP Address: 103.231.177.50

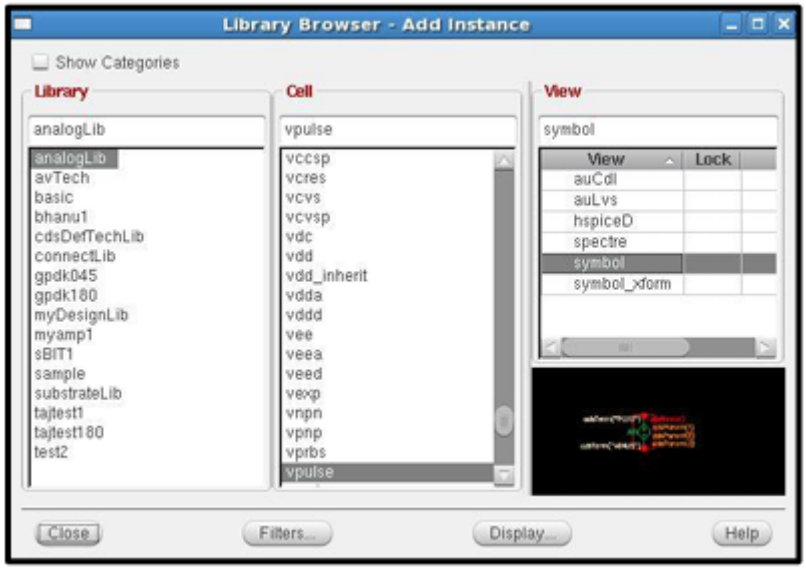
** If you are logging in from your personal pc, cadence is going to be very slow. You have to be careful not maximize any window because cadence will shut down and you would have to start again.

Transient analysis NAND Gate:

1. You have to log in using your ID and Password. Both of which are user_xx.
2. Follow the instructions as before to create a new folder and copy cshrc and cdslib.
3. Refer to Lab 1 in your Lab sheet (Page 5) to create a new cell and build the NAND circuit in the following figure.



To add the vpulse inputs, you can refer to the lab manual (page 28, part 6). After clicking on **Create Instance,** they are added not from the gpdk library, but from the analogLib.

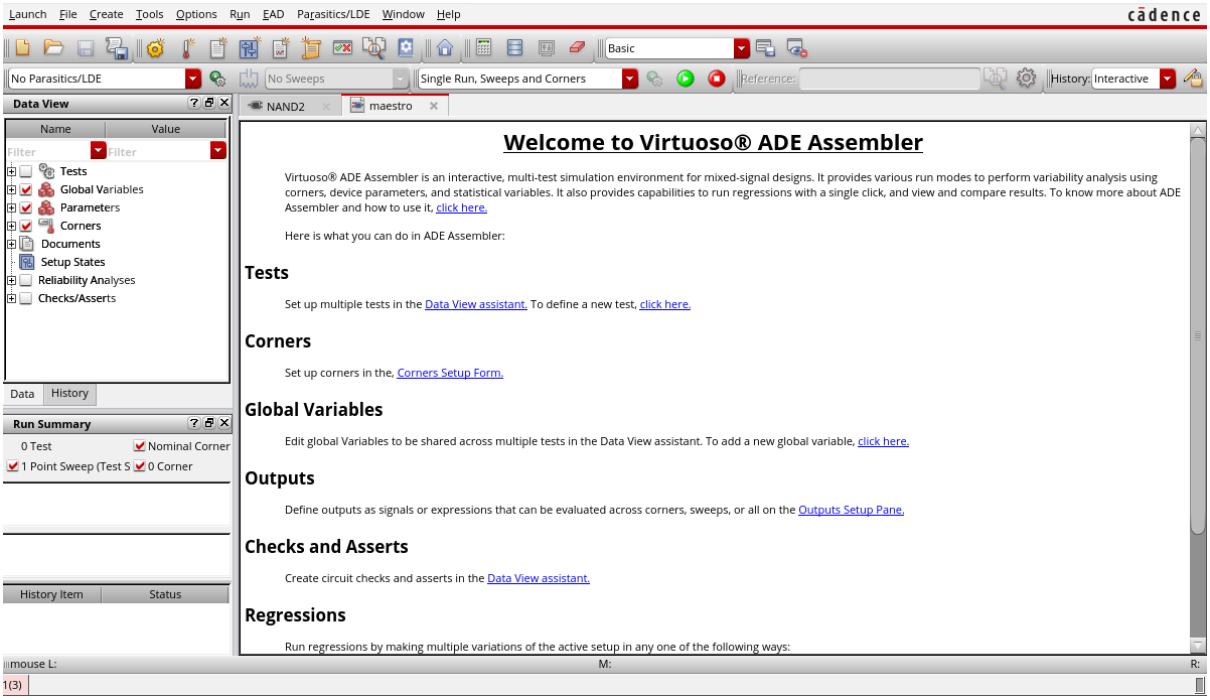


4. The input pulses should have the given properties

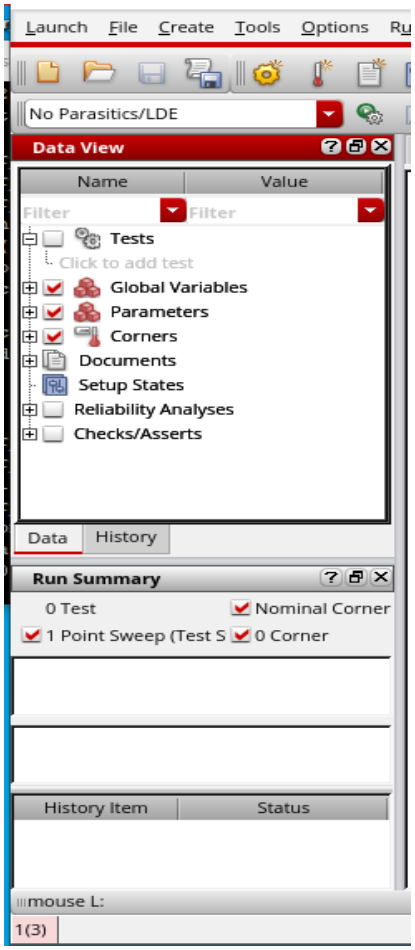
Fig. 25: Properties of vpulse for input **a**

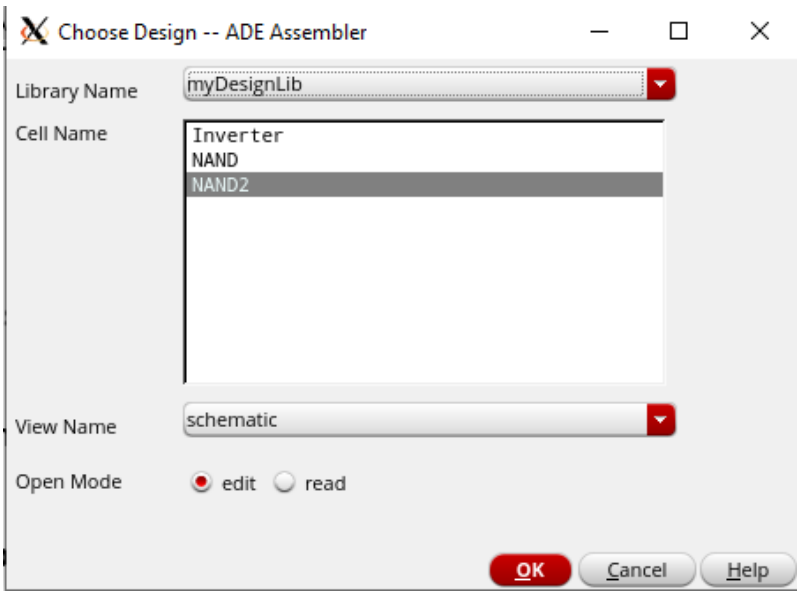
Fig. 26: Properties of vpulse for input **b**

5. Check and Save the schematic. From the schematic diagram click **– launch** > **ADE Assembler.** Select **Create New View.** Press **Ok.** An window like the following would open up.

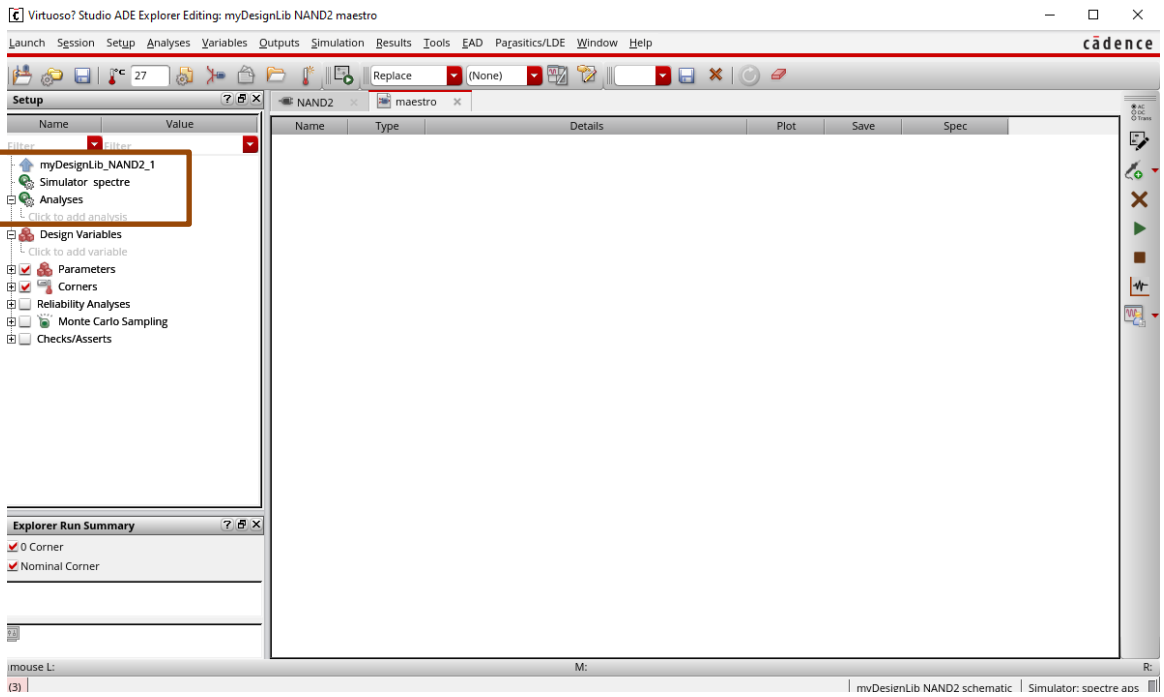


6. In the right Data View Panel, you have to see if it shows your schematics name. If your schematics name is already there, you can skip this step. If it shows only '**Tests'** like the given figure, then you have to click on the **Plus icon** beside the Tests to expand. After that click on **Click to add test.** A window will open, and you have to select your cell and click on ok.

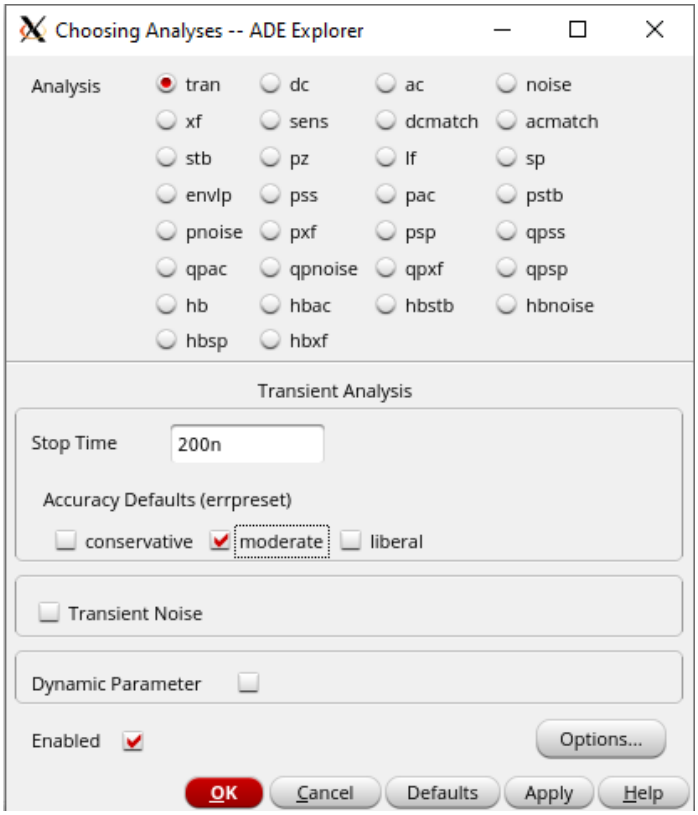




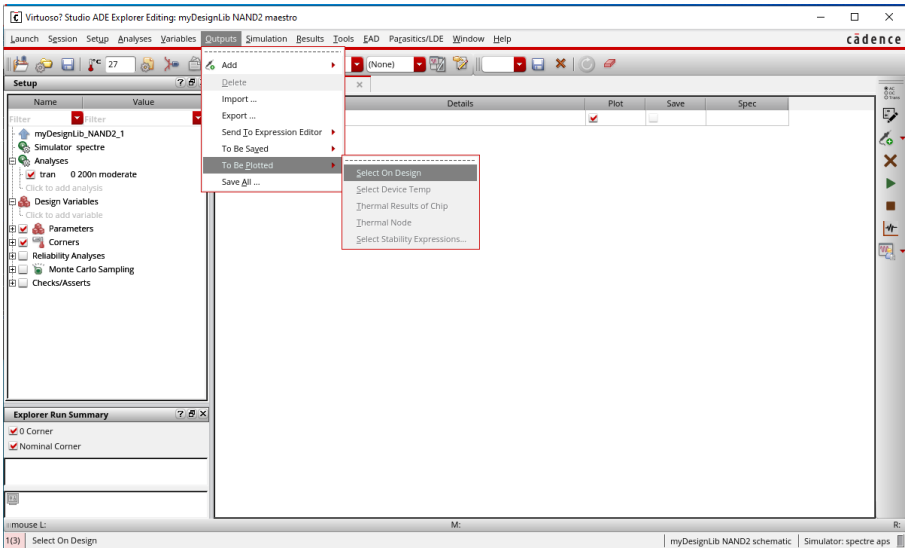
7. When the schematic cell is selected as top view, the maestro window will look like the following figure.

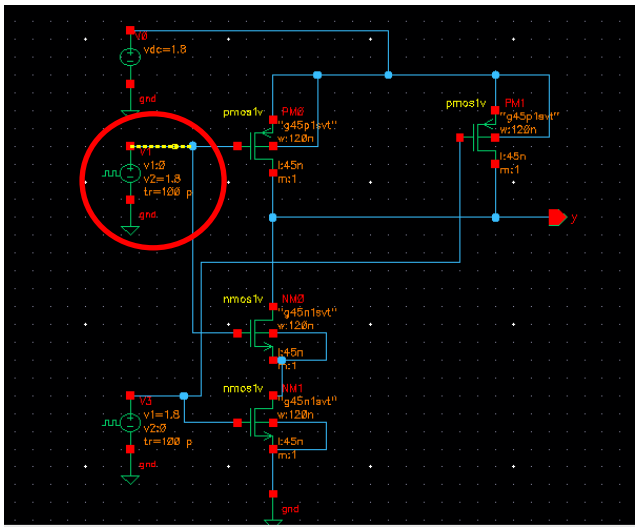


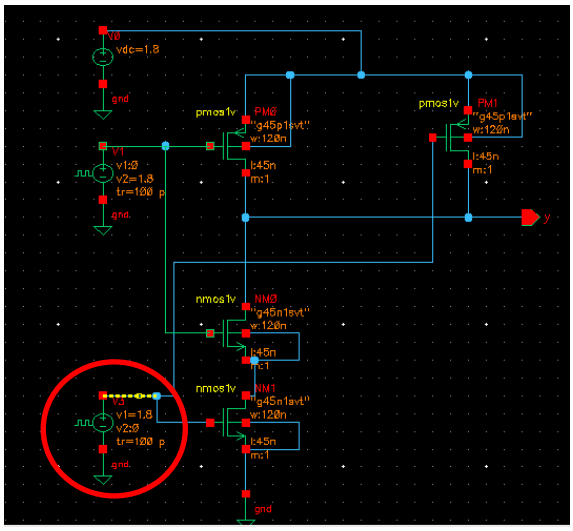
8. For transient analysis, click expand **Analyses** click on **Click to add analysis.** Select the configurations as followed.

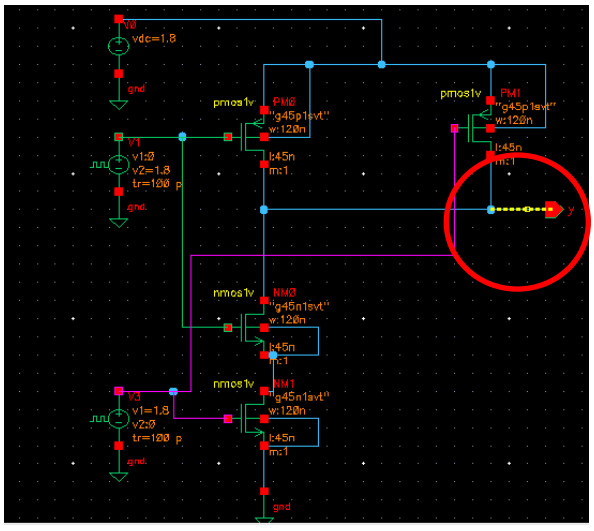


9. In this step, select the nodes voltages to be plotted. Go to **Outputs > To be plotted > Select On Design.** It will take you back to the schematic file. You have to click (single click each time) on the **input voltage nodes** and the **output voltage node.**

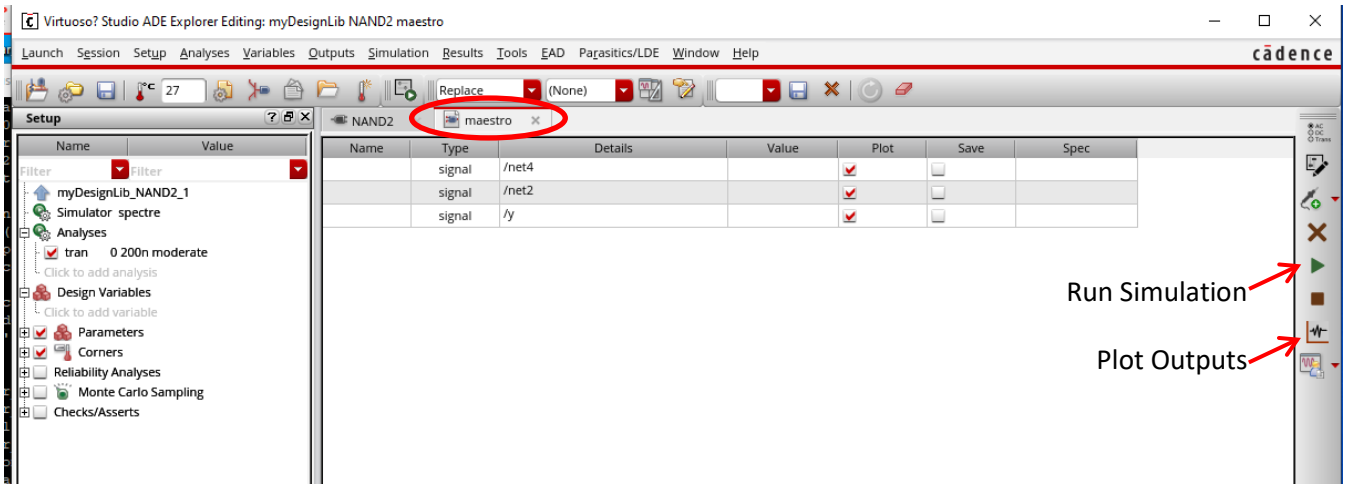




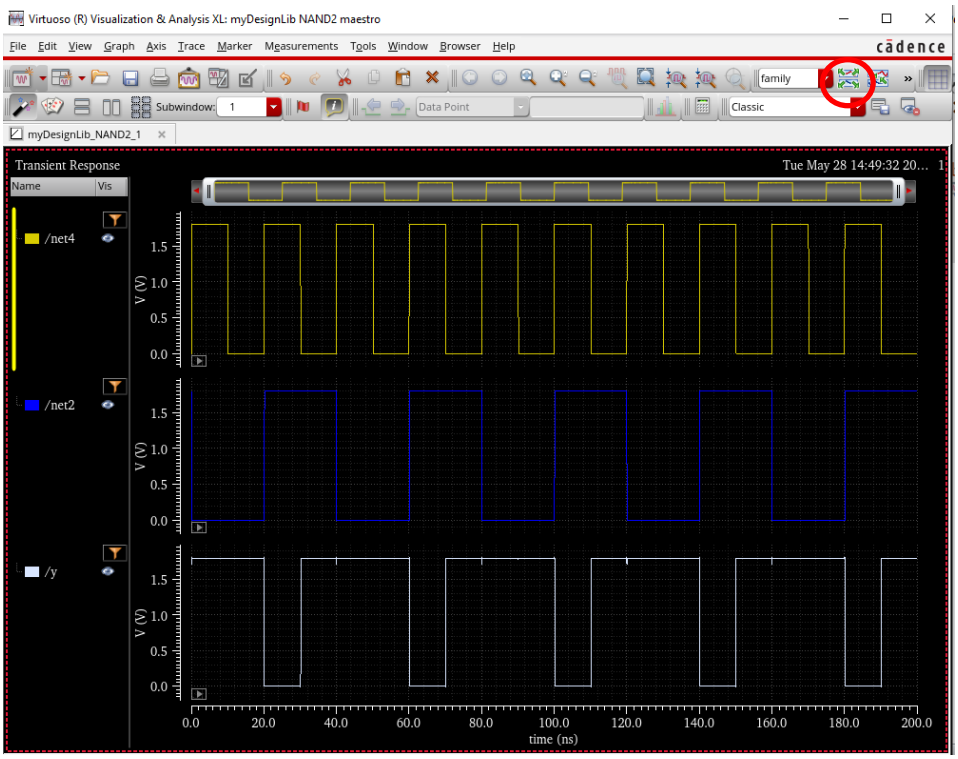




10. After the outputs have been selected, go back to the maestro window and there will be three rows in the screen. Now click on the green **Run Simulation** button from the right panel



to start simulation. A popup window will open and after successful simulation, there should be a no error report at the end. And the output plot should open up automatically. **If not**, then click on the **Plot Outputs** button from the right panel. Click on the **Split all Strips** button from the top panel to view the waves separately.



As this was a NAND gate, so you can see that at any time instant, if the inputs are both high, then the output is low. And if the inputs are both low, then the output is high.

Report Problem:

(a) Design a NAND gate and plot the transient analysis output. Include a theoretical truth table of a two input NAND gate and justify the output plot of your circuit.

(b) Design a NOR gate and plot the transient analysis output. Include a theoretical truth table of a two input NOR gate and justify the output plot of your circuit.