ASSIGNMENT

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

TESTING AND DESIGNING OF VLSI LAB

REPORT ON TRANSIENT ANALYSIS OF NAND and NOR GATES

Submitted by:

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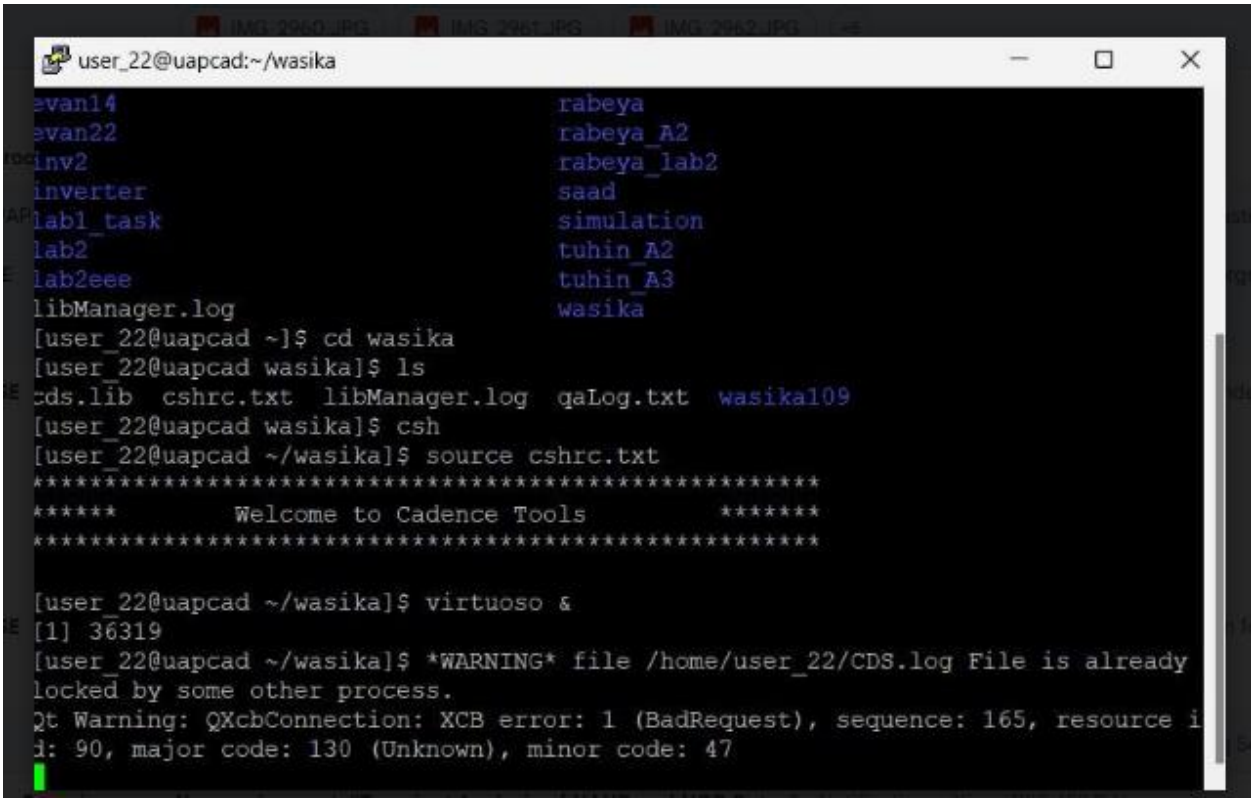
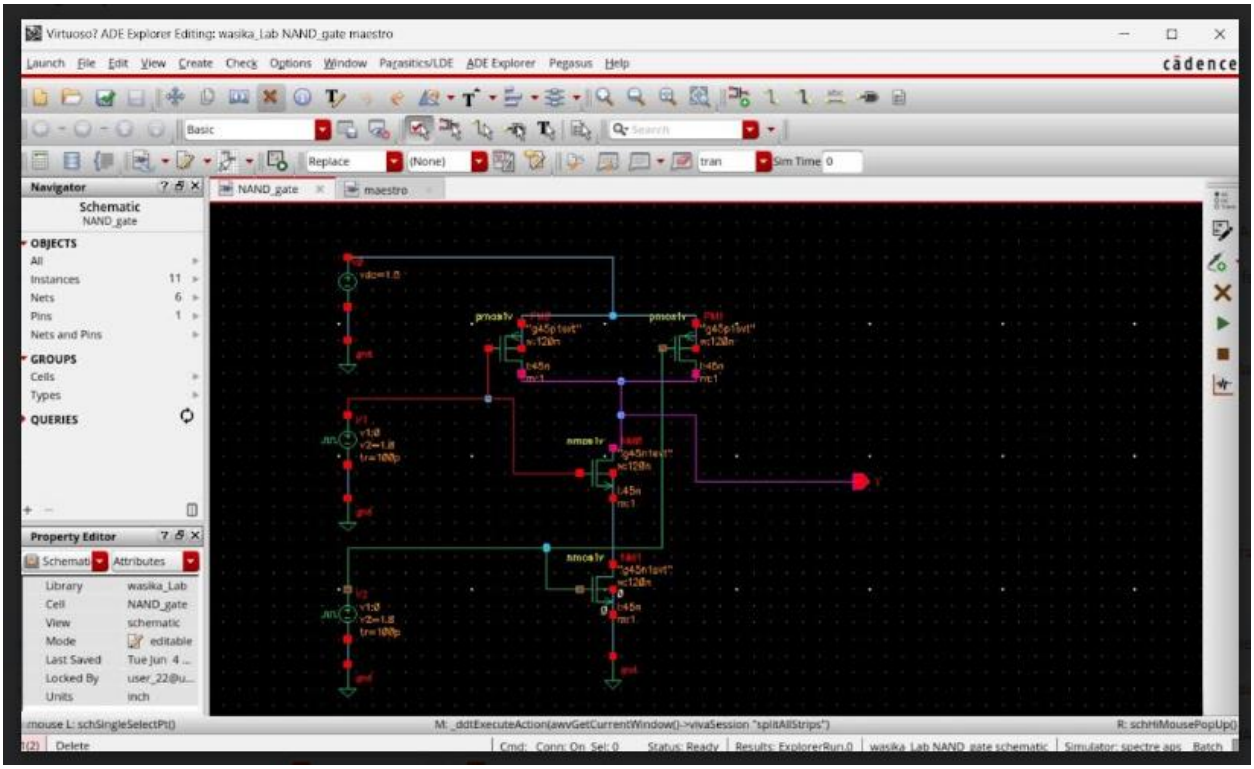
Id- 20101109

Section -B2

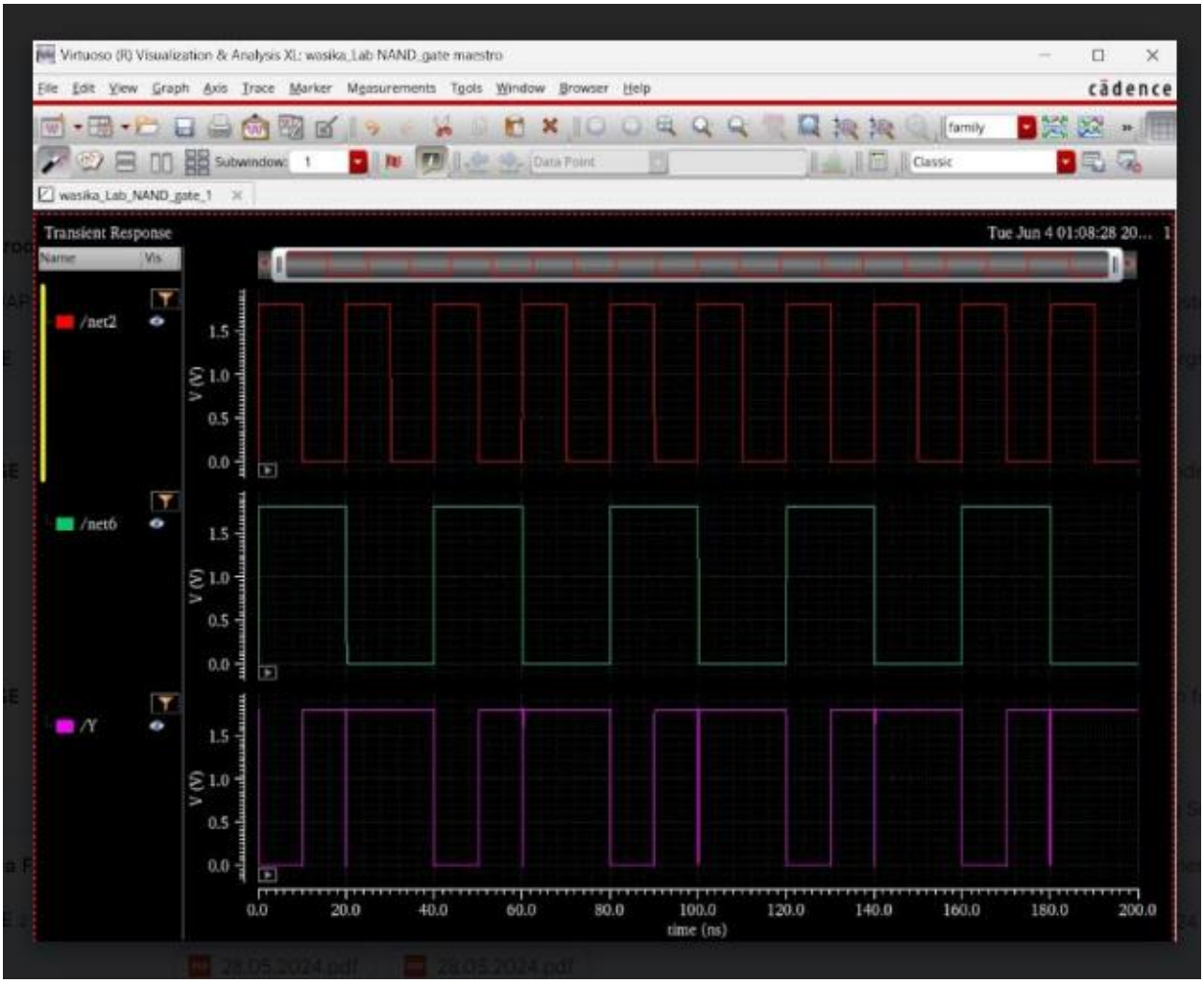
Date of submission- 4th June ,2024

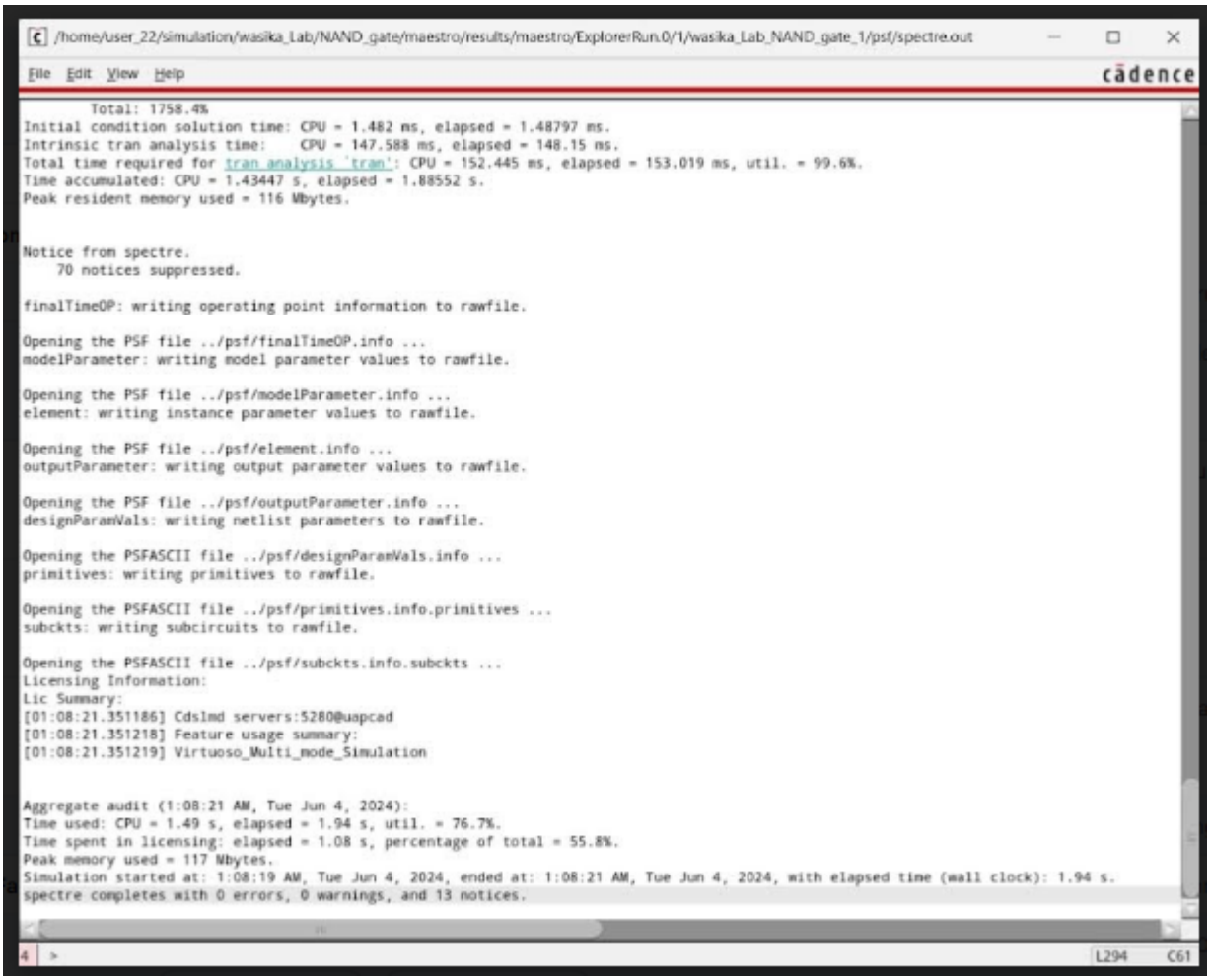


FOR NAND GATE:



Output:


Virtuoso (R) Visualization & Analysis XL: wasika_Lab NAND_gate maestro
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Subwindow: 1
wasika_Lab_NAND_gate_1
Transient Response
Tue Jun 4 01:08:28 20... 1
Name
Vis
/net2
/net6
/Y
V (V)
1.5
1.0
0.5
0.0
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0
time (ns)

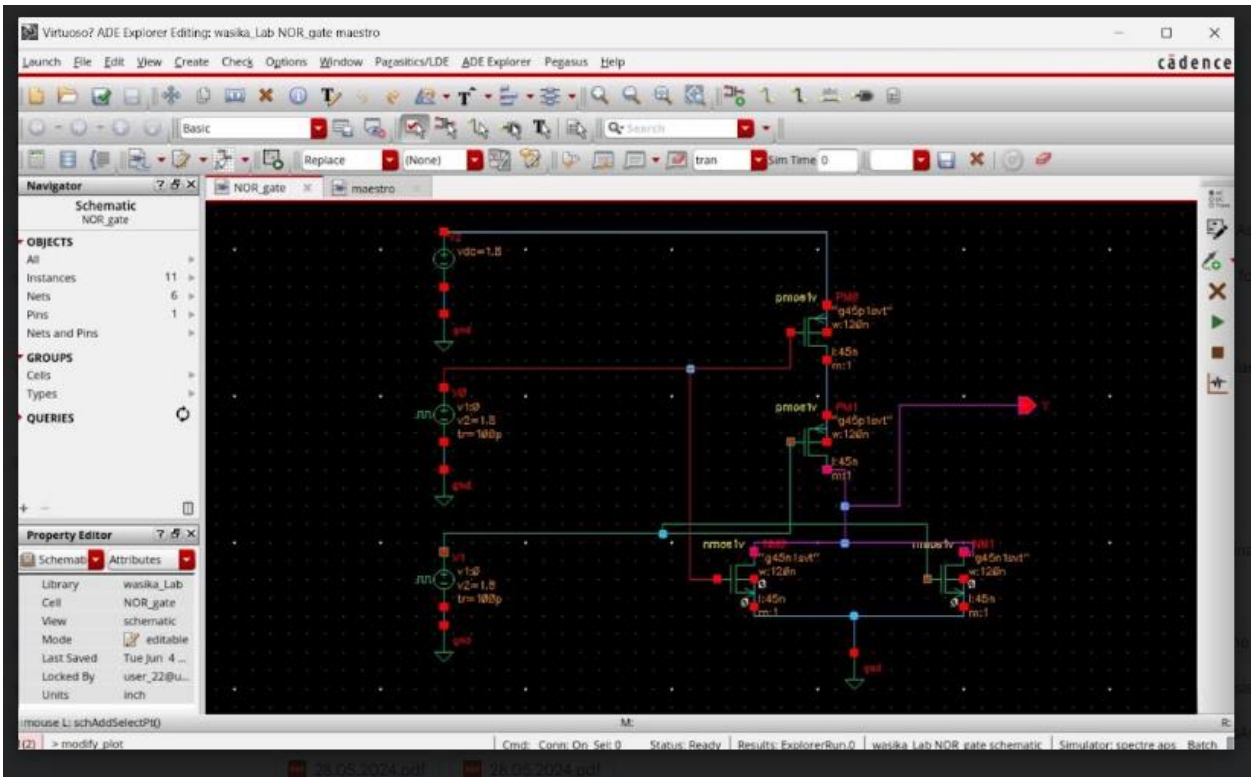

/home/user_22/simulation/wasika_Lab/NAND_gate/maestro/results/maestro/ExplorerRun.0/1/wasika_Lab_NAND_gate_1/psf/spectre.out
File Edit View Help
cadence
Total: 1758.4%
Initial condition solution time: CPU = 1.482 ms, elapsed = 1.48797 ms.
Intrinsic tran analysis time: CPU = 147.588 ms, elapsed = 148.15 ms.
Total time required for tran analysis 'tran': CPU = 152.445 ms, elapsed = 153.019 ms, util. = 99.6%.
Time accumulated: CPU = 1.43447 s, elapsed = 1.88552 s.
Peak resident memory used = 116 Mbytes.
Notice from spectre.
70 notices suppressed.
finalTimeOP: writing operating point information to rawfile.
Opening the PSF file ../psf/finalTimeOP.info ...
modelParameter: writing model parameter values to rawfile.
Opening the PSF file ../psf/modelParameter.info ...
element: writing instance parameter values to rawfile.
Opening the PSF file ../psf/element.info ...
outputParameter: writing output parameter values to rawfile.
Opening the PSF file ../psf/outputParameter.info ...
designParamVals: writing netlist parameters to rawfile.
Opening the PSFASCII file ../psf/designParamVals.info ...
primitives: writing primitives to rawfile.
Opening the PSFASCII file ../psf/primitives.info.primitives ...
subckts: writing subcircuits to rawfile.
Opening the PSFASCII file ../psf/subckts.info.subckts ...
Licensing Information:
Lic Summary:
[01:08:21.351186] Cdslmd servers:5280@uapcad
[01:08:21.351218] Feature usage summary:
[01:08:21.351219] Virtuoso_Multi_mode_Simulation
Aggregate audit (1:08:21 AM, Tue Jun 4, 2024):
Time used: CPU = 1.49 s, elapsed = 1.94 s, util. = 76.7%.
Time spent in licensing: elapsed = 1.08 s, percentage of total = 55.8%.
Peak memory used = 117 Mbytes.
Simulation started at: 1:08:19 AM, Tue Jun 4, 2024, ended at: 1:08:21 AM, Tue Jun 4, 2024, with elapsed time (wall clock): 1.94 s.
spectre completes with 0 errors, 0 warnings, and 13 notices.
L294 C61

Truth-table for NAND gate:

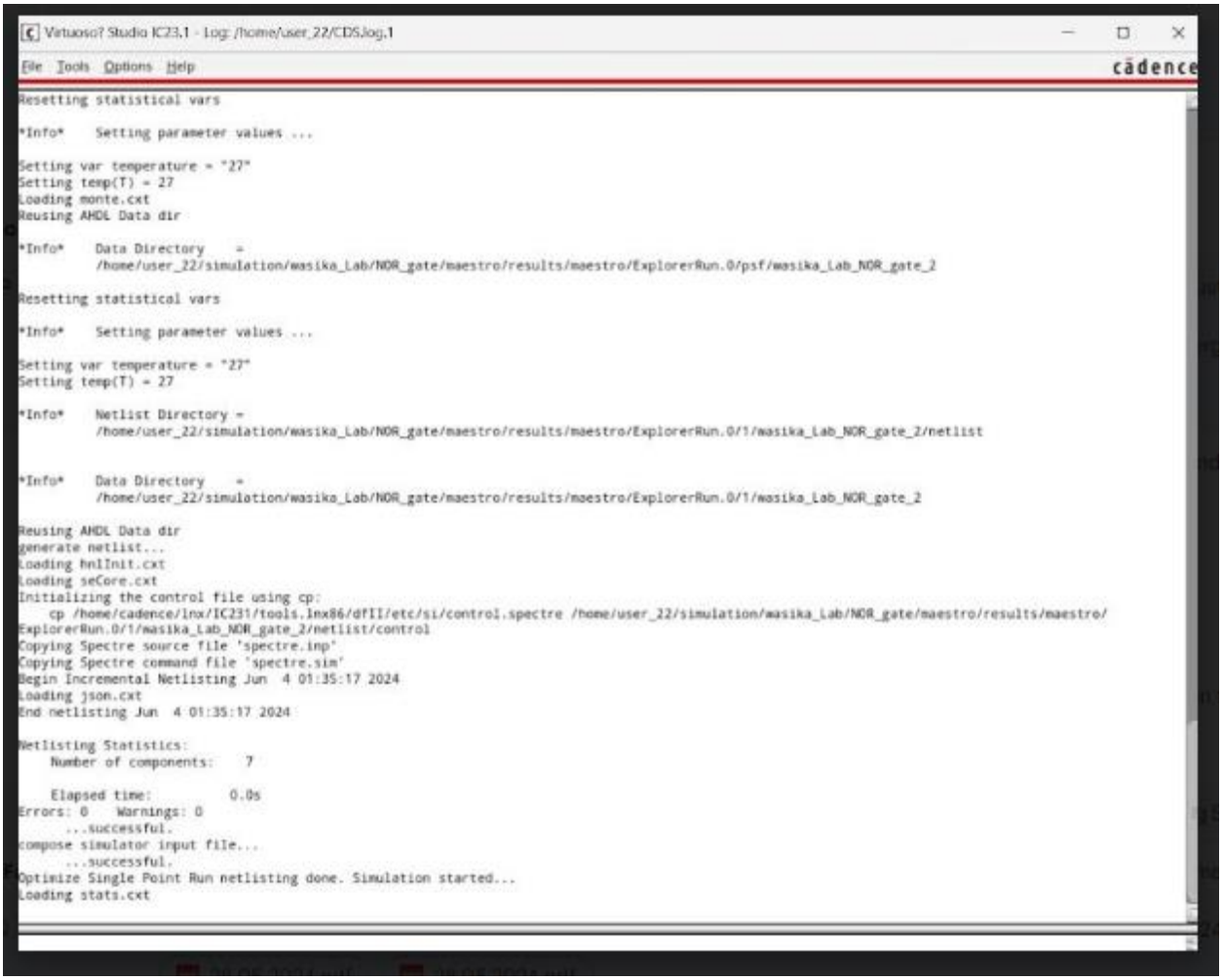
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

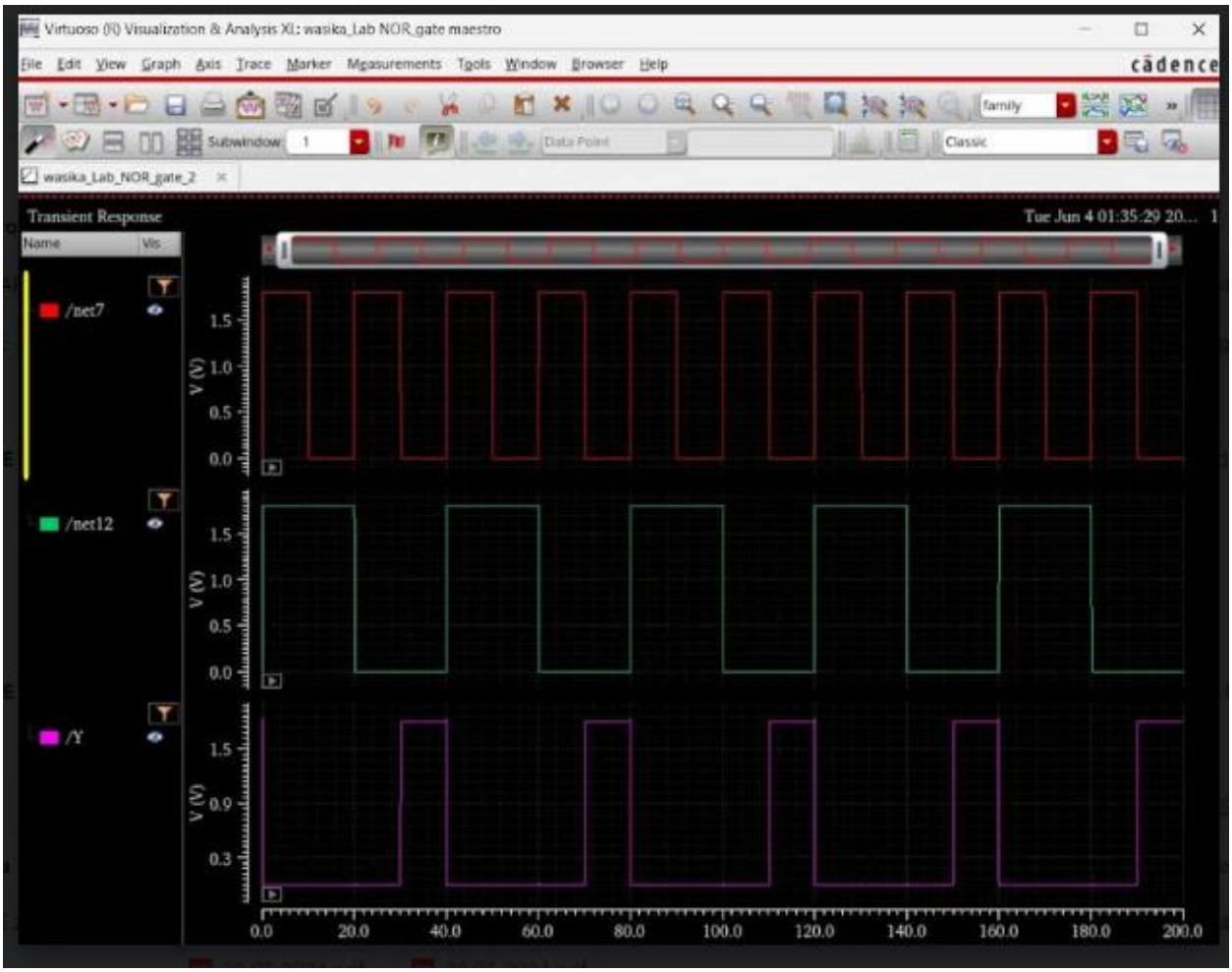
As the truth table matches without our output, we can say that there are no errors in the designing part.

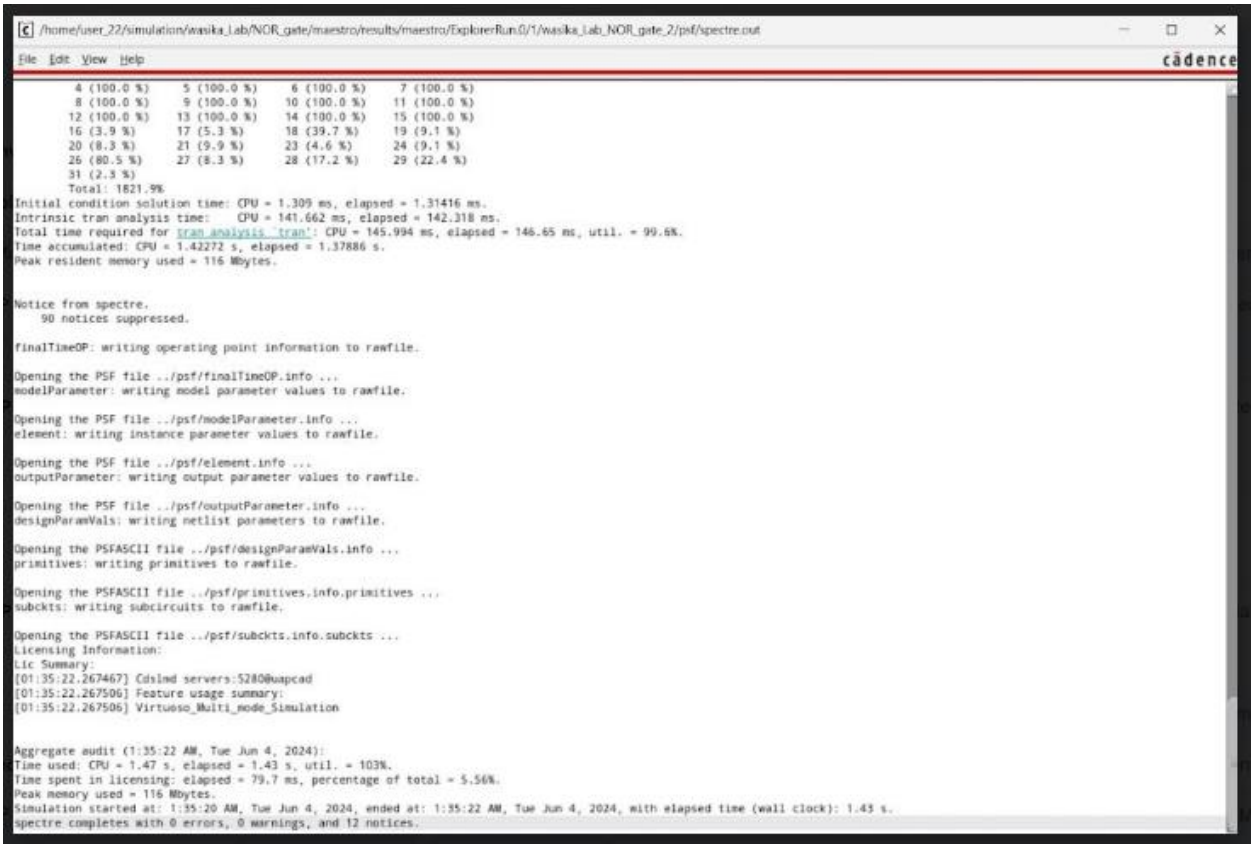
For NOR gate:


Virtuoso? ADE Explorer Editing: wasika_Lab NOR_gate maestro
Launch File Edit View Create Check Options Window Parasitics/LDE ADE Explorer Pegasus Help
cadence
Navigator
Schematic
NOR_gate
OBJECTS
All
Instances 11
Nets 6
Pins 1
Nets and Pins
GROUPS
Cells
Types
QUERIES
Property Editor
Schemati
Attributes
Library wasika_Lab
Cell NOR_gate
View schematic
Mode editable
Last Saved Tue Jun 4 ...
Locked By user_22@u...
Units inch
NOR_gate
maestro
vdc=1.8
pmos1v
nmos1v
v1=0
v2=1.8
tr=100p
gnd
Y
mouse L: schAddSelectPt()
M:
R:
> modify_plot
Cmd: Conn: On Sel: 0
Status: Ready
Results: ExplorerRun.0
wasika_Lab NOR_gate schematic
Simulator: spectre aps
Batch

Output:


Virtuoso® Studio IC23.1 - Log: /home/user_22/CDS.log.1
File Tools Options Help
cadence
Resetting statistical vars
Info Setting parameter values ...
Setting var temperature = "27"
Setting temp(T) = 27
Loading monte.cxt
Reusing AHDL Data dir
Info Data Directory =
/home/user_22/simulation/wasika_Lab/NOR_gate/maestro/results/maestro/ExplorerRun.0/psf/wasika_Lab_NOR_gate_2
Resetting statistical vars
Info Setting parameter values ...
Setting var temperature = "27"
Setting temp(T) = 27
Info Netlist Directory =
/home/user_22/simulation/wasika_Lab/NOR_gate/maestro/results/maestro/ExplorerRun.0/1/wasika_Lab_NOR_gate_2/netlist
Info Data Directory =
/home/user_22/simulation/wasika_Lab/NOR_gate/maestro/results/maestro/ExplorerRun.0/1/wasika_Lab_NOR_gate_2
Reusing AHDL Data dir
generate netlist...
Loading hnlInit.cxt
Loading seCore.cxt
Initializing the control file using cp:
cp /home/cadence/lnx/IC231/tools.lnx86/dfII/etc/si/control.spectre /home/user_22/simulation/wasika_Lab/NOR_gate/maestro/results/maestro/
ExplorerRun.0/1/wasika_Lab_NOR_gate_2/netlist/control
Copying Spectre source file 'spectre.inp'
Copying Spectre command file 'spectre.sim'
Begin Incremental Netlisting Jun 4 01:35:17 2024
Loading json.cxt
End netlisting Jun 4 01:35:17 2024
Netlisting Statistics:
Number of components: 7
Elapsed time: 0.0s
Errors: 0 Warnings: 0
...successful.
compose simulator input file...
...successful.
Optimize Single Point Run netlisting done. Simulation started...
Loading stats.cxt


Virtuoso (R) Visualization & Analysis XL: wasika_Lab NOR_gate maestro
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
wasika_Lab_NOR_gate_2
Transient Response
Tue Jun 4 01:35:29 20... 1
Name
/net7
/net12
/Y
V (V)
1.5
1.0
0.5
0.0
0.9
0.3
0.0
20.0
40.0
60.0
80.0
100.0
120.0
140.0
160.0
180.0
200.0



Truth-table:

A	B	Output
0	0	1
1	0	0
0	1	0
1	1	0

As the result of the truth table matches with the output, we can say that there is no errors in the designing part.