CSE325 Memory Manger

Assignment #5

Design and Implement a Memory Manager

Design document due: April 3,16:00
Implementation due: April 12,16:00

You are to work in groups of 2 or 3, with names of group members listed on the design document.

Functionality

You are to design a memory manager to manage the physical memory of a system, using paged memory. Your physical memory size is 1 MB and backing store size is 50MB. You do not need a page-replacement algorithm for this assignment. You will develop a design document that will consist of at least the following information:

- The high-level state diagram(s) to be implemented
- A description of each possible memory state
- The physical memory layout, logical memory limit per process
- Descriptions of the page tables and other memory manager data structures (what they are and what they are used for)
- Any design decisions you made (including things like page size, page table size, max number of page tables, etc)

Constraints on your design:

- Single-core system
- No system calls are allowed in your implementation of the memory manager
- System calls are allowed in the testing interface portion of this assignment
- Page size can be no larger than 4K Bytes

Your design must be approved before you perform the implementation. If you turn in your design early, it is likely to be approved early. Designs may not necessarily be approved as submitted and changes may be required.

Assignment Deliverables

1. Design document as defined above
2. Code implementing the design
3. Test set of commands that exercises your code
4. Captured results of your test set, annotated to show compliance with instructions.