Joyce Kwong

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Education

Ph.D. Candidate — **Massachusetts Institute of Technology** — Cambridge, MA
Electrical Engineering
Research interests: low-power and low-voltage digital design, design methodology to mitigate process variation, biomedical system applications
Advisor: Professor Anantha P. Chandrakasan
Expected graduation: Spring 2010

M.S. — **Massachusetts Institute of Technology** — Cambridge, MA
Electrical Engineering, June 2006
Thesis title: A Sub-threshold Library and Methodology
Advisor: Professor Anantha P. Chandrakasan

B.A.Sc. — **University of Waterloo** — Waterloo, Canada
Computer Engineering, June 2004
Received Governor General's Medal for highest standing in B.A.Sc. program

Research Experience

MIT
Department of Electrical Engineering and Computer Science

Research Assistant — June 2006-present

- Current research activities: design of a 0.5V-1.0V biomedical DSP featuring custom FIR and FFT accelerators and a voltage-scalable SRAM.
- Implemented and tested a 65nm sub-threshold microcontroller based on the MSP430 instruction set. Silicon demonstrated functionality down to 0.3V. Published work resulted in outstanding student paper award at ISSCC.
- Responsible for microcontroller logic design, timing closure, place and route, and system integration with SRAM and DC-DC converter. Part of a 3-person graduate research team.

MIT
Department of Electrical Engineering and Computer Science

Research Assistant — Sept. 2004-June 2006

- Designed sub-threshold standard cell library in 65nm CMOS, developing sizing strategies to achieve robust circuit operation. Silicon demonstrated operation down to 0.3V.
- Designed digital filter with built-in error correction capability as a demonstration of error resilient architectures for sub-threshold logic.

University of Waterloo
Department of Electrical and Computer Engineering

Undergraduate Research Assistant — Jan. 2001-Apr. 2004

- Created MATLAB simulations to validate theoretical results in electromagnetic plane wave scattering.

Internship Experience

Dallas, TX — **Texas Instruments** — July-Aug. 2008
- Defined architecture of a voltage-scalable DSP for biomedical applications.
- Designed custom hardware blocks for signal processing.

Freising, Germany — **Texas Instruments** — June-Aug. 2006
- Implemented MSP430 microcontroller including a new memory interface in 65nm CMOS. Fabricated chip achieved 50MHz at 1.2V.
- Characterized power breakdown of microcontroller to find opportunities for further improvement.

Santa Clara, CA — **NVIDIA** — June-Aug. 2004, Sept.-Dec. 2002, Sept.-Dec. 2003, Jan.-Apr. 2002
- Performed design and verification of frame-buffer interface module in Graphics Processing Unit (GPU).
- Performed silicon characterization of GPU interface to external memory.

Toronto, Canada — **ViXS Systems** — May-Aug. 2001
- Created C models and Verilog PLI application for verification of an MPEG video processor.

Toronto, Canada — **Nortel Networks** — Sept.-Dec. 2000, Jan.-Apr. 2000
- Performed laboratory verification and debugging of embedded voicemail systems.

Teaching Experience

MIT — Department of Electrical Engineering and Computer Science — Fall 2007
- Teaching Assistant for 6.374, Analysis and Design of Digital Integrated Circuits.
- Held office hours, created problem sets, assisted with student design projects, performed grading and course administration.
- Rated 6.7/7.0 by students.

Skills

- Digital ASIC, SRAM, and system design
- Cadence Integrated Circuit Design Suite, Cadence AMS, Synopsys Design Compiler, Astro, Primetime, Nanosim, HSPICE, Liberty NCX, Magma Talus, MATLAB, P-CAD
- Verilog, VHDL, Perl, SKILL, Tcl, C, C++
- Fluent in English and Cantonese; some knowledge of French

Publications

J. Kwong, Y. K. Ramadass, N. Verma, A. P. Chandrakasan, "A 65nm Sub-V_t Microcontroller with Integrated SRAM and Switched-Capacitor DC-DC Converter," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 115-126, Jan. 2009.

J. Kwong, A. P. Chandrakasan, "Advances in Ultra-Low-Voltage Design," *IEEE Solid-State Circuits Newsletter*, vol. 13, no. 4, pp. 20-27, Fall 2008.

A. P. Chandrakasan, D. C. Daly, J. Kwong, Y. K. Ramadass, “Next Generation Micro-Power Systems,” *IEEE Symposium on VLSI Circuits*, pp. 2-5, June 2008.

J. Kwong, Y. K. Ramadass, N. Verma, M. Koesler, K. Huber, H. Moormann, A. Chandrakasan, “A 65nm Sub-V_t Microcontroller with Integrated SRAM and Switched-Capacitor DC-DC Converter,” *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 318-319, Feb. 2008.

N. Verma, J. Kwong, A. Chandrakasan, "Nanometer MOSFET Variation in Minimum Energy Subthreshold Circuits,” *IEEE Transactions on Electron Devices*, pp. 163-174, Jan. 2008.

Y. K. Ramadass, J. Kwong, N. Verma, A. P. Chandrakasan, “Adaptive Supply Voltage Delivery for Ultra-Dynamic Voltage Scaled Systems,” in *Adaptive Techniques for Dynamic Processor Optimization*, Alice Wang, Samuel Naffziger, Eds. New York, NY: Springer, 2008, pp. 95-122.

A. Wang, B. H. Calhoun, N. Verma, J. Kwong, A. Chandrakasan, "Ultra-Dynamic Voltage Scaling for Energy Starved Electronics," *Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, pp. 451-454, Mar. 2007.

J. Kwong, A. P. Chandrakasan, "Variation-Driven Device Sizing for Minimum Energy Sub-threshold Circuits," *International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 8-13, Oct. 2006.

A. P. Chandrakasan, N. Verma, J. Kwong, D. Daly, N. Ickes, D. Finchelstein, B. Calhoun, "Micropower Wireless Sensors," Presented at *NSTI Nanotech*, May 7-11, 2006, vol. 3, pp. 459-462.

J. Kwong, A. Wang, B. H. Calhoun, A. P. Chandrakasan, “Logic Families in Sub-threshold” in *Sub-threshold Design for Ultra-Low Power Systems*, Alice Wang, Benton Highsmith Calhoun, Anantha P. Chandrakasan, New York, NY: Springer, 2006, pp. 92-102.

R. H. MacPhie, K. L. Wu, J. Kwong, “Scattering of a Plane Wave by a Perfectly Conducting Cube,” *IEEE AP-S International Symposium and USNC/URSI National Radio Science Meeting*, June 2002.

Awards/Activities

- Co-recipient of the ISSCC 2008 Jack Kilby Award for Outstanding Student Paper
- TI Graduate Woman’s Fellowship for Leadership in Microelectronics (2007-2008)
- NSERC Doctoral Postgraduate Scholarship (2007-2009)
- Best Presentation Award at MTL Annual Research Conference (2009)
- Governor General’s Medal (2004)

- Co-president of MIT Graduate Women of Course 6 (2005)
- MIT Intercollegiate badminton (2009)