Lab Practical - 04

Aim :

To implement RTL NAND and NOR using B=50, R1 = 2k, Rc = 4k, R2 = 20k. Verify the results by transient analysis.

Software : ngspice

Theory :

Resistor-transistor logic (RTL) is a class of digital circuits that uses resistors in combination with bipolar junction transistors (BJTs) to implement logic gates. The basic building block of RTL is the bipolar junction transistor, which can be used in two different modes: the common-emitter (CE) mode and the common-base (CB) mode.

In the CE mode, the input to the circuit is applied to the transistor's base terminal, and the output is taken from the collector terminal. This mode is commonly used in digital circuits because it provides a high voltage gain and a low input impedance. In the CB mode, the input is applied to the collector terminal and the output is taken from the base terminal. This mode is used in analog circuits because it provides a low voltage gain and a high input impedance.

When the inputs of the NAND gate are high, the base-emitter voltage of the NPN transistor will be forward-biased, allowing a large current to flow through the collector-emitter circuit. This will cause the output voltage to be close to the negative power supply voltage. When either input is low, the base-emitter voltage will be reverse-biased, preventing current from flowing through the collector-emitter circuit, and the output voltage will be close to the positive power supply voltage. A RTL NOR gate can be implemented similarly.

To verify the results of the circuit we can use Transient Analysis, this method allows you to simulate the circuit over a certain period of time with different input values and check the output voltage response.

This method can be used to check the circuit's performance in different conditions and see if it meets the design specifications.

Circuit :

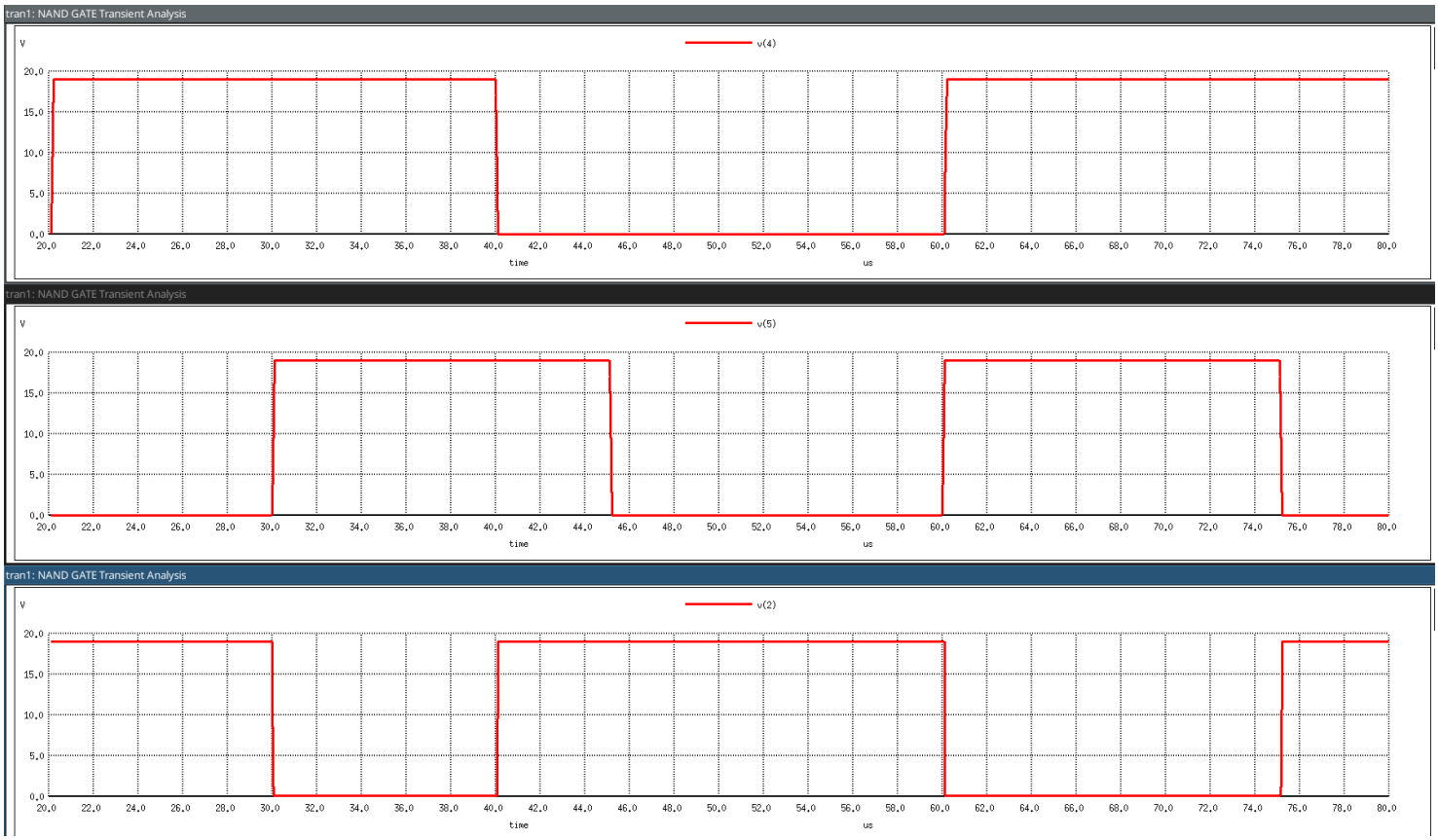
Code and Output :

NAND GATE

```
.title NAND GATE Transient Analysis
.model BJT NPN (Bf=50)
Vc 1 0 dc 19
V1 4 0 pulse (19 0 0 0.1u 0.1u 20u 40u)
V2 5 0 pulse (0 19 0 0.1u 0.1u 15u 30u)
Rc 2 1 4k
R1 4 3 2k
R2 5 6 20k
Q1 2 3 7 BJT
Q2 7 6 0 BJT

* Simulation
.tran 10u 80u 20u

* Control Statements
.control
run
set color0=white
set xbrushwidth=3.5
plot V(4)
plot V(2)
plot V(5)
.endc
.end
```



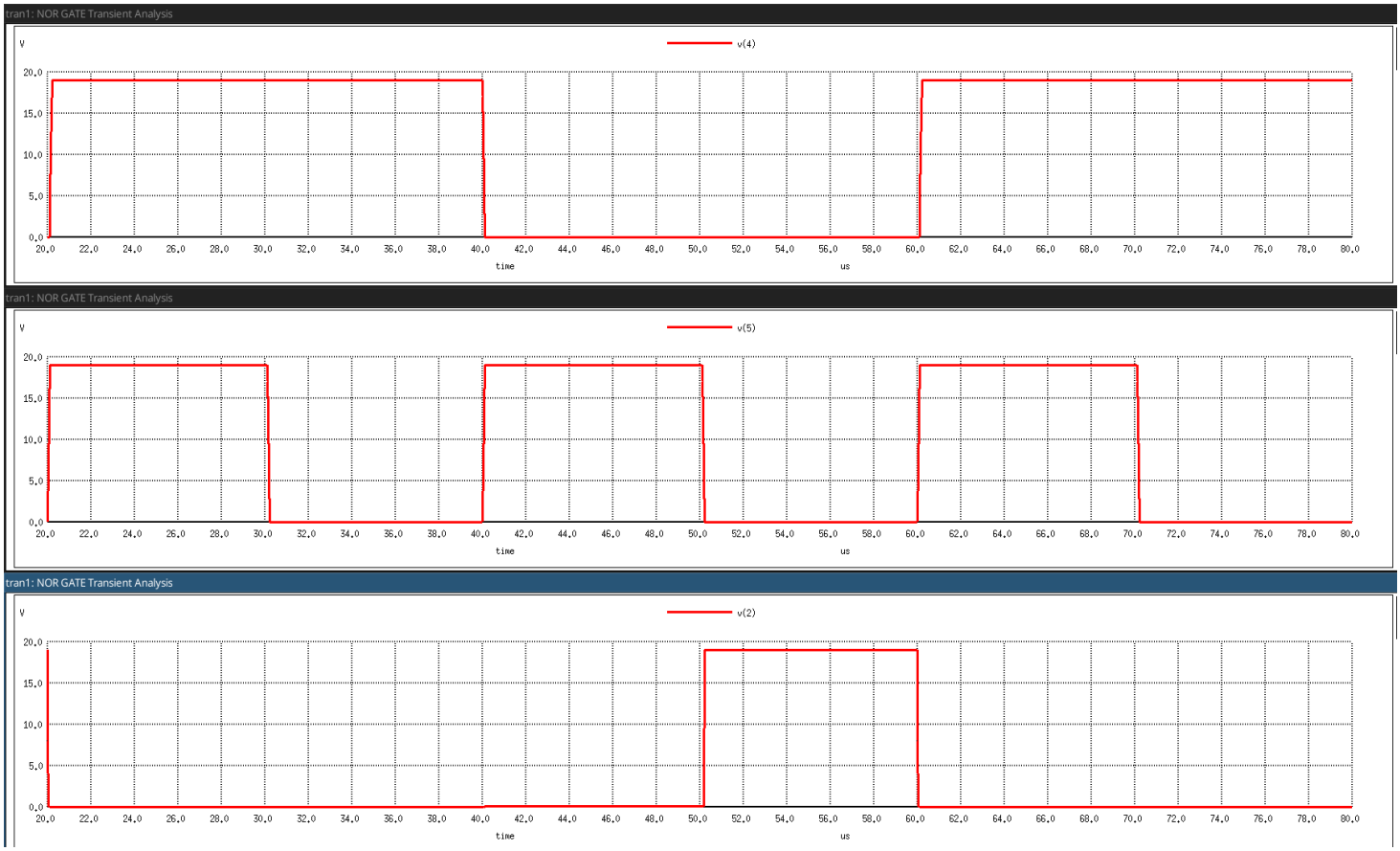
NOR GATE

```
.title NOR GATE Transient Analysis
.model BJT NPN (Bf=50)
Vc 1 0 dc 19
V1 4 0 pulse (19 0 0 0.1u 0.1u 20u 40u)
V2 5 0 pulse (0 19 0 0.1u 0.1u 10u 20u)
Rc 2 1 4k
R1 4 3 2k
R2 5 6 20k
Q1 2 3 0 BJT
Q2 2 6 0 BJT

* Simulation
.tran 10u 80u 20u

* Control Statements
```

```
.control
run
set color0=white
set xbrushwidth=3.5
plot V(4)
plot V(2)
plot V(5)
.endc
.end
```



Conclusion :