

Symbol	Description	Min.	Typ.	Max.	Units
$t_{\text{TWIS,SU_STO},400\text{kbps}}$	TWI slave setup time from SCL high to STOP condition, 400 kbps	1300			ns
$t_{\text{TWIS,BUF},100\text{kbps}}$	TWI slave bus free time between STOP and START conditions, 100 kbps		4700		ns
$t_{\text{TWIS,BUF},400\text{kbps}}$	TWI slave bus free time between STOP and START conditions, 400 kbps		1300		ns

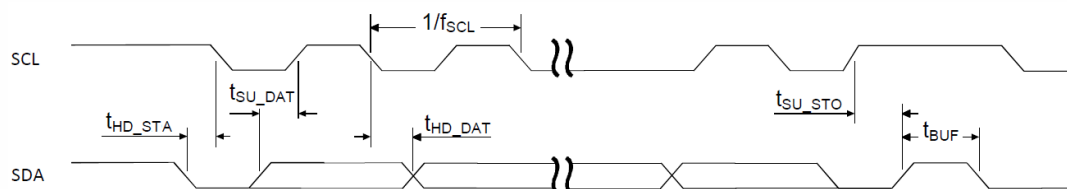


Figure 187: TWIS timing diagram, 1 byte transaction

6.33 UART — Universal asynchronous receiver/transmitter

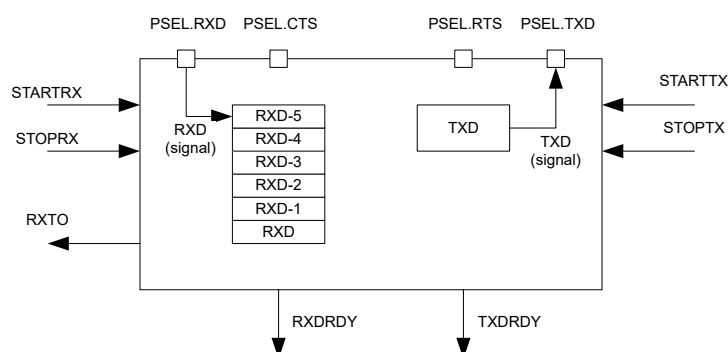


Figure 188: UART configuration

6.33.1 Functional description

Listed here are the main features of UART.

The UART implements support for the following features:

- Full-duplex operation
- Automatic flow control
- Parity checking and generation for the 9th data bit

As illustrated in [UART configuration](#) on page 502, the UART uses the TXD and RXD registers directly to transmit and receive data. The UART uses one stop bit.

Note: The external crystal oscillator must be enabled to obtain sufficient clock accuracy for stable communication. See [CLOCK — Clock control](#) on page 85 for more information.

6.33.2 Pin configuration

The different signals RXD, CTS (Clear To Send, active low), RTS (Request To Send, active low), and TXD associated with the UART are mapped to physical pins according to the configuration specified in the PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers respectively.

If the CONNECT field of a PSEL.xxx register is set to Disconnected, the associated UART signal will not be connected to any physical pin. The PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD registers and their configurations are only used as long as the UART is enabled, and retained only for the duration the device is in ON mode. PSEL.RXD, PSEL.CTS, PSEL.RTS, and PSEL.TXD must only be configured when the UART is disabled.

To secure correct signal levels on the pins by the UART when the system is in OFF mode, the pins must be configured in the GPIO peripheral as described in [Pin configuration](#) on page 503.

Only one peripheral can be assigned to drive a particular GPIO pin at a time. Failing to do so may result in unpredictable behavior.

UART pin	Direction	Output value
RXD	Input	Not applicable
CTS	Input	Not applicable
RTS	Output	1
TXD	Output	1

Table 132: GPIO configuration

6.33.3 Shared resources

The UART shares registers and resources with other peripherals that have the same ID as the UART.

All peripherals with the same ID as the UART must be disabled before configuring and using the UART. Disabling a peripheral that has the same ID as the UART will not reset any of the registers that are shared with the UART. It is therefore important to configure all relevant UART registers explicitly to ensure that it operates correctly.

See [Instantiation](#) on page 23 for details on peripherals and their IDs.

6.33.4 Transmission

A UART transmission sequence is started by triggering the STARTTX task.

Bytes are transmitted by writing to the TXD register. When a byte has been successfully transmitted, the UART will generate a TXDRDY event after which a new byte can be written to the TXD register. A UART transmission sequence is stopped immediately by triggering the STOPTH task.

If flow control is enabled, a transmission will be automatically suspended when CTS is deactivated, and resumed when CTS is activated again, as shown in the following figure. A byte that is in transmission when CTS is deactivated will be fully transmitted before the transmission is suspended. For more information, see [Suspending the UART](#) on page 505.

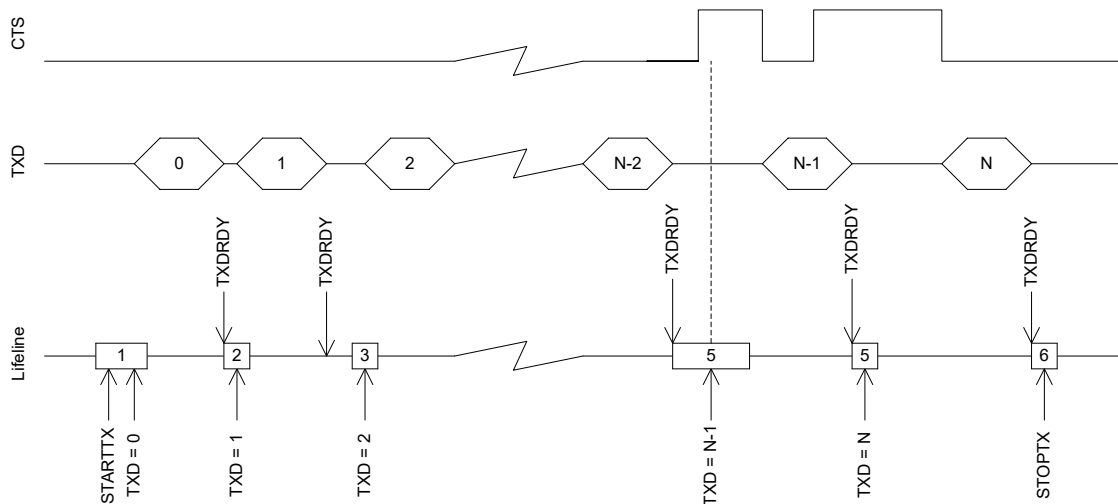


Figure 189: UART transmission

6.33.5 Reception

A UART reception sequence is started by triggering the STARTRX task.

The UART receiver chain implements a FIFO capable of storing six incoming RXD bytes before data is overwritten. Bytes are extracted from this FIFO by reading the RXD register. When a byte is extracted from the FIFO, a new byte pending in the FIFO will be moved to the RXD register. The UART will generate an RXDRDY event every time a new byte is moved to the RXD register.

When flow control is enabled, the UART will deactivate the RTS signal when there is only space for four more bytes in the receiver FIFO. The counterpart transmitter is therefore able to send up to four bytes after the RTS signal is deactivated before data is being overwritten. To prevent overwriting data in the FIFO, the counterpart UART transmitter must therefore make sure to stop transmitting data within four bytes after the RTS line is deactivated.

The RTS signal will first be activated again when the FIFO has been emptied, that is, when all bytes in the FIFO have been read by the CPU, see [UART reception](#) on page 505.

The RTS signal will also be deactivated when the receiver is stopped through the STOPRX task as illustrated in [UART reception](#) on page 505. The UART is able to receive four to five additional bytes if they are sent in succession immediately after the RTS signal has been deactivated. This is possible because the UART is, even after the STOPRX task is triggered, able to receive bytes for an extended period of time dependent on the configured baud rate. The UART will generate a receiver timeout event (RXTO) when this period has elapsed.

To prevent loss of incoming data, the RXD register must only be read one time following every RXDRDY event.

To secure that the CPU can detect all incoming RXDRDY events through the RXDRDY event register, the RXDRDY event register must be cleared before the RXD register is read. The reason for this is that the UART is allowed to write a new byte to the RXD register, and can generate a new event immediately after the RXD register is read (emptied) by the CPU.

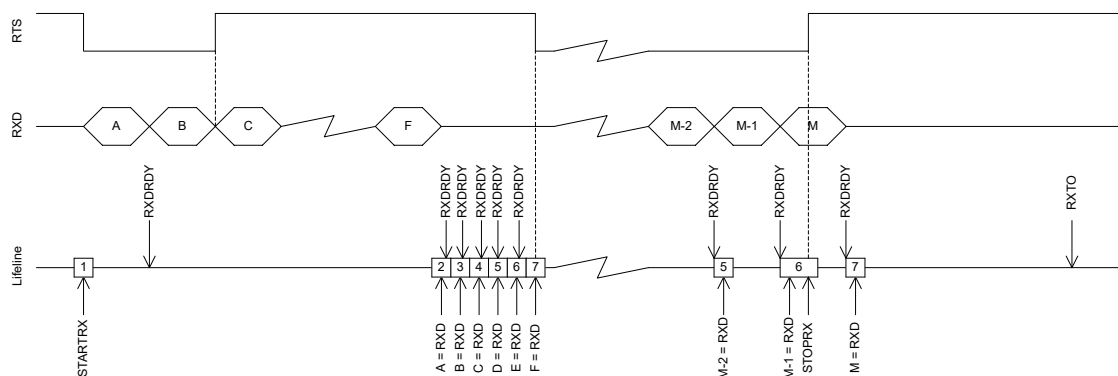


Figure 190: UART reception

As indicated in occurrence 2 in the figure, the RXDRDY event associated with byte B is generated first after byte A has been extracted from RXD.

6.33.6 Suspending the UART

The UART can be suspended by triggering the SUSPEND task.

SUSPEND will affect both the UART receiver and the UART transmitter, i.e. the transmitter will stop transmitting and the receiver will stop receiving. UART transmission and reception can be resumed, after being suspended, by triggering STARTTX and STARTRX respectively.

Following a SUSPEND task, an ongoing TXD byte transmission will be completed before the UART is suspended.

When the SUSPEND task is triggered, the UART receiver will behave in the same way as it does when the STOPRX task is triggered.

6.33.7 Error conditions

An ERROR event, in the form of a framing error, will be generated if a valid stop bit is not detected in a frame. Another ERROR event, in the form of a break condition, will be generated if the RXD line is held active low for longer than the length of a data frame. Effectively, a framing error is always generated before a break condition occurs.

6.33.8 Using the UART without flow control

If flow control is not enabled, the interface will behave as if the CTS and RTS lines are kept active all the time.

6.33.9 Parity and stop bit configuration

Automatic even parity generation for both transmission and reception can be configured using the register **CONFIG** on page 514. See the register description for details.

The amount of stop bits can also be configured through the register **CONFIG** on page 514.

6.33.10 Registers

Base address	Peripheral	Instance	Description	Configuration
0x40002000	UART	UART0	Universal asynchronous receiver/transmitter	Deprecated

Table 133: Instances

Register	Offset	Description
TASKS_STARTRX	0x000	Start UART receiver
TASKS_STOPRX	0x004	Stop UART receiver
TASKS_STARTTX	0x008	Start UART transmitter
TASKS_STOPTX	0x00C	Stop UART transmitter
TASKS_SUSPEND	0x01C	Suspend UART
EVENTS_CTS	0x100	CTS is activated (set low). Clear To Send.
EVENTS_NCTS	0x104	CTS is deactivated (set high). Not Clear To Send.
EVENTS_RXDRDY	0x108	Data received in RXD
EVENTS_TXDRDY	0x11C	Data sent from TXD
EVENTS_ERROR	0x124	Error detected
EVENTS_RXT0	0x144	Receiver timeout
SHORTS	0x200	Shortcuts between local events and tasks
INTENSET	0x304	Enable interrupt
INTENCLR	0x308	Disable interrupt
ERRORSRC	0x480	Error source
ENABLE	0x500	Enable UART
PSEL.RTS	0x508	Pin select for RTS
PSEL.TXD	0x50C	Pin select for TXD
PSEL.CTS	0x510	Pin select for CTS
PSEL.RXD	0x514	Pin select for RXD
RXD	0x518	RXD register
TXD	0x51C	TXD register
BAUDRATE	0x524	Baud rate. Accuracy depends on the HFCLK source selected.
CONFIG	0x56C	Configuration of parity and hardware flow control

Table 134: Register overview

6.33.10.1 TASKS_STARTRX

Address offset: 0x000

Start UART receiver

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID		A																																	
Reset 0x00000000		0 0																																	
ID	Acce Field	Value ID	Value	Description																															
A	W	TASKS_STARTRX		Start UART receiver																															
			Trigger	1	Trigger task																														

6.33.10.2 TASKS_STOPRX

Address offset: 0x004

Stop UART receiver

Bit number		31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																	
ID		A																																	
Reset 0x00000000		0 0																																	
ID	Acce Field	Value ID	Value	Description																															
A	W	TASKS_STOPRX		Stop UART receiver																															
			Trigger	1	Trigger task																														

6.33.10.3 TASKS_STARTTX

Address offset: 0x008

Start UART transmitter

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				A																															
Reset 0x00000000				0 0																															
ID	Acce Field	Value ID	Value	Description																															
A	W TASKS_STARTTX			Start UART transmitter																															
		Trigger	1	Trigger task																															

6.33.10.4 TASKS_STOPTX

Address offset: 0x00C

Stop UART transmitter

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				A																															
Reset 0x00000000				0 0																															
ID	Acce Field	Value ID	Value	Description																															
A	W TASKS_STOPTX			Stop UART transmitter																															
		Trigger	1	Trigger task																															

6.33.10.5 TASKS_SUSPEND

Address offset: 0x01C

Suspend UART

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			A																															
Reset 0x00000000			0 0																															
ID	Acce Field	Value ID	Value	Description																														
A	W TASKS_SUSPEND			Suspend UART																														
		Trigger	1	Trigger task																														

6.33.10.6 EVENTS_CTS

Address offset: 0x100

CTS is activated (set low). Clear To Send.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			A																															
Reset 0x00000000			0 0																															
ID	Acce Field	Value ID	Value	Description																														
A	RW EVENTS_CTS			CTS is activated (set low). Clear To Send.																														
		NotGenerated	0	Event not generated																														
		Generated	1	Event generated																														

6.33.10.7 EVENTS_NCTS

Address offset: 0x104

CTS is deactivated (set high). Not Clear To Send.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			A																															
Reset 0x00000000			0 0																															
ID	Acce Field	Value ID	Value	Description																														
A	RW EVENTS_NCTS			CTS is deactivated (set high). Not Clear To Send.																														
		NotGenerated	0	Event not generated																														
		Generated	1	Event generated																														

6.33.10.8 EVENTS_RXDRDY

Address offset: 0x108

Data received in RXD

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			A																															
Reset 0x00000000			0 0																															
ID	Acce Field	Value ID	Value	Description																														
A	RW EVENTS_RXDRDY			Data received in RXD																														
		NotGenerated	0	Event not generated																														
		Generated	1	Event generated																														

6.33.10.9 EVENTS_TXDRDY

Address offset: 0x11C

Data sent from TXD

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			A																															
Reset 0x00000000			0 0																															
ID	Acce Field	Value ID	Value	Description																														
A	RW EVENTS_TXDRDY			Data sent from TXD																														
		NotGenerated	0	Event not generated																														
		Generated	1	Event generated																														

6.33.10.10 EVENTS_ERROR

Address offset: 0x124

Error detected

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			A																															
Reset 0x00000000			0 0																															
ID	Acce Field	Value ID	Value	Description																														
A	RW EVENTS_ERROR			Error detected																														
		NotGenerated	0	Event not generated																														
		Generated	1	Event generated																														

6.33.10.11 EVENTS_RXT0

Address offset: 0x144

Receiver timeout

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			A																															
Reset 0x00000000			0 0																															
ID	Acce Field	Value ID	Value	Description																														
A	RW	EVENTS_RXT0		Receiver timeout																														
		NotGenerated	0	Event not generated																														
		Generated	1	Event generated																														

6.33.10.12 SHORTS

Address offset: 0x200

Shortcuts between local events and tasks

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			B A																															
Reset 0x00000000			0 0																															
ID	Acce	Field	Value	ID	Value	Description																												
A	RW	CTS_STARTRX				Shortcut between event CTS and task STARTRX																												
			Disabled	0	Disable shortcut																													
			Enabled	1	Enable shortcut																													
B	RW	NCTS_STOPRX				Shortcut between event NCTS and task STOPRX																												
			Disabled	0	Disable shortcut																													
			Enabled	1	Enable shortcut																													

6.33.10.13 INTENSET

Address offset: 0x304

Enable interrupt

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			F																E		D		C		B		A							
Reset 0x00000000			0 0																															
ID	Acce	Field	Value	ID	Value	Description																												
A	RW	CTS				Write '1' to enable interrupt for event CTS																												
			Set	1	Enable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
B	RW	NCTS				Write '1' to enable interrupt for event NCTS																												
			Set	1	Enable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
C	RW	RXDRDY				Write '1' to enable interrupt for event RXDRDY																												
			Set	1	Enable																													
			Disabled	0	Read: Disabled																													
			Enabled	1	Read: Enabled																													
D	RW	TXDRDY				Write '1' to enable interrupt for event TXDRDY																												
			Set	1	Enable																													

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID				F																E				D							C	B	A			
Reset 0x00000000				0 0																																
ID	Acce	Field	Value ID	Value	Description																															
A	RW	CTS			Write '1' to disable interrupt for event CTS																															
			Clear	1	Disable																															
			Disabled	0	Read: Disabled																															
			Enabled	1	Read: Enabled																															
B	RW	NCTS			Write '1' to disable interrupt for event NCTS																															
			Clear	1	Disable																															
			Disabled	0	Read: Disabled																															
			Enabled	1	Read: Enabled																															
C	RW	RXDRDY			Write '1' to disable interrupt for event RXDRDY																															
			Clear	1	Disable																															
			Disabled	0	Read: Disabled																															
			Enabled	1	Read: Enabled																															
D	RW	TXDRDY			Write '1' to disable interrupt for event TXDRDY																															
			Clear	1	Disable																															
			Disabled	0	Read: Disabled																															
			Enabled	1	Read: Enabled																															
E	RW	ERROR			Write '1' to disable interrupt for event ERROR																															
			Clear	1	Disable																															
			Disabled	0	Read: Disabled																															
			Enabled	1	Read: Enabled																															
F	RW	RXTO			Write '1' to disable interrupt for event RXTO																															
			Clear	1	Disable																															
			Disabled	0	Read: Disabled																															
			Enabled	1	Read: Enabled																															

Error source

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			D C B A																															
Reset 0x00000000			0 0																															
ID	Acce Field	Value ID	Value	Description																														
A	RW	OVERRUN		Overrun error																														
				A start bit is received while the previous data still lies in RXD. (Previous data is lost.)																														
			NotPresent	0	Read: error not present																													
			Present	1	Read: error present																													
B	RW	PARITY		Parity error																														
				A character with bad parity is received, if HW parity check is enabled.																														
			NotPresent	0	Read: error not present																													
			Present	1	Read: error present																													
C	RW	FRAMING		Framing error occurred																														
				A valid stop bit is not detected on the serial data input after all bits in a character have been received.																														
			NotPresent	0	Read: error not present																													
			Present	1	Read: error present																													
D	RW	BREAK		Break condition																														
				The serial data input is '0' for longer than the length of a data frame. (The data frame length is 10 bits without parity bit, and 11 bits with parity bit.).																														
			NotPresent	0	Read: error not present																													
			Present	1	Read: error present																													

6.33.10.16 ENABLE

Address offset: 0x500

Enable UART

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
ID				A A A A																																
Reset 0x00000000				0 0																																
ID	Acce	Field	Value ID	Value	Description																															
A	RW	ENABLE			Enable or disable UART																															
			Disabled	0	Disable UART																															
			Enabled	4	Enable UART																															

6.33.10.17 PSEL.RTS

Address offset: 0x508

Pin select for RTS

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0									
ID			C																								B												A	A	A	A	A
Reset 0xFFFFFFFF			1																																								
ID	Acce	Field	Value	ID	Value	Description																																					
A	RW	PIN	[0..31]	Pin number																																							
B	RW	PORT	[0..1]	Port number																																							
C	RW	CONNECT		Connection																																							
		Disconnected	1	Disconnect																																							
		Connected	0	Connect																																							

6.33.10.18 PSEL.TXD

Address offset: 0x50C

Pin select for TXD

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
ID			C																												B		A	A	A	A
Reset 0xFFFFFFFF			1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
ID	Acce Field	Value ID	Value				Description																													
A	RW PIN		[0..31]				Pin number																													
B	RW PORT		[0..1]				Port number																													
C	RW CONNECT						Connection																													
		Disconnected	1				Disconnect																													
		Connected	0				Connect																													

6.33.10.19 PSEL.CTS

Address offset: 0x510

Pin select for CTS

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0									
ID			C																								B												A	A	A	A	A
Reset 0xFFFFFFFF			1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1								
ID	Acce	Field	Value ID		Value		Description																																				
A	RW	PIN			[0..31]		Pin number																																				
B	RW	PORT			[0..1]		Port number																																				
C	RW	CONNECT					Connection																																				
			Disconnected		1		Disconnect																																				
			Connected		0		Connect																																				

6.33.10.20 PSEL.RXD

Address offset: 0x514

Pin select for RXD

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			C																															
Reset 0xFFFFFFFF			1 1																															
ID	Acce Field	Value ID	Value	Description																														
A	RW PIN		[0..31]	Pin number																														
B	RW PORT		[0..1]	Port number																														
C	RW CONNECT			Connection																														
		Disconnected	1	Disconnect																														
		Connected	0	Connect																														

6.33.10.21 RXD

Address offset: 0x518

RXD register

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				A A A A A A A A																															
Reset 0x00000000				0 0																															
ID	Acce Field			Value ID			Value			Description																									
A	R	RXD								RX data received in previous transfers, double buffered																									

6.33.10.22 TXD

Address offset: 0x51C

TXD register

Bit number				31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID				A A A A A A A A																															
Reset 0x00000000				0 0																															
ID	Acce	Field	Value	ID	Value	Description																													
A	W	TXD				TX data to be transferred																													

6.33.10.23 BAUDRATE

Address offset: 0x524

Baud rate. Accuracy depends on the HFCLK source selected.

Bit number			31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																															
ID			A A																															

Bit number			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
ID			A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A				
Reset 0x04000000			0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
ID	Acce Field	Value ID	Value			Description																																
		Baud57600	0x00EBF000			57600 baud (actual rate: 57762)																																
		Baud76800	0x013A9000			76800 baud (actual rate: 76923)																																
		Baud115200	0x01D7E000			115200 baud (actual rate: 115942)																																
		Baud230400	0x03AFB000			230400 baud (actual rate: 231884)																																
		Baud250000	0x04000000			250000 baud																																
		Baud460800	0x075F7000			460800 baud (actual rate: 470588)																																
		Baud921600	0x0EBED000			921600 baud (actual rate: 941176)																																
		Baud1M	0x10000000			1Mega baud																																

6.33.10.24 CONFIG

Address offset: 0x56C

Configuration of parity and hardware flow control

Bit number				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
ID				C																												B	B	B	A			
Reset 0x00000000				0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
ID	Acce	Field	Value	ID	Value	Description																																
A	RW	HWFC				Hardware flow control																																
			Disabled	0	Disabled																																	
			Enabled	1	Enabled																																	
B	RW	PARITY				Parity																																
			Excluded	0x0	Exclude parity bit																																	
			Included	0x7	Include parity bit																																	
C	RW	STOP				Stop bits																																
			One	0	One stop bit																																	
			Two	1	Two stop bits																																	

6.33.11 Electrical specification

6.33.11.1 UART electrical specification

Symbol	Description	Min.	Typ.	Max.	Units
f_{UART}	Baud rate for UART ⁴¹ .			1000	kbps
$t_{\text{UART,CTSH}}$	CTS high time	1			μs
$t_{\text{UART,START}}$	Time from STARTRX/STARTTX task to transmission started		1		μs

6.34 UARTE — Universal asynchronous receiver/transmitter with EasyDMA

The Universal asynchronous receiver/transmitter with EasyDMA (UARTE) offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware at a rate up to 1 Mbps, and EasyDMA data transfer from/to RAM.

Listed here are the main features for UARTE:

⁴¹ High baud rates may require GPIOs to be set as High Drive, see [GPIO](#) for more details.