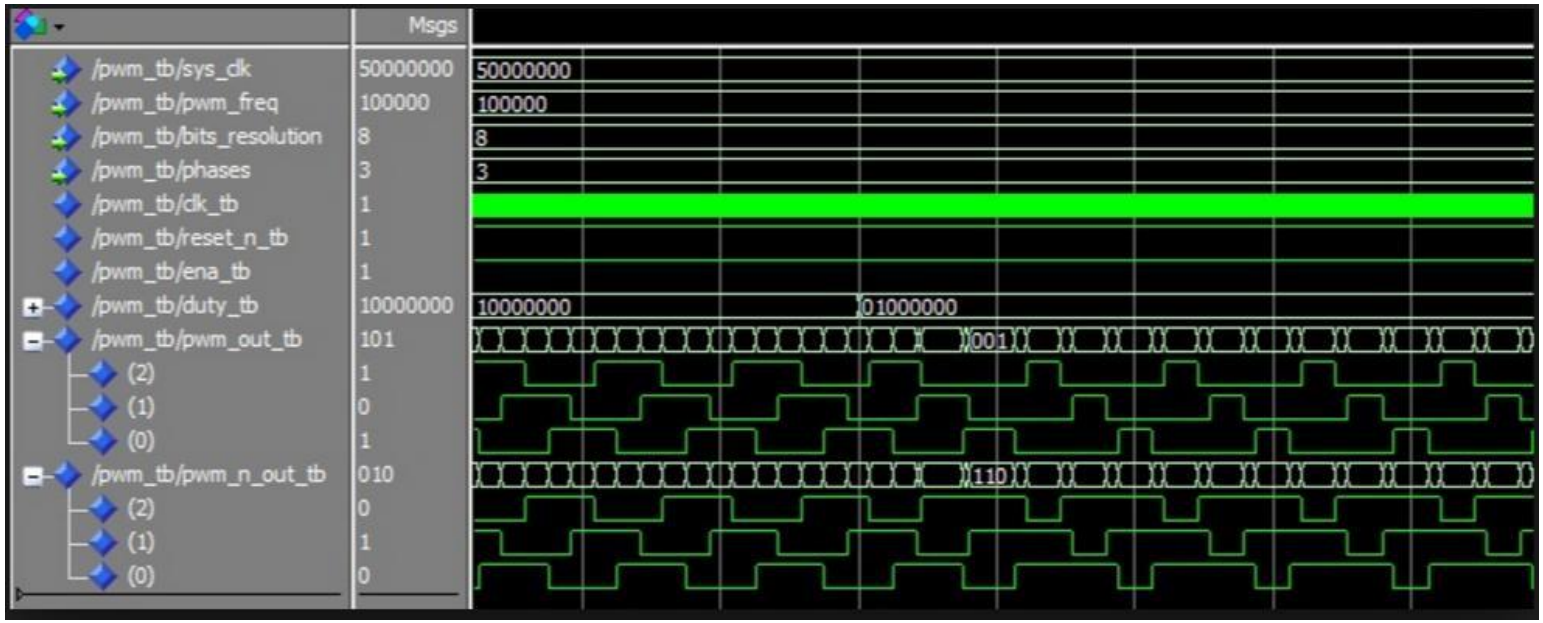
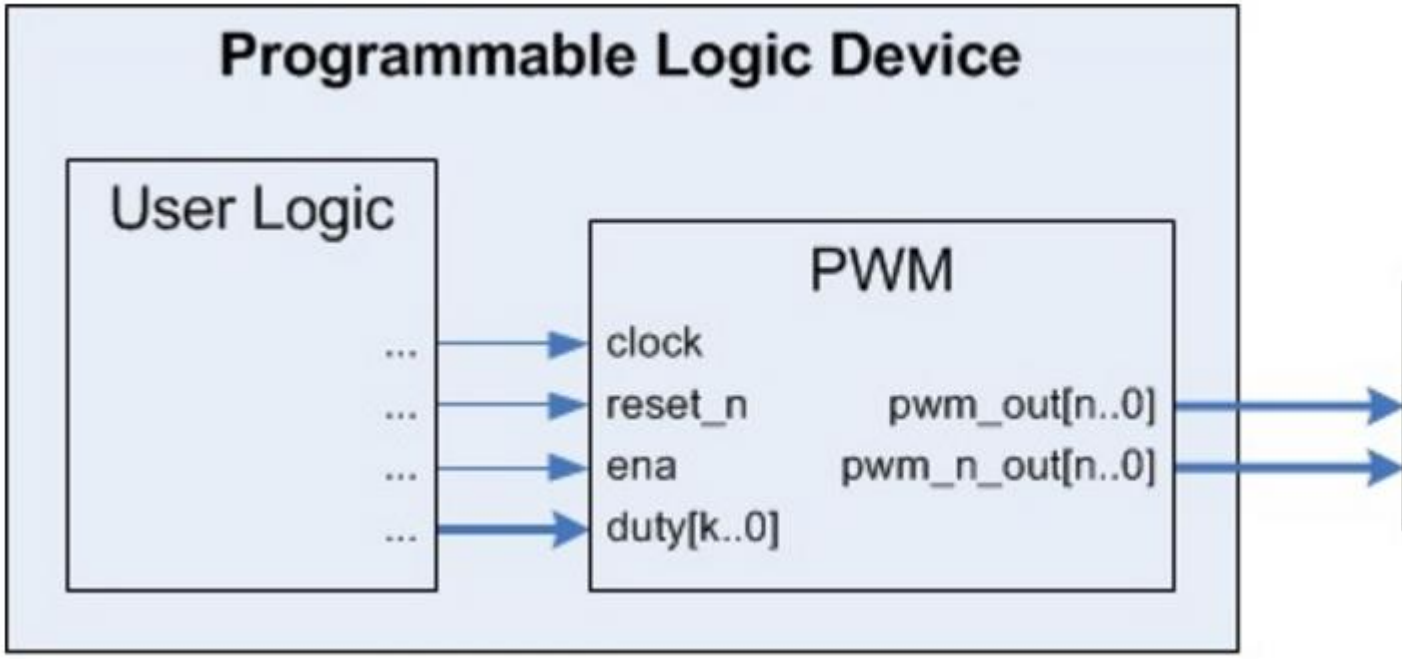
Laboratorio DSP-FPGA
Trabajo Practico
Generador de PWM sobre FPGA



Enunciado

Se deberá implementar un generador de PWM en VHDL.

El generador tendrá la siguiente interface:



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PORT

Port Descriptions

Table 2 describes the PWM generator's ports.

Table 2. Port Descriptions

Port	Width	Mode	Data Type	Interface	Description
clk	1	in	standard logic	user logic	System clock.
reset_n	1	in	standard logic	user logic	Asynchronous active low reset.
ena	1	in	standard logic	user logic	0: PWM continues outputting current duty cycle. 1: latches in the new duty cycle and adjusts the PWM outputs at the center of their pulses.
duty	M*	in	standard_logic_vector	user logic	New duty cycle.
pwm_out	N^	out	standard_logic_vector	load	Output PWM signals. The PWM modulates around the center of the the pulse. The phases are evenly spaced over the period.
pwm_n_out	N^	out	standard_logic_vector	load	Inverse of the PWM outputs.

Notes

* M is the duty cycle's specified resolution in bits, set by the *bits_resolution* generic.

^ N is the specified number of outputs (and phases), set by the *phases* generic.

Generics

Table 1. Generic Parameters

Generic	Data Type	Description
sys_clk	integer	System clock frequency in Hz.
pwm_freq	integer	Frequency of PWM in Hz.
bits_resolution	integer	The number of bits of resolution setting the duty cycle.
phases	integer	The number of output PWMs and phases.

Valores Actuales

Parameter	Value	Type
sys_clk	50000000	Signed Integer
pwm_freq	100000	Signed Integer
bits_resolution	8	Signed Integer
phases	1	Signed Integer

El numero de fases es la cantidad de canales PWM que salen del modulo. En el caso de ser mas de uno su separación será de 360º /numero de fases. Es decir se deben distribuirse uniformemente en un periodo. **La implementación es opcional**

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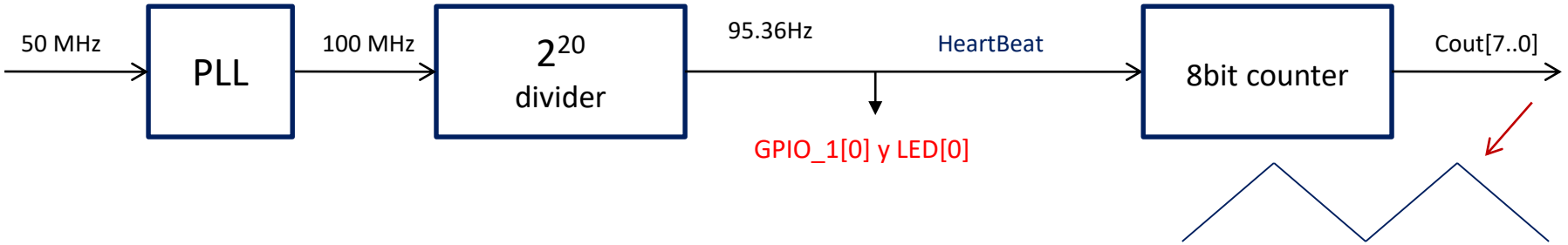
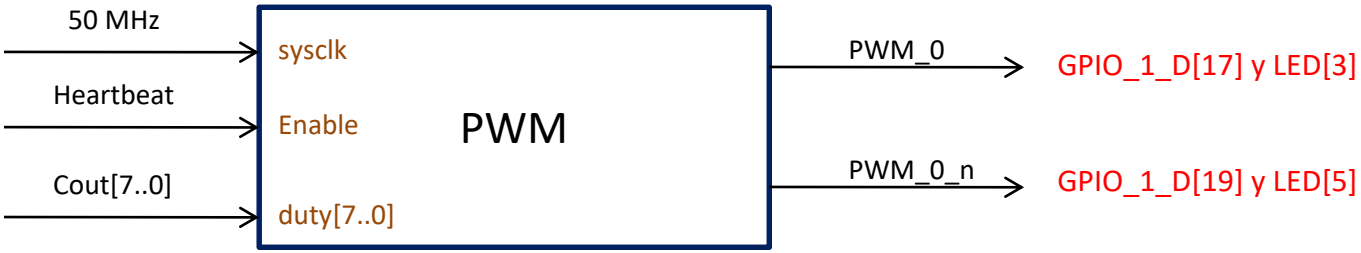
Se deberá implementar el siguiente diagrama en bloques





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pwm_freq	100000	Signed Integer
bits_resolution	8	Signed Integer
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Aplicación: Modulación del duty cycle con una rampa periódica

DE0-Nano

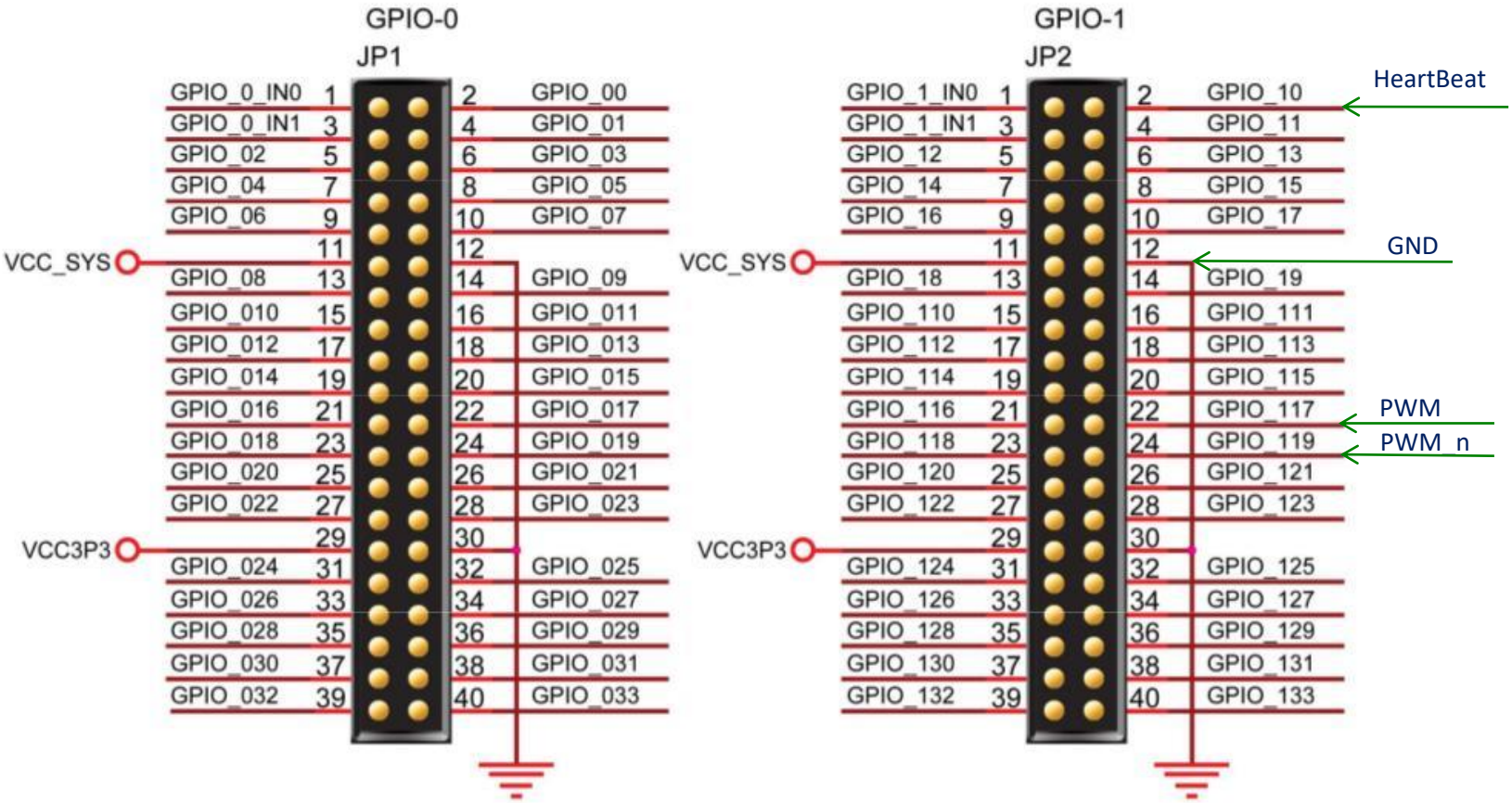
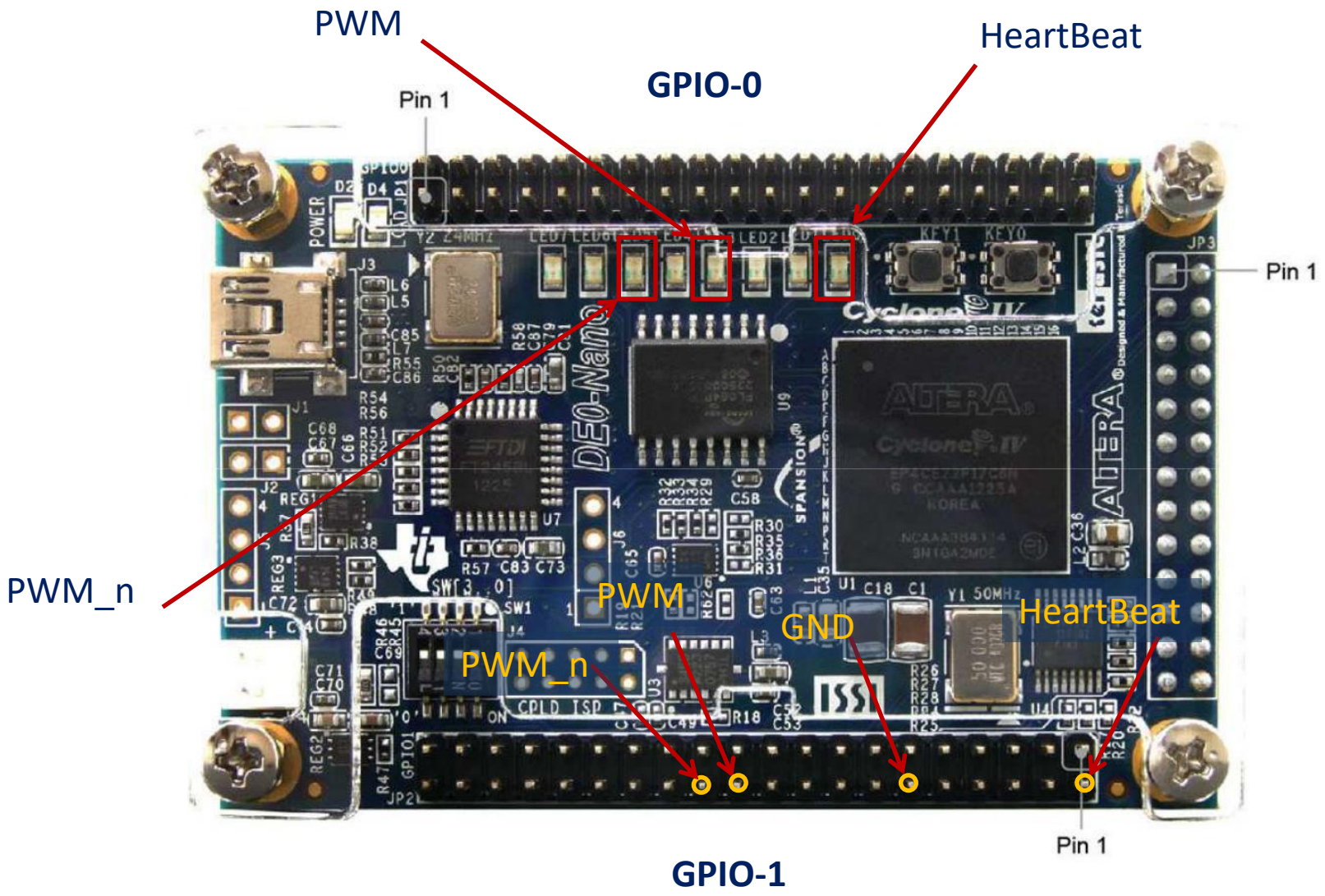


Figure 3-8 Pin arrangement of the GPIO expansion headers

DE0-Nano


PWM
HeartBeat
GPIO-0
Pin 1
Pin 1
PWM_n
PWM
GND
HeartBeat
PWM_n
Pin 1
GPIO-1