Comparing Performance of 1 bit Full Adder and Mirror Adder using Cadence Virtuoso

A PROJECT

Submitted in fulfillment of the requirements for the practical coursework

of

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by

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DISCIPLINE OF ELECTRICAL ENGINEERING

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I hereby certify that the work which is being presented in the report titled as **Comparing Performance of 1-bit Full Adder and Mirror Adder using Cadence Virtuoso** submitted for requirements of the practical coursework of **M Tech (VDN)** in the Discipline of Electrical Engineering, **Indian Institute of Technology Indore**, is an authentic record of my own work carried out during the time period from July 2023 to Nov 2023 under the supervision of **Prof. Santosh Kumar Vishvakarma**. The matter presented in this report has been cited properly wherever necessary.

(Abu Said Parvej Alam)

This is to certify that the above statement made by the candidates is correct to the best of my knowledge.

(Prof. Santosh Kumar Vishvakarma)

ACKNOWLEDGEMENTS

First of all, I would like to thank our Supervisor Prof. Santosh Kumar Vishvakarma whose constant motivation, guidance and suggestion helped me to accomplish the task. I would also like to thank him for providing me Cadence software resources associated with Nanoscale Devices, VLSI Circuit and System Design (NSDCS) Lab. We would like to Thank NSDCS PhD Scholar Mr. Shashank, Mr Vikash and Mr Narendra and from Master's program Mr. Radheshyam and Mr Sagar sir for constant guidance and support and fellow project members along with MTech VDN students for motivation towards achieving the task.

SYNOPSIS

Digital circuits are composed of basic building blocks that perform arithmetic and logical operations. One of the most common and essential building blocks is the binary adder, which can add two binary digits. **In this project, we aim to compare the performance in terms of power consumption, area utilization and analysis of propagation delay of two types of binary adders that are widely used in digital circuits: conventional adder and mirror adder.**

A binary adder is a device that can perform the arithmetic operation of adding two binary digits. A conventional adder uses 28 transistors (14 NMOS and 14 PMOS) to implement a full adder to add two bits and a carry bit, while A mirror adder is an improved version of the conventional adder that uses only 24 transistors (12 NMOS and 12 PMOS) by **exploiting the symmetry of the full adder circuit.** The mirror adder reduces the number of transistors by mirroring the XOR gates and sharing the inputs and outputs of some transistors. To assess the performance of both adder designs, we use a leading electronic design automation (EDA) tool **"Cadence Virtuoso software"** to design and simulate both adders and measure their power consumption, area utilization, propagation delay, and worst-case delay scenario as our evaluation platform. Our research objectives encompass the following critical metrics: **power consumption, area utilization, and the analysis of propagation delay** scenarios. By evaluating these aspects, I aim to illuminate the comparative advantages and disadvantages of these adder designs. In the pursuit of these objectives, I developed and implemented both adder configurations using Cadence, meticulously measuring their power efficiency, physical footprint, speed of operation, and potential pitfalls in worst-case scenarios.

I find that the mirror adder has lower power consumption, smaller area, and faster speed than the conventional adder in most cases. This is because the mirror adder has fewer transistors, which reduces the parasitic capacitance and resistance of the circuit. However, the mirror adder also has a higher worst case delay scenario due to the increased fan-out of some nodes. The fan-out is the number of inputs that are connected to an output. A higher fan-out increases the load capacitance and resistance of the output node, which slows down the signal propagation. I discuss the trade-offs and implications of using different types of adders for various applications. I conclude that the mirror adder is more suitable for applications that require low power consumption, small area, and high speed, such as mobile devices, embedded systems, and high-performance computing. The conventional adder is more suitable for applications that require reliable and consistent performance, such as security systems, communication systems, and error correction codes.

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<1> INTRODUCTION

In the ever-evolving field of digital design, optimizing the performance of fundamental basic arithmetic units, such as adders, is of paramount importance. The full adder, a cornerstone of digital circuits, serves as a vital building block for arithmetic and logical operations. However, conventional full adder designs often come at the cost of increased transistor count, raising concerns about power consumption, area utilization, and propagation delay.

This project titled as "**Comparing Performance of Conventional Adder and Mirror Adder in terms of power consumption, area utilization and analysis of propagation delay Using Cadence Virtuoso**" aims to conduct a comprehensive comparative analysis between the performances of a conventional full adder with an innovative improved counterpart (alternative) known as the mirror adder. The primary metrics of interest include **power consumption**, **area utilization** and the **analysis of propagation delay** scenarios. **Cadence Virtuoso**, a well-established electronic design automation tool (**EDA**), is used to facilitate this comparative analysis.

This work includes making schematic of 1 bit binary full adder relies on 28-transistors and Mirror adder relies on 24-transistors in **Cadence Virtuoso**. Model library **ts018_scl_prim** (SCL 180nm) has been used to make schematics. Pmos18 and Nmos18 have been used from model library to realize design. **Analog library** has been used for capacitor, voltage source and ground. Functional verification of the schematics has been carried out to verify the functionality of the 1 bit binary full adder. I began by taking the truth table and producing logic expressions. After extracting a simplified expression for the **Sum** and **Carry outputs,** I was able to produce the associated CMOS schematic. Once the schematic was drawn, simulated and verified we determined the associated Euler path. From the Euler path I derived the stick diagram used to create our layout.

Digital computers perform a variety of information processing tasks. Among the basic tasks encountered are the various arithmetic operations. The most basic arithmetic operation is the addition of binary digits. A full adder is a basic building block of arithmetic circuits, such as ripple-carry adders, carry-look ahead adders, and carry-select adders.

This is a design with three inputs (A, B, and Cin) and two outputs (Sum and Cout). A conventional full adder uses 28 transistors (14 NMOS and 14 PMOS) to execute its arithmetic functions, while a mirror adder uses only 24 transistors (12 NMOS and 12 PMOS). A mirror adder achieves this by exploiting the inversion property of the full adder logic, which states that inverting all inputs and outputs of a full adder results in the same functionality. A mirror adder alternates between regular and inverted full adders, eliminating the need for inverters between them by mirroring the XOR gates and sharing the inputs and outputs of some transistors. This reduces the area, power consumption and the delay of the circuit which results faster speed, but also introduces some challenges such as charge sharing and charge leakage and higher fan-out which results higher worst case delay scenario. A mirror adder can be used to build a ripple-carry adder, which is an adder that uses multiple full adders to add N-bit numbers.

Propagation Delay is the time taken for the output to change after the input changes. **Power consumption** is the amount of energy required to operate the circuit. **Area** is the physical size of the circuit layout. Worst case delay scenario is the situation where the input combination causes the maximum delay in the output. The fan-out is the number of inputs that are connected to an output. A higher fan-out increases the load capacitance and resistance of the output node, which slows down the signal propagation. The "**mirror**" in the name "mirror adder" is derived from a technique that exploits the symmetric properties of the circuit to eliminate redundancy and optimize transistor placement. This technique ensures that the transistor count is minimized while maintaining the full adder's functionality. Besides this, the mirror adder also has some disadvantages like complex design, more sensitive to process variations etc. for which the new concept has a relatively less widespread adoption in Industry Level. In summary, the mirror adder is an innovative approach to adder circuit design that offers substantial advantages in terms of reduced transistor count, lower power consumption, and smaller area utilization. However, it can be more complex to design and may have certain limitations related to process variability and industry adoption. The choice between a mirror adder and a CMOS full adder depends on the specific requirements and constraints of a given digital circuit application.

<2> THEORY AND WORKING PRINCIPLE

A full adder is a central to most digital combinational circuit that performs complex arithmetic operations in digital systems, such as addition, subtraction, and multiplication. It is so called "Adder" because it adds together two binary bits, plus a carry-in bit to produce a sum and carry-out bit. The first two inputs are A and B and the third input is an input carry as Cin, The output carry is designated as Cout and the normal output is designated as Sum which is SUM. Full adders are made from XOR, AND and OR gates in hardware. Full adders are commonly connected to each other to add bits to an arbitrary length of bits, such as 32 or 64 bits. A full adder is effectively two half adders, an XOR and an AND gate, connected by an OR gate. The sum bit (Sum) is computed using the XOR (exclusive OR) gate. Mathematically, it can be expressed as Sum = A XOR B XOR Cin. This operation produces the result of adding the two input bits (A and B) along with the carry-in bit (Cin). The carry-out bit (Cout) is determined using a combination of AND and OR gates. It is calculated as Cout = (A AND B) OR (Cin AND (A XOR B)) = (A AND B) OR (B AND Cin) OR (A AND Cin). This operation considers the logic relationships between the input bits to determine if there is any carry generated during the addition.

Inputs			Outputs	
A	**B**	**C_{in}**	**C_{out}**	**Sum**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**0**	**1**
0	**1**	**0**	**0**	**1**
0	**1**	**1**	**1**	**0**
1	**0**	**0**	**0**	**1**
1	**0**	**1**	**1**	**0**
1	**1**	**0**	**1**	**0**
1	**1**	**1**	**1**	**1**

Table 1: Truth Table of 1 bit binary full adder circuit.

The operation of a full adder is based on Boolean logic equations and can be described as follows:

$$Sum = \bar{A}\,\bar{B}\,C_{in} + \bar{A}\,B\,\bar{C}_{in} + A\,\bar{B}\,\bar{C}_{in} + A\,B\,C_{in} = A \oplus B \oplus C_{in} \quad \text{..... (1)}$$

$$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\bar{C}_{in} + ABC_{in} = AB + BC_{in} + AC_{in} = AB + C_{in}(A+B) \quad \text{..... (2)}$$

$$\bar{C}_{out} = \overline{AB + C_{in}(A+B)} \quad \text{.....(3)}$$

The expression for Sum can be further reduced by the following logical simplifications:

$$Sum = (A+B+C_{in})\overline{(BC_{in} + AC_{in} + AB)} + ABC_{in} = (A+B+C_{in})\bar{C}_{out} + ABC_{in} \quad \text{.....(4)}$$

$$\overline{Sum} = \overline{(A + B + C_{in})\bar{C}_{out} + ABC_{in}} \quad \text{.....(5)}$$

From (2) $C_{out} = AB + C_{in}(A+B)$, it is evident that if $A = B$ then the carry output is equal to their value i.e. $C_{out} = A$ or $C_{out} = B$. If $A \neq B\ (i.e.\ A = \bar{B})$ then we have $C_{out} = C_{in}$ (the full adder is said to be in propagate mode), and hence the full adder has to wait for the computation of C_{out} .

A mirror adder is an improved version of the conventional CMOS (Complementary Metal-Oxide-Semiconductor) full adder that uses only 24 (12 NMOS and 12 PMOS) transistors by exploiting the symmetry of the full adder circuit, which states that inverting all inputs and outputs of a full adder results in the same functionality. A mirror adder alternates between regular and inverted full adders, eliminating the need for inverters between them by mirroring the XOR gates and sharing the inputs and outputs of some transistors. The "mirror" in the name "mirror adder" is derived from a technique that exploits the symmetric properties of the circuit to eliminate redundancy and optimize transistor placement. This technique ensures that the transistor count is minimized while maintaining the full adder's functionality.

The circuit is designed in such a way that the PMOS and NMOS networks are not complementary rather the NMOS and PMOS chains are symmetrical, which allows certain transistors to be removed. The mirror adder consists of two stages: the carry stage and the sum stage. The carry stage computes the carry output Cout as the logical OR of three terms: A&B, B&Cin, and A&Cin. The sum stage computes the sum output Sum as the logical OR of two terms: A&B&Cin and $\bar{C}_{out}$&(A|B|Cin). The mirror

adder’s carry generation stage consists of two series of transistors. The use of two series of transistors is likely for optimizing the efficiency and speed of carry propagation. The first series of transistors (NMOS transistors) is used to determine when the carry should be generated (i.e., when both A and B are high). The second series of transistors (PMOS transistors) is used to determine when the carry should be inverted. The series of transistors work in parallel to compute different parts of the carry signal, and then they are logically OR-ed together to produce the final carry output. Similar to the carry generation stage, the sum generation stage of a mirror adder also consists of two series of transistors, one for generating the sum bit and another for inverting the sum when necessary based on the value of Cin.

The NMOS and PMOS chains in the carry-generation circuitry are completely symmetrical, which allows for a maximum of two series transistors to be observed in this stage. It's worth noting that the symmetrical nature of the NMOS and PMOS chains in both the carry and sum stages contributes to the mirror adder's efficiency, which means that they have the same logic function and transistor sizes. This symmetry ensures that the logic functions and transistor sizes are balanced, helping to minimize the overall transistor count while maintaining the adder's functionality. The primary advantage of the mirror adder is that it utilizes only 24 transistors, as opposed to the 28 transistors used in a conventional full adder. This reduction can lead to lower power consumption and a smaller physical footprint. It is particularly valuable in applications where power consumption is a critical concern. With fewer transistors, the mirror adder design can be more cost-effective in terms of both manufacturing and power usage.

<3> VARIOUS DESIGN ANALYSIS

Design- 01. Conventional Full Adder when body terminal (substrate) of pmos connected to Vdd and of nmos to Vss.

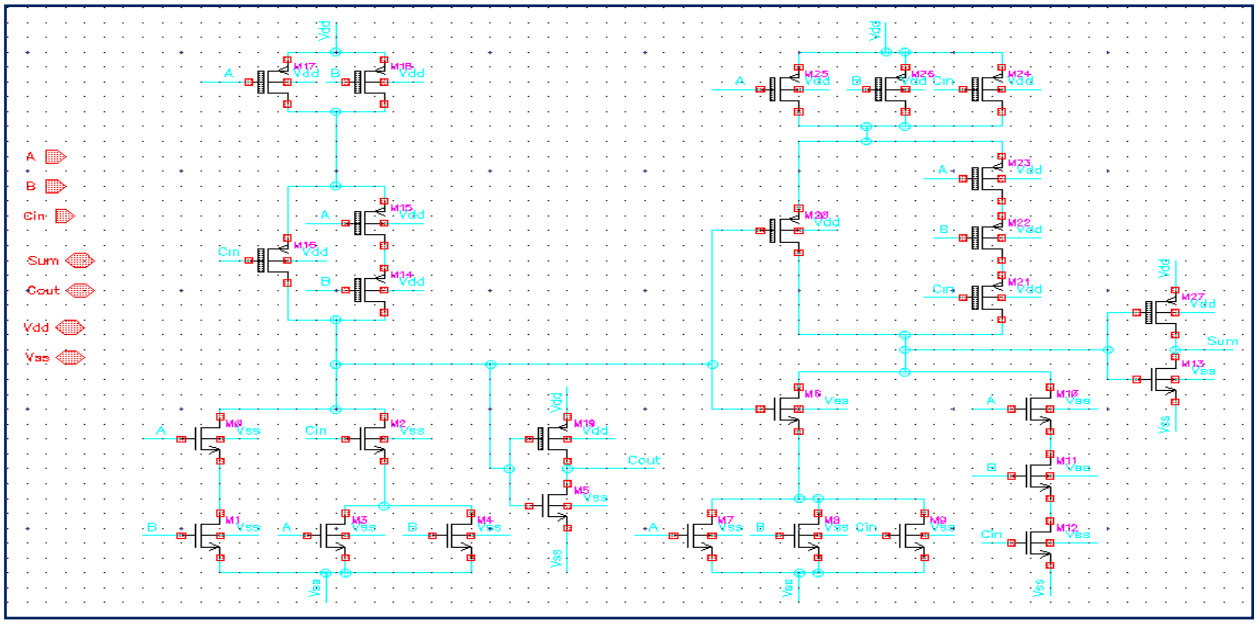


Fig-01 (a):- Schematic when body (pmos) connected to Vdd & body (nmos) connected to Vss.

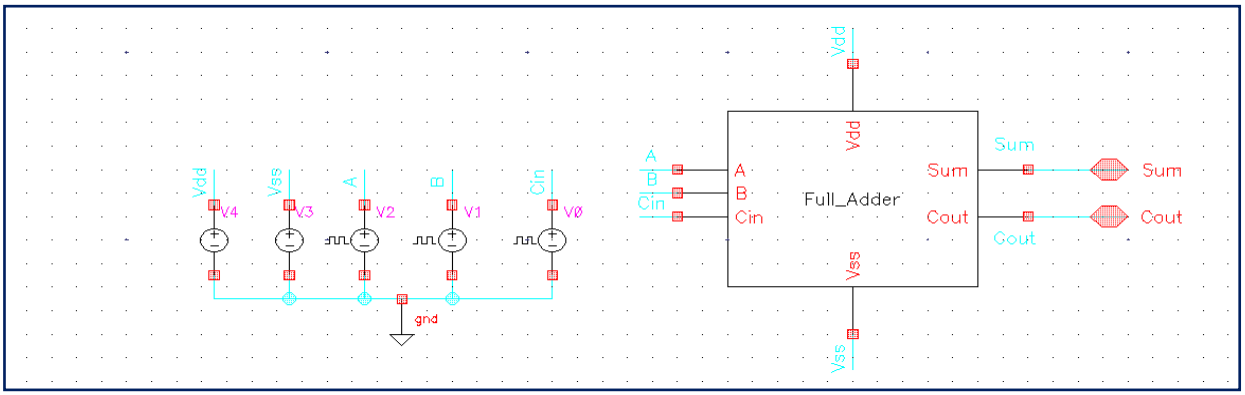


Fig-01 (b):- Test bench in Ideal Case when NO LOAD Capacitance connected.

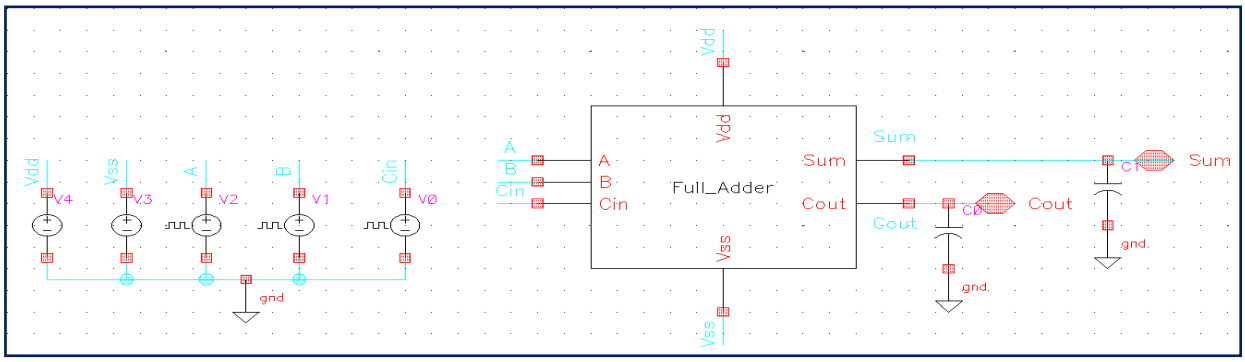


Fig-01 (c):- Test bench in Practical Case when 100fF capacitance considered at output.

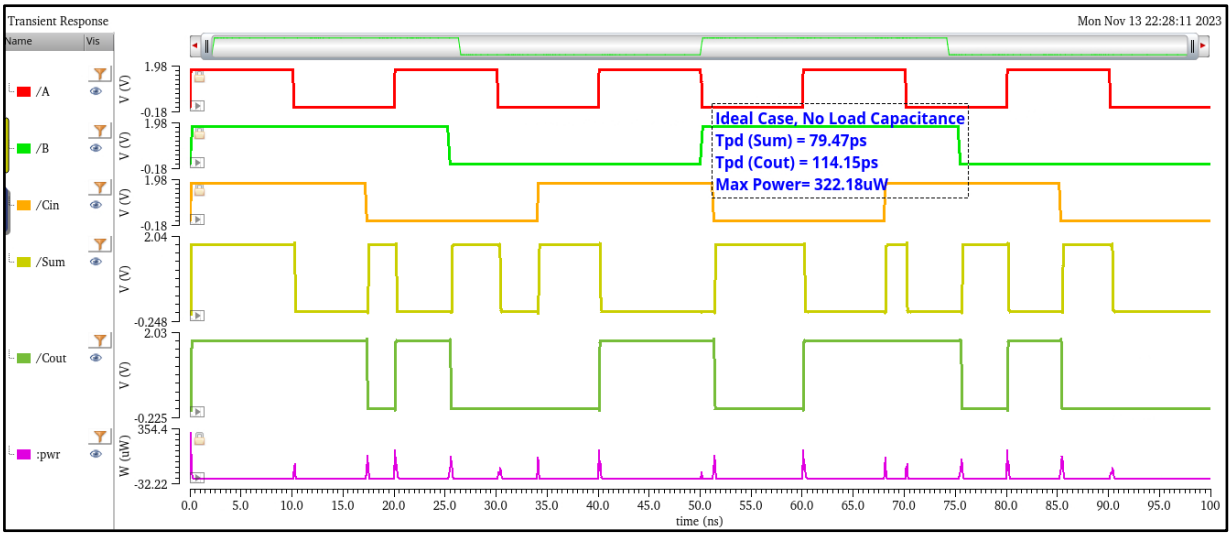


Fig-01 (d):- Transient analysis waveform in Ideal Case.

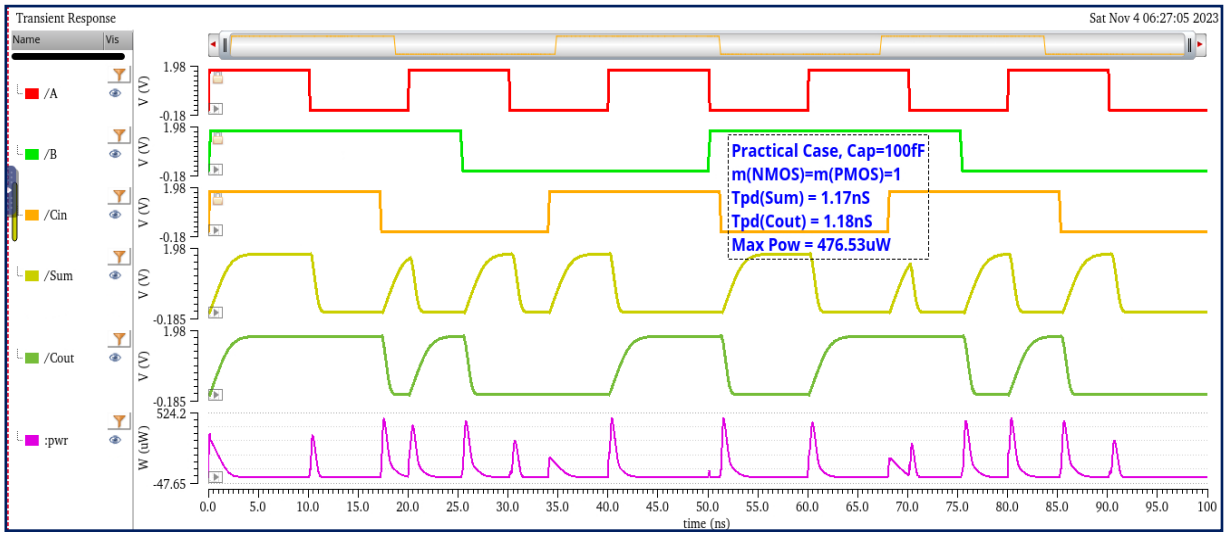
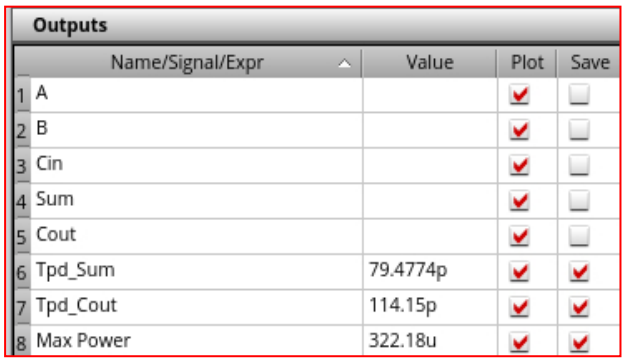


Fig-01 (e):- Transient analysis waveform in Practical Case when width for all MOS are same.

The two plots indicate that when the load capacitance is taken into account at the output of a full adder for both the Sum and Carry signals, it becomes evident that the propagation delays of the Sum and Carry signals increase and that results more power consumption. Propagation delay is the time it takes for a signal to travel from the input of a circuit to its output. The propagation delay of Sum (Sum) and Carry (Cout) signals increases because the load capacitance adds to the overall difficulty of driving the output. As the load capacitance increases, it takes more time for the voltage levels at the output to stabilize or reach their final values. The increased propagation delay can affect the overall performance of the circuit, especially in scenarios where fast signal transitions are crucial. It may lead to a slower operation of the full adder and can impact the timing constraints in larger digital systems.

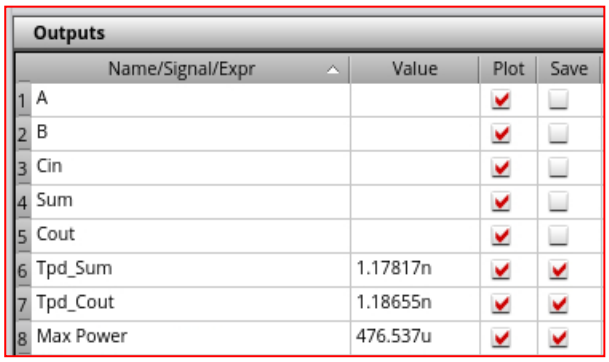
ADEL (Advanced Design Environment for Logics) Window



Outputs

	Name/Signal/Expr	Value	Plot	Save
1	A		☑	☐
2	B		☑	☐
3	Cin		☑	☐
4	Sum		☑	☐
5	Cout		☑	☐
6	Tpd_Sum	79.4774p	☑	☑
7	Tpd_Cout	114.15p	☑	☑
8	Max Power	322.18u	☑	☑

(i) Ideal Case Result



Outputs

	Name/Signal/Expr	Value	Plot	Save
1	A		☑	☐
2	B		☑	☐
3	Cin		☑	☐
4	Sum		☑	☐
5	Cout		☑	☐
6	Tpd_Sum	1.17817n	☑	☑
7	Tpd_Cout	1.18655n	☑	☑
8	Max Power	476.537u	☑	☑

(ii) Practical Case Result

Fig-01 (f):- Propagation Delay and Power Consumption in Ideal and Practical Case respectively.

I have taken following steps to analyze and optimize performance of various designs of adders throughout our project working:--

To analyze the **propagation delay** and **power consumption** of the circuit I have conducted an experiment by varying the input signal rising and falling times (**i.e. tr = tf = Ti**) and recording the resulting propagation delay (tpd) values for both the sum (**Tpd_Sum**) and carry (**Tpd_Cout**) outputs and also the maximum power consumption. The range of values used for the rising and falling times for inputs are 1ps, 10ps, 100ps and 300ps. Adjusting the width of PMOS and NMOS transistors is a common technique in digital circuit design to influence performance parameters such as speed, power consumption, and signal integrity. So I have also adjusted width of pMOS and nMOS to gauge performance of various design of adder circuits. For example, wider transistors generally lead to faster but more power-consuming design. In first case I have taken same driving strength of both pMOS and nMOS i.e. width for both pMOS and nMOS is equal to 420nm. This case is depicted as m(PMOS)=m(nMOS)=1. In second case to further probe the propagation delay and power consumption I have adjusted the width of all pMOS two times of all nMOS by considering the mobility of electron and hole. This case is depicted as m(PMOS)=2, m(nMOS)=1. In final case I have optimized the width ratio of all MOS according to circuit configuration of adder so that equal resistance is achieved of each path. This likely involved realizing a basic unit inverter to maintain consistent performance across different parts of the circuit. This case is depicted as optimized sized w.r.t inverter. By optimizing MOS width ratios and ensuring equal resistance in each path, the final case aimed to enhance the overall performance and reliability of the digital circuit, providing a more balanced and efficient design. **I have investigated the performance of full adder, by systematically varying input signal characteristics (varying Ti) and adjusting the widths of PMOS and NMOS transistors.** The goal aimed to provide a comprehensive understanding of how these factors collectively impact the propagation delay, power consumption and overall performance of the digital circuit. **The various results are shown below in tabular form:-**

Conventional Full Adder when body of pmos connected to Vdd and of nmos to Vss.				
Different Designs	**Time Delay of Input Pulse (Ti)**	**Time Delay of Sum(Tpd_Sum)**	**Time Delay of Carry(Tpd_Cout)**	**Max Power Consumption**
Ideal Design (When no output capacitance considered and all the nMOS and pMOS are of equal size)	*Ti = 0 Sec*	79.47 pSec	114.15 pSec	322.18 uWatt
	Ti = 1 pSec	82.25 pSec	41.38 pSec	2.47 mWatt
	Ti = 10 pSec	79.57 pSec	43.24 pSec	1.60 mWatt
	Ti = 100 pSec	69.56 pSec	61.23 pSec	532.12 uWatt
	Ti = 300 pSec	53.11 pSec	75.63 pSec	286.63 uWatt
Practical Design (When a **100 fF** output capacitance considered and all nMOS and pMOS are of **equal size**)	*Ti = 0 Sec*	1.178 nSec	1.186 nSec	476.53 uWatt
	Ti = 1 pSec	1.177 nSec	1.115 nSec	2.453 mWatt
	Ti = 10 pSec	1.174 nSec	1.115 nSec	1.601 mWatt
	Ti = 100 pSec	1.170 nSec	1.135 nSec	532.61 uWatt
	Ti = 300 pSec	1.165 nSec	1.151 nSec	478.29 uWatt
Practical Design (When a 100 fF output capacitance considered and all pMOS are of twice of nMOS size), **m(pMOS) = 2** and **m(nMOS) = 1**.	*Ti = 0 Sec*	704.54 pSec	702.31 pSec	607.93 uWatt
	Ti = 1 pSec	721.58 pSec	623.57 pSec	2.488 mWatt
	Ti = 10 pSec	717.61 pSec	623.86 pSec	1.689 mWatt
	Ti = 100 pSec	698.68 pSec	641.50 pSec	664.83 uWatt
	Ti = 300 pSec	691.21 pSec	667.35 pSec	607.81 uWatt
Practical Design (When a 100 fF output capacitance considered and all MOS Transistor sizes have been **optimized w.r.t unit Inverter**)	*Ti = 0 Sec*	647.41 pSec	626.10 pSec	963.08 uWatt
	Ti = 1 pSec	724.94 pSec	621.69 pSec	5.283 mWatt
	Ti = 10 pSec	721.18 pSec	622.79 pSec	3.724 mWatt
	Ti = 100 pSec	704.50 pSec	639.05 pSec	1.515 mWatt
	Ti = 300 pSec	707.70 pSec	664.45 pSec	824.06 uWatt

Table 2: Conventional Full Adder when body of pmos connected to Vdd and of nmos to Vss.

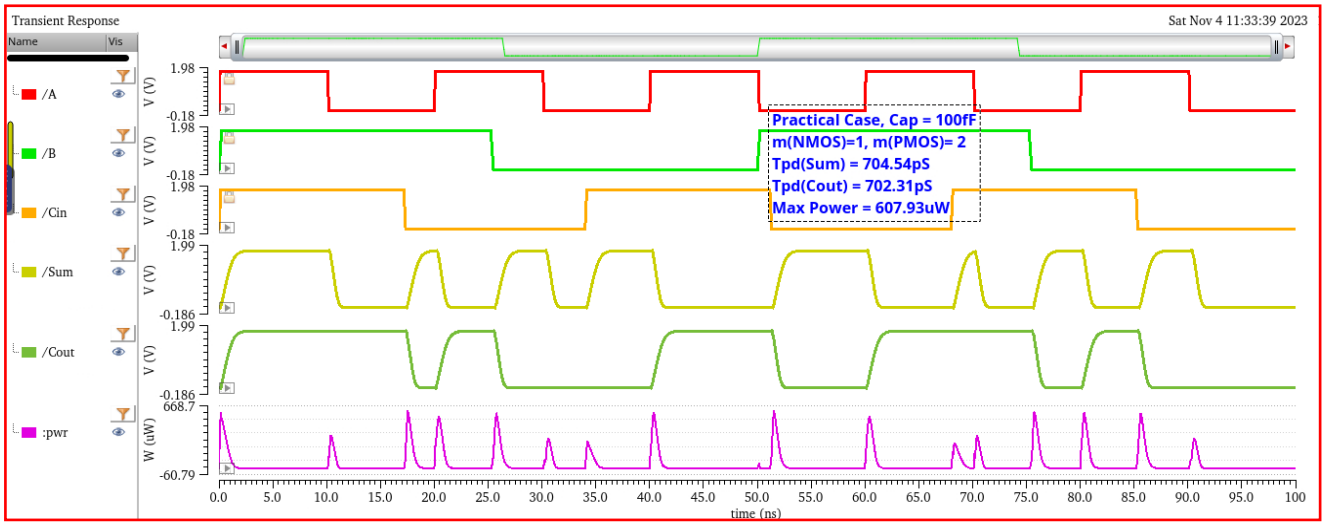


Fig-01 (g):- Transient analysis waveform in Practical Case when width of all pMOS is twice of nMOS.

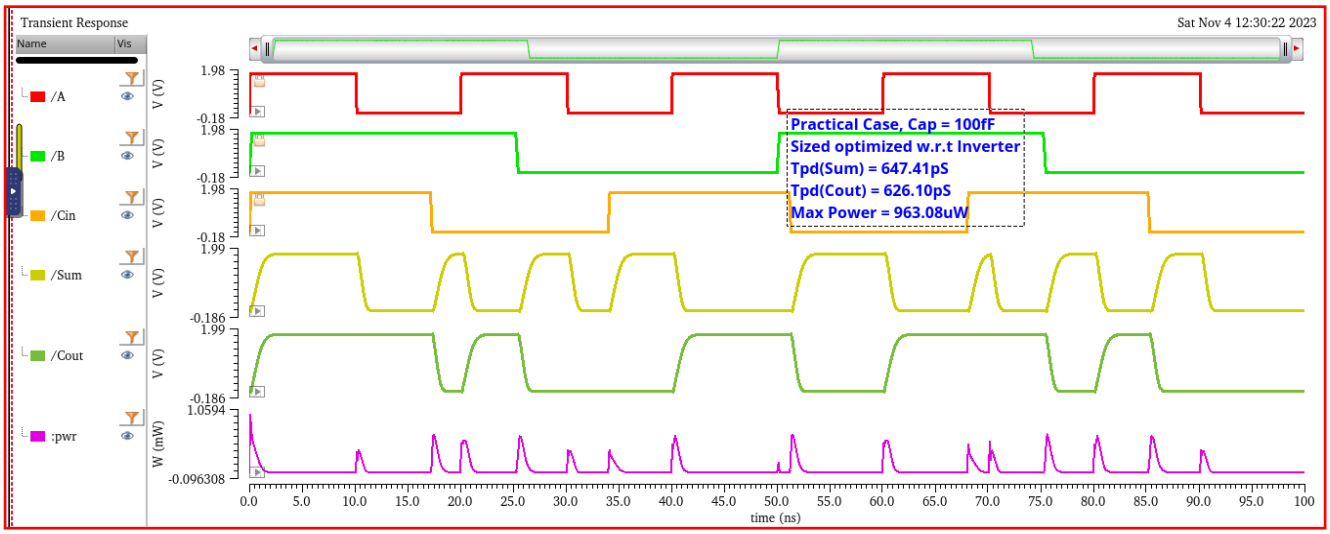


Fig-01 (h):- Transient analysis waveform in Practical Case when width is optimized wrt unit inverter.

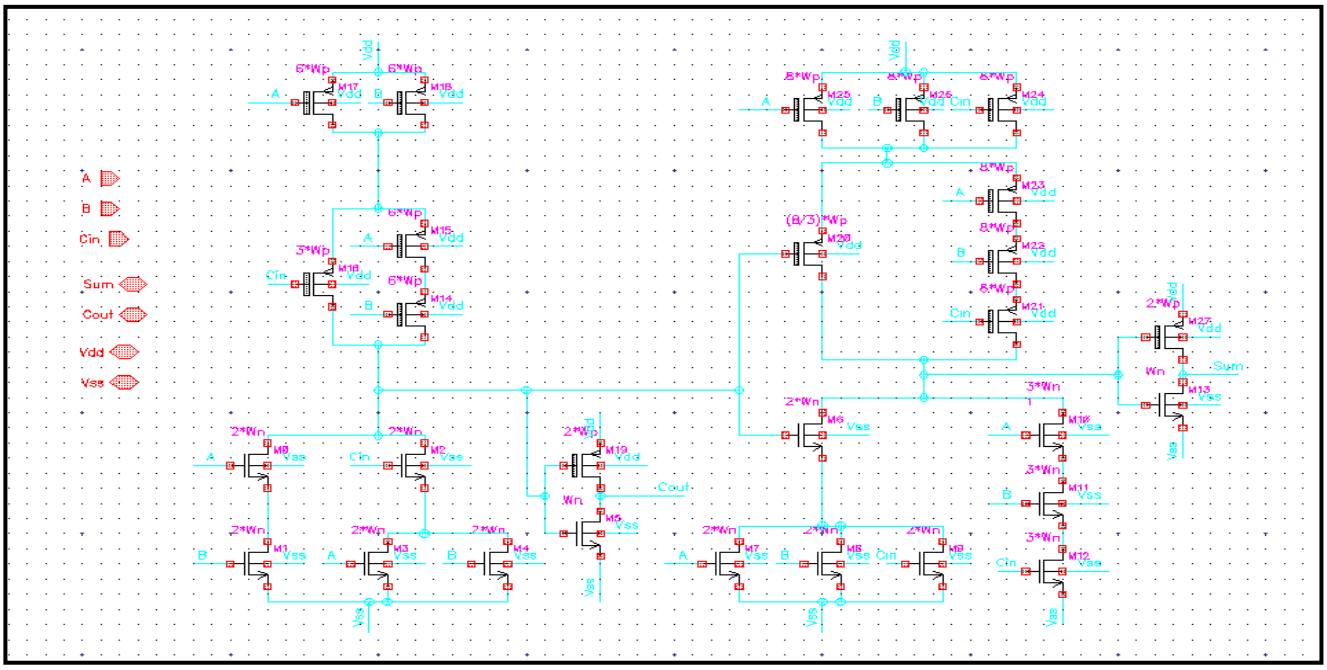


Fig-01 (i):- Schematic design optimized for pMOS and nMOS with respect to standard unit inverter.

Design- 02. Conventional Full Adder when body (substrate) of pmos and nmos connected to source.

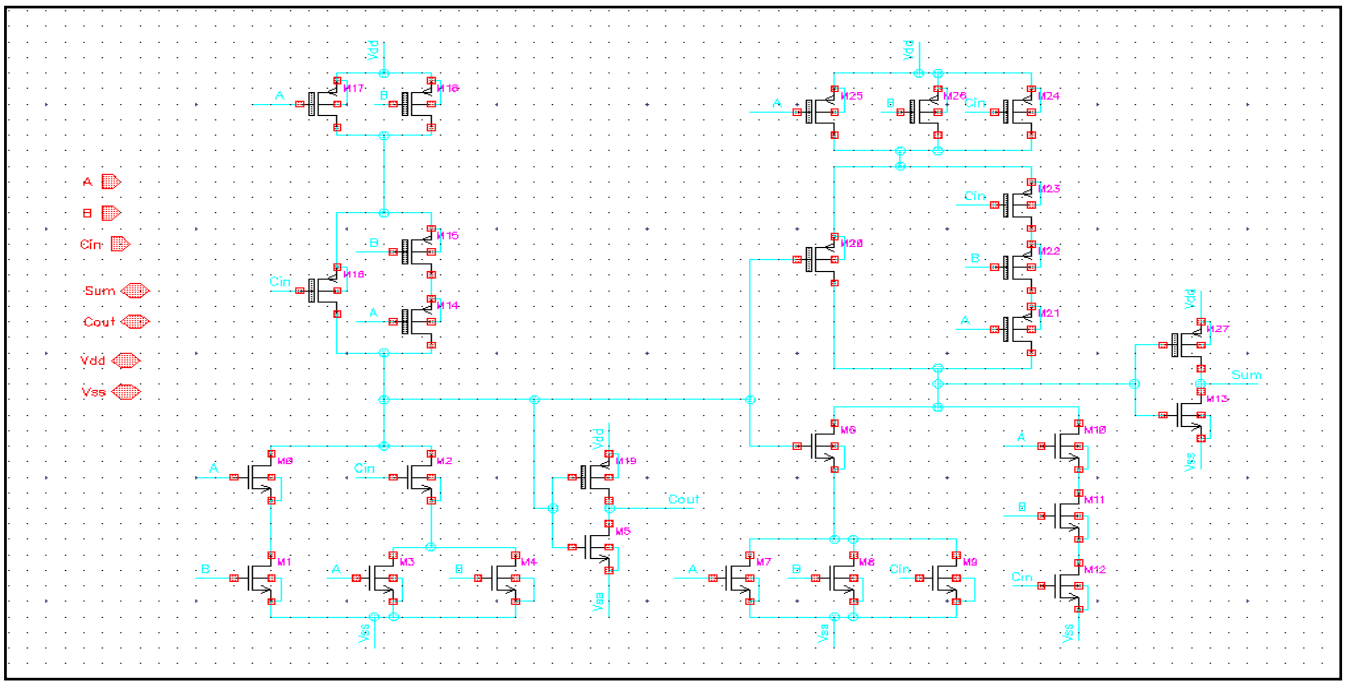


Fig-02 (a):- Schematic when body of pmos and nmos connected to Source.

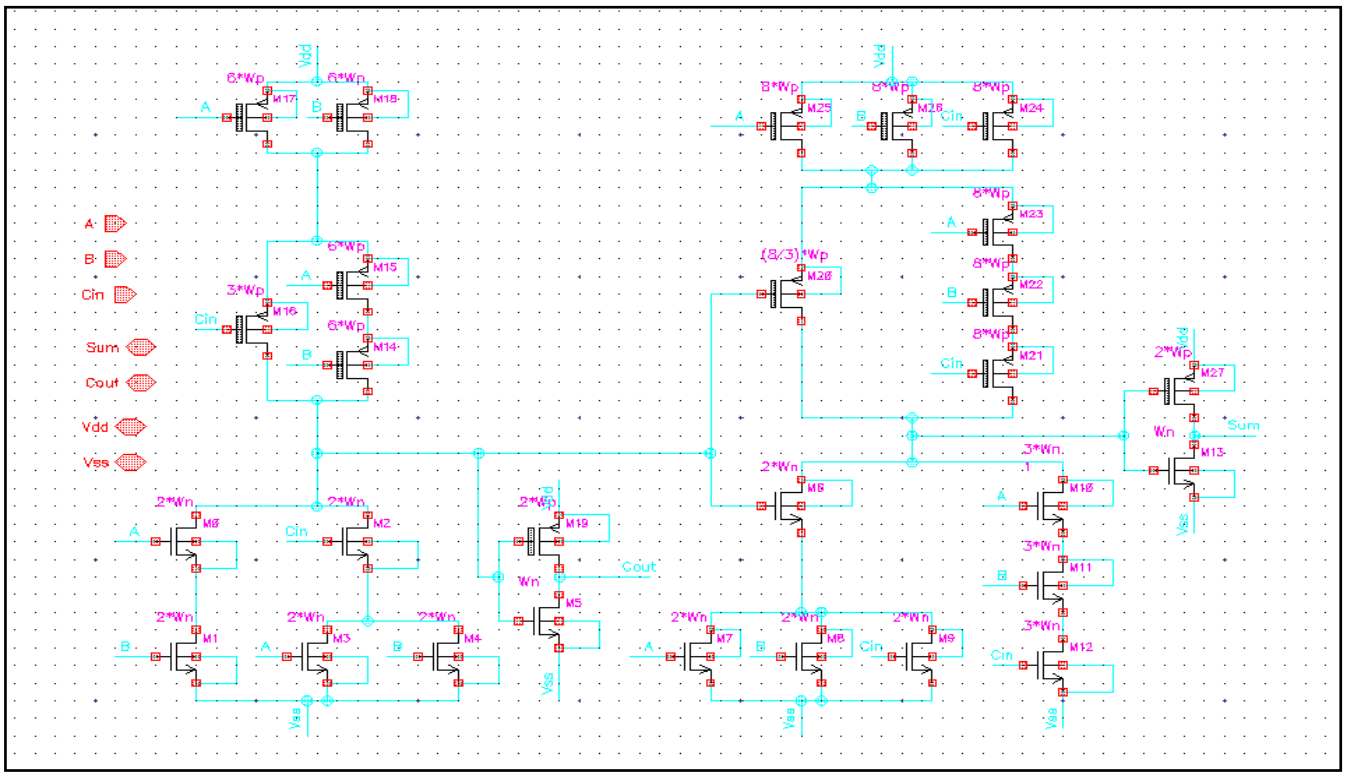


Fig-02 (b):- Schematic design optimized for pMOS and nMOS with respect to standard unit inverter.

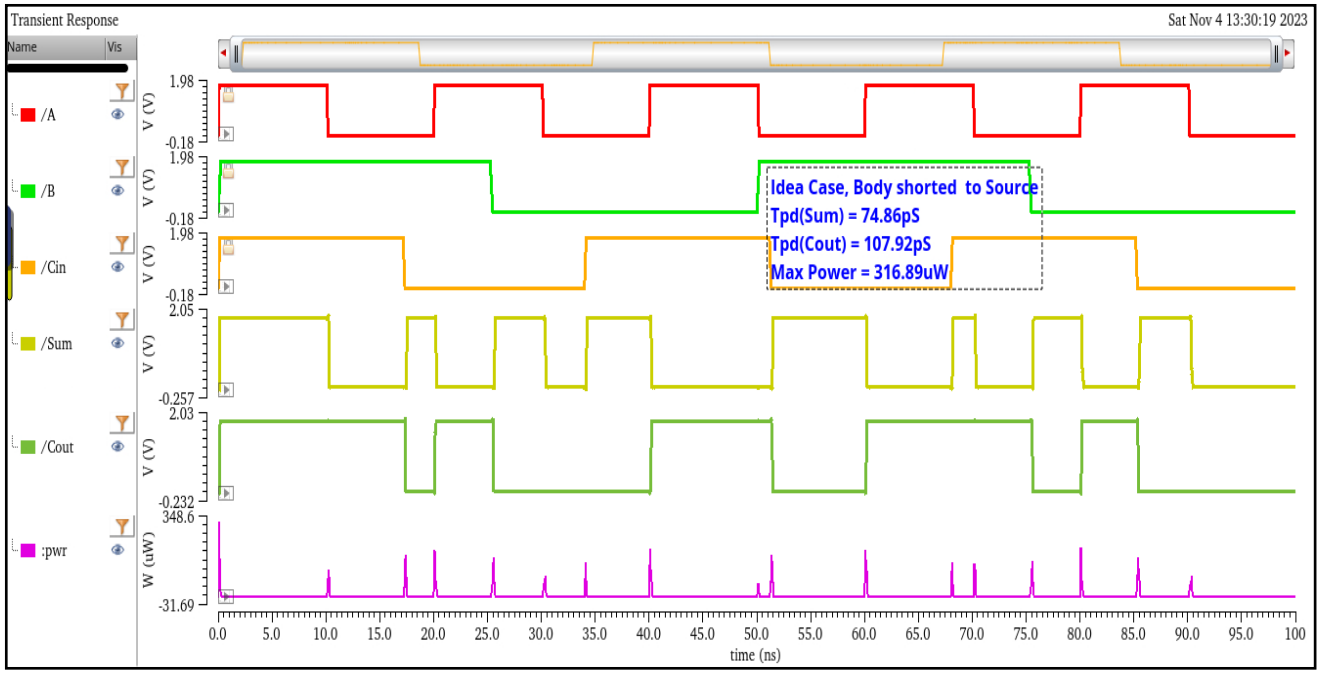


Fig-02 (c):- Transient analysis waveform in Ideal Case.

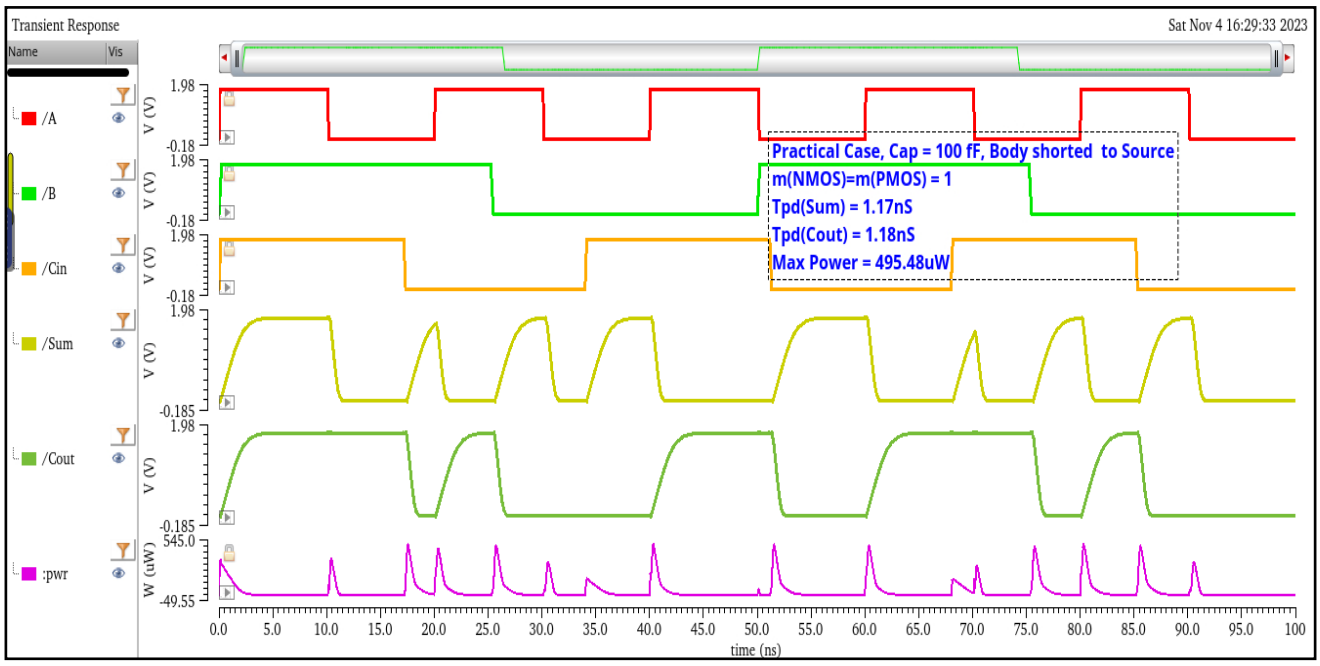


Fig-02 (d):- Transient analysis waveform in Practical Case when width for all MOS are same.

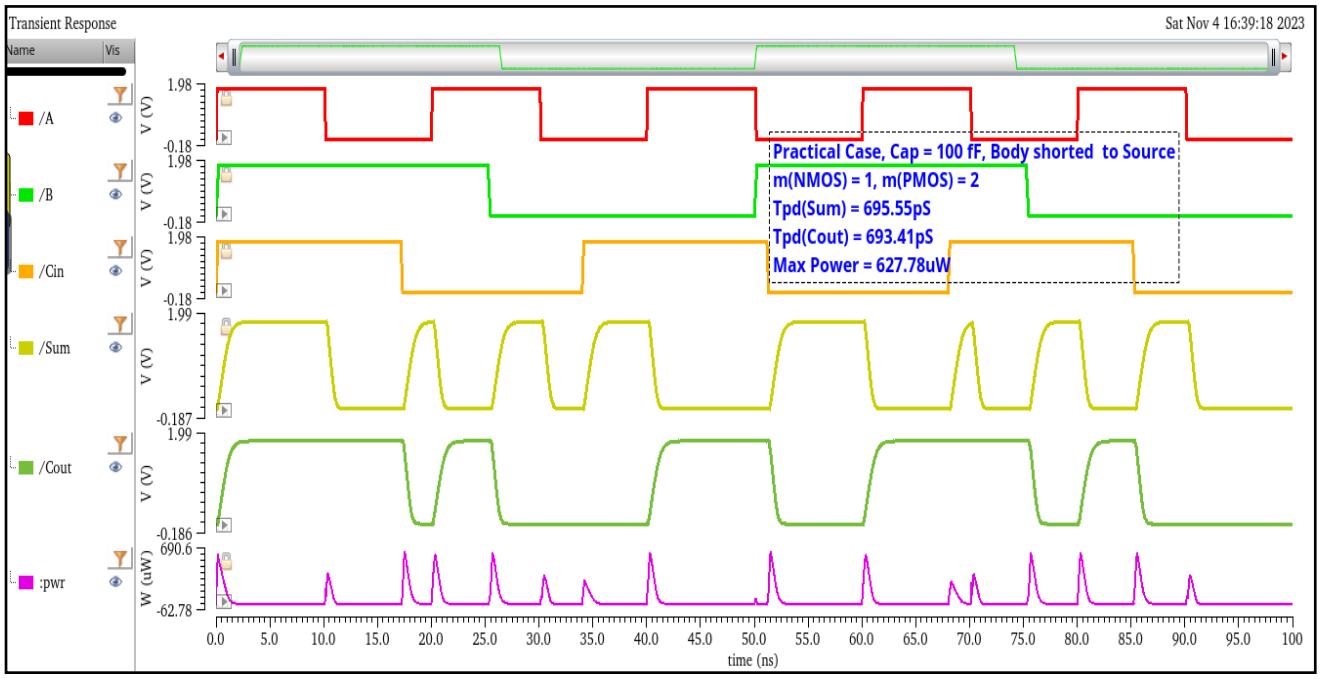


Fig-02 (e):- Transient analysis waveform in Practical Case when width of all pMOS is twice of nMOS.

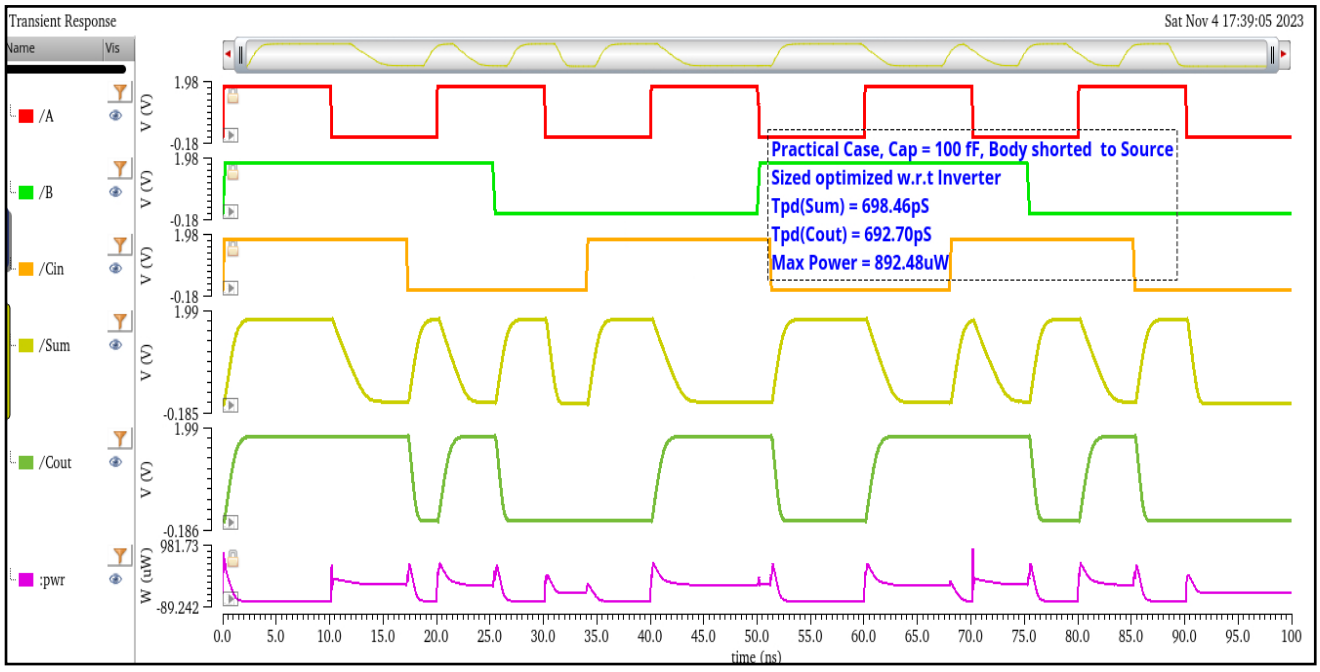


Fig-02 (f):- Transient analysis waveform in Practical Case when width is optimized wrt unit inverter.

Conventional Full Adder when Body terminal shorted to Source terminal				
Different Designs	**Time Delay of Input Pulse (Ti)**	**Time Delay of Sum(Tpd_Sum)**	**Time Delay of Carry(Tpd_Cout)**	**Max Power Consumption**
Ideal Design (When no output capacitance considered and all the nMOS and pMOS are of equal size)	*Ti = 0 Sec*	74.866 pSec	107.92 pSec	316.89 uWatt
	Ti = 1 pSec	64.827 pSec	41.345 pSec	4.405 mWatt
	Ti = 10 pSec	62.995 pSec	42.961 pSec	2.174 mWatt
	Ti = 100 pSec	62.606 pSec	58.393 pSec	564.68 uWatt
	Ti = 300 pSec	47.079 pSec	67.185 pSec	273.54 uWatt
Practical Design (When a **100 fF** output capacitance considered and all nMOS and pMOS are of **equal size**)	*Ti = 0 Sec*	1.171 nSec	1.180 nSec	495.48 uWatt
	Ti = 1 pSec	1.156 nSec	1.110 nSec	4.176 mWatt
	Ti = 10 pSec	1.155 nSec	1.115 nSec	2.155 mWatt
	Ti = 100 pSec	1.154 nSec	1.131 nSec	565.33 uWatt
	Ti = 300 pSec	1.152 nSec	1.139 nSec	496.26 uWatt
Practical Design (When a 100 fF output capacitance considered and all pMOS are of twice of nMOS size), **m(pMOS) = 2** and **m(nMOS) = 1**.	*Ti = 0 Sec*	695.55 pSec	693.41 pSec	627.78 uWatt
	Ti = 1 pSec	687.52 pSec	620.39 pSec	6.697 mWatt
	Ti = 10 pSec	686.15 pSec	621.24 pSec	2.386 mWatt
	Ti = 100 pSec	680.99 pSec	636.56 pSec	701.57 uWatt
	Ti = 300 pSec	679.80 pSec	657.51 pSec	627.52 uWatt
Practical Design (When a 100 fF output capacitance considered and all MOS Transistor sizes have been **optimized w.r.t unit inverter**)	*Ti = 0 Sec*	968.46 pSec	692.46 pSec	892.48 uWatt
	Ti = 1 pSec	666.58 pSec	618.93 pSec	42.73 mWatt
	Ti = 10 pSec	666.68 pSec	620.01 pSec	6.21 mWatt
	Ti = 100 pSec	673.10 pSec	635.71 pSec	1.46 mWatt
	Ti = 300 pSec	672.68 pSec	656.57 pSec	749.59 uWatt

Table 3: Conventional Full Adder when Body terminal shorted to Source terminal

Design- 03. Mirror Adder when body terminal (substrate) of pmos connected to Vdd and of nmos to Vss.

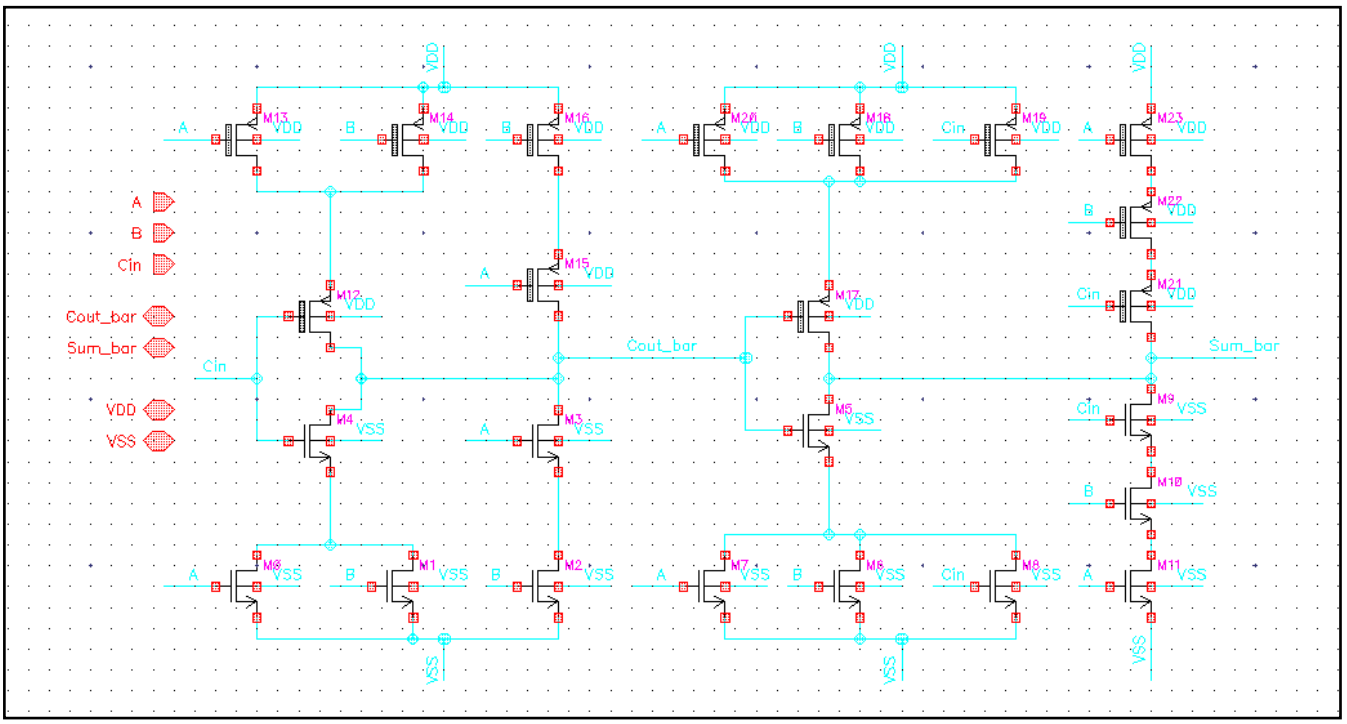


Fig-03 (a):- Schematic for mirror adder when body (pmos) connected to Vdd & body (nmos) to Vss.

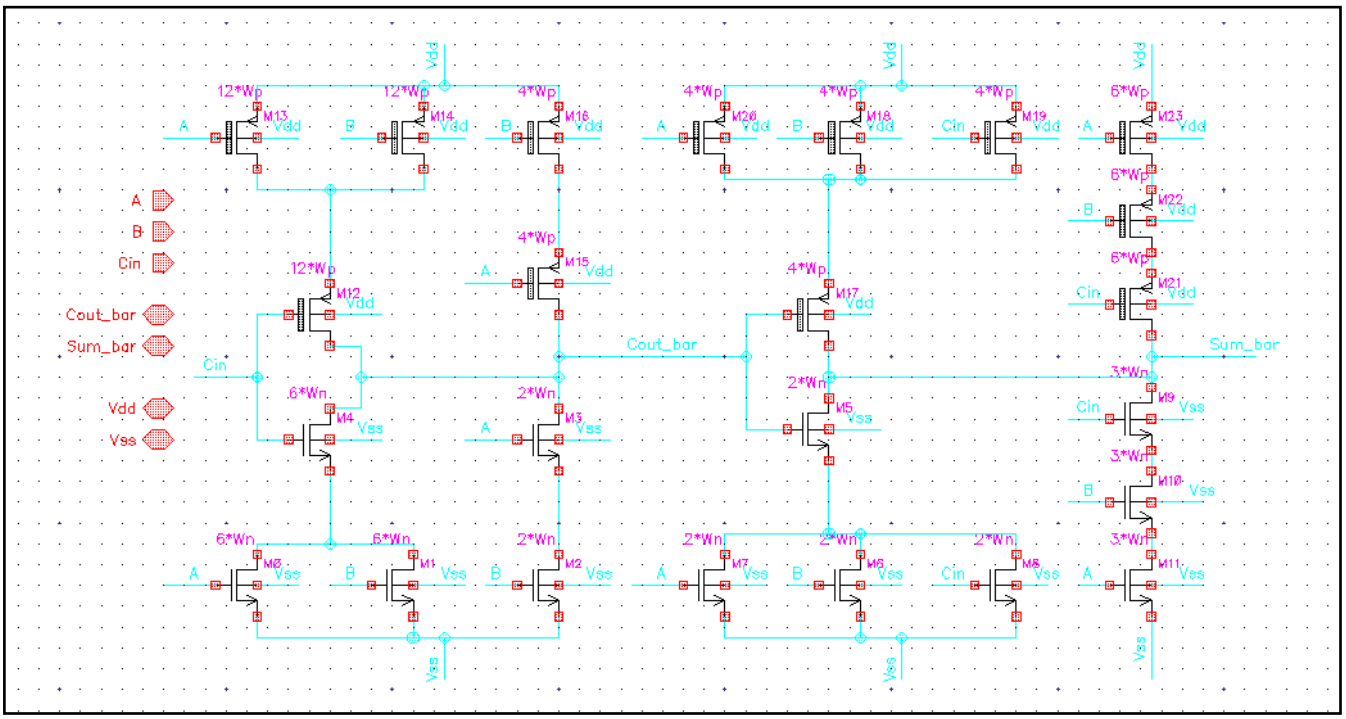


Fig-03 (b):- Schematic design optimized for pMOS and nMOS with respect to standard unit inverter.

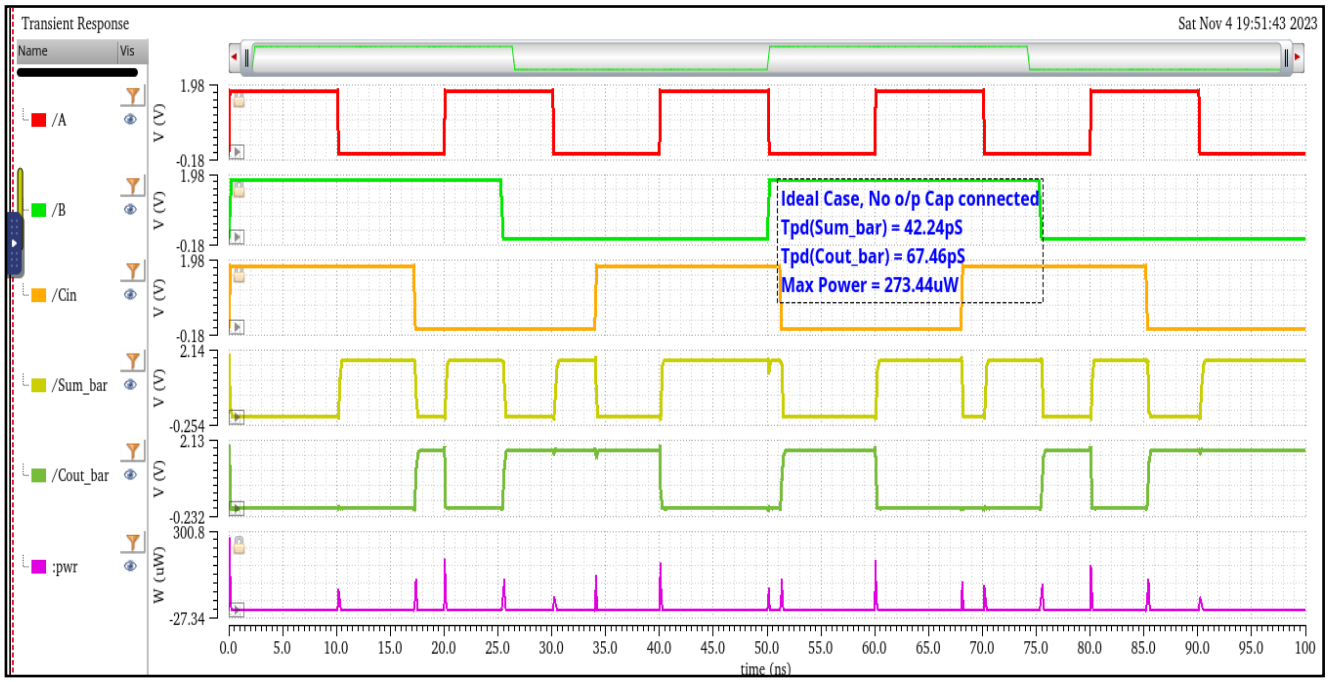


Fig-03 (c):- Transient analysis waveform in Ideal Case.

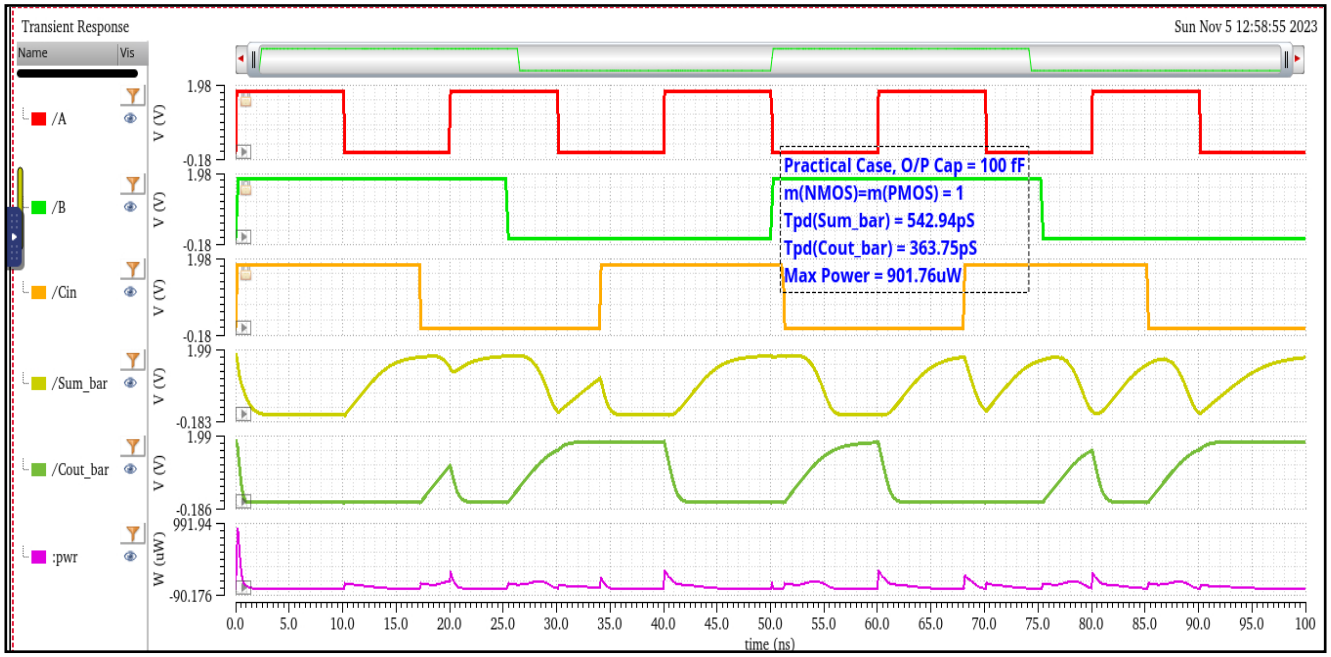


Fig-03 (d):- Transient analysis waveform in Practical Case when width for all MOS are same.

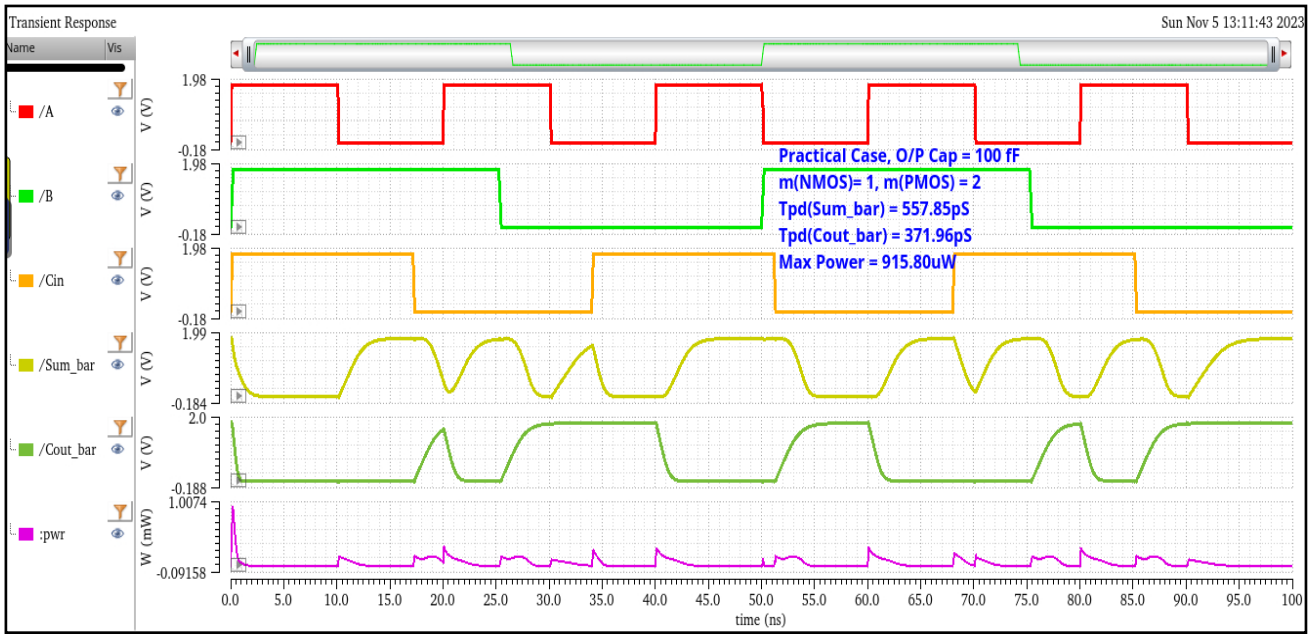


Fig-03 (e):- Transient analysis waveform in Practical Case when width of all pMOS is twice of nMOS.

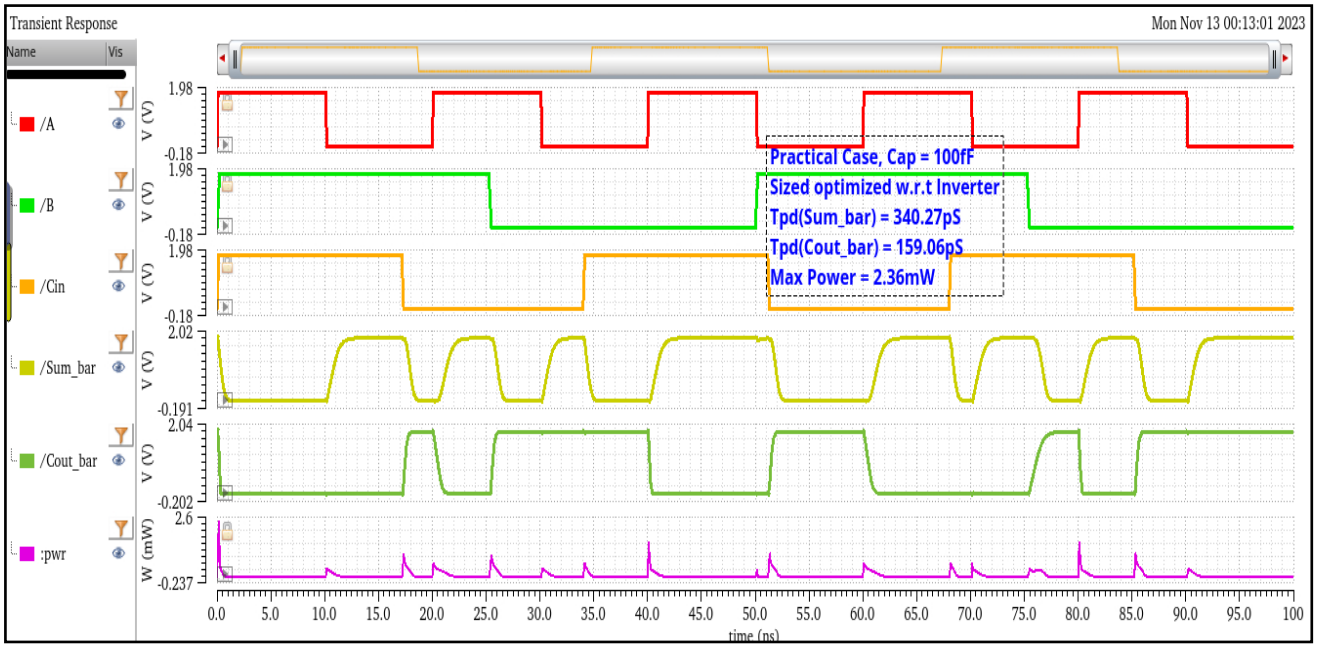


Fig-03 (f):- Transient analysis waveform in Practical Case when width is optimized wrt unit inverter.

Mirror Adder when body of pmos connected to Vdd and body of nmos to Vss				
Different Designs	**Time Delay of Input Pulse (Ti)**	**Time Delay of Sum_bar (Tpd_Sum_bar)**	**Time Delay of Carry_out_bar (Tpd_Cout_bar)**	**Max Power Consumption**
Ideal Design (When no output capacitance considered and all the nMOS and pMOS are of equal size)	*Ti = 0 Sec*	50.35 pSec	77.06 pSec	298.25 uWatt
	Ti = 1 pSec	16.81 pSec	13.82 pSec	2.49 mWatt
	Ti = 10 pSec	18.18 pSec	15.49 pSec	1.66 mWatt
	Ti = 100 pSec	14.82 pSec	28.34 pSec	465.44 uWatt
	Ti = 300 pSec	13.63 pSec	30.36 pSec	239.27 uWatt
Practical Design (When a **100 fF** output capacitance considered and all nMOS and pMOS are of **equal size**)	*Ti = 0 Sec*	542.94 pSec	363.75 pSec	901.67 uWatt
	Ti = 1 pSec	547.95 pSec	277.50 pSec	2.38 mWatt
	Ti = 10 pSec	546.97 pSec	279.86 pSec	1.40 mWatt
	Ti = 100 pSec	536.90 pSec	298.99 pSec	1.11 mWatt
	Ti = 300 pSec	507.918 pSec	341.37 pSec	922.78 uWatt
Practical Design (When a 100 fF output capacitance considered and all pMOS are of twice of nMOS size), **m(pMOS) = 2** and **m(nMOS) = 1**.	*Ti = 0 Sec*	557.85 pSec	371.96 pSec	915.80 uWatt
	Ti = 1 pSec	573.20 pSec	286.35 pSec	2.429 mWatt
	Ti = 10 pSec	570.70 pSec	288.26 pSec	1.445 mWatt
	Ti = 100 pSec	554.32 pSec	307.40 pSec	1.133 mWatt
	Ti = 300 pSec	522.35 pSec	349.70 pSec	938.97 uWatt
Practical Design (When a 100 fF output capacitance considered and all MOS Transistor sizes have been **optimized w.r.t unit Inverter**)	*Ti = 0 Sec*	340.27 pSec	159.06 pSec	2.367 mWatt
	Ti = 1 pSec	294.78 pSec	83.23 pSec	6.78 mWatt
	Ti = 10 pSec	253.08 pSec	85.17 pSec	4.50 mWatt
	Ti = 100 pSec	293.08 pSec	95.17 pSec	3.51 mWatt
	Ti = 300 pSec	303.55 pSec	143.57 pSec	1.98 uWatt

Table 4: Mirror Adder when body of pmos connected to Vdd and body of nmos to Vss.

Design- 04. Mirror Adder when body (substrate) of pmos and nmos connected to source.

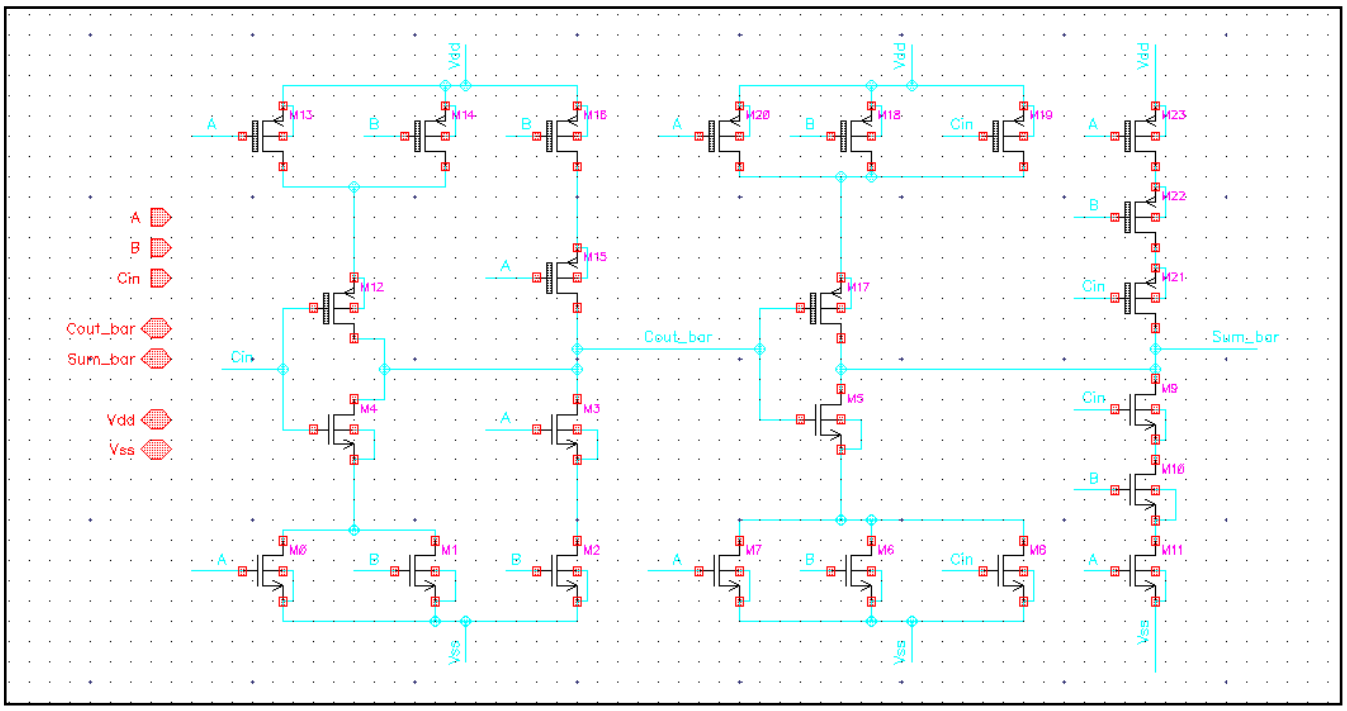


Fig-04 (a):- Schematic for mirror adder when body of pmos and nmos connected to Source.

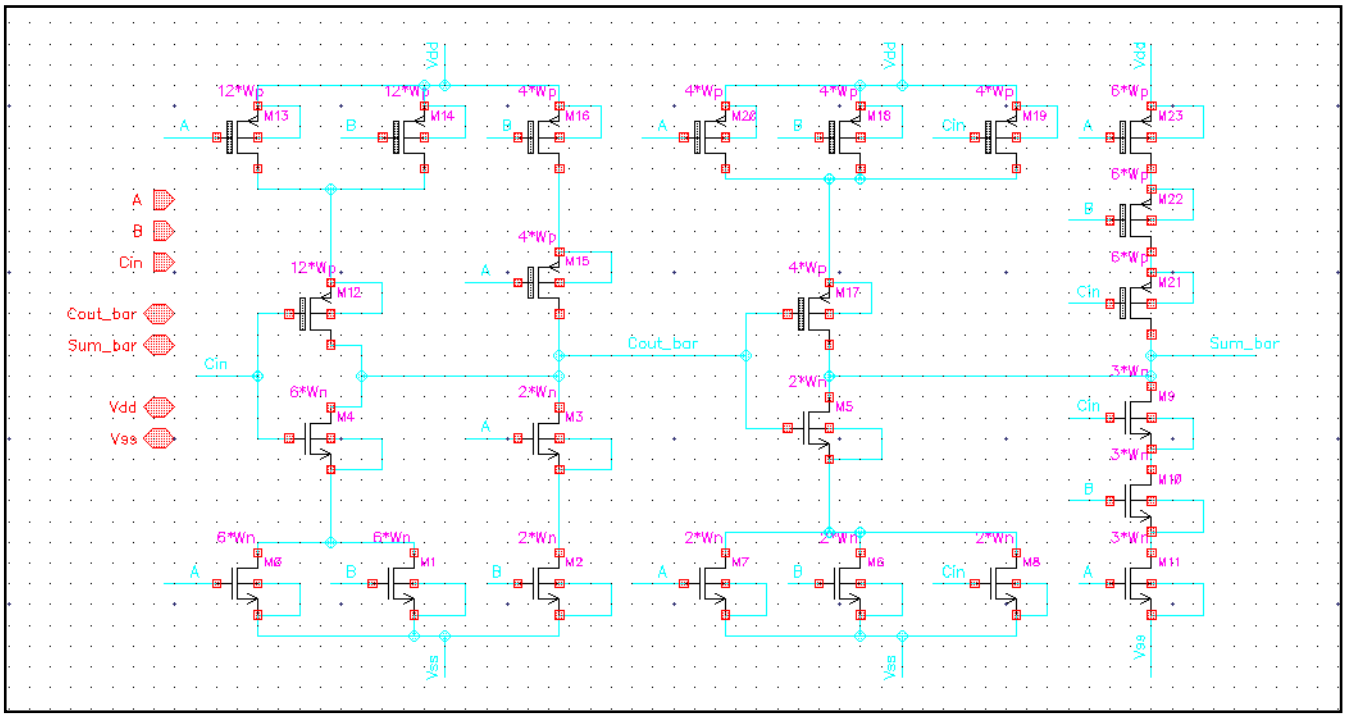


Fig-04 (b):- Schematic design optimized for pMOS and nMOS with respect to standard unit inverter.

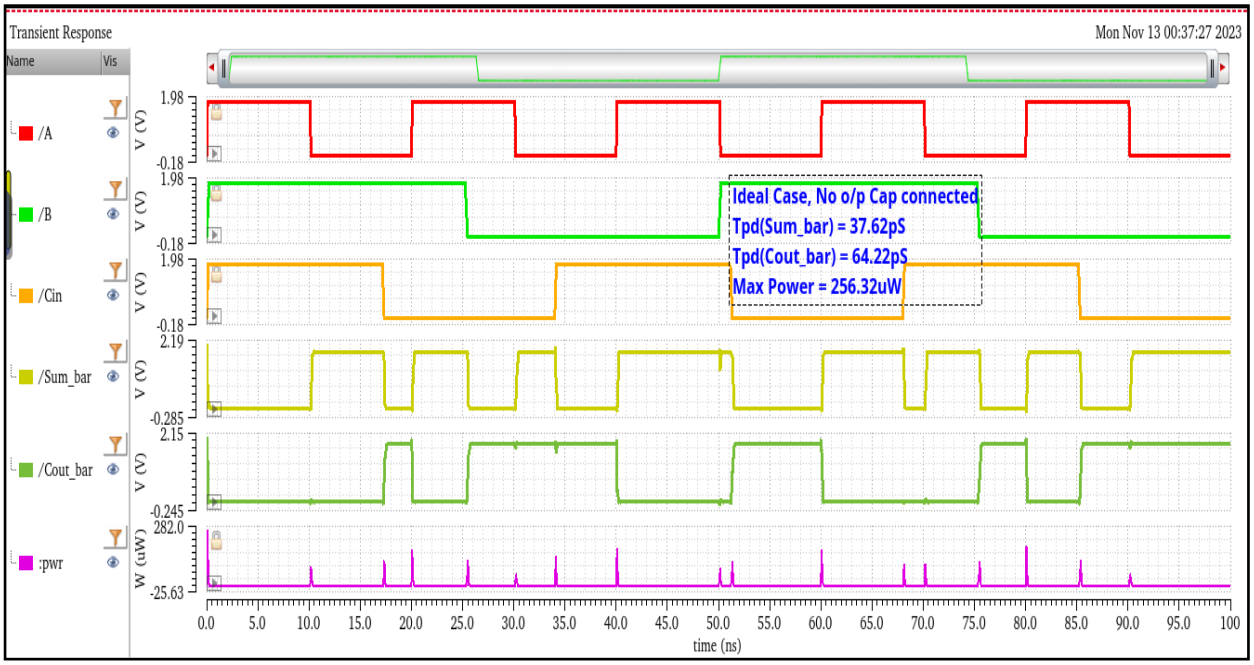


Fig-04 (c):- Transient analysis waveform in Ideal Case for mirror adder.

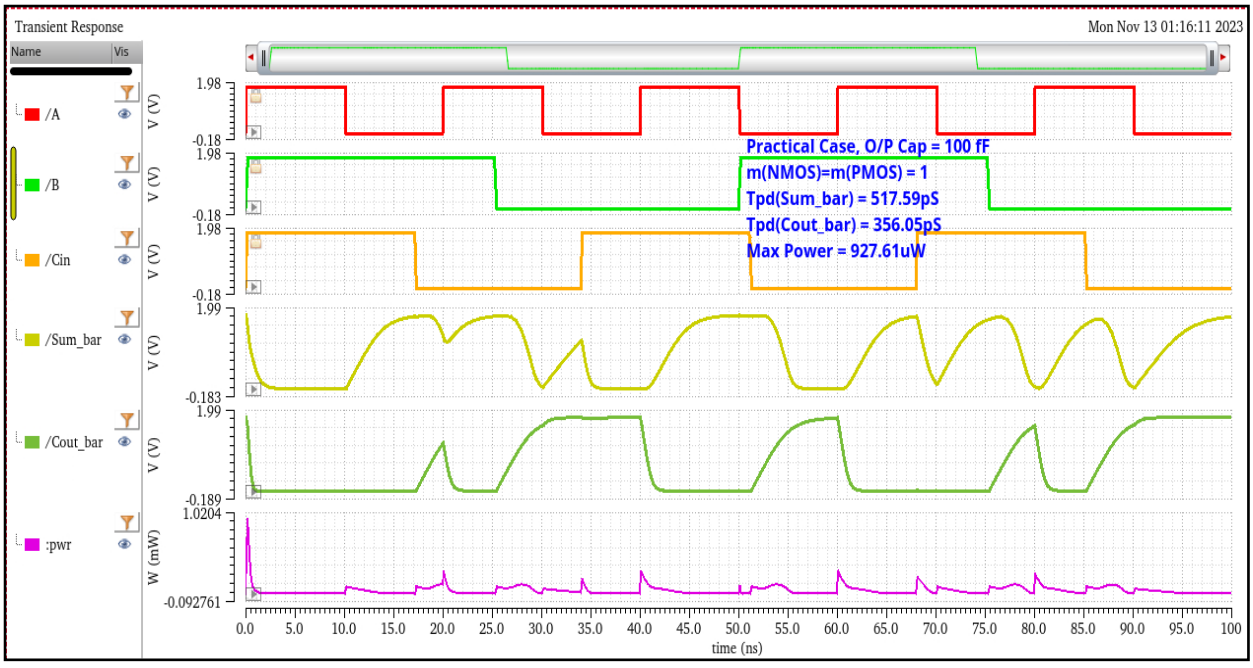


Fig-04 (d):- Transient analysis waveform in Practical Case when width for all MOS are same.

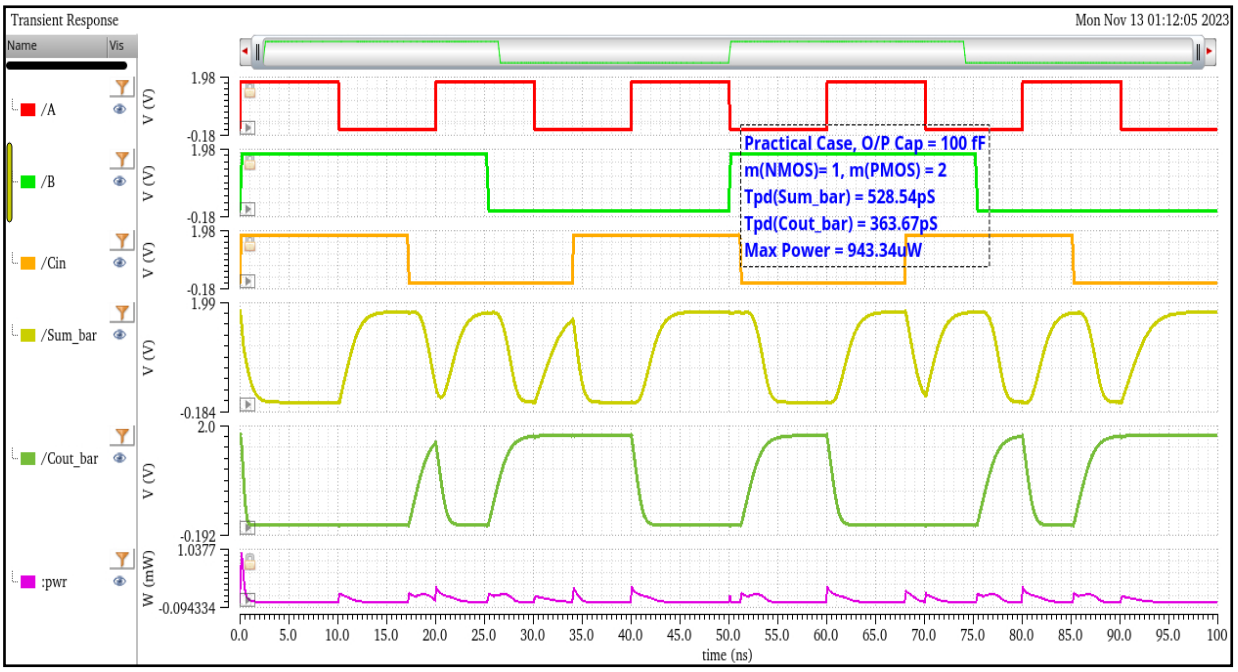


Fig-04 (e):- Transient analysis waveform in Practical Case when width of all pMOS is twice of nMOS.

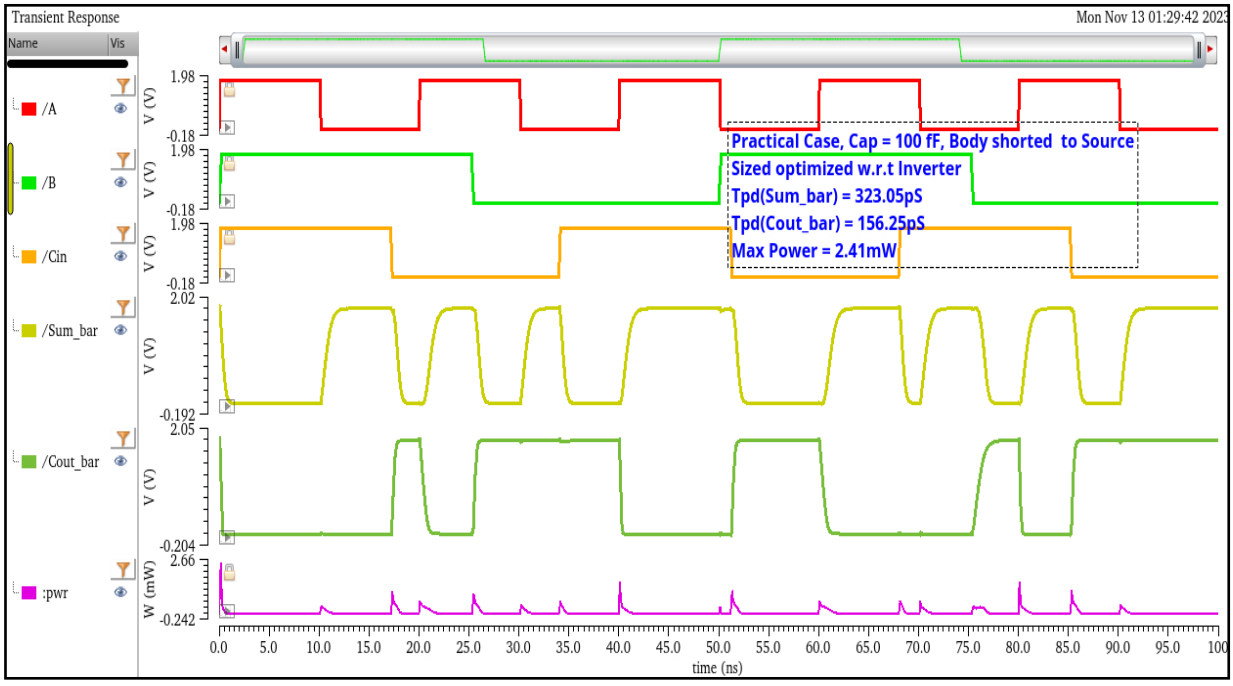


Fig-04 (f):- Transient analysis waveform in Practical Case when width is optimized wrt unit inverter.

Mirror Adder when Body terminal shorted to Source terminal.				
Different Designs	**Time Delay of Input Pulse (Ti)**	**Time Delay of Sum_bar (Tpd_Sum_bar)**	**Time Delay of Carry_out_bar (Tpd_Cout_bar)**	**Max Power Consumption**
Ideal Design (When no output capacitance considered and all the nMOS and pMOS are of equal size)	*Ti = 0 Sec*	37.62 pSec	64.22 pSec	256.32 uWatt
	Ti = 1 pSec	14.62 pSec	14.27 pSec	5.89 mWatt
	Ti = 10 pSec	16.49 pSec	15.46 pSec	2.29 mWatt
	Ti = 100 pSec	22.65 pSec	24.81 pSec	467.17 uWatt
	Ti = 300 pSec	6.82 pSec	21.75 pSec	229.54 uWatt
Practical Design (When a **100 fF** output capacitance considered and all nMOS and pMOS are of **equal size**)	*Ti = 0 Sec*	517.59 pSec	356.05 pSec	927.61 uWatt
	Ti = 1 pSec	517.36 pSec	270.11 pSec	3.22 mWatt
	Ti = 10 pSec	517.08 pSec	271.87 pSec	1.68mWatt
	Ti = 100 pSec	508.06 pSec	290.81 pSec	1.15 mWatt
	Ti = 300 pSec	482.21 pSec	332.92 pSec	945.44 uWatt
Practical Design (When a 100 fF output capacitance considered and all pMOS are of twice of nMOS size), **m(pMOS) = 2** and **m(nMOS) = 1**.	*Ti = 0 Sec*	528.54 pSec	363.67pSec	943.34 uWatt
	Ti = 1 pSec	535.35 pSec	277.36 pSec	4.21 mWatt
	Ti = 10 pSec	534.44 pSec	279.62 pSec	1.73 mWatt
	Ti = 100 pSec	519.79 pSec	299.19 pSec	1.17 mWatt
	Ti = 300 pSec	491.72 pSec	340.85 pSec	963.11 uWatt
Practical Design (When a 100 fF output capacitance considered and all MOS Transistor sizes have been **optimized w.r.t unit Inverter**)	*Ti = 0 Sec*	323.05 pSec	156.25 pSec	2.41 mWatt
	Ti = 1 pSec	270.44 pSec	81.08 pSec	13.21 mWatt
	Ti = 10 pSec	270.03 pSec	83.16 pSec	5.35 mWatt
	Ti = 100 pSec	271.89 pSec	101.03 pSec	3.45 mWatt
	Ti = 300 pSec	284.25 pSec	140.24 pSec	2.01 uWatt

Table 5: Mirror Adder when Body terminal shorted to Source terminal.

I have analyzed **four different configurations** of full adder and mirror adder and their performance parameters like propagation delay for both Sum and Carry and power consumption under varying condition of input signal characteristics (varying tr = tf =Ti) and adjusting the widths(Wn and Wp) of MOS transistors has been recorded in tabular form.

By observing the all data of the tables I have drawn following conclusion-

- When the load capacitance is taken into account at the output of a full adder for both the Sum and Carry signals, the propagation delays of the Sum and Carry signals increase and that results in more power consumption comparing the ideal case where I have not considered any load capacitance.
- When width ratio of pMOS and nMOS are same and a load capacitance is connected at outputs then in this case circuit takes more time to reach the output in steady state.
- As I increase the driving strength of pMOS as compared to nMOS the time to reach the output at steady state becomes less because as driving strength increases propagation delay decreases and at the same time power consumption increases.

Till now I have already learned that if I increase width ratio of MOS transistor the time delay decreases but at the same time power consumption increases. But as we know, we cannot design our circuit **only on** the basis of power consumption or propagation delay. In digital circuit design **"power-delay product"** is an important parameter and for optimum design we have to make the overall power-delay product to minimum level. This is the reason we have to make a trade-off between power consumption and propagation delay so that our power-delay product remain under controllable limit and we get optimum performance of digital circuits.

Considering all the constraints discussed above I have designed my circuits in **Cadence Virtuoso** where I have optimized the width ratio of all MOS according to circuit configuration of adder so that equal resistance is achieved of each path. So I can conclusively say that an adder design where I have adjusted the width ratio of pMOS and nMOS (Considering the basic unit CMOS Inverter circuit), it's found that "power-delay" product is optimum (minimum) for this design and it is giving better performance as compared to those circuit where pMOS and nMOS width are not adjusted accordingly. **The layout and post simulation result of these optimum designs are recorded below:-**

<4> LAYOUT AND POST-LAYOUT SIMULATION

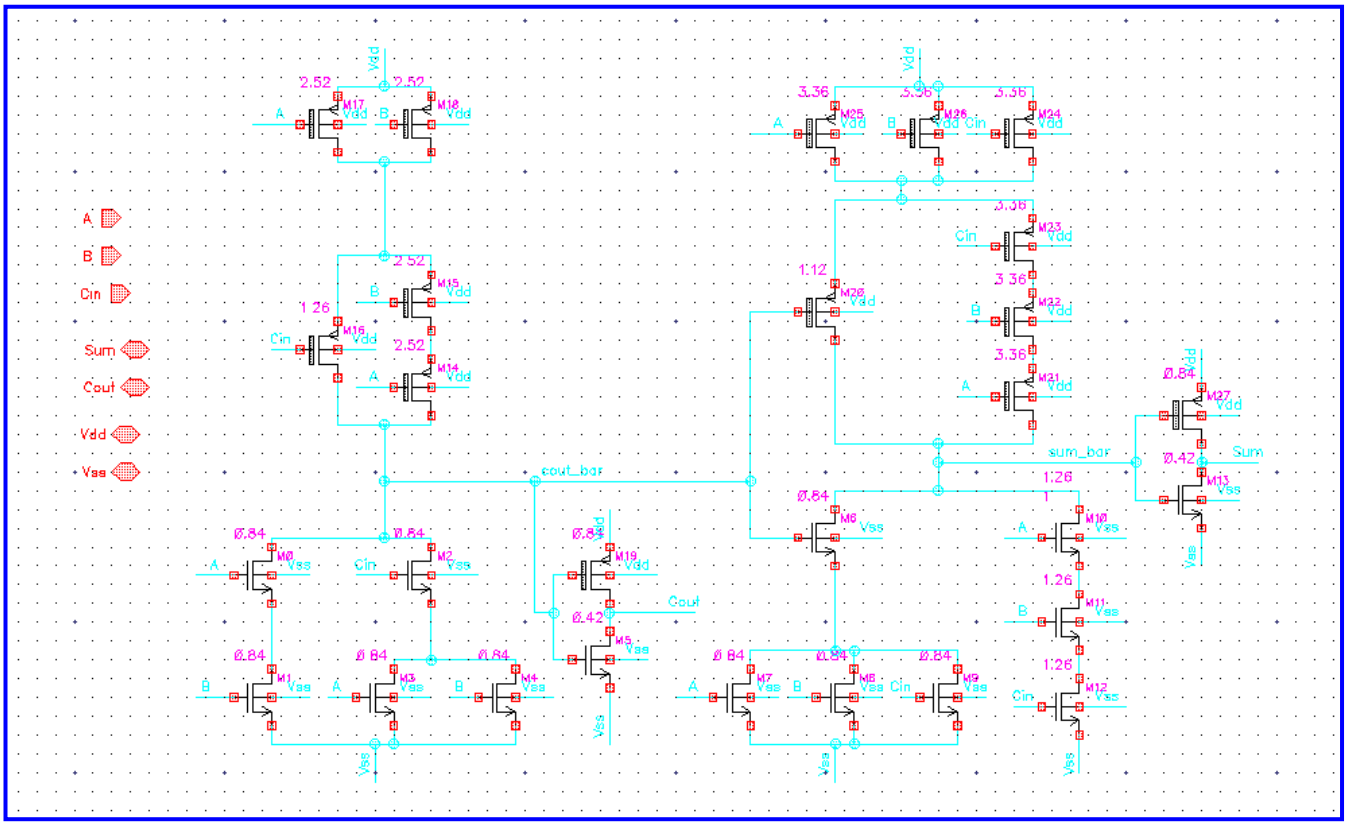


Fig-05 (a):- Full Adder Schematic for optimum design when body (pmos) connected to Vdd & body (nmos) connected to Vss.

In this schematic (fig-05.a) width of each pMOS and nMOS are defined as multiple of 0.42 um (420nm) according to the circuit configuration considering basic unit CMOS Inverter so that equal resistance is achieved of each path.

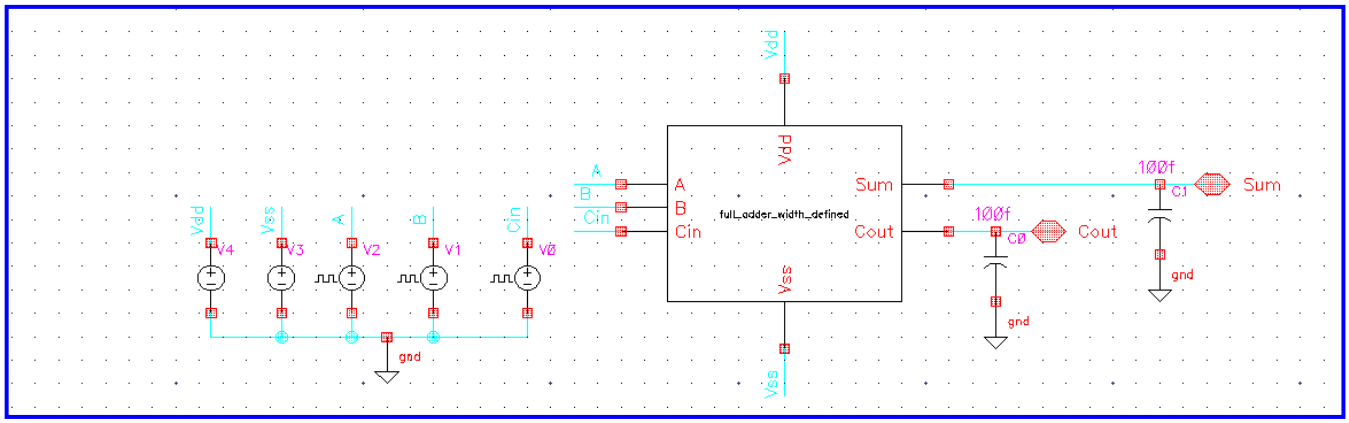


Fig-05 (b):- Test bench in Practical Case for optimum design when 100fF capacitance considered at output.

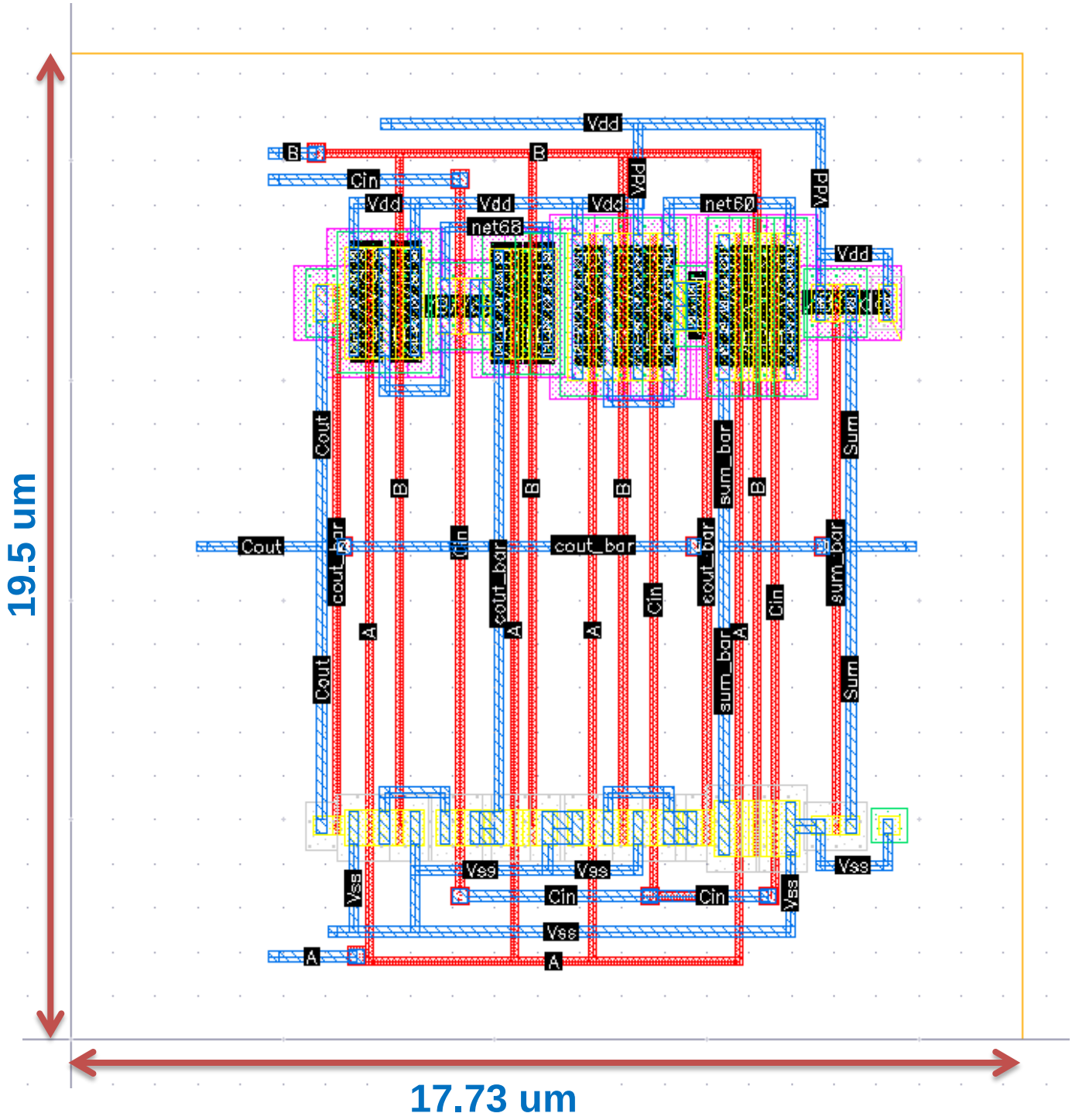


Fig-05 (c):- Layout of full adder for optimum design.

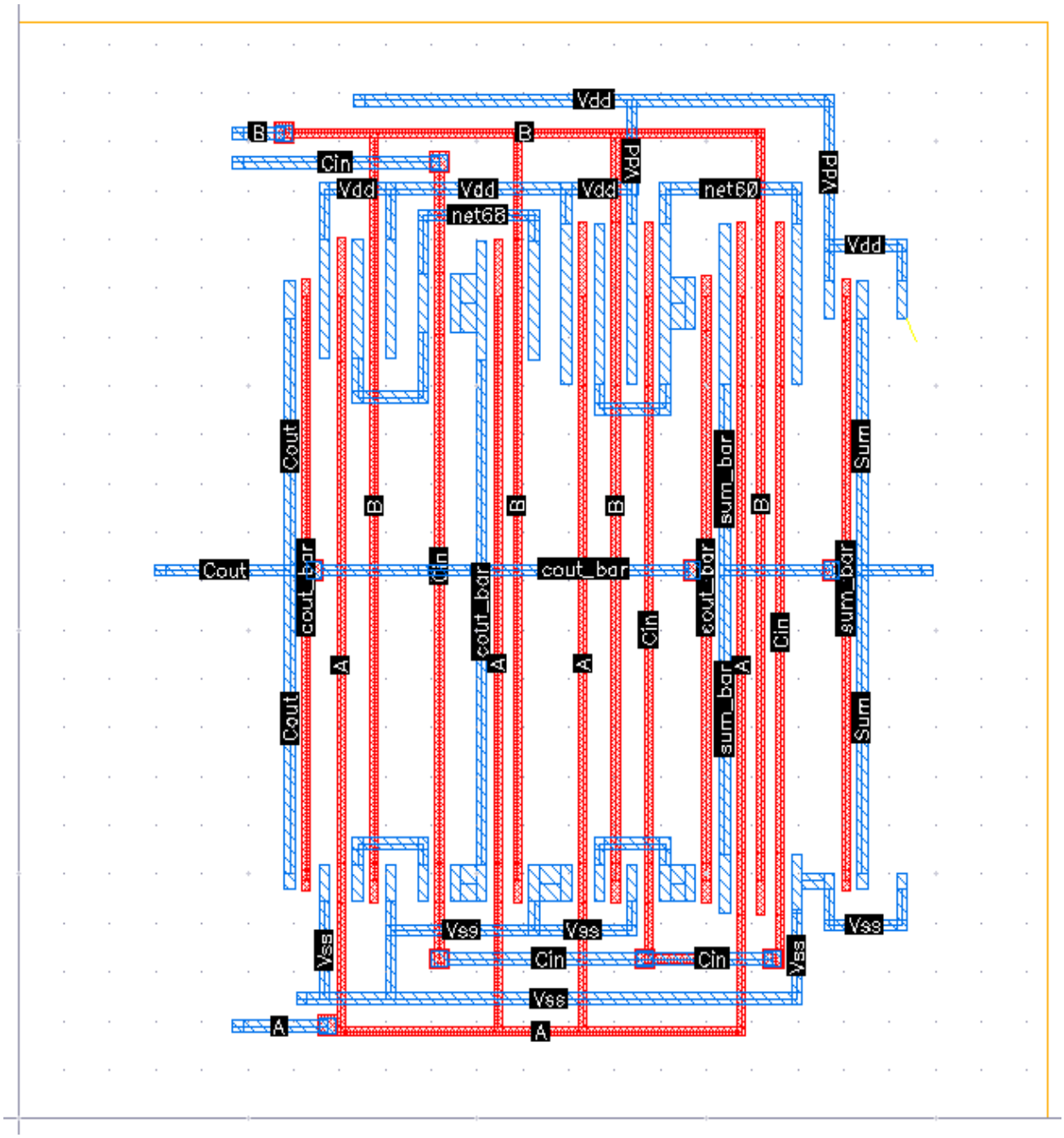


Fig-05 (d):- Layout with polysilicon, metal layer and contacts only for optimized full adder.

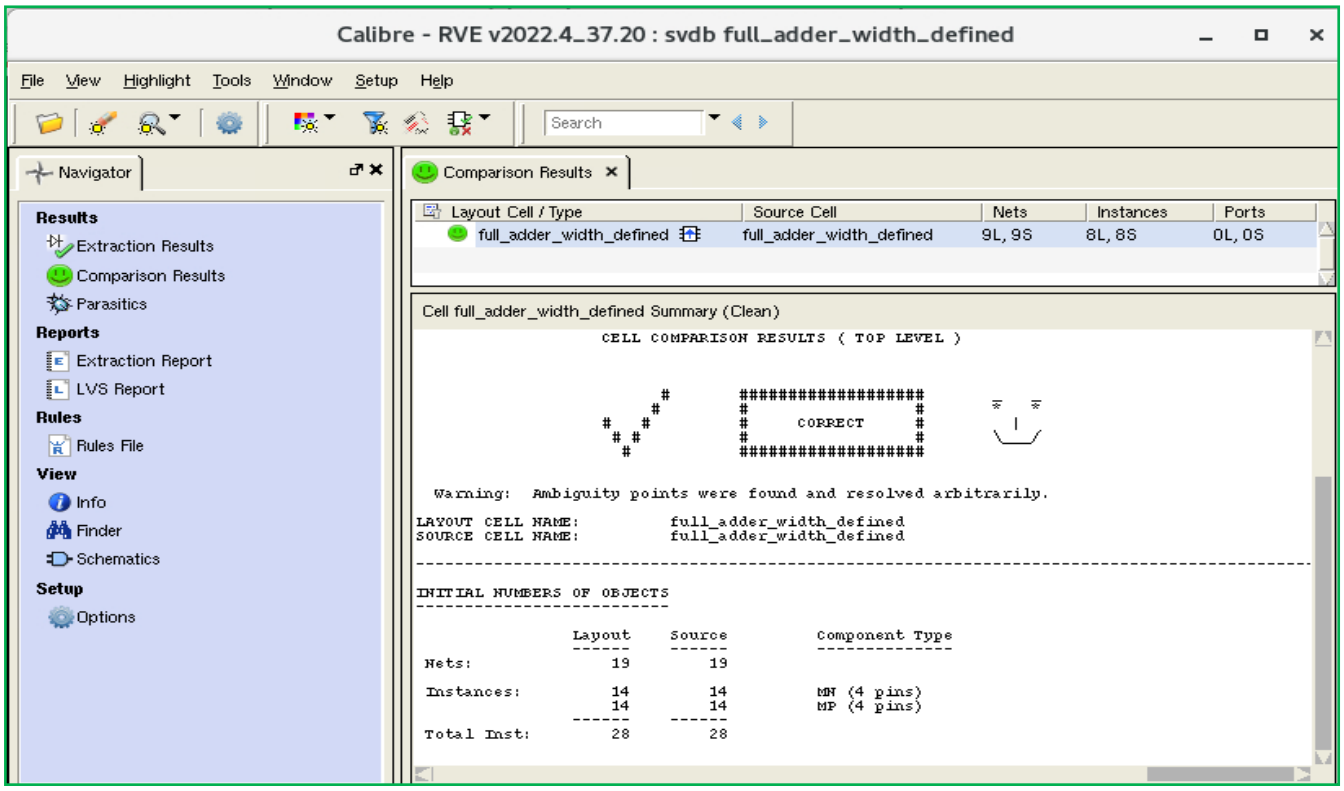


Fig-05 (e):- LVS (Layout vs Schematic) Report verification for optimized full adder design.

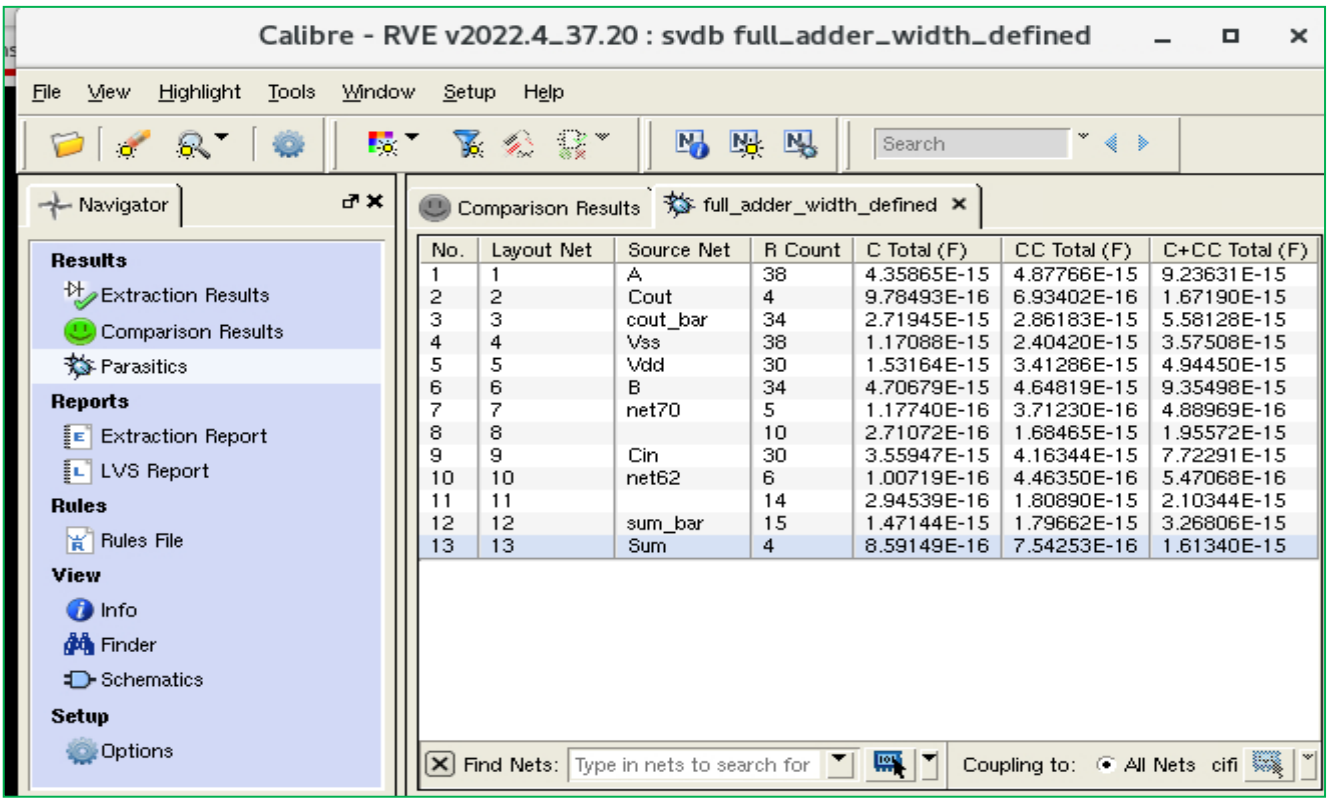


Fig-05 (f):- Parasitics Extraction Report for optimized full adder design.

ADEL (Advanced Design Environment for Logics) Window

Outputs

	Name/Signal/Expr	Value	Plot	Save
1	A		☑	☐
2	B		☑	☐
3	Cin		☑	☐
4	Sum		☑	☐
5	Cout		☑	☐
6	Tpd_Sum	647.415p	☑	☑
7	Tpd_Cout	626.103p	☑	☑
8	Max Power	963.083u	☑	☑

(i) Pre-Layout Simulation Result

Outputs

	Name/Signal/Expr	Value	Plot	Save
1	A		☑	☐
2	B		☑	☐
3	Cin		☑	☐
4	Sum		☑	☐
5	Cout		☑	☐
6	Tpd_Sum	662.515p	☑	☑
7	Tpd_Cout	651.184p	☑	☑
8	Max Power	972.235u	☑	☑

(ii) Post-Layout Simulation Result

Fig-05 (g):- Propagation Delay and Power Consumption in **Pre-Layout Simulation** and **Post-Layout Simulation** respectively for optimized full adder design.

The data obtained in ADEL shows that there is an increment in Propagation delay and Power loss in Post-Layout Simulation result as compared to Pre-Layout Simulation result and the reason behind this increment is parasitic components consideration which is shown below in the graph.

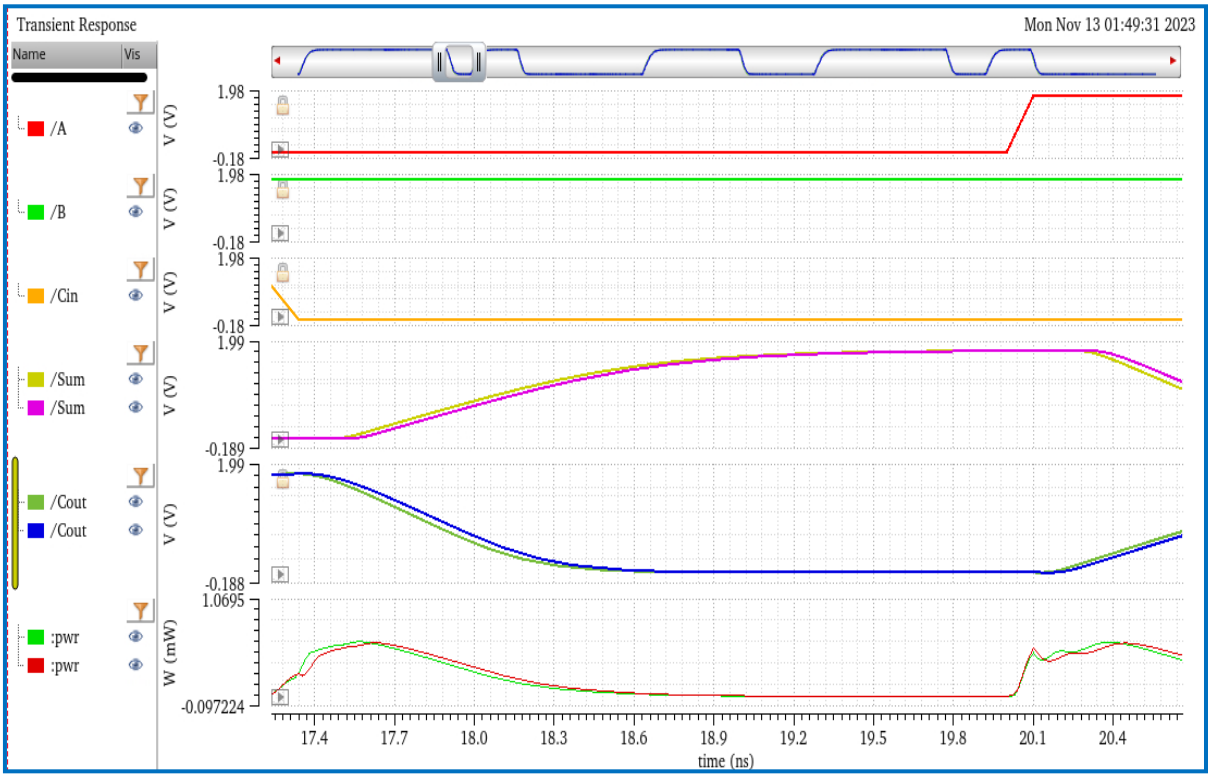


Fig-05 (h):- Comparison of Propagation Delay and Power Consumption in **Pre-Layout Simulation** and **Post-Layout Simulation** respectively for optimized full adder design.

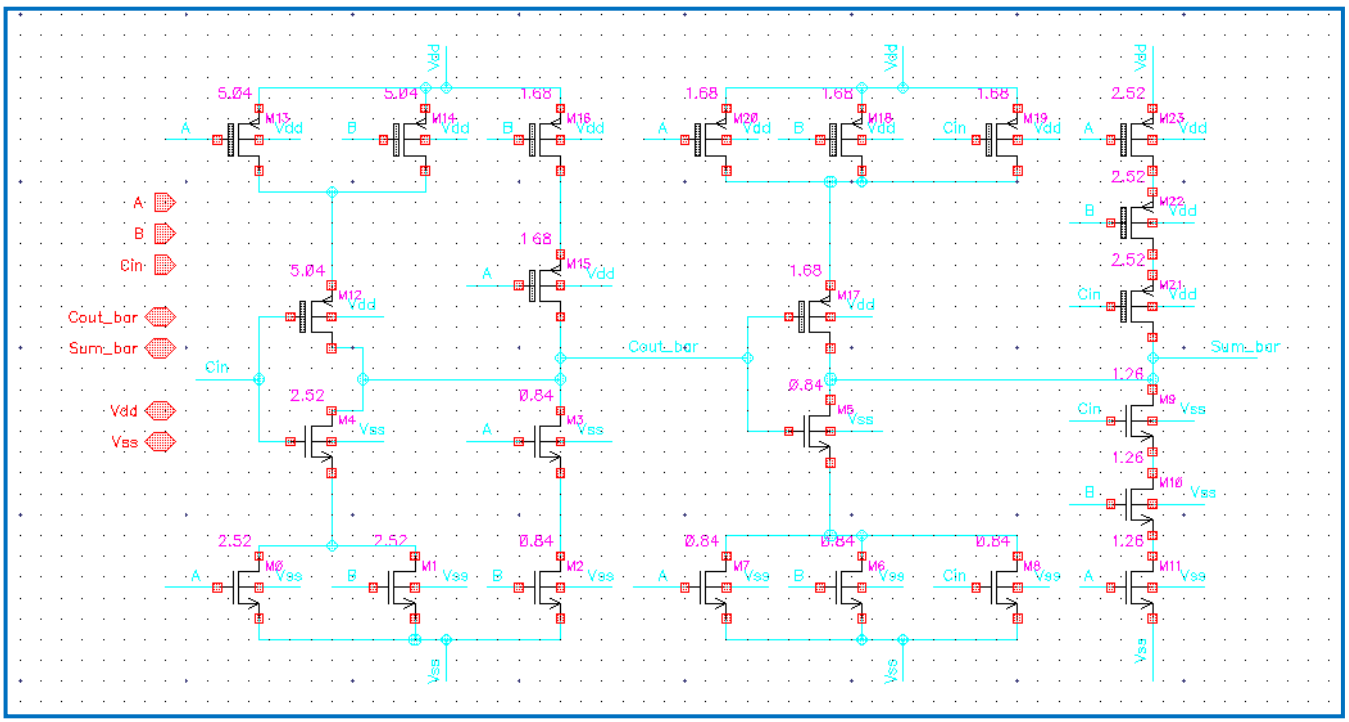


Fig-05 (i):- Mirror Adder Schematic for optimum design when body (pmos) connected to Vdd & body (nmos) connected to Vss.

In this schematic (fig-05.h) width of each pMOS and nMOS are defined as multiple of 0.42 um (420nm) according to the circuit configuration considering basic unit CMOS Inverter so that equal resistance is achieved of each path.

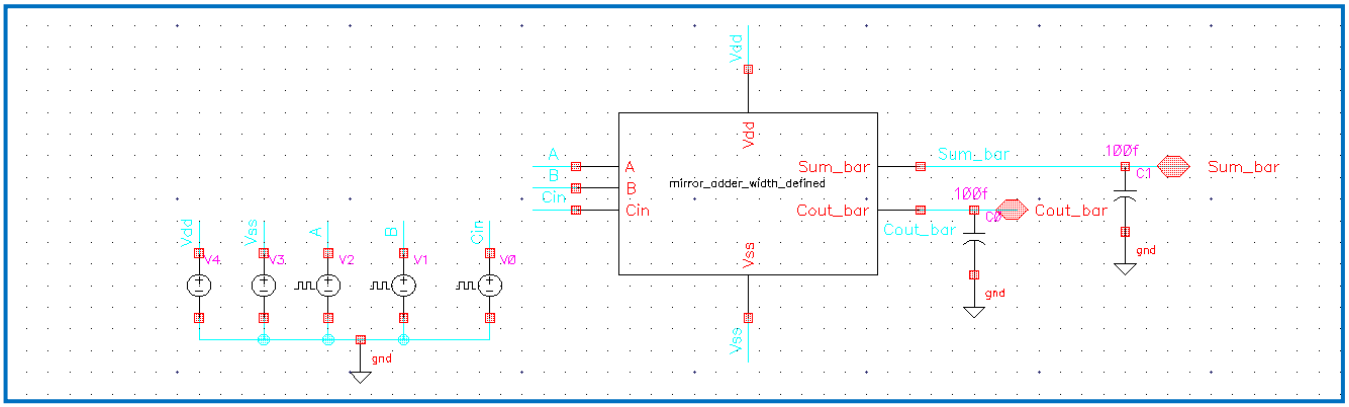


Fig-05 (j):- Test bench in Practical Case for optimum design when 100fF capacitance considered at output.

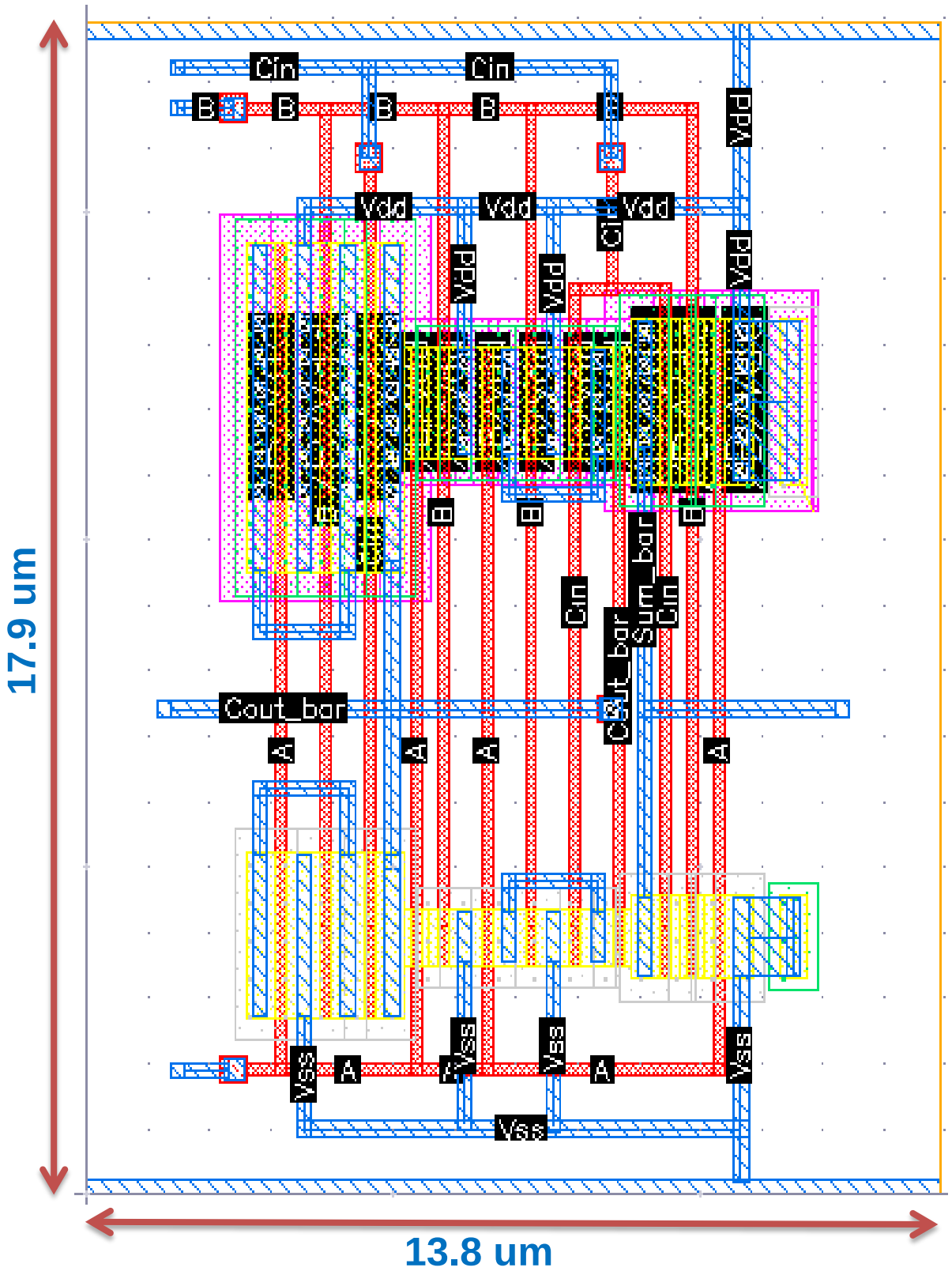


Fig-05 (k):- Layout of mirror adder for optimum design.

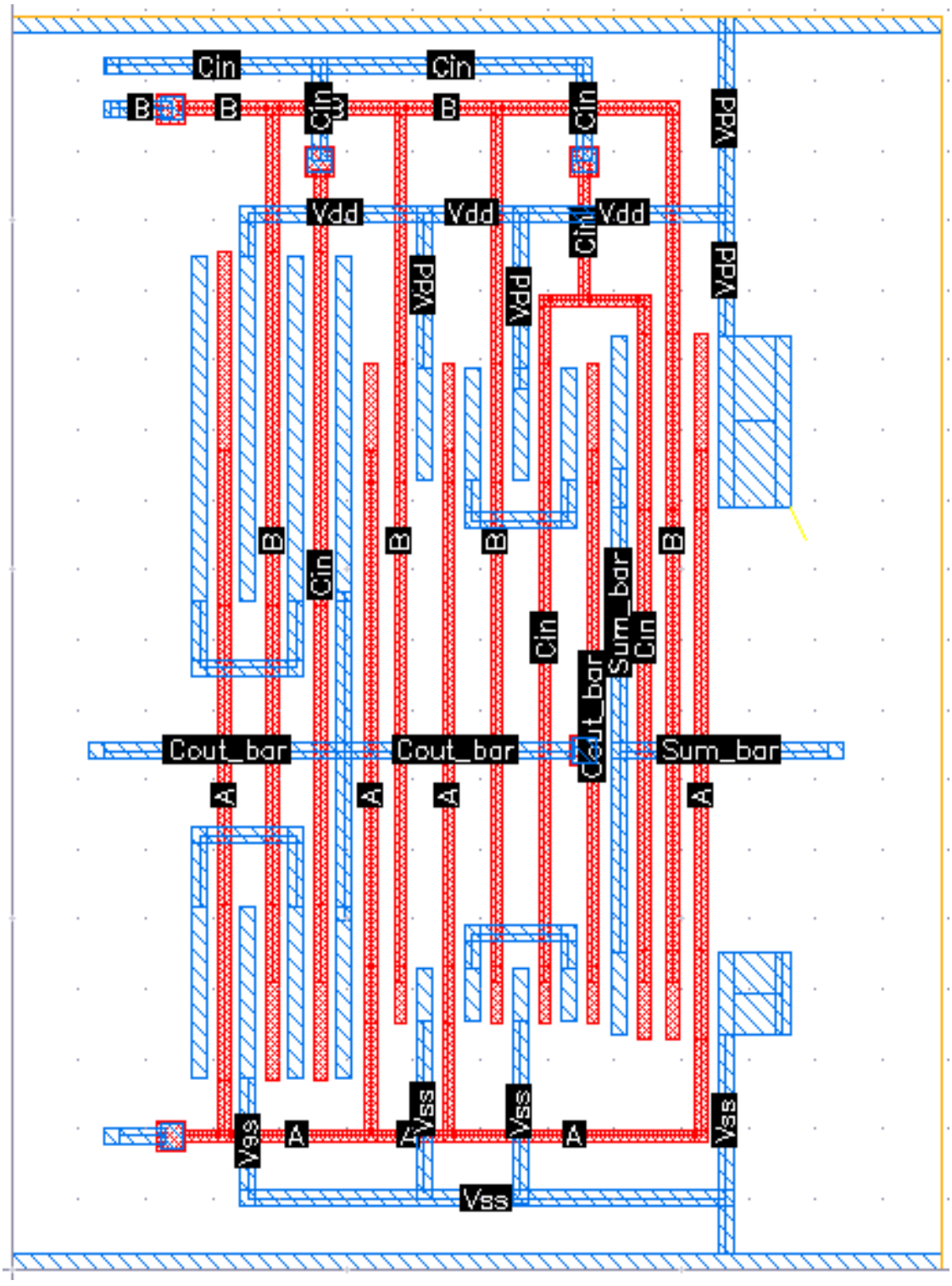


Fig-05 (l):- Layout with polysilicon, metal layer and contacts only for optimized Mirror adder.

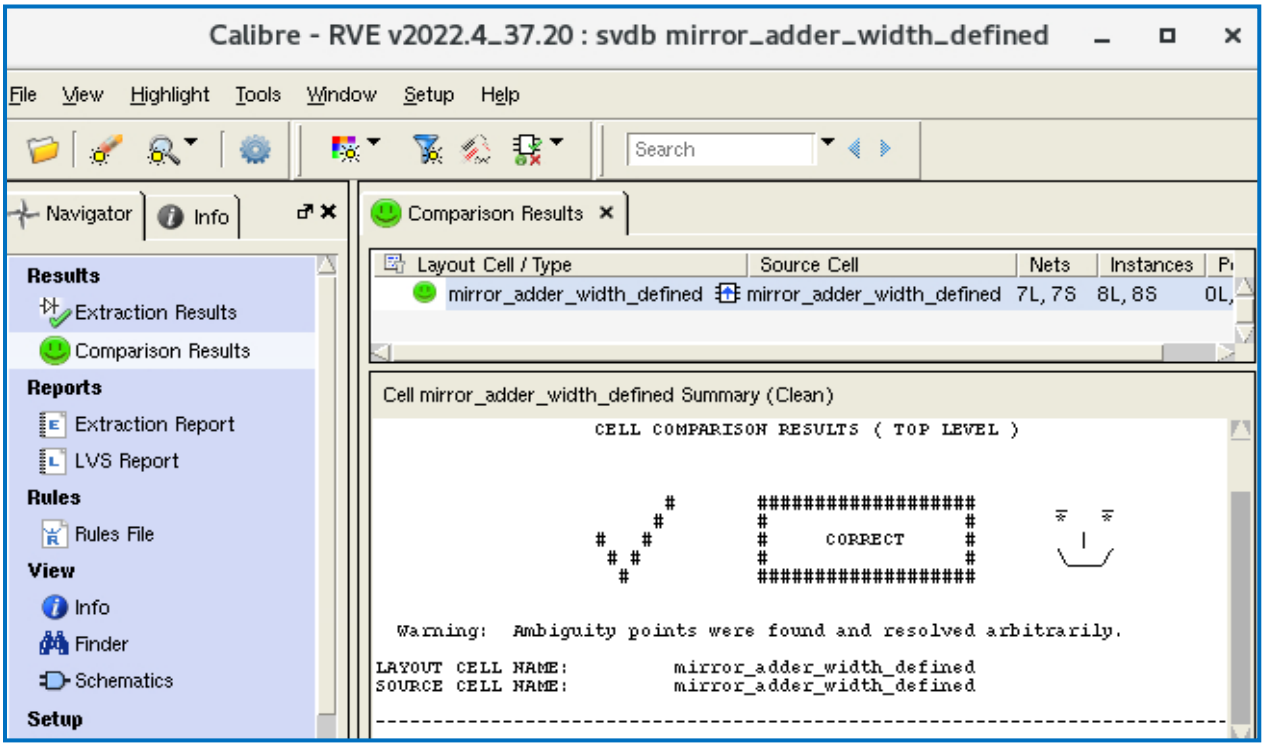


Fig-05 (m):- LVS (Layout vs Schematic) Report verification for optimized Mirror adder design.

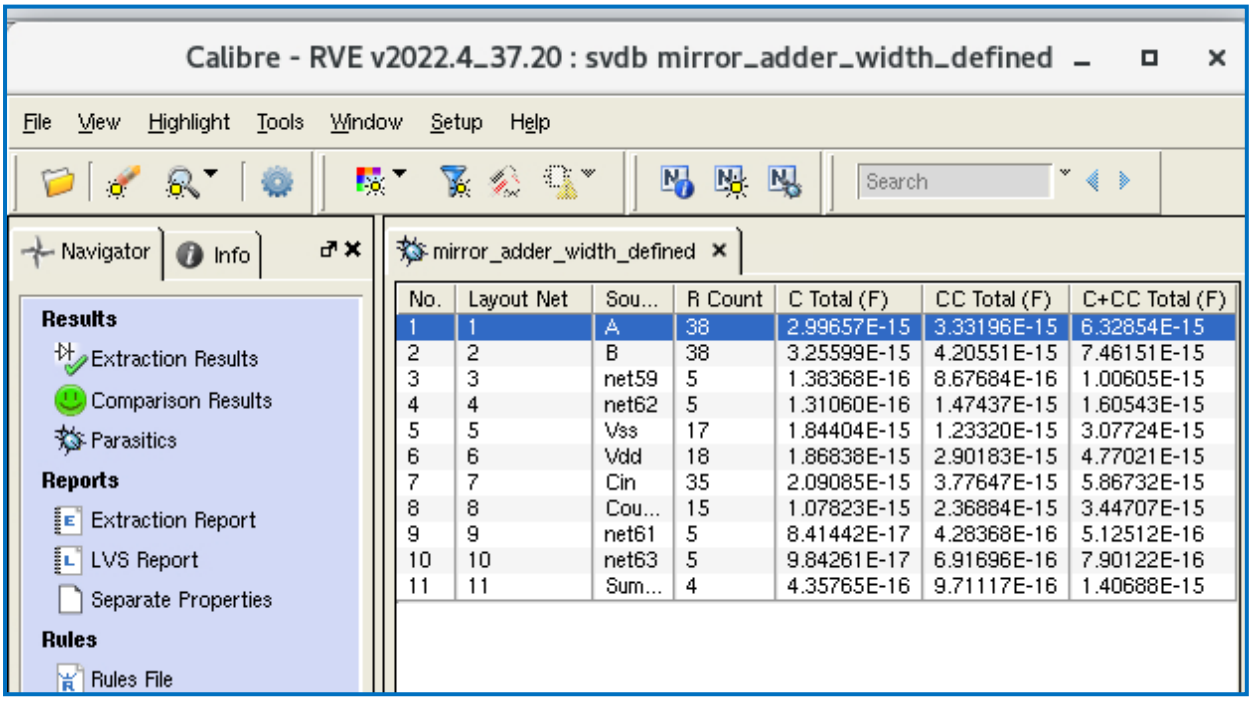


Fig-05 (n):- Parasitics Extraction Report for optimized Mirror adder design.

ADEL (Advanced Design Environment for Logics) Window

Outputs

	Name/Signal/Expr	Value	Plot	Save
1	A		✓	✓
2	B		✓	✓
3	Cin		✓	✓
4	Sum_bar		✓	✓
5	Cout_bar		✓	✓
6	Tpd_Sum_bar	340.279p	✓	✓
7	Tpd_Cout_bar	159.065p	✓	✓
8	Max Power	2.36787m	✓	✓

(i) Pre-Layout Simulation Result

Outputs

	Name/Signal/Expr	Value	Plot	Save
1	A		✓	✓
2	B		✓	✓
3	Cin		✓	✓
4	Sum_bar		✓	✓
5	Cout_bar		✓	✓
6	Tpd_Sum_bar	337.556p	✓	✓
7	Tpd_Cout_bar	165.148p	✓	✓
8	Max Power	2.4223m	✓	✓

(ii) Post-Layout Simulation Result

Fig-05 (o):- Propagation Delay and Power Consumption in **Pre-Layout Simulation** and **Post-Layout Simulation** respectively for optimized Mirror adder design.

The data obtained in ADEL shows that there is an increment in Power-delay product in Post-Layout Simulation result as compared to Pre-Layout Simulation result and the reason behind this increment is parasitic components consideration which is shown below in the graph.

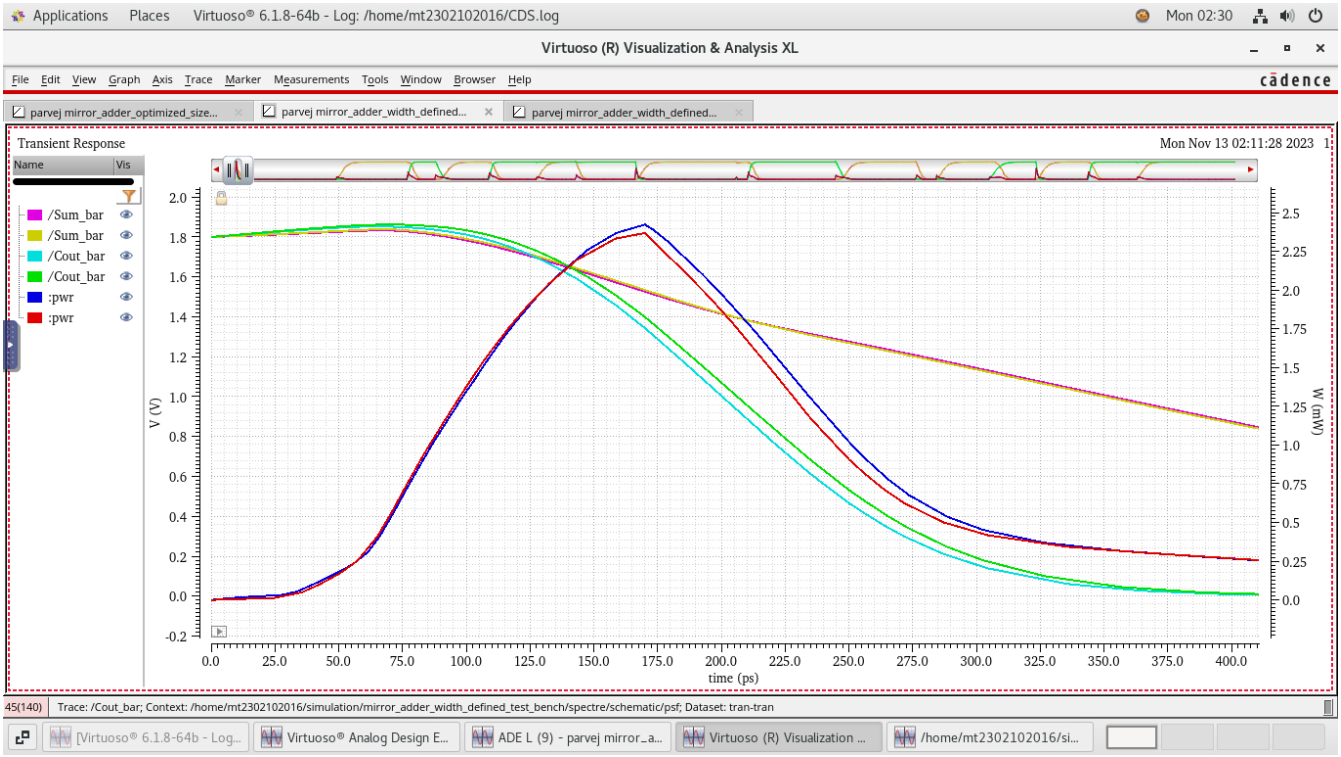


Fig-05 (p):- Comparison of Propagation Delay and Power Consumption in **Pre-Layout Simulation** and **Post-Layout Simulation** respectively for optimized Mirror adder design.

<5> RESULT AND COMPARISON

The performance of conventional adder and mirror adder can be compared in terms of **power**, **area**, **delay**, and **power-delay product**. Here are some points to consider:

- Power: A mirror adder consumes less power than a conventional adder, because it has fewer transistors and lower input capacitance. According to Fig:5(o)(ii) and Fig:5(g)(ii), a mirror adder consumes **972.235 uWatt** of power at 1.8 V supply voltage, while a conventional adder consumes **2.422 mWatt** of power at the same voltage. This means that a mirror adder saves power consumption compared to a conventional adder.

- Area: The mirror adder is more optimized than the conventional adder in terms of area. It occupies less area than a conventional adder, because it has fewer transistors and lower output loading. According to Fig-5(k) and Fig-5(c)**,** a mirror adder occupies **247.02 um^2** of area, while a conventional adder occupies **345.73 um^2** of area. This means that a mirror adder saves about 28.55% of area compared to a conventional adder.

- Delay: A mirror adder has Lower delay than a conventional adder, because it has longer carry propagation path and higher output resistance for some/most case. According to Fig-5(o)(ii) and Fig-5(g)(ii), a mirror adder has **0.337 nsec delay for sum** and **0.165 nsec of delay for cout** at 1.8 V supply voltage, while a conventional adder has **0.622 ns of delay for sum** and **0.652 nsec delay for cout** at the same voltage. This means that a mirror adder is faster than a conventional adder.

- Speed: Nmos and Pmos chains are completely symmetrical in mirror adder schematic, This guarantees identical rising and falling timing if the Nmos and Pmos devices are properly sized, that result faster speed than the conventional adder in most cases.

- Power-Delay product scenario: The power delay product scenario for both conventional and mirror adders is such that it is optimum for mirror adder as compared to conventional full adder . In case of mirror adder power delay product is calculated and it is found to be **0.399 pJoule** and in case of mirror adder and in case of conventional full adder it is **0.6434 pJoule** . Thus we can say that mirror adder design is superior to conventional full adder.

<6> CONCLUSION

In conclusion, the "**Comparing Performance of Conventional Adder and Mirror Adder in Terms of Power, Area, Delay, and Power-Delay Product Scenario Using Cadence**" project provides a comprehensive examination of these adder designs, enabling informed decisions regarding their deployment in digital circuits and offering insights into the broader realm of power-efficient, area-optimized, and low-delay digital design practices.

The advantage of using a mirror adder is that it reduces the number of transistors by four compared to a conventional full adder. This means that it has lower area, lower input capacitance, lower output loading, and lower switching power. The disadvantage of using a mirror adder is that it has some issues related to dynamic logic, such as charge sharing, charge leakage, noise margin, clock feed through, and input restrictions. Therefore, a mirror adder requires careful design and optimization to overcome these challenges.

Full Adder can be relatively power-hungry and slower compared to more optimized designs like the mirror adder. Complementary transistor pairs make the circuit layout straight forward. CMOS (Conventional CMOS Full Adder) generates carry through a static gate. The advantage of using CCMOS is that it has layout regularity, high noise margins and stability at low voltage due to complementary transistor pair and smaller number of interconnecting wires and disadvantage is that it uses Cout signal to generate sum which produces an unwanted additional delay. It has weak o/p driving capability due to series transistors in output stage and consumes more power and large silicon area.

The structure of the mirror adder allows for high-speed addition of binary numbers by generating both the carry and sum outputs in a compact and efficient manner using transistor circuits. The mirror adder is particularly popular for its high-speed operation and compact structure.

In summary, both the conventional full adder and the mirror adder serve the same purpose of binary addition. The conventional full adder uses logic gates for its operation, providing flexibility, while the mirror adder uses transistor-based circuits, specifically CMOS technology, to achieve high-speed and efficient addition operations. The choice between these two designs depends on the specific requirements of the application, with the mirror adder being a more efficient and faster choice for arithmetic operations.

<7> FUTURE WORK

This project has practical implications for digital circuit design, as it explores the potential benefits of adopting the mirror adder design over the conventional full adder. Improved performance metrics could lead to more efficient and energy-conscious digital systems.

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