ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

Call for Papers
ASP-DAC 2020

http://www.aspdac.com/
January 13-16, 2020
China National Convention Center (CNCC)
Beijing, China

Aims of the Conference:
ASP-DAC 2020 is the 25th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:
Original papers in, but not limited to, the following areas are invited.

[1] System-Level Modeling and Design Methodology:
1.1. HW/SW co-design, co-simulation and co-verification
1.2. System-level design exploration, synthesis, and optimization
1.3. System-level formal verification
1.4. System-level modeling, simulation and validation tools/methodology

[2] Embedded Systems and Cyberphysical Systems:
2.1. Many- and multi-core SoC architecture
2.2. IP/platform-based SoC design
2.3. Domain-specific architecture
2.4. Dependable architecture
2.5. Cyber physical system
2.6. Internet of things

[3] Embedded Systems Software:
3.1. Kernel, middleware, and virtual machine
3.2. Compiler and toolchain
3.3. Real-time system
3.4. Resource allocation for heterogeneous computing platform
3.5. Storage software and application
3.6. Human-computer interface

[4] Memory Architecture and Near/In Memory Computing:
4.1. Storage system and memory architecture
4.2. On-chip memory architectures and management: Scratchpads, compiler, controlled memories, etc.
4.3. Memory and storage hierarchies with emerging memory technologies
4.4. Near-memory and in-memory computing
4.5. Memory architecture and management for emerging memory technologies

[5] Neural Network and Neuromorphic Computing:
5.1. Hardware and devices for neuromorphic and neural network computing
5.2. Design method for learning on a chip
5.3. Systems for neural computing (including deep neural networks)
5.4. Neural network acceleration techniques including GPGPU, FPGA and dedicated ASICs
5.5. CAD for bio-inspired and neuromorphic systems

[6] Analog, RF, Mixed Signal, and Photonics:
6.1. Analog/mixed-signal/RF synthesis
6.2. Analog layout, verification, and simulation techniques
6.3. High-frequency electromagnetic simulation of circuit
6.4. Mixed-signal design consideration
6.5. Communication architectures using nanophotonics, RF, 3D, etc.
6.6. Networks-on-chip and NoC-based system design

[7] Low Power Design and Approximate Computing:
7.1. Power modeling, analysis and simulation
7.2. Low-power design and methodology
7.3. Thermal aware design
7.4. Energy harvesting and battery management
7.5. Hardware techniques for approximate/stochastic computing

[8] Logic/High-Level Synthesis and Optimization:
8.1. High-level synthesis tool and methodology
8.2. Combinational, sequential and asynchronous logic synthesis
8.3. Logic synthesis and physical design technique for FPGA
8.4. Technology mapping

[9] Physical Design:
9.1. Floorplanning, partitioning and placement
9.2. Interconnect planning and synthesis
9.3. Placement and routing optimization
9.4. Clock network synthesis
9.5. Post layout and post-silicon optimization
9.6. Package/PCB/3D-IC routing

[10] Design for Manufacturability and Reliability:
10.1. Reticle enhancement, lithography-related design and optimization
10.2. Resilience under manufacturing variation
10.3. Design for manufacturability, yield, and defect tolerance
10.4. Reliability, aging and soft error analysis
10.5. Design for reliability, aging, and robustness
10.6. Machine learning for smart manufacturing and process control

[11] Timing and Signal/Power Integrity:
11.1. Deterministic/statistical timing and performance analysis and optimization
11.2. Power/ground and package modeling, analysis and optimization
11.3. Signal/power integrity, EM modeling and analysis
11.4. Extraction, TSV and package modeling
11.5. 2D/3D on-chip power delivery network analysis and optimization

[12] Testing, Validation, Simulation, and Verification:
12.1. ATPG, BIST and DFT
12.2. System test and 3D IC test
12.3. Online test and fault tolerance
12.4. Memory test and repair
12.5. RTL and gate-leveling modeling, simulation, and verification
12.6. Circuit-level formal verification
12.7. Device/circuit-level simulation tool and methodology

[13] Hardware and Embedded Security:
13.1. Hardware-based security
13.2. Detection and prevention of hardware Trojans
13.3. Side-channel attacks, fault attacks and countermeasures
13.4. Design and CAD for security
13.5. Cyberphysical system security
13.6. Nanoelectronic security
13.7. Supply chain security and anti-counterfeiting

[14] Emerging Technologies and Applications:
14.1. Biomedical, biochip, and biodata processing.
14.2. Big/thick data, datacenter
14.3. Advanced multimedia application
14.4. Energy-storage/smart-grid/smart-building design and optimization
14.5. Automotive system design and optimization
14.6. New transistor/device and process technology: spintronic, phase-change, single-electron etc.
14.7. Nanotechnology, MEMS, quantum computing etc.

Please note that each paper shall be accompanied by at least one different conference registration at the speaker's registration rate (e.g., two speaker registrations are needed for presenting two accepted papers). But any registered co-author can present the work at the conference. ACM and IEEE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author of the paper. ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals.

Submission of Papers:

Deadline for submission:	**5 PM AOE (Anywhere on earth)**	**July 5 (Fri), 2019**
Notification of acceptance:		**Sep. 9 (Mon), 2019**
Deadline for final version:	**5 PM AOE (Anywhere on earth)**	**Nov. 4 (Mon), 2019**

For detailed instructions for submission, please refer to the "Authors' Guide" at: **http://www.aspdac.com/**

ASP-DAC 2020 Chairs

General Co-Chairs:	**Tim Cheng (Hong Kong University of Science and Technology)**
	Huazhong Yang (Tsinghua University)
Technical Program Chair:	**Tsung-Yi Ho (National Tsing Hua University)**
Technical Program Vice Chairs:	**Sheldon Tan (University of California, Riverside)**
	Yiran Chen (Duke University)

Panels, Special Sessions, and Tutorials: Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (aspdac2020@aspdac.com) no later than August 2 (Fri), 2020.
Contact: Conference Secretariat: aspdac2020@aspdac.com TPC Secretariat: tpc@aspdac20.com