ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE

Call for Papers
ASP-DAC 2023

http://www.aspdac.com/
Mid January, 2023
Virtual Conference

Aims of the Conference:
ASP-DAC 2023 is the 28th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design, CAD and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to design and Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:
Original papers in, but not limited to, the following areas are invited.

[1] System-Level Modeling and Design Methodology:
1.1. HW/SW co-design, co-simulation and co-verification
1.2. System-level design exploration, synthesis, and optimization
1.3. System-level formal verification
1.4. System-level modeling, simulation and validation tools/methodology
1.5. Networks-on-chip and NoC-based system design

[2] Embedded, Cyberphysical (CSP) and IoT Systems:
2.1. Many- and multi-core SoC architecture
2.2. IP/platform-based SoC design
2.3. Domain-specific architecture
2.4. Dependable architecture
2.5. Cyber physical system
2.6. Internet of things

[3] Embedded Systems Software:
3.1. Kernel, middleware, and virtual machine
3.2. Compiler and toolchain
3.3. Real-time system
3.4. Resource allocation for heterogeneous computing platform
3.5. Storage software and application
3.6. Human-computer interface

[4] Memory Architecture and Near/In Memory Computing:
4.1. Storage system and memory architecture
4.2. On-chip memory architectures and management: Scratchpads, compiler, controlled memories, etc.
4.3. Memory and storage hierarchies with emerging memory technologies
4.4. Near-memory and in-memory computing
4.5. Memory architecture and management for emerging memory technologies

[5] AI/Machine Learning Circuits, Architecture and System Designs:
5.1. Hardware and devices for deep neural networks
5.2. Design method for learning on a chip
5.3. Systems and design methods for deep neural computing
5.4. Neural network acceleration co-design techniques
5.5. Design techniques for AI of Things

[6] FPGA and Reconfigurable Computing:
6.1. Novel reconfigurable architectures
6.2. Design methods for FPGA and reconfigurable architectures
6.3. HW/SW prototyping and emulation on FPGAs
6.4. FPGA-based prototyping for analog, mixed-signal, RF systems
6.5. AI/ML acceleration on reconfigurable accelerators

[7] Photonic/RF/Analog-Mixed Signal Design:
7.1. Analog/mixed-signal/RF synthesis
7.2. Analog layout, verification, and simulation techniques
7.3. High-frequency electromagnetic simulation of circuit
7.4. Mixed-signal design consideration
7.5. Communication and computing using photonics

[8] Approximate, Bio-Inspired and Neuromorphic Computing:
8.1. Circuit and system techniques for approximate and stochastic computing
8.2. Neuromorphic computing
8.3. CAD for approximate and stochastic systems
8.4. CAD for bio-inspired and neuromorphic systems

[9] High-Level, Behavioral, and Logic Synthesis and Optimization:
9.1. High-level/Behaviroal synthesis tool and methodology
9.2. Combinational, sequential and asynchronous logic synthesis
9.3. Technology mapping, resource scheduling, allocation and synthesis
9.4. Functional and logic timing ECO (Engineering change order)
9.5. Interaction between logic synthesis and physical design

[10] Physical Design:
10.1. Floorplanning, partitioning and placement and routing optimization
10.2. Interconnect planning and synthesis
10.3. Clock network synthesis
10.4. Post layout and post-silicon optimization
10.5. Package/PCB/3D-IC routing

[11] Design for Manufacturability/Reliability and Analysis for Timing and Low Power:
11.1. Reticle enhancement, lithography-related design and optimization
11.2. Resilience under manufacturing variation
11.3. Design for manufacturability, yield, and defect tolerance
11.4. Design for reliability, aging and soft error analysis
11.5. Power modeling, analysis and simulation
11.6. Low-power design and optimization at circuit and system levels
11.7. Thermal aware design and dynamic thermal management
11.8. Energy harvesting and battery management
11.9. Deterministic/statistical timing analysis and optimization, Signal/power integrity, EM modeling and analysis

[12] Testing, Validation, Simulation, and Verification:
12.1. ATPG, BIST and DFT
12.2. System test and 3D IC test
12.3. Online test and fault tolerance
12.4. Memory test and repair
12.5. RTL and gate-leveling modeling, simulation, and verification
12.6. Circuit-level formal verification
12.7. Device/circuit-level simulation tool and methodology

[13] Hardware and Embedded Security:
13.1. Hardware-based security
13.2. Detection and prevention of hardware Trojans
13.3. Side-channel attacks, fault attacks and countermeasures
13.4. Design and CAD for security
13.5. Cyberphysical system security
13.6. Nanoelectronic security
13.7. Supply chain security and anti-counterfeiting

[14] Emerging Devices, Technologies and Applications:
14.1. Quantum and Ising computing
14.2. Nanotechnology, MEMS
14.3. Biomedical, biochip, and biodata processing.
14.4. Edge, fog and cloud computing
14.5. Energy-storage/smart-grid/smart-building design and optimization
14.6. Automotive system design and optimization
14.7. New transistor/device and process technology: spintronic, phase-change, single-electron etc.

ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals. The submission must not include information that serves to identify the authors of the manuscript, such as name(s) or affiliation(s) of the author(s), anywhere in the manuscript, abstract, references and bibliographic citations. Note that each paper shall be accompanied by at least one different conference registration at the speaker's registration rate (e.g., two speaker registrations are needed for presenting two accepted papers). But any registered co-author can present the work at the conference. ACM and IEEE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author paper.

Submission of Papers:

Deadline for abstract submission:	**5 PM AOE (Anywhere on earth)**	**July 24, 2022**
Deadline for PDF uploading:	**5 PM AOE (Anywhere on earth)**	**July 29, 2022**
Notification of acceptance:		**Mid Sept. 2022**
Deadline for final version:	**5 PM AOE (Anywhere on earth)**	**Early Nov. 2022**

For detailed instructions for submission, please refer to the "Authors' Guide" at:
http://www.aspdac.com/

ASP-DAC 2023 Chairs

General Co-Chairs:	**Atsushi Takahashi (Tokyo Institute of Technology)**
Technical Program Chair:	**Gi-Joon Nam (IBM Research)**
Technical Program Vice Chairs:	**Iris Hui-Ru Jiang (National Taiwan University)**

Panels, Special Sessions, and Tutorials: Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (aspdac2023@aspdac.com) no later than TBD.

Contact: Conference Secretariat: aspdac2023@aspdac.com TPC Secretariat: aspdac2023.tpc@gmail.com