Class-A Power Amplifier Design Proposal Team Helios

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***Abstract*—The final project for Dr. Aslan's Fall 2012 Electronics I course was to design a power amplifier for use in audio applications. The goal was to apply knowledge of power supplies (diodes and transformers) and amplifiers (BJT transistors with hybrid pi model) to design a Class-A power amplifier from end to end. Particular emphasis was placed on collaborative design and CAD-assisted verification via Multisim software, as well as having as large a bandwidth as possible.**

Team Helios chose a common emitter to emitter follower design as a base. Choosing to employ a bipolar dual-rail power supply to the system –so as to increase maximum voltage swing and have zero power output in the absence an applied signal (no heat dissipation)– necessitated the introduction of a third transistor to act as a voltage shift. The result is an amplifier that has an approximate voltage gain of 142 and a power output of approximately five milliwatts across resistive loads varying from 2 to 16 ohms, as per the specification. Efficiency was measured as approximately five percent compared to the DC input. Total cost was determined to be X dollars. Lead times from manufacture to customer delivery are conservatively given at two months.

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I. INTRODUCTION AND PRODUCT SPECIFICATIONS

THE client, Good Speakers Inc., has commissioned the design of a Class-A Power Amplifier for use in audio applications. The following specifications are provided.

- Input: $V_s = 1mVpk$, $R_s = 50\Omega$
- Output: Speaker that ranges from 2Ω to 16Ω.
- Onboard 12V DC power supply (bipolar permited)
- USB connector for charging purposes (investigate whether this is possible)
- High power gain
- High efficiency
- Minimum cost

II. IMPLICATIONS OF SPECIFICATIONS

Given the audio application of the amplifier, one can reasonably assume that the frequency of the input signal will fall between 22 Hz and 22 kHz. While the client desires as wide a bandwidth as possible, the audio bandwidth is the most crucial to meet. The lower bound of 22 Hz would require significantly larger capacitors to place the lower cutoff value at said frequency. Team Helios assumes a lower bound of 100 Hz in calculations, knowing that the effect on these low frequencies past the 100 Hz cutoff is negligible. In addition, the chosen design that uses DC coupling to minimize the need for capacitors has an added effect of reducing attenuation at each cutoff frequency.

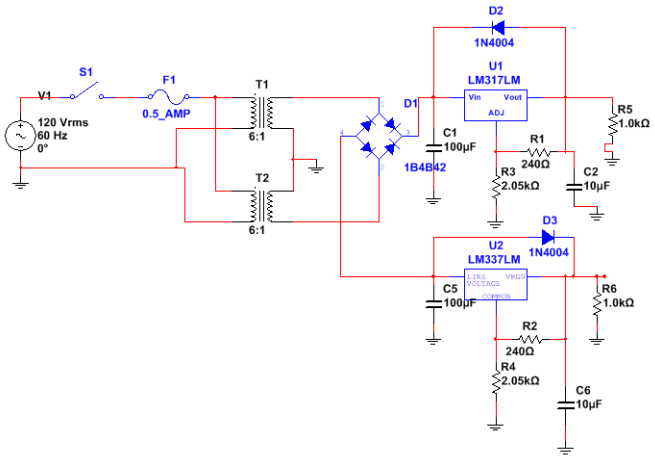
The request to investigate possibilities of USB charging was at first interpreted as an indication that the circuit needed to be powered by battery. Further communication with client indicates that this assumption wasn't accurate. The client is interested in the ability to charge the signal source – mp3 player, iPod, etc– as it is playing. This is possible. However, the charging currents required by USB devices vary considerably, and the ability to charge and operate at the same time is widespread but not universal.

The high power gain and high efficiency requirements are restricted by the request for a Class A amplifier; such amplifiers have a maximum theoretical efficiency of 25%, with typical designs in the single digits.

III. POWER SUPPLY DESIGN

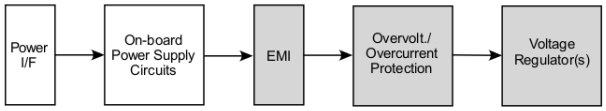
The following design is an improvement on the basic models introduced at the start of semester. It takes into account various sources of noise and distortion common to mains input. It also

attempts to mitigate common sources of design failure, such as inrush current and overvoltage. Finally, it further addresses safety concerns with the introduction of arc-resistant fuses and is a step in the right direction for approval by certifiers such as Underwriters Laboratories.



A. Block Diagram

From mains input to DC output, there are multiple issues to address. Switching and fusing off mains before hitting the transformer is a given. Along the way, one may address EMI, inrush current, and overvoltage protections for the voltage regulator chips.



B. Considerations

Don't have Jonathan's report on the different types of caps yet. Holding off on this part for now.

IV. Rejected Amplifier Designs

Various approaches and topologies were investigated. From single-transistor to CE-EF to op-amp implementations, each design was examined on a broad level with advantages and drawbacks determined.

A. Transformer Coupled

This design used a single CE transistor, replacing R_C with a transformer to increase efficiency.

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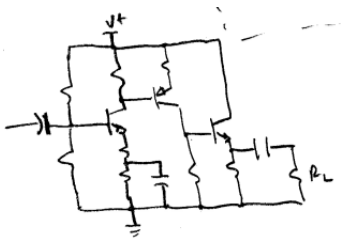
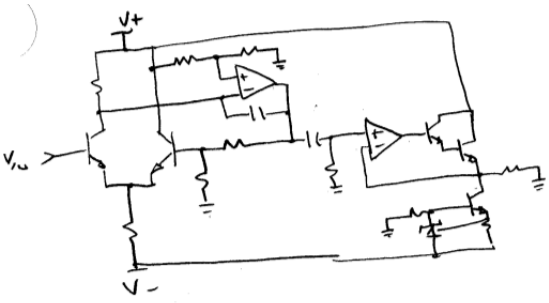
B. CE-EF one rail

This design used a CE-EF implementation with a single 12 V rail.



C. Op-Amp Implementation

This design implemented the specification utilizing Op-Amps.



D. Comparison Summary

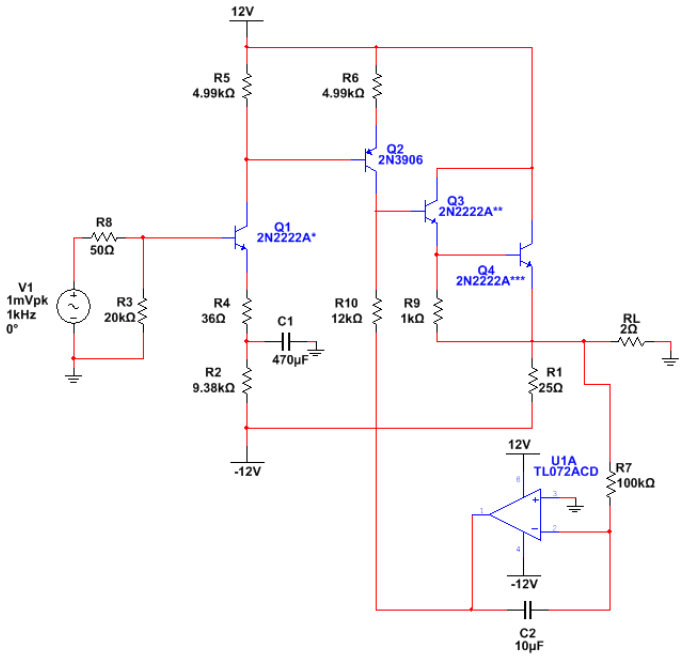
The following table summarizes the comparisons of these designs.

	Advantages	Drawbacks
A	-Single transistor -Peak efficiency of 50%	-Transformers are bulky -Outdated design
B	-CE-EF gives good impedence matching -Intuitive	-Always drawing power -Hum on bypass cap
C	-Very stable	-Team unfamiliar with Op-Amps

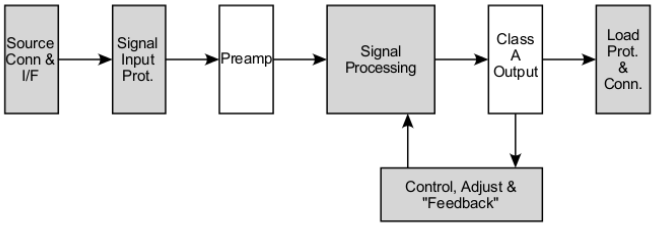
The bulkiness of the transformer coupled design removed it as a choice. The hum on the bypass capacitor eliminated the CE-EF one rail design. The Op-Amp implementation, while very stable, was not chosen as team Helios is unfamiliar with Op-Amps.

V. Selected Amplifer Design

The following schematic is the chosen design of team Helios. It is comprised of a CE transistor, followed by a complimentary transistor that acts as voltage shift, followed by a Darlington pair to act as the EF to the load.



A. Block Diagram



B. Design Approach

The traditional approach for design, starting with KVL and $I_C = \beta I_B$, functions well for single-transistor implementations. It is thorough and rigourous and the hybrid pi model is very accurate for the frequency range under consideration. However, this design methodology's heavy dependence on assumptions for system behaviour that can change and are at times interdependent can often lead to line after line of dense calculation that must be revamped continuously for each iteration of the design. Performing such calculations manually is error prone, and writing software to automate the process is outside of the scope of this project.

Consequently, a work backward approach was taken, starting from arbitrarily selected target output values –for example, require 10 mW output power– and working backwards to determine requirements at each stage of the amplifier. For example: in the given design, a target output of 5 mW was selected. This implies an RMS voltage on the output. Knowing that this must come from the emitter-follower stage (Darlington pair in the chosen design), one can conclude that the RMS voltage entering the emitter-follower must be greater than $1.4V$, since V_{BE} is approximated as $0.7V$. Knowing that the voltage shift gain is approximately one, one can conclude that this voltage is also the input and output of the voltage shift stage and, consequently, that our common emitter (which performs the actual voltage gain) needs to output this. At this point, one may set up the DC conditions on the CE and tweak R_{E1} as necessary to influence the voltage gain.

This fast and loose approach permits a more rapid development process that can always be checked against the more formal mathematics once ballpark values are determined. In our case, design verification was performed using Multisim.

C. Calculations

Haven't gotten any calculations yet. Granted, the above does a good job on the philosophizing.

D. Considerations

Tweaking R_{E1}, servo feedback control, why use darlington instead of single transistor?, variance in output power as load increases from 2 to 16 ohms.

VI. Cost Analysis of Selected Design

I didn't anticipate this being an all-night affair, but it has been :D For now, cost analysis will merely be the raw cost of components. I'll consider adding in production cost and delivery tables for the presentation over the weekend.

VII. Conclusion

Essentially reiterate the abstract. Place emphasis on cost and how we have not just met but exceeded customer specifications.