

Class-A Power Amplifier Design Proposal

Team Helios

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Abstract—The final project for Dr. Aslan’s Fall 2012 Electronics I course was to design a power amplifier for use in audio applications. The goal was to apply knowledge of power supplies (diodes and transformers) and amplifiers (BJT transistors with hybrid pi model) to design a Class-A power amplifier from end to end. Particular emphasis was placed on collaborative design and CAD-assisted verification via Multisim software.

Team Helios chose a common emitter to emitter follower design as a base. Choosing to employ a bipolar dual-rail power supply to the system –so as to increase maximum voltage swing and have zero power output in the absence an applied signal (no heat dissipation)– necessitated the introduction of a third transistor to act as a voltage shift. The result is an amplifier that has an approximate voltage gain of 142 and a power output of approximately five milliwatts across resistive loads varying from 2 to 16 ohms, as per the specification. Efficiency was measured as approximately five percent compared to the DC input. Total cost was determined to be X dollars. Lead times from manufacture to customer delivery are conservatively given at two months.

CONTENTS

I	Introduction and Product Specifications	1
II	Implications of Specifications	1
III	Power Supply Design	1
III-A	Block Diagram	2
III-B	Considerations	2
IV	Rejected Amplifier Designs	2
IV-A	First	2
IV-B	Second	2
IV-C	Third	2
IV-D	Comparison Summary	2
V	Selected Amplifier Design	2
V-A	Block Diagram	2
V-B	Design Approach	2
V-C	Calculations	3
V-D	Considerations	3
VI	Cost Analysis of Selected Design	3
VII	Conclusion	3

VIII	Derived Component Values	3
VIII-A	RC high-pass	3
VIII-B	RL low-pass	3
VIII-C	RLC band-pass	3
VIII-D	RLC band-stop	3
IX	Experimental Procedure	3
X	Collected Data and Analysis	4
X-A	RC High-pass	4
X-B	RL Low-pass	4
X-C	RLC Band-Pass	4
X-D	RLC Band-Stop	4
XI	Conclusion	5

I. INTRODUCTION AND PRODUCT SPECIFICATIONS

THE client, Good Speakers Inc., has commissioned the design of a Class-A Power Amplifier for use in audio applications. The following specifications are provided.

- blah
- blah
- blah
- blah

II. IMPLICATIONS OF SPECIFICATIONS

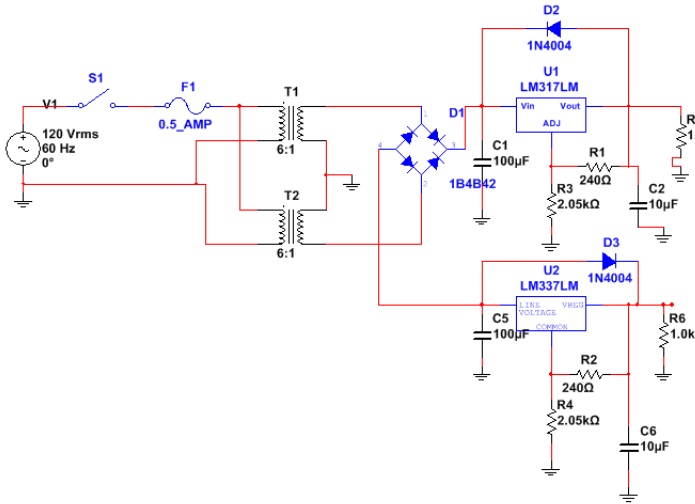
Given the audio application of the amplifier, one can reasonably assume that the frequency of the input signal will fall between 22 Hz and 22 kHz. While the client desires as wide a bandwidth as possible, the audio bandwidth is the most crucial to meet. The lower bound of 22 Hz would require significantly larger capacitors to place the lower cutoff value at said frequency. Team Helios assumes a lower bound of 100 Hz in calculations, knowing that the effect on these low frequencies past the 100 Hz cutoff is negligible. In addition, the chosen design that uses DC coupling to minimize the need for capacitors has an added effect of reducing attenuation at each cutoff frequency.

asdf

III. POWER SUPPLY DESIGN

The following design is an improvement on the basic models introduced at the start of semester. It takes into account various sources of noise and distortion common to mains input. It also

attempts to mitigate common sources of design failure, such as inrush current and overvoltage. Finally, it further addresses safety concerns with the introduction of arc-resistant fuses and is a step in the right direction for approval by certifiers such as Underwriters Laboratories.



A. Block Diagram

asdf

B. Considerations

asdf

IV. REJECTED AMPLIFIER DESIGNS

Various approaches and topologies were investigated. From single-transistor to CE-EF to op-amp implementations, each design was examined on a broad level with advantages and drawbacks determined.

A. First

my transformer design

B. Second

similar design to chosen one that doesn't use bipolar supply (increases hum).

C. Third

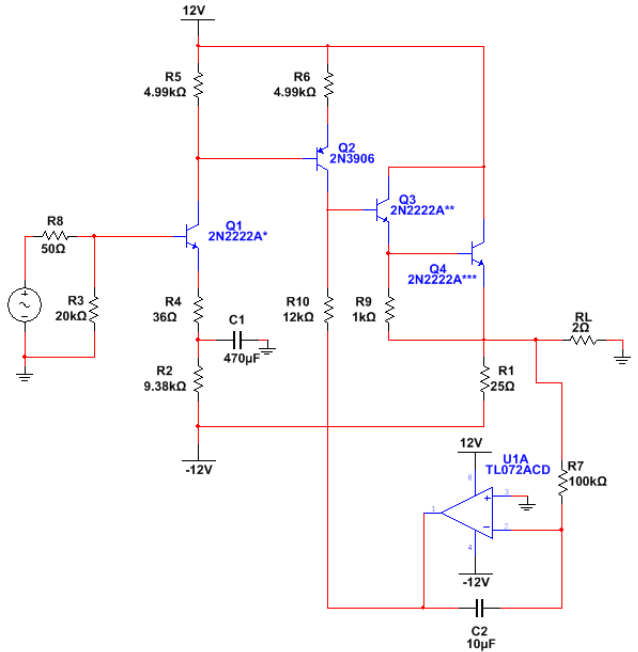
one of the designs that used lots of op-amps (usable, but lack of familiarity with op-amps resulted in using the selected design)

D. Comparison Summary

Advantages Drawbacks

V. SELECTED AMPLIFIER DESIGN

The full schematic is below



A. Block Diagram

adsf

B. Design Approach

The traditional approach for design, starting with KVL and $I_C = \beta I_B$, functions well for single-transistor implementations. It is thorough and rigorous and the hybrid pi model is very accurate for the frequency range under consideration. However, this design methodology's heavy dependence on assumptions for system behaviour that can change and are at times interdependent can often lead to line after line of dense calculation that must be revamped continuously for each iteration of the design. Performing such calculations manually is error prone, and writing software to automate the process is outside of the scope of this project.

Consequently, a work backward approach was taken, starting from arbitrarily selected target output values—for example, require 10 mW output power—and working backwards to determine requirements at each stage of the amplifier. For example: in the given design, a target output of 5 mW was selected. This implies an RMS voltage on the output. Knowing that this must come from the emitter-follower stage (Darlington pair in the chosen design), one can conclude that the RMS voltage entering the emitter-follower must be greater than 1.4V, since V_{BE} is approximated as 0.7V. Knowing that the voltage shift gain is approximately one, one can conclude that this voltage is also the input and output of the voltage shift stage and, consequently, that our common emitter (which performs the actual voltage gain) needs to output this. At this point, one may set up the DC conditions on the CE and tweak R_{E1} as necessary to influence the voltage gain.

This fast and loose approach permits a more rapid development process that can always be checked against the more formal mathematics once ballpark values are determined. In our case, design verification was performed using Multisim.

C. Calculations

Still haven't gotten any calculations. Granted, the above does a good job on the philosophizing.

D. Considerations

asdf

VI. COST ANALYSIS OF SELECTED DESIGN

asdf

VII. CONCLUSION

asdf

VIII. DERIVED COMPONENT VALUES

This section documents the general process for finding ideal component values to meet the specifications. In each of these cases it is assumed ω_o is in terms of rad/s. In each case, one started by selecting an available value for one of the components, and then finding the available value for the subsequent components that would bring the resonant frequency closest to that requested.

A. RC high-pass

For an RC high-pass circuit, the following relationship may be exploited to determine proper R and C values:

$$\omega_o = \frac{1}{RC}$$

A choice of $C = 1\mu\text{F}$ led to a value of $R = 27\Omega$. This selection provides a resonant frequency of 37,037 rad/s (5894 Hz).

B. RL low-pass

For an RL low-pass circuit, the following relationship may be exploited to determine proper R and L values:

$$\omega_o = \frac{R}{L}$$

A choice of $L = 4.7 \text{ mH}$ led to a value of $R = 37\Omega$. This selection provides a resonant frequency of 2765.95 rad/s (440.2 Hz).

C. RLC band-pass

For an RLC band-pass circuit, the following relationships may be exploited to determine proper R, C, and L values:

$$\begin{aligned}\omega_o &= \sqrt{\frac{1}{LC}} \\ \omega_2 &= \frac{\frac{R}{L} + \sqrt{\left(\frac{R}{L}\right)^2 + 4\omega_o^2}}{2} \\ \beta &= (\omega_2 - \omega_o) \cdot 2 \\ Q &= \frac{\omega_o}{\beta}\end{aligned}$$

Start by selecting an available inductor. Then find an appropriate available capacitor so as to approach the desired resonant frequency. Once one has L and C values, utilize the second equation above, in conjunction with the third and fourth, to find a resistor that will narrow the bandwidth to a range sufficiently small to meet the minimum Q-factor. One is essentially using brute force over the available resistor components to find ω_2 , and then checking whether the resulting bandwidth (and thus resulting Q-factor) is appropriate. The following values exceed the specification and approach a Q-factor of 15:

- 1) $L = 4.7\text{mH}$
- 2) $C = 10\text{nF}$
- 3) $R = 47\Omega$
- 4) $\omega_o = 145,864 \text{ rad/s}$ (23,215 Hz)
- 5) $Q = 14.34$

D. RLC band-stop

A band-stop filter may be designed as though one were creating a band-pass filter. One must still wire the band-stop filter components correctly though. The same relationships and process as above may be utilized to arrive at component values.

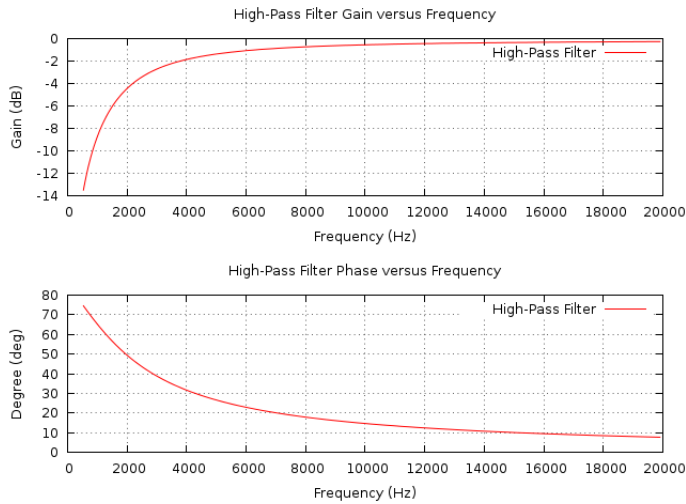
- 1) $L = 2.2\text{mH}$
- 2) $C = 10\text{nF}$
- 3) $R = 27\Omega$
- 4) $\omega_o = 213,200 \text{ rad/s}$ (33,931 Hz)
- 5) $Q = 17.37$

IX. EXPERIMENTAL PROCEDURE

- 1) Construct each filter above on the NI ELVIS board.
- 2) Apply the proper wiring from pin outs for the function generator (the source for the circuit) and the probes utilized by the bode analyzer. It is recommended that one uses A1 for the source and A0 for the response.
- 3) Engage the bode analyzer. Adjust the step, minimum frequency, and maximum frequency options as necessary in order to generate a usable plot for analysis.
- 4) Should the bode analyzer throw a warning regarding "OVERFLOW," restart the bode analyzer.

X. COLLECTED DATA AND ANALYSIS

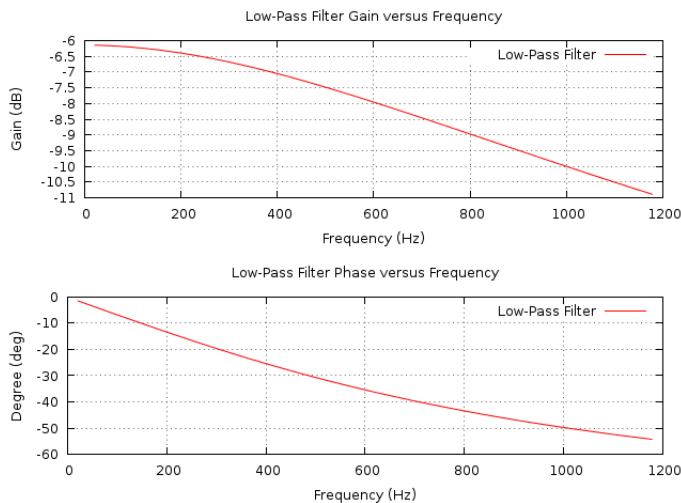
A. RC High-pass



Value	Expected	Measured	% error
ω_o (Hz)	5894	2747	-53.4
phase (deg)	45	41.096	-8.67

The measured resonant frequency is much lower than anticipated. Further inspection of the components revealed that a 62Ω resistor had actually been used. Knowing this, the expected value would have been 2567 Hz, much closer to the measured value and with a much smaller percent error (-6.55%).

B. RL Low-pass

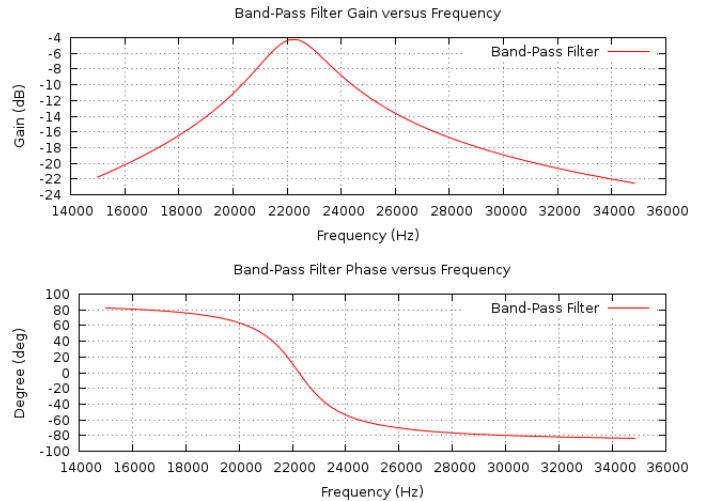


Value	Expected	Measured	% error
ω_o (Hz)	440	NA	NA
phase (deg)	45	NA	NA

As one can see from the above graph, the filter never exceeded a -6 dB gain, regardless of settings given to the bode analyzer. It is as though the gain has been shifted

downward by 6 dB across all frequencies. As well, the line is significantly less concave than the high-pass filter. A source for this behaviour was unable to be determined.

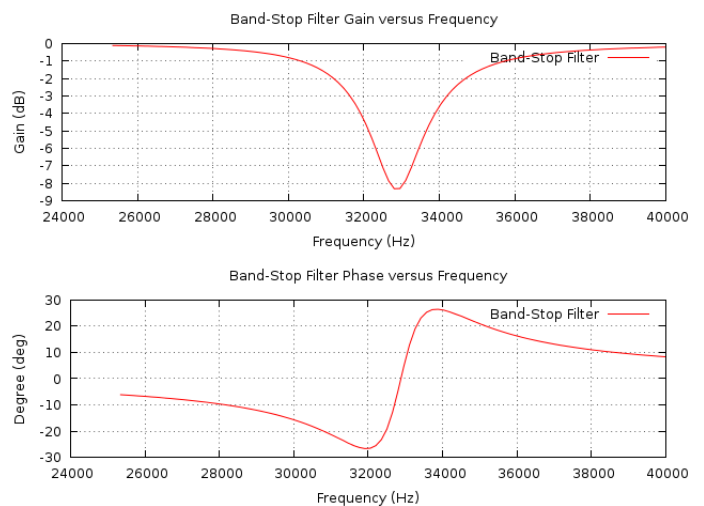
C. RLC Band-Pass



Value	Expected	Measured	% error
ω_o (Hz)	23,215	22,288	-3.99
phase (deg)	0	-2.07	NA

The bode plots behaved as expected both in general shape and values returned. Given that the expected phase degree is zero, one cannot use the typical formula for percent error. However, the small difference indicates that the phase plot was behaving as expected.

D. RLC Band-Stop



Value	Expected	Measured	% error
ω_o (Hz)	33,931	32,804	-3.32
phase (deg)	0	-4.53	NA

Once again the general shape is as expected. As well, the values are well within the 5% margins requested.

XI. CONCLUSION

The general behaviour was confirmed for three of the four basic filters. Several groups reported trouble with the low-pass filter, regardless of its RL or RC nature. Errors exceeding 5% are expected, given that the tolerance on the resistors alone is 10% on either side of the listed value. However, the band-pass and band-stop were both within tolerance even with such components.