Class-A Power Amplifier Design Proposal Team Helios

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***Abstract*—The final project for Dr. Aslan's Fall 2012 Electronics I course was to design a power amplifier for use in audio applications. The goal was to apply knowledge of power supplies (diodes and transformers) and amplifiers (BJT transistors with hybrid pi model) to design a Class-A power amplifier from end to end. Particular emphasis was placed on collaborative design and CAD-assisted verification via Multisim software, as well as having as large a bandwidth as possible.**

Team Helios chose a common emitter to emitter follower design as a base. Choosing to employ a bipolar dual-rail power supply to the system –so as to increase maximum voltage swing and have zero power output in the absence an applied signal (no heat dissipation)– necessitated the introduction of a third transistor to act as a voltage shift. The result is an amplifier that has an approximate voltage gain of 142 and a power output of approximately five milliwatts across resistive loads varying from 2 to 16 ohms, as per the specification. Efficiency was measured as approximately five percent compared to the DC input. Total cost was determined to be X dollars. Lead times from manufacture to customer delivery are conservatively given at two months.

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I. INTRODUCTION AND PRODUCT SPECIFICATIONS

THE client, Good Speakers Inc., has commissioned the design of a Class-A Power Amplifier for use in audio applications. The following specifications are provided.

- Input: $V_s = 1mVpk$, $R_s = 50\Omega$
- Output: Speaker that ranges from 2Ω to 16Ω.
- Onboard 12V DC power supply (bipolar permited)
- USB connector for charging purposes (investigate whether this is possible)
- High power gain
- High efficiency
- Minimum cost

II. IMPLICATIONS OF SPECIFICATIONS

Given the audio application of the amplifier, one can reasonably assume that the frequency of the input signal will fall between 22 Hz and 22 kHz. While the client desires as wide a bandwidth as possible, the audio bandwidth is the most crucial to meet. The lower bound of 22 Hz would require significantly larger capacitors to place the lower cutoff value at said frequency. Team Helios assumes a lower bound of 100 Hz in calculations, knowing that the effect on these low frequencies past the 100 Hz cutoff is negligible. In addition, the chosen design that uses DC coupling to minimize the need for capacitors has an added effect of reducing attenuation at each cutoff frequency.

The request to investigate possibilities of USB charging was at first interpreted as an indication that the circuit needed to be powered by battery. Further communication with client indicates that this assumption wasn't accurate. The client

is interested in the ability to charge the signal source – mp3 player, iPod, etc– as it is playing. This is possible. However, the charging currents required by USB devices vary considerably, and the ability to charge and operate at the same time is widespread but not universal.

The high power gain and high efficiency requirements are restricted by the request for a Class A amplifier; such amplifiers have a maximum theoretical efficiency of 25%, with typical designs in the single digits.

III. Power Supply Design

The following design is an improvement on the basic models introduced at the start of semester. It takes into account various sources of noise and distortion common to mains input. It also attempts to mitigate common sources of design failure, such as inrush current and overvoltage. Finally, it further addresses safety concerns with the introduction of arc-resistant fuses and is a step in the right direction for approval by certifiers such as Underwriters Laboratories.

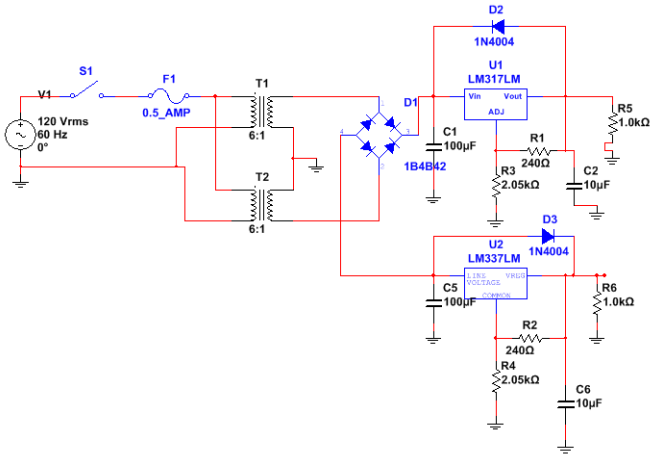

Fig. 1. Final PSU Schematic

A. Block Diagram

From mains input to DC output, there are multiple issues to address. Switching and fusing off mains before hitting the transformer is a given. Along the way, one may address EMI, inrush current, and overvoltage protections for the voltage regulator chips.

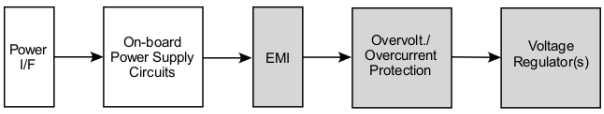

Fig. 2. PSU Block Diagram

B. Considerations

Don't have Jonathan's report on the different types of caps yet. Holding off on this part for now.

IV. Rejected Amplifier Designs

Various approaches and topologies were investigated. From single-transistor to CE-EF to op-amp implementations, each design was examined on a broad level with advantages and drawbacks determined.

A. Transformer Coupled

This design used a single CE transistor, replacing R_C with a transformer to increase efficiency.

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B. CE-EF one rail

This design used a CE-EF implementation with a single 12 V rail.

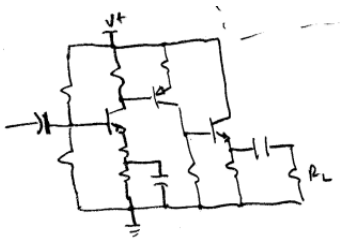

Fig. 3. Rejected CE-EF Single Rail

C. Op-Amp Implementation

This design implemented the specification utilizing Op-Amps.

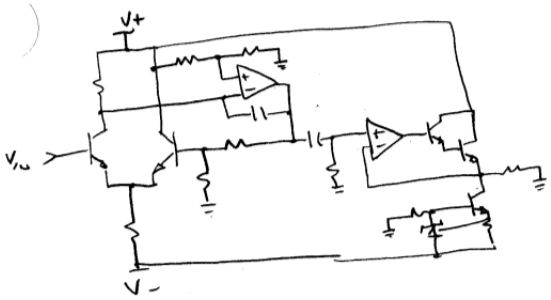

Fig. 4. Rejected Op-Amp Implementation

D. Comparison Summary

The following table summarizes the comparisons of these designs.

	Advantages	Drawbacks
A	-Single transistor -Peak efficiency of 50%	-Transformers are bulky -Outdated design
B	-CE-EF gives good impedence matching -Intuitive	-Always drawing power -Hum on bypass cap
C	-Very stable	-Team unfamiliar with Op-Amps

The bulkiness of the transformer coupled design removed it as a choice. The hum on the bypass capacitor eliminated the CE-EF one rail design. The Op-Amp implementation, while very stable, was not chosen as team Helios is unfamiliar with Op-Amps.

V. Selected Amplifer Design

The following schematic is the chosen design of team Helios. It is comprised of a CE transistor, followed by a complimentary transistor that acts as voltage shift, followed by a Darlington pair to act as the EF to the load.

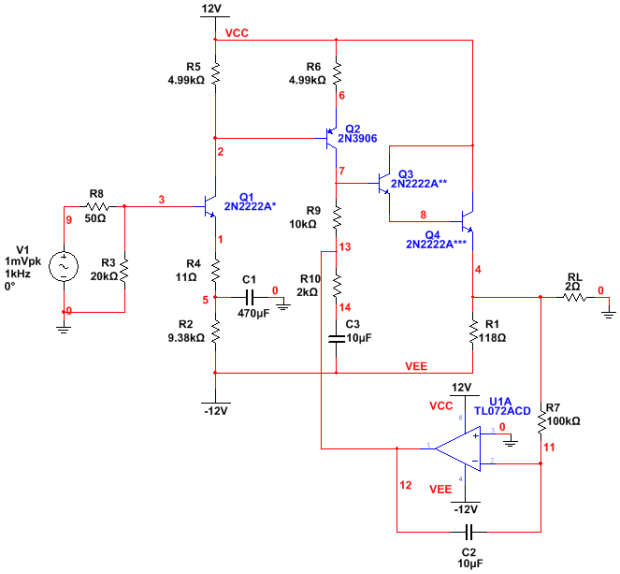

Fig. 5. Final Amp Schematic

A. Block Diagram

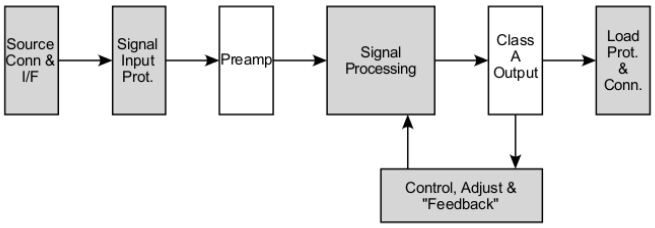

Fig. 6. Amp Block Diagram

B. Design Philosophy

The traditional approach for design, starting with KVL and $I_C = \beta I_B$, functions well for single-transistor implementations. It is thorough and rigourous and the hybrid pi model is very accurate for the frequency range under consideration. However, this design methodology's heavy dependence on assumptions for system behaviour that can change and are at times interdependent can often lead to line after line of dense calculation that must be revamped continuously for each iteration of the design. Performing such calculations manually is error prone, and writing software to automate the process is outside of the scope of this project.

Consequently, a work backward approach was taken, starting from arbitrarily selected target output values –for example, require 10 mW output power– and working backwards to determine requirements at each stage of the amplifier. For example: in the given design, a target output of 5 mW was selected. This implies an RMS voltage on the output. Knowing that this must come from the emitter-follower stage (Darlington pair in the chosen design), one can conclude that the RMS voltage entering the emitter-follower must be greater than $1.4V$, since V_{BE} is approximated as $0.7V$. Knowing that the voltage shift gain is approximately one, one can conclude that this voltage is also the input and output of the voltage shift stage and, consequently, that our common emitter (which performs the actual voltage gain) needs to output this. At this point, one may set up the DC conditions on the CE and tweak R_{E1} as necessary to influence the voltage gain.

This fast and loose approach permits a more rapid development process that can always be checked against the more formal mathematics once ballpark values are determined. In our case, design verification was performed using Multisim.

C. Analysis and Calculations

Given the specification and application, the following are the primary objectives of any design, and each is addressed by the design from Team Helios.

- **Meet Design Requirements –** These must be met first prior to any improvements on the design.
- **Prevent DC at Load –** Since a speaker is the specified load and speakers are easily destroyed by DC, keeping DC from reaching the load is a design con straint that is implied from the customers design requirements.
- **Directly Coupled –** There are three choices of coupling our emitter-fol lower: capacitively coupled, transformer coupling or direct coupling. Capacitive coupling and transformer-coupling both have serious downsides (bad low-fre quency response, bulky, expensive, frequency dependence, etc). If its possible, DC-coupling should be used.
- **Non-inverting from input to output –** With an eye toward perfor mance improvement, better technologies (like opamps) could be used to more cheaply/compactly improve performance and cost-effectively allow feature enhancements/additions. Although its not impossible to retrofit an inverting stage with an opamp (theres always more than one way to achieve desired perfor mance), it would help ease the design process.

1) Design Approach: The following serves as a more detailed explanation of the design philosophy described above.

1) Select a modest goal for the amplifiers output level: since this was not in the specifications, we chose –through a little trial-and-error– a 5mW output level into 2 Ω. Matching the output level with the specified input level yields an AV of 141 (see equation (2), below).
2) A CE amplifier with bipolar-supply emitter-bias has a shot of the base being close to ground (ref: pg 241-244 of classroom text). It made sense to start there.
3) Run a high-enough I_E so that a reasonably-sized R_C will give us the gain we need.
4) Assume that $V_{DCLOAD} = 0$.
5) Find a way to mesh the voltage level at the Darlington pairs base and the VC both under quiescent conditions.

6) If V_{CEQ} is half-way between ground and +12V (V_{CC}), the signal can swing $\pm$ 6V. Given that the signal at the emitter will effectively not vary (were supposed to accommodate an input signal of $1mV_{PK}$), we dont have to worry about premature clipping due to V_e and V_c conflicting. Besides, since well couple the AC voltage at the collector with the load (through level-shift and the CC Darlington), a $2.12V_{RMS}$ signal into 2Ω is way overkill (the resultant potential power at the load would be 2W).

2) CE Gain Stage: Picking an R_C of 4.99k with a V_C of 6V gives an I_C of 1.2mA. This yields:

$$r'_e = 20.8\Omega \tag{1}$$

Ignoring loading on R_C, this yields a maximum gain of 238. This is almost double the gain that we need:

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{\sqrt{P_{OUT} \cdot R_{LOAD}}}{V_{IN}} = \frac{\sqrt{(5mW) \cdot (2\Omega)}}{\frac{2}{2\sqrt{2}} mV_{pp}} = 141 \tag{2}$$

Once this is established, we can select the value for R_E to give us ground at the base. Working up from -12V:

$$R_E = \frac{12V - 0.7V}{1.2ma} \approx 10k\Omega \tag{3}$$

For an A_V of 141,

$$R_{E1} = \frac{R_C}{A_V} - r'_e \approx 15\Omega \tag{4}$$

This value will be tweaked once the whole circuits been put together. The final CE circuit along with C_B is given below:

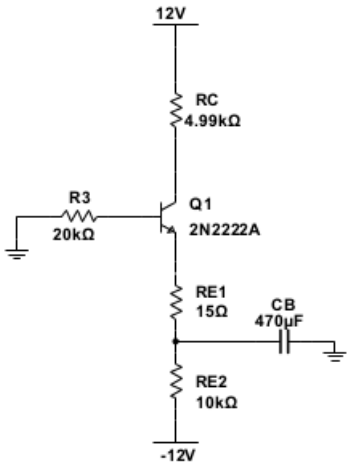

Fig. 7. CE Stage

3) Output Driver: The specification is lacking in certain details like maximum input levels. However, given that the input signal is specified as 0 to $2mV_{pp}$, well assume that the maximum is $2mV_{pp}$ while the minimum is 0. Adding just a little extra for good measure, well assume the peak current into the load to be 100mA (10mW into 2Ω). In a Class A amplifier, the current either flows into the load or into a current sink/source. An emitter follower can only source current, not sink it. So for the negative swing across the load to reach its peak, we need a current sink to provide the peak current. A pull-down resistor to the negative rail can do (in a pinch) instead of a transistor-based current sink:

$$R_{sink} = \frac{12V - 0.2V}{100mA} = 118\Omega \tag{5}$$

This will provide our peak negative current to the load, when the emitter follower cant.

4) Bridging the Gap: We have two remaining issues to meet our stated goals of:

- Direct-coupled output, and,
- Non-inverting output

Assuming that theres a mechanism that allows us to have the CC emitter at 0V, the base voltage for the Darlington would be a nominal quiescent voltage of 1.4V. Unfortunately, the col lector voltage of the CE has a VC_{EQ} of 6V. We need a circuit to shift the voltage from 6 to 1.4 and to invert the signal phase, like this:

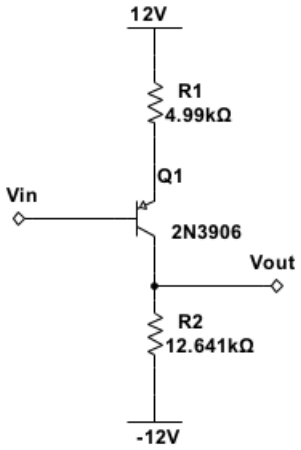

Fig. 8. Level-shifter Stage

Although theres a slight amount of gain, you can see that if R_2 had twice the value as R_1, the volt age across R_1 would be double across R2. This is due to the fact that V_{IN} is constant (ignoring the AC component) and sets up a fixed current in R_1 which, in turn, flows through R_2 causing a volt age drop equivalent to $V_{R2} = I_E \cdot R_2$. Stated another way, 6V across 5kΩ is the same current as 12V across 10kΩ. In this case, well adjust the value of R_2 so that the q-current set up in R_1 gives us a voltage across R_2 of 1.4V above ground. This is where we expect the base of the Darlington to roughly be. Thus, the drop across the value for R_2 shown in Figure 3 will be 13.4V above the neg ative rail, or 1.4V above ground! Also, this stage is an inverter that takes the inverted signal from the CE and re-aligns the polarity fed to the non-inverting emitter followers to match the input sig nal.

This resistor value can be tweaked to give us exactly i0V_{DC} across the load by using a multi-turn potentiometer in series with R_2. This solution may be good for a breadboard/prototype, but would not be good solution for a real product because:

- The pots value will drift with time/temperature/mechanical vibration, and,
- Each amplifier would have to be individually trimmed

To avoid this scenario, we can use an ingenious opamp stage called a "servo" amplifier.

5) Final Touch: The operation of a servo amp is simple: configured as an inverting integrator, an opamp is con- nected to a node of interest to adjust and the output (-180° out of phase) is injected into another node that can control the node that its monitoring. Figure 4 shows a typical servo application:

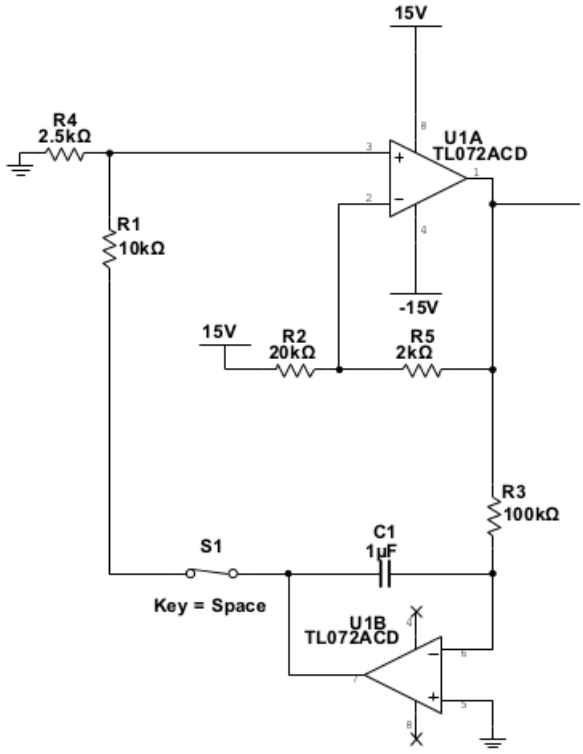

Fig. 9. Use of Op-Amps for Feedback Control

In the above figure, U1A is an inverting amplifier of gain $-\frac{R_5}{R_2}$. Since were feeding 15V into R2, the output of U1A (when S1 is open) is -1.5V. Closing S1 causes the servo to sense the -1.5V and apply slowly increasing opposite voltage. The voltage climbs to the point that the output of U1A become 0V. Any signal with a frequency lower than the servos cutoff frequency will be corrected...as long as U1Bs output can swing sufficient large to adjust U1As offsets via the voltage divider consist ing of R_1 & R_4.

All of these stages, along with the Darlington EF, form Team Helios' final schematic given at the start of this section.

Observe how R_{E1} has been tweaked as a result of design verification using various simulation tools of multisim. As well, observe how R_E on the level shifter is split when a servo is employed.

VI. Cost Analysis of Selected Design

I didn't anticipate this being an all-night affair, but it has been :D For now, cost analysis will merely be the raw cost of components. I'll consider adding in production cost and delivery tables for the presentation over the weekend.

VII. Conclusion

Essentially reiterate the abstract. Place emphasis on cost and how we have not just met but exceeded customer specifications.