

1.4. Hardware Random Number Generator

Preston Maness

Motivation



Why?

- Familiarize myself with an important aspect of modern cryptographic systems.
- Gain experience with signal shaping.
- Explore the interface between hardware and software and how it can be both exploited and hardened.

On the Shoulders of Giants



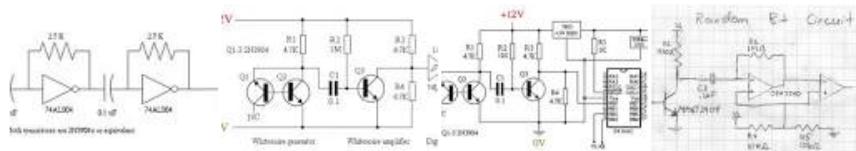
hardware random number generator schematic



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[Images for hardware random number generator schematic](#) - Report images



[Rob Seward :: True Random Number Generator](#)

robseward.com/tp/adv_tech/random_generator/ ▾

I've included **circuit diagrams** as well as links to instructions for fabricating ... True **random number generators** create sequences that are impossible to predict.

[Hardware Random Bit Generator - Jfet.org](#)

web.jfet.org/hw-rng.html ▾

These are some notes about building a **hardware random bit generator**. ... who contemplates arithmetic methods for the generation of **random numbers** is in a state of sin. ... This **circuit** uses avalanche noise in a reverse-biased PN junction, the ...

[HOW TO – Build your own "True Random Number Generator" | MAKE](#)

 makezine.com/2006/10/06/how-to-build-your-own-tru/ ▾

by Phillip Torrone

 Oct 6, 2006 · I've included **circuit diagrams** as well as links to instructions for fabricating your ... True **random number generators** create sequences that are ...

[Building a Hardware Random Bit Generator for EVPmaker](#)

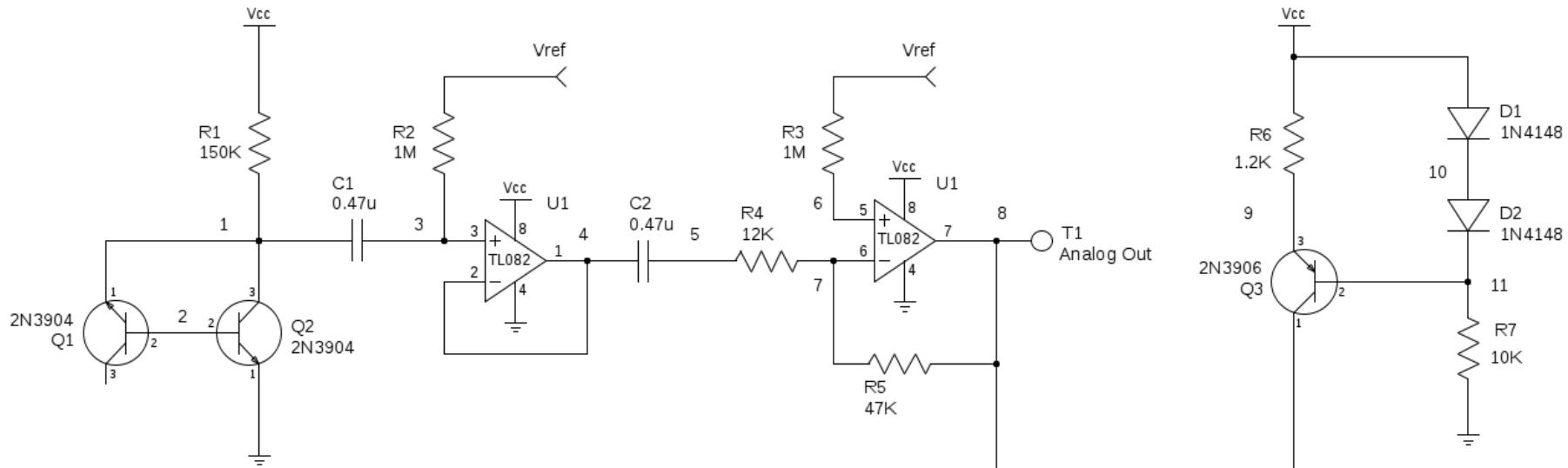
www.tonbandstimmen.de > Start > Software > EVPmaker ▾

I have built the **circuit** on a piece of perforated **circuit board**. ... To get a 32-bit **random number**, the port has to be queried 32 times, while each individual bit is ...

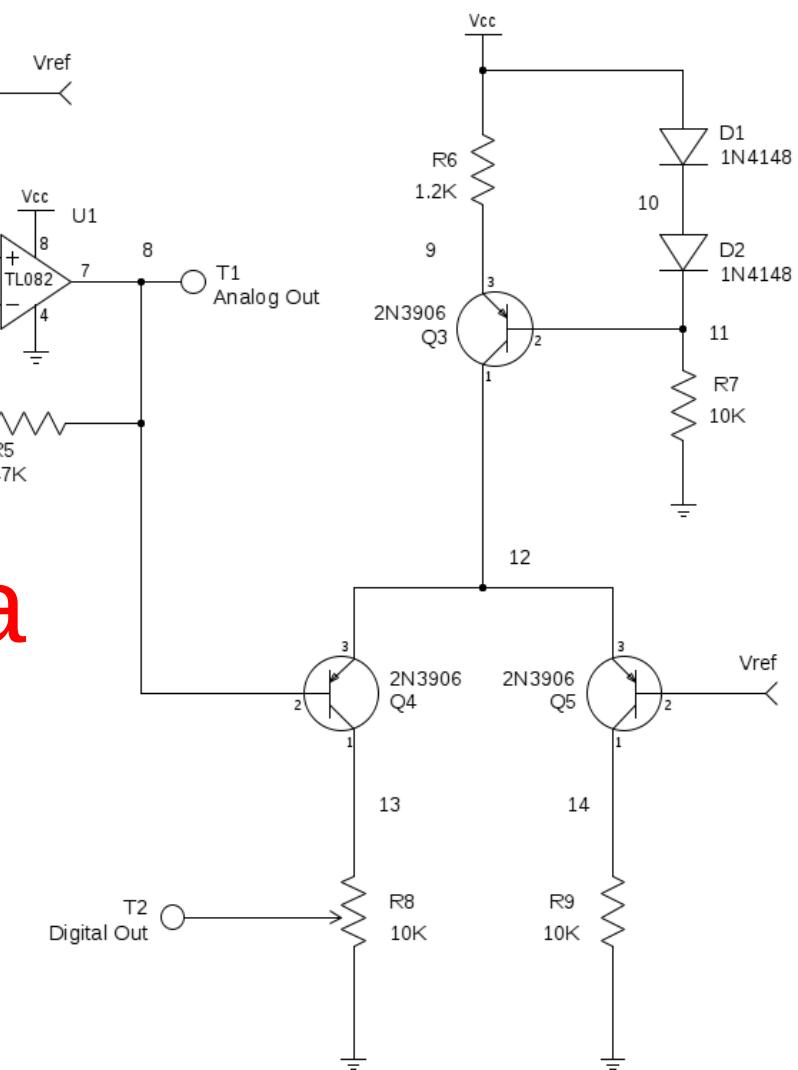
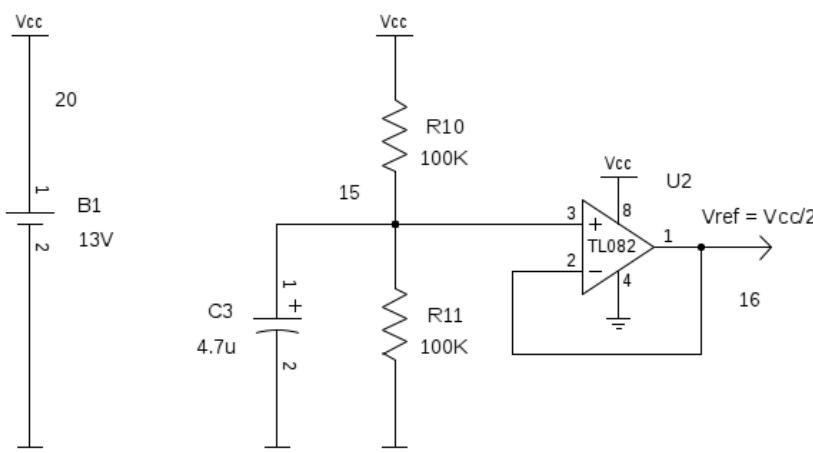
[Random Sequence Generator based on Avalanche Noise](#)

holdenc.altervista.org/avalanche/ ▾

After my experiments with a random sequence **generator** based on Chua **Circuit**, I started investigating other methods for building **hardware random number** ...

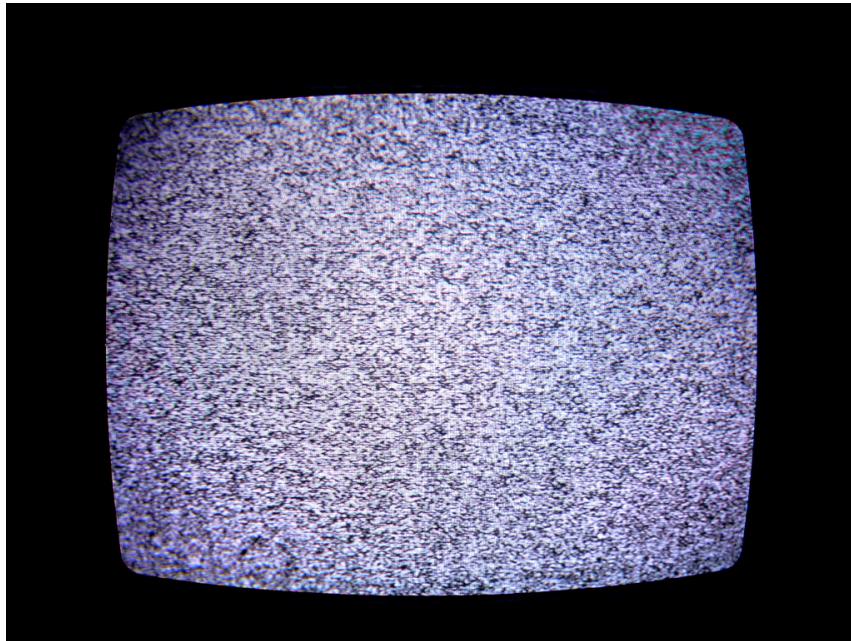


Giorgio Vazzana



Random Bit Generator based on Avalanche Noise			
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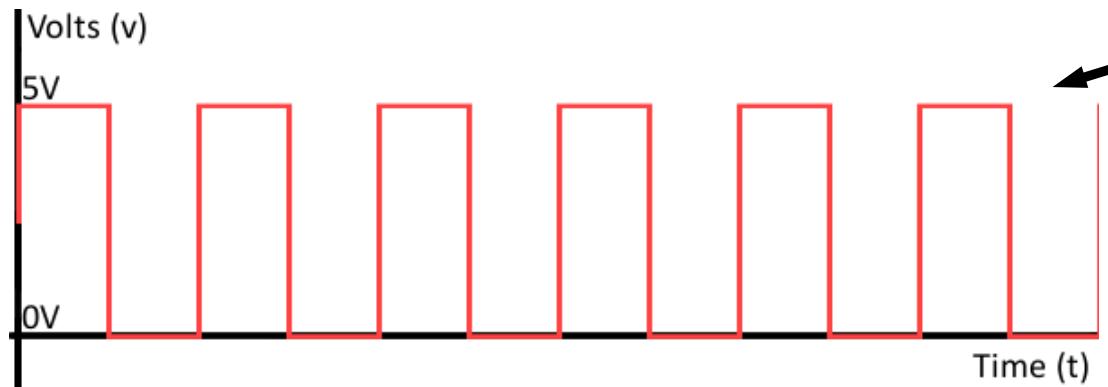
General Principle



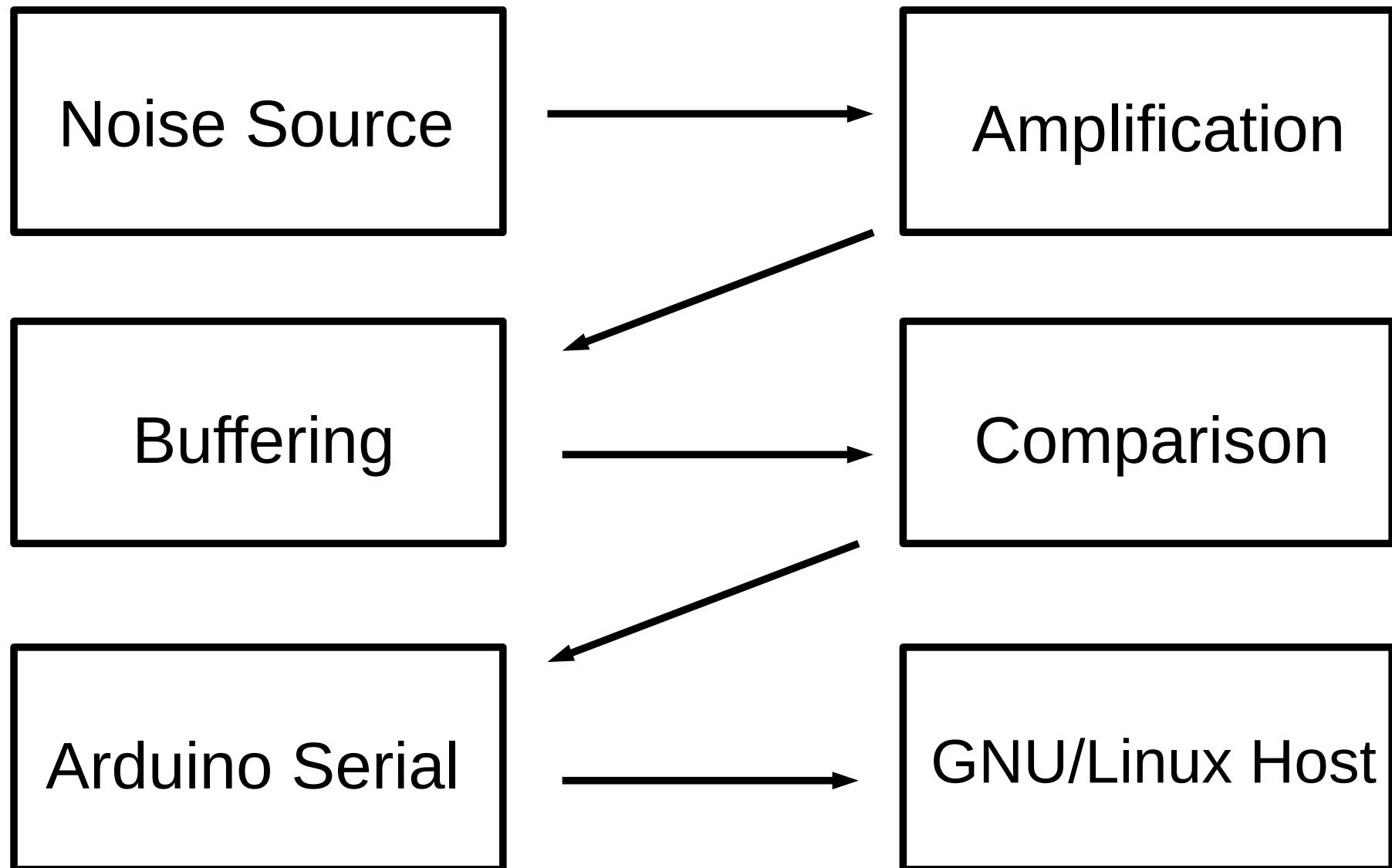
Amplify



Digitize



Hardware Block Diagram

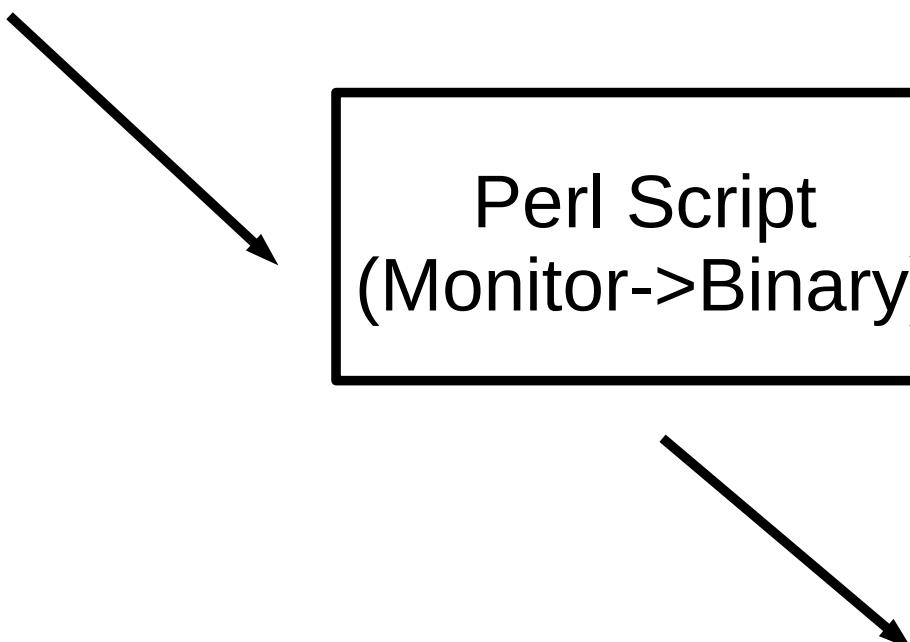


Software Stack

Serial Monitor
(Arduino)

Perl Script
(Monitor->Binary)

Dieharder RNG
Stress Tester



Deliverables

- Functioning prototype that outputs bits to the host.
- Host is able to read this bitstream.
- Host tests the randomness of bitstream.
- Inclusion of verified bitstream into entropy pool.
- Hardware-side verification.
- Automated testing.

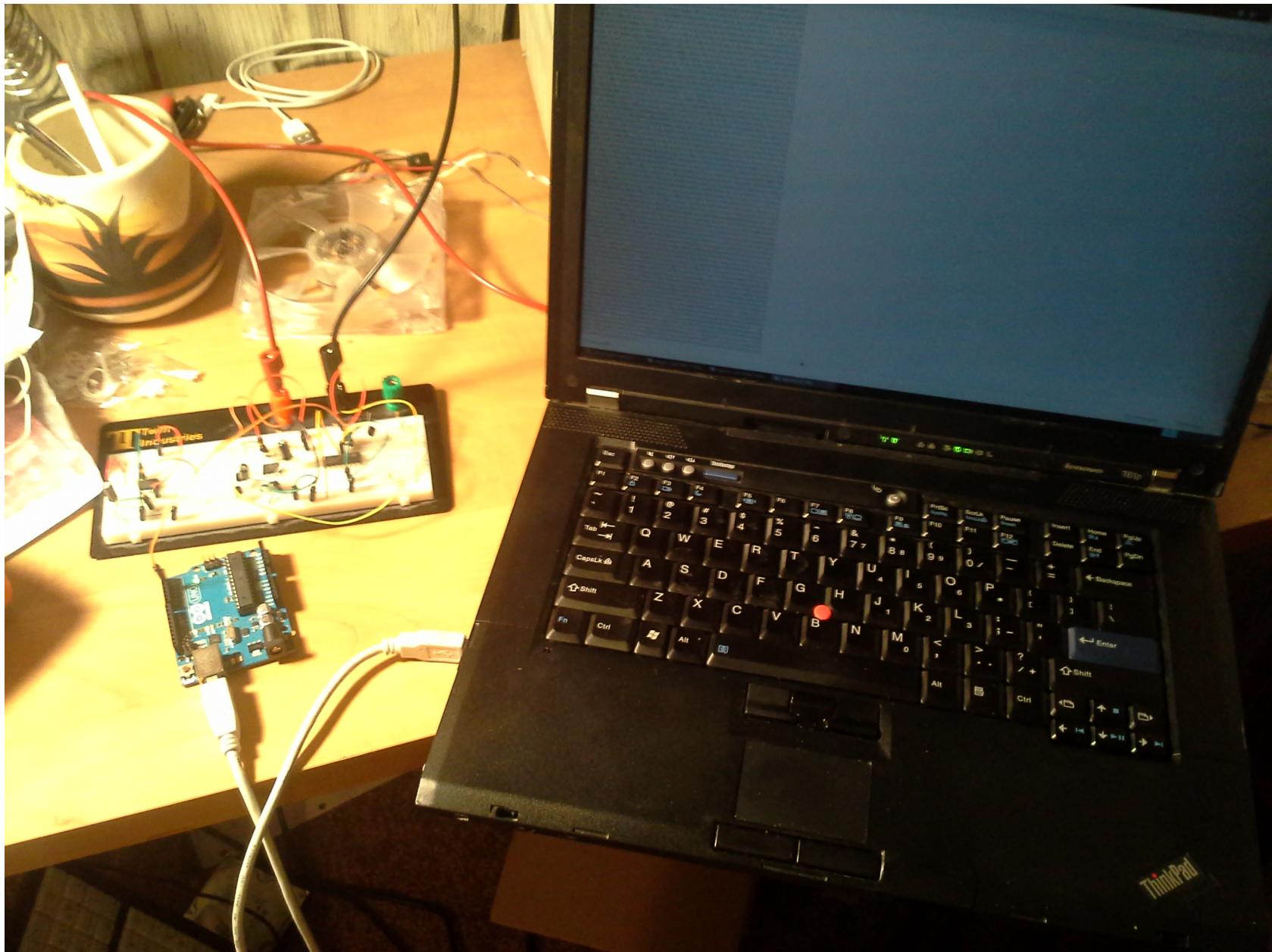
Timeline

Timeframe	Goals
<i>Continuous</i>	<ul style="list-style-type: none">• Research, Verify, Research, and Research some more.
<i>By end of September</i>	<ul style="list-style-type: none">• Verification pipeline determined (dieharder).• Hardware to host communication.
<i>By end of October</i>	<ul style="list-style-type: none">• Verification pipeline functional and providing results of its tests.
<i>By end of semester</i>	<ul style="list-style-type: none">• Verified bitstream.• Automated testing.

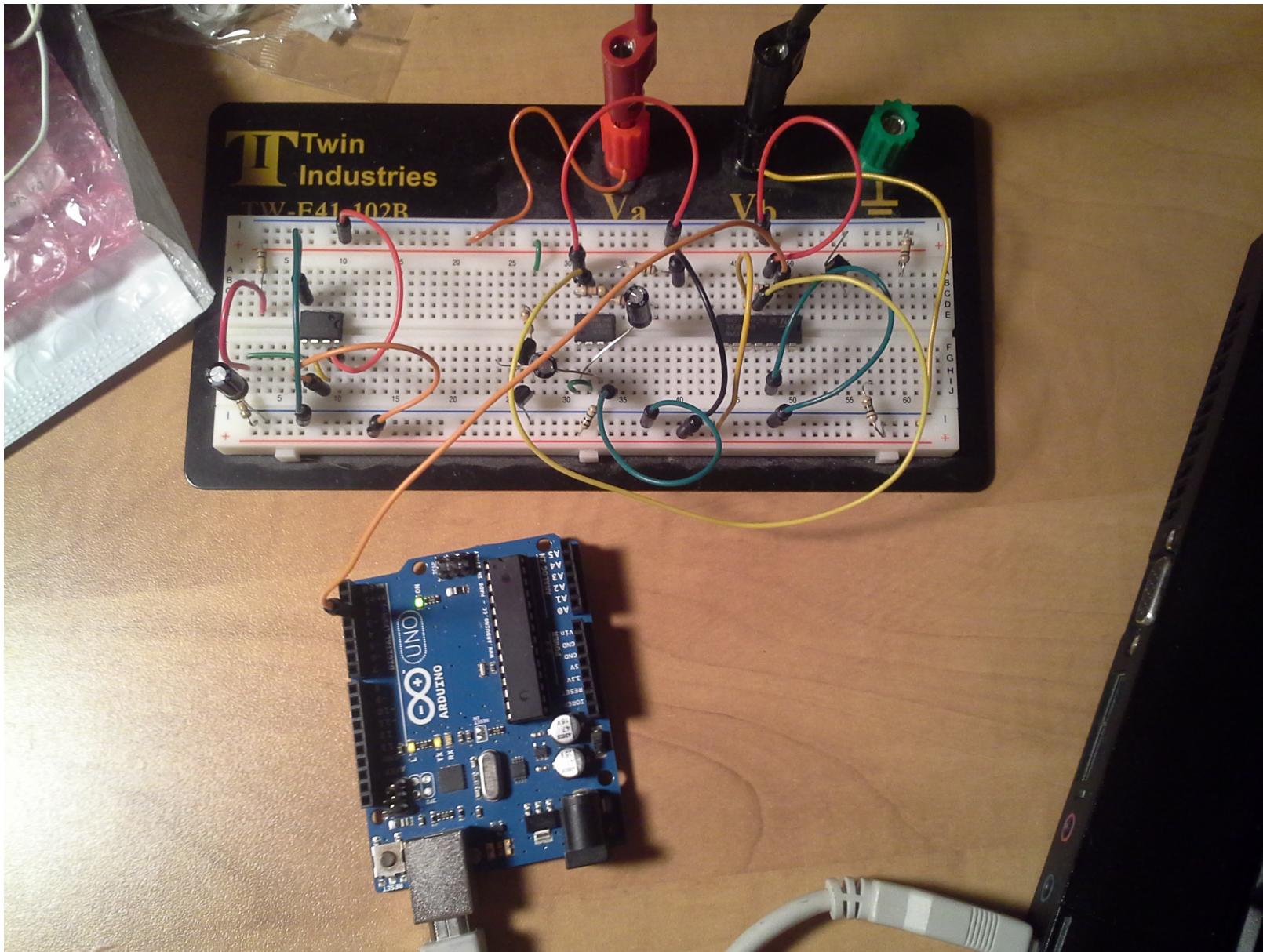
Expense Report

Item	Quantity	Cost
Op-Amp (TL082)	50	\$9.99
BJT (2N3904)	50	\$4.98
Comparator (LM339N)	10	\$3.50
Arduino Uno	1	\$25 (Already Owned)
Resistors	100	~\$5 (Already Owned)
Capacitors	20	~\$5 (Already Owned)
Wiring	Varied	\$2.98
	TOTAL: OUT OF POCKET:	\$56.45 \$21.45

Messy Lab Benches!



Messy Breadboards!



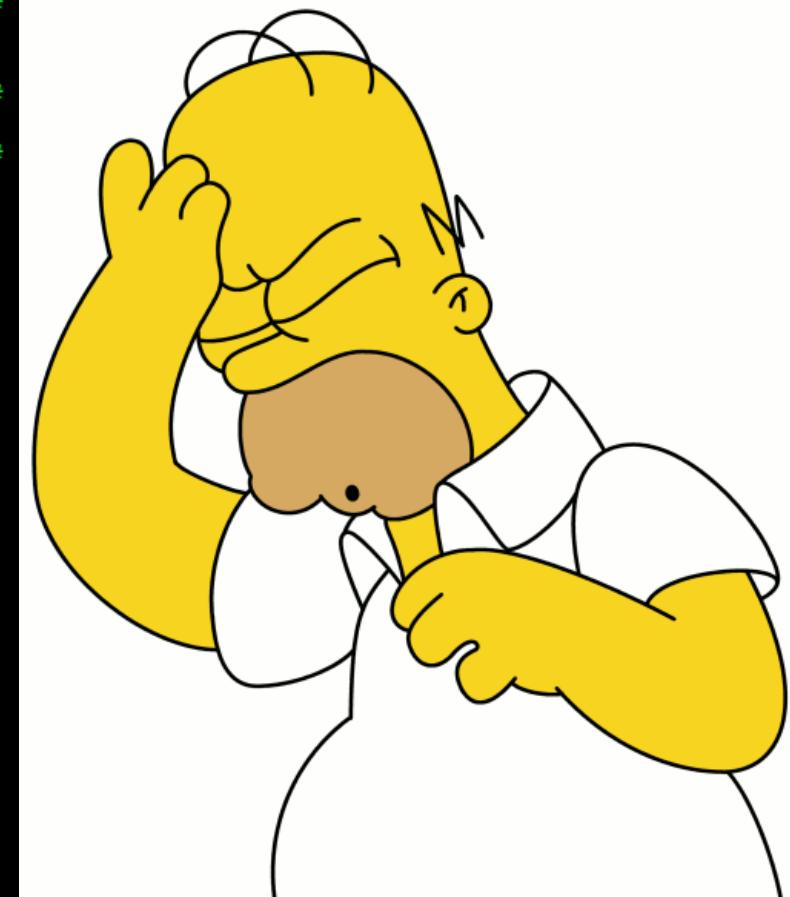
Messy Progress!

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Autoscroll

D'OH!

```
preston@neo:~/ee4390-senior-design-i/src/dieharder-3.31.1/dieharder$ ./dieharder  
-g 201 -a -f ../../rand-stream.bin  
#=====  
# dieharder version 3.31.1 Copyright 2003 Robert G. Brown  
#=====  
rng_name | filename | rands/second|  
file_input_raw| ../../rand-stream.bin| 3.55e+07 |  
#=====  
test_name |ntup| tsamples |psamples| p-value |Assessment|  
#=====  
# The file file_input_raw was rewound 288 times  
diehard_birthdays| 0| 100| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 2373 times  
diehard_operm5| 0| 1000000| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 5042 times  
diehard_rank_32x32| 0| 40000| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 6293 times  
diehard_rank_6x8| 0| 100000| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 6840 times  
diehard_bitstream| 0| 2097152| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 11213 times  
diehard_opso| 0| 2097152| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 14128 times  
diehard_oqso| 0| 2097152| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 15495 times  
diehard_dna| 0| 2097152| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 15628 times  
diehard_count_1s_str| 0| 256000| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 18297 times  
diehard_count_1s_byt| 0| 256000| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 18347 times  
diehard_parking_lot| 0| 12000| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 18381 times  
diehard_2dsphere| 2| 8000| 100|0.0000000| FAILED  
# The file file_input_raw was rewound 18406 times  
diehard_3dsphere| 3| 4000| 100|0.0000000| FAILED
```



The file was rewound...



OVER 9000 TIMES!

Speed Issues

MY SAMPLING RATE IS BAD



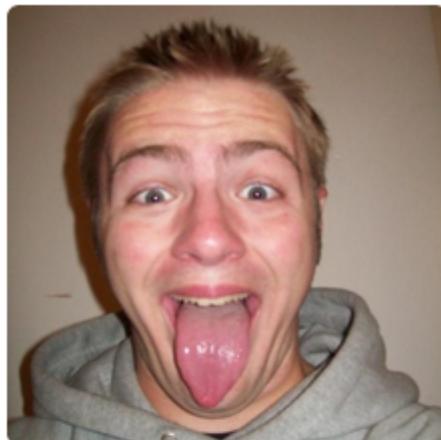
AND I SHOULD FEEL BAD

Looking Forward

- Successful verification via faster sampling.
 - Inclusion into kernel entropy pool.
 - Automate testing harness.
-
- Verify with hardware.
 - Parallelized implementation with rapid sampling of each stream to increase throughput.

Stalk The Project Manager!

<https://github.com/agroskater?tab=repositories>



Preston Maness
agroskater

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✉ http://aspensmonster.com
⌚ Joined on Jul 27, 2011

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ee4323-digital-image-processing

Digital Image Processing with MATLAB

Last updated 6 days ago

Matlab 0 0



cs4328-operating-systems

Repo for CS4328 OS class with Dr. Ziliang during Fall 2013 at Texas State University.

Last updated 6 days ago

c 0 0



ee4352-cmos-vlsi

CMOS VLSI Design with Dr. Aslan Fall 2013 ; Final project 4-bit ALU.

Last updated 6 days ago

Verilog 0 0



cs3339-computer-architecture

Work for Dr. Burtscher's CS3339 Computer Architecture class at Texas State University

Last updated 25 days ago

c 0 0



ee4390-senior-design-i

The project is a hardware RNG. The repo holds code, documentation, schematics/netlists/models, and other work for EE4390 Senior Design I with Dr. Stapleton, Fall 2013.

Perl 0 0