CS 6290, Fall 2014

Project 3 - Report

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As part of this project, we were required to complete simulator for five cache coherence protocols: MSI, MESI, MOSI, MOESI, and MOESIF. I implemented all the five protocols and then validated my implementation against the given standard output for validation traces.

Once all my implementations passed validation, I simulated given experimental traces using the implemented protocols and recorded statistics required for comparing the performance of different protocols, like run times (in cycles) and other statistics (cache misses, cache-to-cahe transfers, and silent upgrades) for different trace-protocol combinations. I then made plots of run times and other statistics versus different protocols for each trace.

All the recorded statistics, corresponding plots for each experimental trace, and discussion on the performance of difference protocols for corresponding trace can be found in subsequent sections.

1 experiment 1

1.1 Results

Experiment 1 simulates memory operations on 4 processors and each process performs 3 operations. Results from simulation run for different cache coherence protocols is tabulated below.

Protocol	Run Time (cycles)	Cache Misses	Silent Upgrades	$-to-$ Transfers
MSI	317	7	0	4
MESI	317	7	0	4
MOSI	217	7	0	5
MOESI	217	7	0	5
MOESIF	217	7	0	5

Figure 1 shows the variation in run time and Figure 2 shows variation in other statistics for the given trace with different protocols.

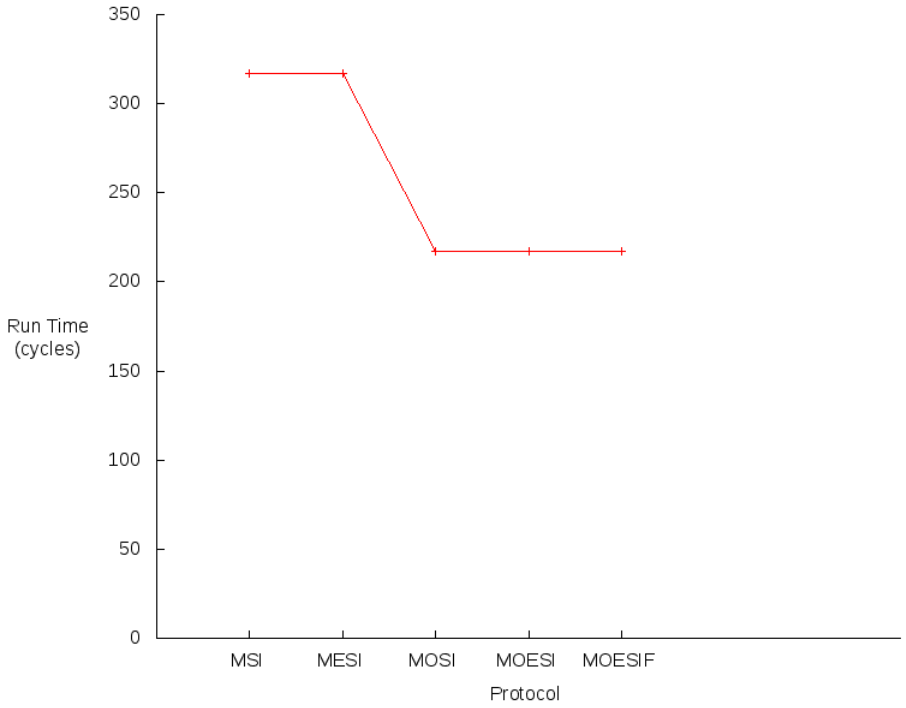

Figure 1: Run times for experiment 1

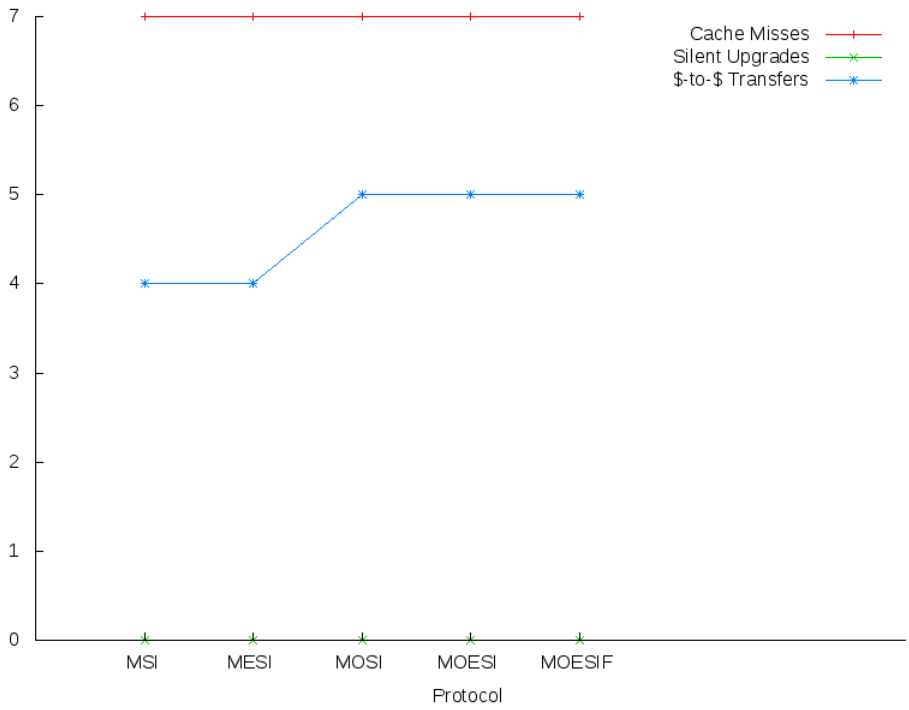

Figure 2: Other statistics for experiment 1

1.2 Analysis

It can be seen that, in terms of run time performance, for this trace $MOESIF = MOESI = MOSI > MESI = MSI$. Looking at other statistics, the reason for this becomes clear. All the protocols cause same number of cache misses however MOSI, MOESI, and MOESIF have one more cache-to-cache transfer resulting in the better run time.

2 experiment 2

2.1 Results

Experiment 2 simulates memory operations on 4 processors and each process performs 26 operations. Results from simulation run for different cache coherence protocols is tabulated below.

Protocol	Run Time (cycles)	Cache Misses	Silent Upgrades	$-to-$ Transfers
MSI	2367	30	0	7
MESI	2267	30	1	8
MOSI	1167	30	0	19
MOESI	1175	31	1	20
MOESIF	885	35	1	27

Figure 3 shows the variation in run time and Figure 4 shows variation in other statistics for the given trace with different protocols.

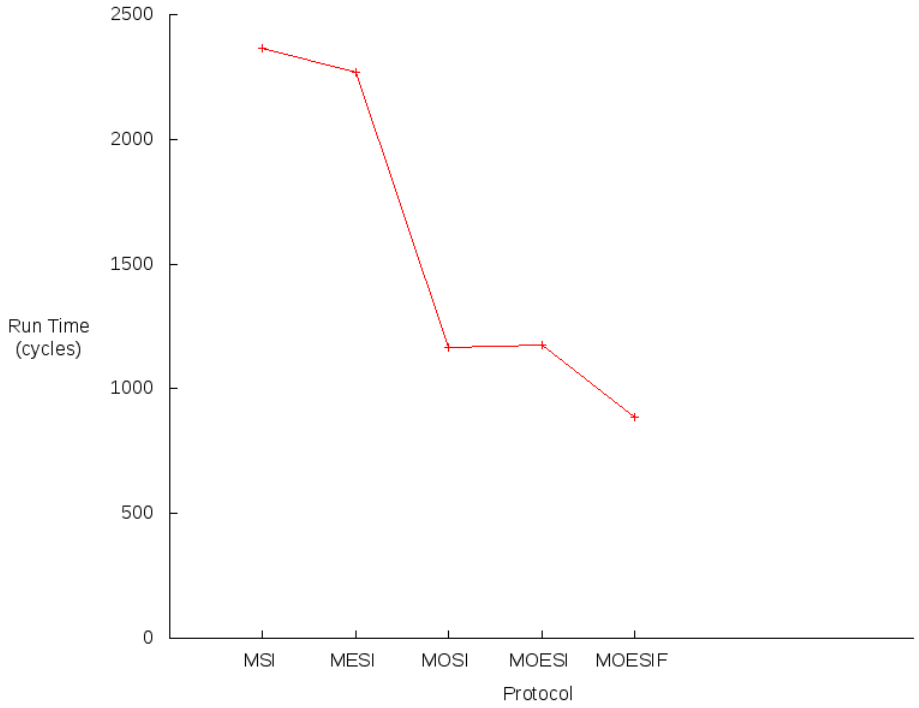

Figure 3: Run times for experiment 2

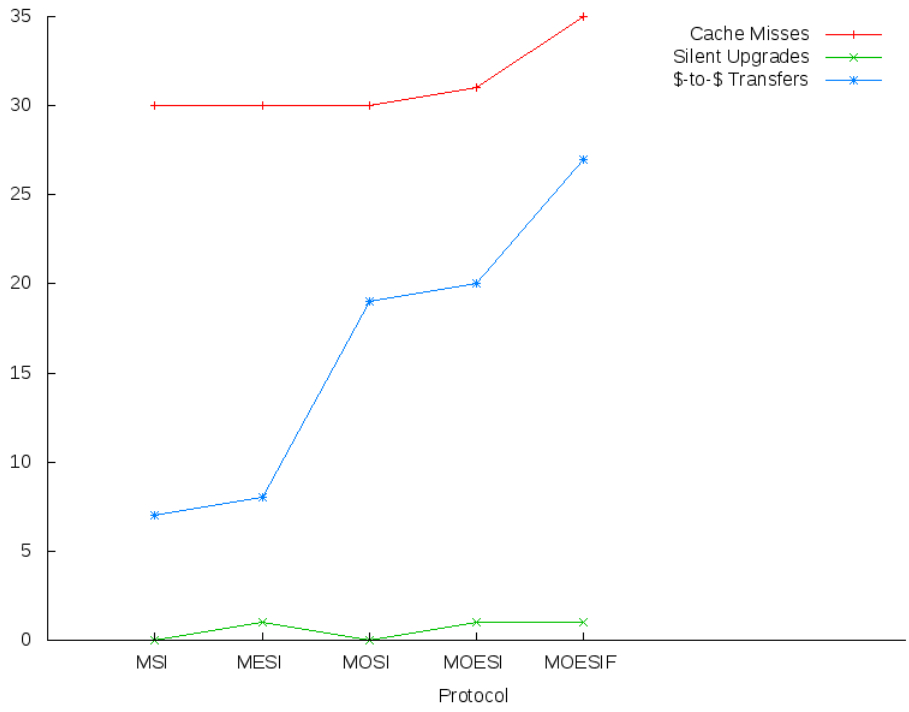

Figure 4: Other statistics for experiment 2

2.2 Analysis

For this trace, run time performance varies as: $MOESIF > MOSI > MOESI > MESI > MSI$. It can be seen from the other statistics plot that number of cache-to-cache transfers for MSI and MESI was significantly lower than other protocols. With almost the same number of cache misses, this explains the higher run times for these two protocols. MOSI and MOESI have almost similar statistics and so have similar runtimes for this trace. MOESIF protocol has more cache misses but the increased number of cache-to-cache transfers more than makes up for higher cache misses and makes MOESIF best performing protocol for this trace.

3 experiment 3

3.1 Results

Experiment 3 simulates memory operations on 8 processors and each process performs 25 operations. Results from simulation run for different cache coherence protocols is tabulated below.

Protocol	Run Time (cycles)	Cache Misses	Silent Upgrades	$-to-$ Transfers
MSI	3723	56	0	20
MESI	2607	48	8	23
MOSI	3723	56	0	20
MOESI	2607	48	8	23
MOESIF	1425	48	8	35

Figure 5 shows the variation in run time and Figure 6 shows variation in other statistics for the given trace with different protocols.

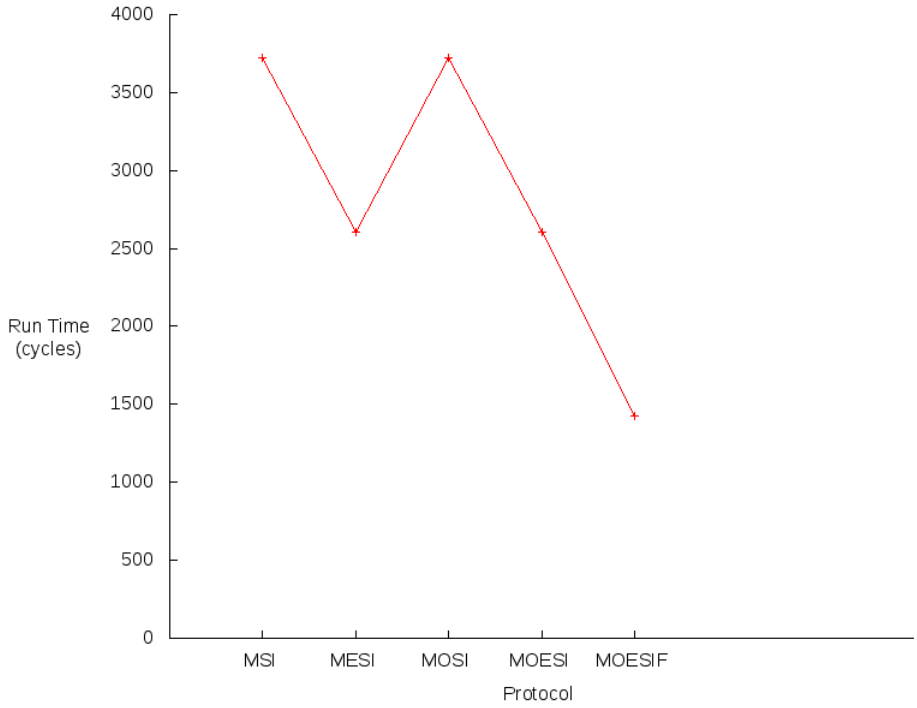

Figure 5: Run times for experiment 3

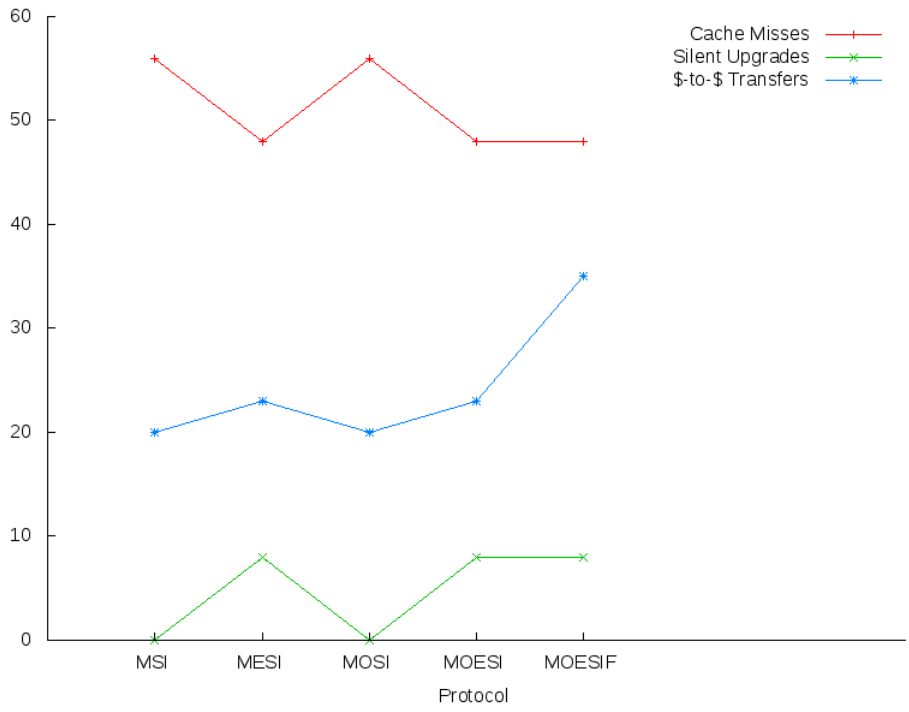

Figure 6: Other statistics for experiment 3

3.2 Analysis

For this trace, run time performance varies as: $MOESIF > MOESI = MESI > MOSI = MSI$. It can be seen that all the other statistics for MSI & MOSI and MESI & MOESI protocol are same and therefore their running times are also same. MOESI & MESI have lower number of cache misses, more silent upgrades, as well as more cache-to-cache transfers than MSI & MOSI, which explains the better running time. All other statistics for MOESIF are same as MESI & MOESIF but it has more cache-to-cache transfers.

4 experiment 4

4.1 Results

Experiment 4 simulates memory operations on 4 processors and each process performs 15 operations. Results from simulation run for different cache coherence protocols is tabulated below.

Protocol	Run Time (cycles)	Cache Misses	Silent Upgrades	$-to-$ Transfers
MSI	2265	27	0	5
MESI	1447	19	3	5
MOSI	1869	29	0	11
MOESI	851	19	3	11
MOESIF	551	19	3	14

Figure 7 shows the variation in run time and Figure 8 shows variation in other statistics for the given trace with different protocols.

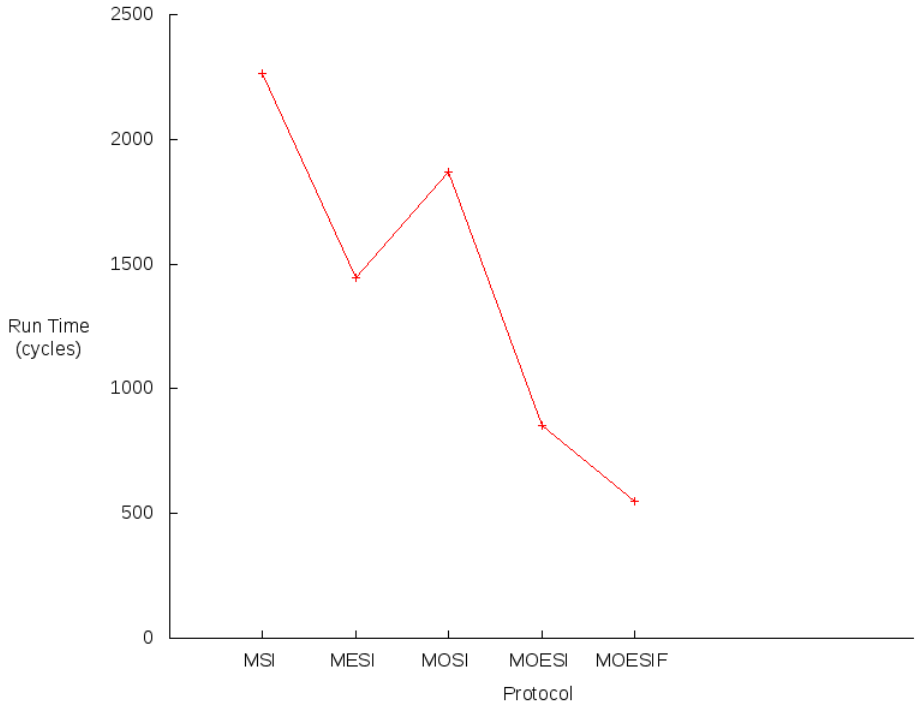

Figure 7: Run times for experiment 4

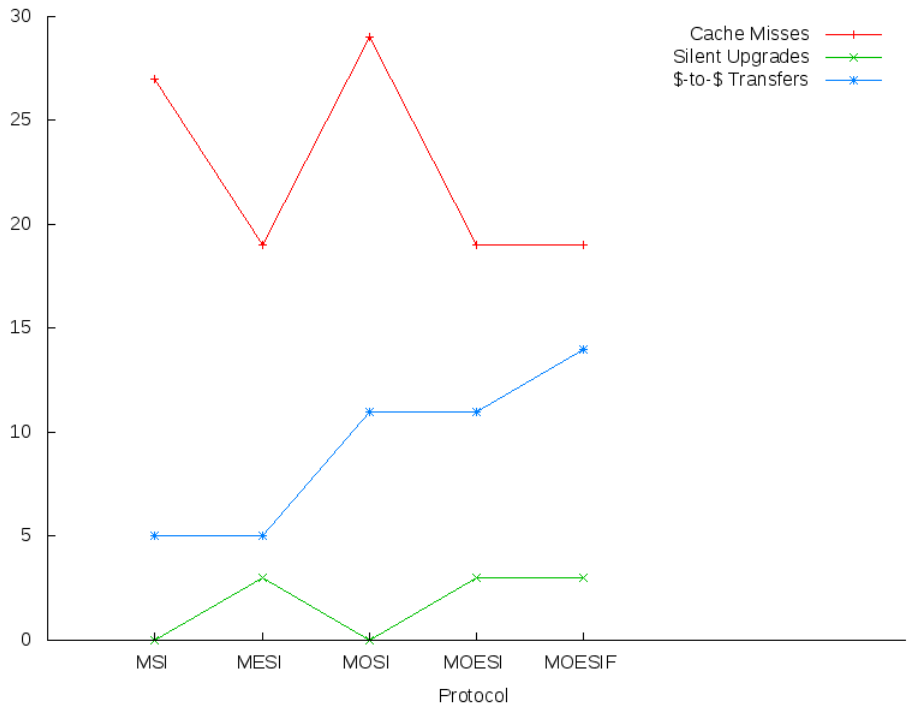

Figure 8: Other statistics for experiment 4

4.2 Analysis

For this trace, run time performance varies as: $MOESIF > MOESI > MESI > MOSI > MSI$. MSI & MOSI have significantly higher number of cache misses than other protocols but MOSI has higher number of cache-to-cache transfers which explains the performance of these two protocols. The other three protocols have same number of cache misses and silent upgrades and the only difference is in the number of cache-to-cache transfers, which explains the order of performance of the other three protocols.

5 experiment 5

5.1 Results

Experiment 5 simulates memory operations on 8 processors with a total of 37 cache accesses distributed variably across the processes. Results from simulation run for different cache coherence protocols is tabulated below.

Protocol	Run Time (cycles)	Cache Misses	Silent Upgrades	$-to-$ Transfers
MSI	1661	21	0	5
MESI	1561	21	0	6
MOSI	1261	21	0	9
MOESI	1161	21	0	10
MOESIF	461	21	0	17

Figure 9 shows the variation in run time and Figure 10 shows variation in other statistics for the given trace with different protocols.

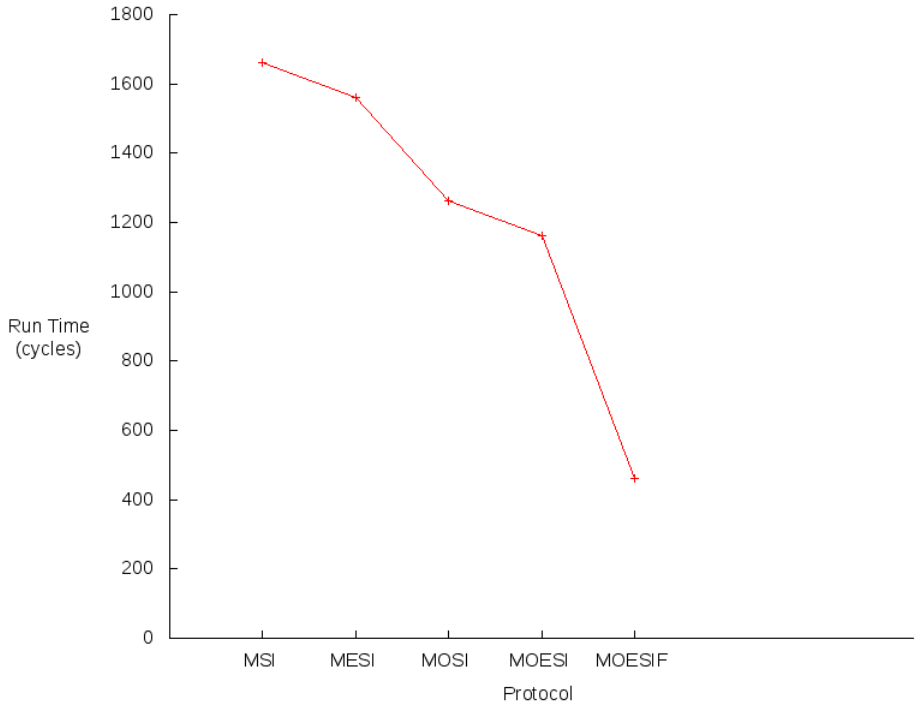

Figure 9: Run times for experiment 5

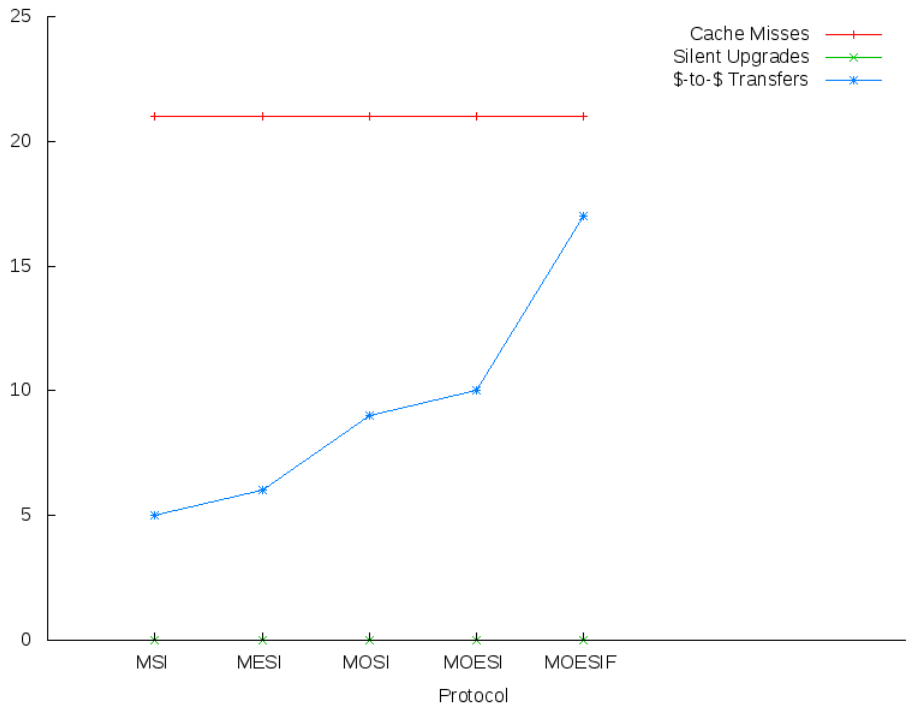

Figure 10: Other statistics for experiment 5

5.2 Analysis

For this trace, run time performance varies as: $MOESIF > MOESI > MOSI > MESI > MSI$. For this trace, number of cache misses, as well as the number of silent upgrades, for all the protocols is same. Therefore, only cache-to-cache transfers matter and an increase in number of cache-to-cache transfers means better run time, thus explaining the order.

6 experiment 6

6.1 Results

Experiment 6 simulates memory operations on 16 processors with a total of 747 cache accesses distributed variably across the processes. Results from simulation run for different cache coherence protocols is tabulated below.

Protocol	Run Time (cycles)	Cache Misses	Silent Upgrades	$-to-$ Transfers
MSI	7775	87	0	12
MESI	4925	62	25	15
MOSI	6975	87	0	20
MOESI	4125	62	25	23
MOESIF	3125	62	25	33

Figure 11 shows the variation in run time and Figure 12 shows variation in other statistics for the given trace with different protocols.

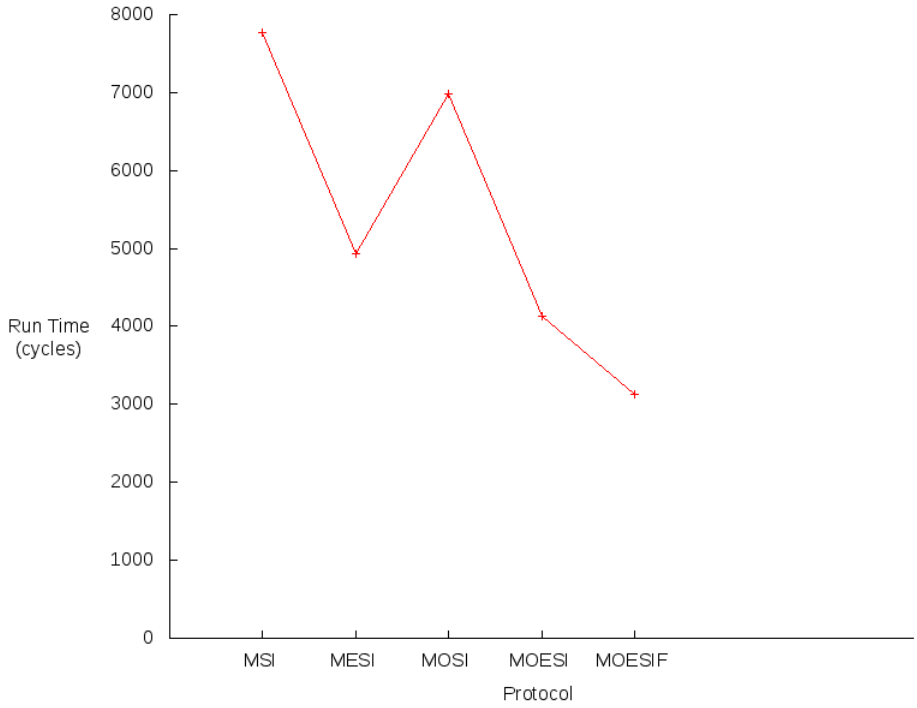

Figure 11: Run times for experiment 6

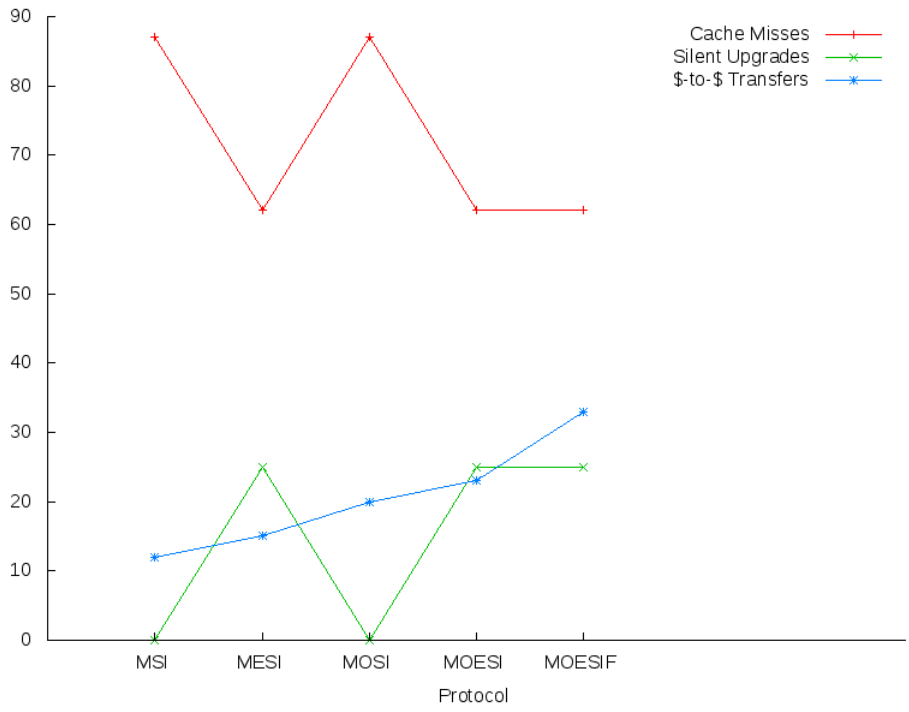

Figure 12: Other statistics for experiment 6

6.2 Analysis

For this trace, run time performance varies as: $MOESIF > MOESI > MESI > MOSI > MSI$. Number of cache misses for MSI & MOSI is same and is much higher than the number of cache misses for MESI, MOESI, & MOESIF. Also, number of cache-to-cache transfers for MOSI is greater than that in MSI, hence the better performance. Similarly, the order between MOESIF, MOESI, & MESI also follows the order of cache-to-cache transfers.

7 experiment 7

7.1 Results

Experiment 7 simulates memory operations on 16 processors with a total of 952 cache accesses distributed variably across the processes. Results from simulation run for different cache coherence protocols is tabulated below.

Protocol	Run Time (cycles)	Cache Misses	Silent Upgrades	$-to-$ Transfers
MSI	6459	79	0	17
MESI	3993	55	24	17
MOSI	5359	79	0	28
MOESI	2909	55	24	28
MOESIF	2909	55	24	28

Figure 13 shows the variation in run time and Figure 14 shows variation in other statistics for the given trace with different protocols.

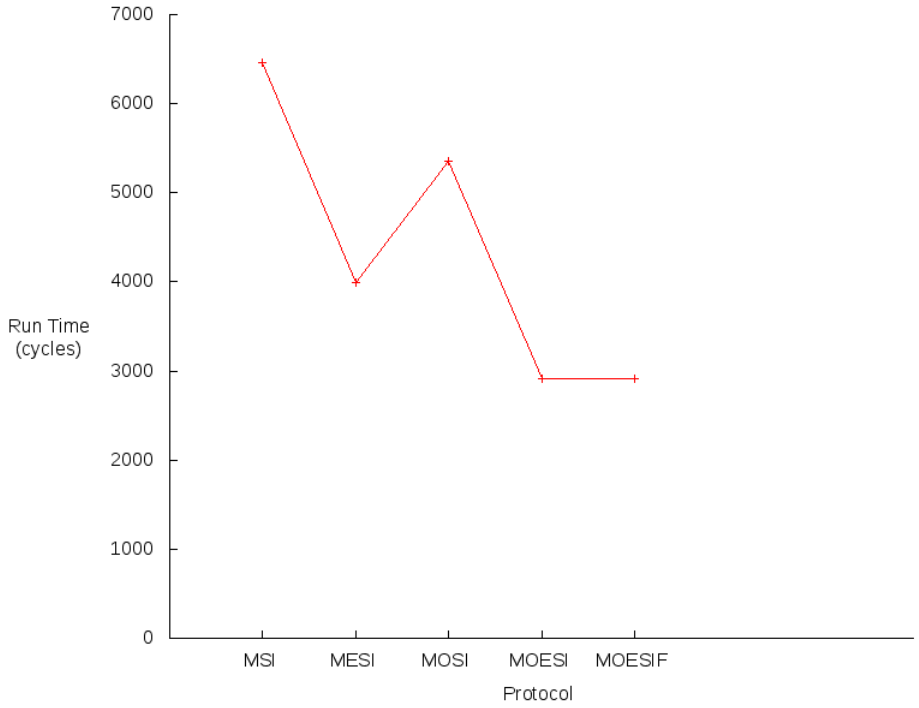

Figure 13: Run times for experiment 7

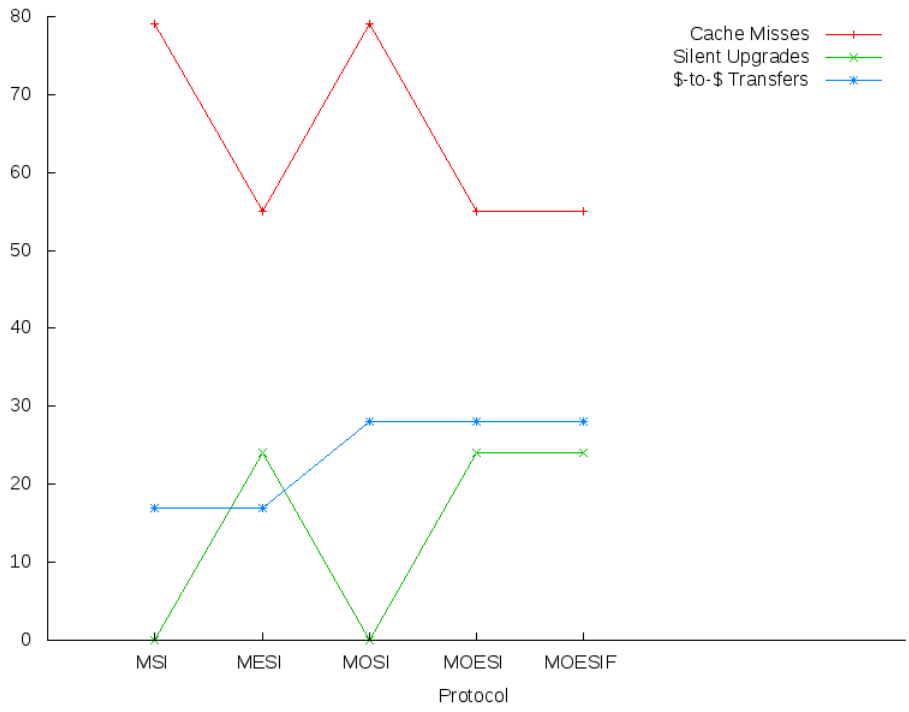

Figure 14: Other statistics for experiment 7

7.2 Analysis

For this trace, run time performance varies as: $MOESIF = MOESI > MESI > MOSI > MSI$. All the statistics are identical for MOESIF & MOESI. MESI has lower number of cache-to-cache transfers and hence the worse run time. Number of cache misses for MSI & MOSI is same and is much higher than the number of cache misses for other protocols. However, MOSI has higher number of cahe-to-cache transfers and therefore better run time.

8 experiment 8

8.1 Results

Experiment 8 simulates memory operations on 16 processors with a total of 800 cache accesses distributed variably across the processes. Results from simulation run for different cache coherence protocols is tabulated below.

Protocol	Run Time (cycles)	Cache Misses	Silent Upgrades	$-to-$ Transfers
MSI	9477	110	0	18
MESI	6441	92	19	30
MOSI	8477	110	0	28
MOESI	5241	92	19	42
MOESIF	4131	92	19	53

Figure 15 shows the variation in run time and Figure 16 shows variation in other statistics for the given trace with different protocols.

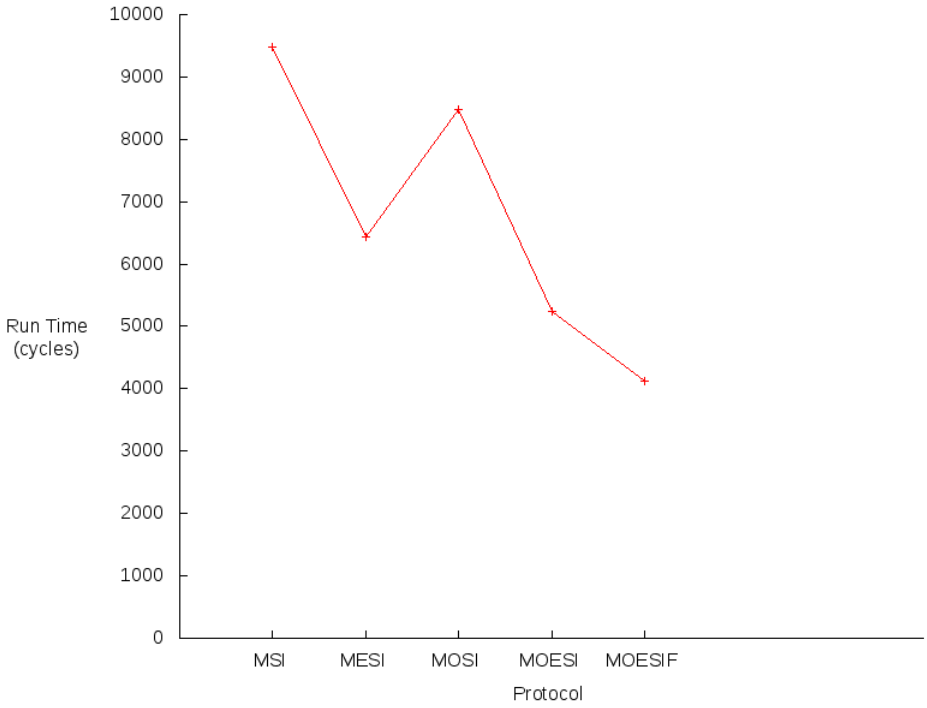

Figure 15: Run times for experiment 8

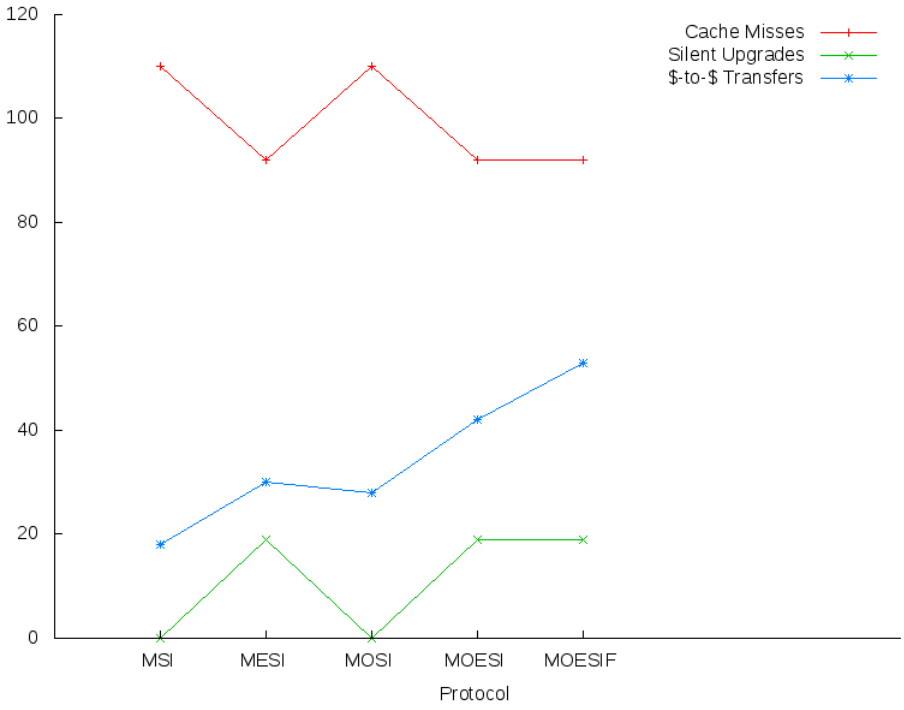

Figure 16: Other statistics for experiment 8

8.2 Analysis

For this trace, run time performance varies as: $MOESIF > MOESI > MESI > MOSI > MSI$. Number of cache misses and number of silent upgrades is same for MOESIF, MOESI, & MESI therefore number of cache-to-cache transfers determines the order of run times. Similarly for MOSI & MSI protocols. The difference between the number of cache misses and silent upgrades decides the ordering of two groups relative to each other, in terms of performance.