CS 6290, Fall 2014

Project 2 - Report

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Given four trace files: `gcc.100k.trace`, `gobmk.100k.trace`, `hmmer.100k.trace`, and `mcf.100k.trace`. An out-of-order superscalar processor, which uses Tomasulo algorithm, needs to be designed for each trace file so that the processor uses least amount of hardware (*as measured by total number of FUs and result buses*) while providing > **95% of the highest value** for retired IPC. Given that:

- There are three types of FUs and there can be 1 or 2 units of each type (k0, k1, and k2).
- Fetch rate (F) can be either 4 or 8.
- There is no restriction on the number of result buses (R).

The approach that I took for designing optimal processor for each trace, as per the given conditions, was to run the simulator for each trace by varying k0, k1, k2, and F in the given ranges. Since there was no restriction specified on R, I decided to use 8 as the upper limit on R for the initial run and increase it later, if required. This resulted in a total of 128 combinations per trace file. Using a Python 2.7 script, I ran the simulator for all these combinations and obtained the corresponding statistics in separate text files for all four trace files.

1 gcc

Data obtained from the first experimental run indicated that maximum IPC for this trace was 2.42207. It was also observed that maximum IPC didn't change with increase in R. Therefore, it was concluded that observed maximum IPC was maximum achievable IPC under the given conditions.

Since upto 95% of the maximum IPC was acceptable, a number of accepted combinations of simulator parameters were obtained. All such combinations for this trace are listed in the table below.

F	R	k0	k1	k2	Total Hardware	Avg IPC	Avg DQ Size	Max DQ Size	Total Run Time (cycles)
4	5	2	2	2	11	2.42207	19953.58789	39581	41287
8	5	2	2	2	11	2.42207	35091.52344	70386	41287
4	6	2	2	2	12	2.42207	19953.58594	39581	41287
8	6	2	2	2	12	2.42207	35091.52344	70386	41287
4	7	2	2	2	13	2.42207	19953.58594	39581	41287
8	7	2	2	2	13	2.42207	35091.52344	70386	41287
4	8	2	2	2	14	2.42207	19953.58594	39581	41287
8	8	2	2	2	14	2.42207	35091.52344	70386	41287
4	4	2	2	2	10	2.411091	20123.78125	39884	41475
8	4	2	2	2	10	2.411091	35193.10156	70573	41475
4	**3**	**2**	**2**	**2**	**9**	**2.366752**	**20666.46484**	**40969**	**42252**
8	3	2	2	2	9	2.366752	35458.66406	71060	42252

It can be seen from the table that minimum total hardware, as quantified by (R + k0 + k1 + k2), is obtained by setting R = 3, k0 = 2, k1 = 2, and k2 = 2. This combination provides an IPC of 2.366752 for this trace. It can also be seen that for the aforementioned parameter values, setting F = 4 would be optimal as it leads to lower average as well as maximum dispatch queue size, while taking same number of cycles.

Therefore, following are the hardware requirements for getting IPC within 95% of the maximum value:

- 3 results buses (R).
- 2 FUs of types 0, 1, and 2 each (k0, k1, and k2 respectively).
- Instrucftion fetch rate (F) of 4.

2 gobmk

Data obtained from the first experimental run indicated that maximum IPC for this trace was 2.364457. It was also observed that maximum IPC didn't change with increase in R. Therefore, it was concluded that observed maximum IPC was maximum achievable IPC under the given conditions.

Since upto 95% of the maximum IPC was acceptable, a number of accepted combinations of simulator parameters were obtained. All such combinations for this trace are listed in the table below.

F	R	k0	k1	k2	Total Hardware	Avg IPC	Avg DQ Size	Max DQ Size	Total Run Time (cycles)
4	5	2	2	2	11	2.364457	20969.99609	42270	42293
8	5	2	2	2	11	2.364457	35747.85547	70241	42293
4	6	2	2	2	12	2.364457	20969.99609	42270	42293
8	6	2	2	2	12	2.364457	35747.85547	70241	42293
4	7	2	2	2	13	2.364457	20969.99609	42270	42293
8	7	2	2	2	13	2.364457	35747.85547	70241	42293
4	8	2	2	2	14	2.364457	20969.99609	42270	42293
8	8	2	2	2	14	2.364457	35747.85547	70241	42293
4	4	2	2	2	10	2.361777	21006.24219	42339	42341
8	4	2	2	2	10	2.361721	35768.86328	70280	42342
4	**3**	**2**	**2**	**2**	**9**	**2.304625**	**21627.49609**	**43520**	**43391**
8	3	2	2	2	9	2.304625	36031.40625	70764	43391

It can be seen from the table that minimum total hardware, as quantified by (R + k0 + k1 + k2), is obtained by setting R = 3, k0 = 2, k1 = 2, and k2 = 2. This combination provides an IPC of 2.304625 for this trace. It can also be seen that for the aforementioned parameter values, setting F = 4 would be optimal as it leads to lower average as well as maximum dispatch queue size, while taking same number of cycles.

Therefore, following are the hardware requirements for getting IPC within 95% of the maximum value:

- 3 results buses (R).
- 2 FUs of types 0, 1, and 2 each (k0, k1, and k2 respectively).
- Instrucftion fetch rate (F) of 4.

3 hmmer

Data obtained from the first experimental run indicated that maximum IPC for this trace was 2.266906. It was also observed that maximum IPC didn't change with increase in R. Therefore, it was concluded that observed maximum IPC was maximum achievable IPC under the given conditions.

Since upto 95% of the maximum IPC was acceptable, a number of accepted combinations of simulator parameters were obtained. All such combinations for this trace are listed in the table below.

F	R	k0	k1	k2	Total Hardware	Avg IPC	Avg DQ Size	Max DQ Size	Total Run Time (cycles)
4	5	2	2	2	11	2.266906	21717.69336	43297	44113
8	5	2	2	2	11	2.266906	35885.85156	71693	44113
4	6	2	2	2	12	2.266854	21718.42578	43301	44114
8	6	2	2	2	12	2.266854	35886.26172	71693	44114
4	7	2	2	2	13	2.266854	21718.42578	43301	44114
8	7	2	2	2	13	2.266854	35886.26172	71693	44114
4	8	2	2	2	14	2.266854	21718.42578	43301	44114
8	8	2	2	2	14	2.266854	35886.26172	71693	44114
4	4	2	2	2	10	2.262546	21769.25586	43422	44198
8	4	2	2	2	10	2.262546	35910.16797	71752	44198
4	**3**	**2**	**2**	**2**	**9**	**2.206385**	**22464.96289**	**44864**	**45323**
8	3	2	2	2	9	2.206385	36254.87109	72457	45323

It can be seen from the table that minimum total hardware, as quantified by (R + k0 + k1 + k2), is obtained by setting R = 3, k0 = 2, k1 = 2, and k2 = 2. This combination provides an IPC of 2.206385 for this trace. It can also be seen that for the aforementioned parameter values, setting F = 4 would be optimal as it leads to lower average as well as maximum dispatch queue size, while taking same number of cycles.

Therefore, following are the hardware requirements for getting IPC within 95% of the maximum value:

- 3 results buses (R).
- 2 FUs of types 0, 1, and 2 each (k0, k1, and k2 respectively).
- Instrucftion fetch rate (F) of 4.

4 mcf

Data obtained from the first experimental run indicated that maximum IPC for this trace was 2.369444. It was also observed that maximum IPC didn't change with increase in R. Therefore, it was concluded that observed maximum IPC was maximum achievable IPC under the given conditions.

Since upto 95% of the maximum IPC was acceptable, a number of accepted combinations of simulator parameters were obtained. All such combinations for this trace are listed in the table below.

F	R	k0	k1	k2	Total Hardware	Avg IPC	Avg DQ Size	Max DQ Size	Total Run Time (cycles)
8	4	2	2	2	10	2.369444	35212.82422	70444	42204
4	5	2	2	2	11	2.369444	20404.9668	40752	42204
8	5	2	2	2	11	2.369444	35213.98828	70446	42204
4	6	2	2	2	12	2.369444	20404.96484	40752	42204
8	6	2	2	2	12	2.369444	35213.98828	70446	42204
4	7	2	2	2	13	2.369444	20404.96484	40752	42204
8	7	2	2	2	13	2.369444	35213.98828	70446	42204
4	8	2	2	2	14	2.369444	20404.96484	40752	42204
8	8	2	2	2	14	2.369444	35213.98828	70446	42204
4	4	2	2	2	10	2.369388	20405.68359	40752	42205
8	3	2	2	2	9	2.324554	35493.12891	70880	43019
4	**3**	**2**	**2**	**2**	**9**	**2.3245**	**20966.50391**	**41941**	**43020**

It can be seen from the table that minimum total hardware, as quantified by (R + k0 + k1 + k2), is obtained by setting R = 3, k0 = 2, k1 = 2, and k2 = 2. This combination provides an IPC of 2.3245 for this trace. It can also be seen that for the aforementioned parameter values, setting F = 4 would be optimal as it leads to lower average as well as maximum dispatch queue size, while taking one cycle more than when fetch rate is set to 8.

Therefore, following are the hardware requirements for getting IPC within 95% of the maximum value:

- 3 results buses (R).
- 2 FUs of types 0, 1, and 2 each (k0, k1, and k2 respectively).
- Instrucftion fetch rate (F) of 4.

From the above results, it can be seen that setting F = 4, R = 3, k0 = 2, k1 = 2, and k2 = 2 leads to near optimal IPC for all the given trace files. Therefore, optimal hardware for all the given traces would have:

- 3 results buses (R).
- 2 FUs of types 0, 1, and 2 each (k0, k1, and k2 respectively).
- Instrucftion fetch rate (F) of 4.

Along with this report, I have submitted following in the archive `project2_asrivastava64.tar.gz`:

- Modified source files (C++): `procsim.hpp`, `procsim.cpp`, and `procsim_driver.cpp`. I also added two files: `tomasulo.hpp` and `tomasulo.cpp` containing declaration and implementation of the simulator class.
- Modified version of `Makefile` for compiling the files and getting the executable.
- The Python script described above, `run_experiments.py`, and four output files, `gcc.100k.txt`, `gobmk.100k.txt`, `hmmer.100k.txt`, and `mcf.100k.txt` produced by running the script.