16 Bits 8 Registradores

Instrução	Operação	Tipo	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOP	nop	NOP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HALT	halt	HALT	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
MOV Rd, Rm	Rd = Rm	MOV	0	0	0	1	0	Rd_2	Rd_1	Rd_0	Rm_2	Rm_1	Rm_0	-	-	-	-	-
MOV Rd, #Im	Rd = #Im	MOV	0	0	0	1	1	Rd_2	Rd_1	Rd_0	Im_7	Im_6	Im_5	Im_4	Im_3	Im_2	Im_1	Im_0
STR [Rm], Rn	[Rm] = Rn	STORE	0	0	1	0	0	-	-	-	Rm_2	Rm_1	Rm_0	Rn_2	Rn_1	Rn_0	-	-
STR [Rm], #Im	[Rm] = #Im	STORE	0	0	1	0	1	Im_7	Im_6	Im_5	Rm_2	Rm_1	Rm_0	Im_4	Im_3	Im_2	Im_1	Im_0
LDR Rd, [Rm]	Rd =[Rm]	LOAD	0	0	1	1	-	Rd_2	Rd_1	Rd_0	Rm_2	Rm_1	Rm_0	-	-	-	-	-
ADD Rd, Rm, Rn	Rd = Rm + Rn	ULA	0	1	0	0	-	Rd_2	Rd_1	Rd_0	Rm_2	Rm_1	Rm_0	Rn_2	Rn_1	Rn_0	-	-
SUB Rd, Rm, Rn	Rd = Rm - Rn	ULA	0	1	0	1	-	Rd_2	Rd_1	Rd_0	Rm_2	Rm_1	Rm_0	Rn_2	Rn_1	Rn_0	-	-
MUL Rd, Rm, Rn	Rd = Rm * Rn	ULA	0	1	1	0	-	Rd_2	Rd_1	Rd_0	Rm_2	Rm_1	Rm_0	Rn_2	Rn_1	Rn_0	-	-
AND Rd, Rm, Rn	Rd = Rm and Rn	ULA	0	1	1	1	-	Rd_2	Rd_1	Rd_0	Rm_2	Rm_1	Rm_0	Rn_2	Rn_1	Rn_0	-	-
ORR Rd, Rm, Rn	Rd = Rm or Rn	ULA	1	0	0	0	-	Rd_2	Rd_1	Rd_0	Rm_2	Rm_1	Rm_0	Rn_2	Rn_1	Rn_0	-	-
NOT Rd, Rm	Rd = ¬Rm	ULA	1	0	0	1	-	Rd_2	Rd_1	Rd_0	Rm_2	Rm_1	Rm_0	-	-	-	-	-
XOR Rd, Rm, Rn	Rd = Rm xor Rn	ULA	1	0	1	0	-	Rd_2	Rd_1	Rd_0	Rm_2	Rm_1	Rm_0	Rn_2	Rn_1	Rn_0	-	-