improV RISC-V Microprocessor Workflow

1. **Kick-off meeting** - overview of the project, describing what we're going to be doing
2. **Role assignment** - break down the project into modules (ALU, Memory, Control, etc.) and identify areas that people want to work on for their standalone module.
3. **Tutorials** - go through a couple of examples of SystemVerilog for design and verification, as well as functional coverage, assertions and UVM.
4. **Create specification** - identify what sort of requirements the processor will have and discuss design and verification methodologies of meeting these requirements.
5. **Start design and verification work**:
    a. Phase 1 - getting the barebones microprocessor designed and validated - provides a simple way of getting used to the tools and languages.
    b. Phase 2 - implement design techniques such as pipelining.
    c. Phase 3 - implementation of verbose design - i.e. diving much more into the depths of microprocessor architecture and organisation. At the end of this phase, there should be a fully designed, pipelined and verified RISC-V microprocessor.
    d. Phase 4 - Individual design and verification work on each member's selected module
    e. Phase 5 - Integration of multiple cores of the microprocessor.