University of Rochester

Ece 200 - Computer Organization

Lab 4 Report

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Abstract

In this lab I simulated a single-cycle 16 bit RISC processor in a mostly structural fashion. In total 26 instructions were implemented.

1 Introduction

2 Single-Cycle Implementation

3 Additional Instructions

4 Test Bench

All 26 instructions were tested in the same test bench code, the input instruction and the expected output is shown in the following table.

Instruction Type	Instruction Code (Hex)	Expected Output (Hex)
and		

Table 1: Test Bench

5 Factorial Code