December						
Memorabe-19-16, No. 19-16	Opcode	31 30 29 28				
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Sold Cine						
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Substitution						
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### SOCK-COMMAND ADD PR					П	1 1 1
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### STRECOMEN OF MAIN PROPERTY OF THE STREET						
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RESCONDIA-SO RE, Ro, No OF RE 0 0 0 1 1 1 1 1 1 1 1	SUB <cond><s> Rd, Rn, Rm OP Rs</s></cond>		0 0 0 0 0 1 0	S R	R	R 0 1 R
ADD-Conduct-29 Mail, Bin, Ban OP Has	RSB <cond><s> Rd, Rn, Rm OP #</s></cond>		0 0 0 0 0 1 1	S R	R	# 0 R
### ADD-CORD-Lecond-2- Mids, Patt, Pat, Patt, Pa	RSB <cond><s> Rd, Rn, Rm OP Rs</s></cond>		0 0 0 0 0 1 1	S R	R	
MONICOCAMINATE No.						# 0 1
ADD-Commond-SP ADD, ADD Per DO DO DO DO S S R R R DO DO DO DO DO						
ADD-CORDAG-SP RAIL, BAIL, BA						
DEAL-Conded-Sp. Male, No. 19						# 0 1
GENCOMMAND R. NR. NO D R NR. R NR. NR NR NR NR						
### CORDINATION STATE STAT						
BRILL-Conded-Sp RELO. PRINT, INC. PR 0 0 0 0 0 1 0 1 0 8 R H R L R 0 0 0 0 0 1 R R R G 0 0 0 0 0 1 1 8 R R R G 0 0 0 0 1 R R R R G 0 0 0 0 0 R R R R R G 0 0 0 0 1 R R R R R G 0 0 0 0 1 R R R R R R G 0 0 0 0 1 R R R R G 0 0 0 0 1 R R R R R G 0 0 0 0 1 R R R R R R G 0 0 0 0 1 R R R R R R G 0 0 0 0 1 R R R R R R R R R						
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### BIRNEAGNER ARE ARE ARE ARE ARE ARE ARE ARE ARE A						
SPR-CORDAD Rd. Ray						
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MSS-conds PSE Conds PSE PS				_	_	# 0 10
Intercond Page Pa				_		
GDP-cond-Xm, Na OP #						
### SPRINGORD ##	CMP <cond> Rn, Rm OP #</cond>		0 0 0 1 0 1 0	1 R	SB	# ⁹ 0 R
SPR-Cond-2 Rd, Rm, Rm OP 8			0 0 0 1 0 1 0	1 R		
CIMPLECORDAD RD, PRO PR				_		
MNK-conds-Sp Rd, Pan Pan Ra Ra Ra Ra Ra Ra Ra				_		
SSR-conds-SPR_d, Fin, Fin OP #				_	_	
ORRIGORATES Nd, RR, NB OF 8						
DREACHORD-SE Rd, Rm, OP 8				-		
MOVECOND-65 Rd, Rm OP Rs						# U IX
BONCEONDA-ES Rd, Rm, Rm OF 8						
BICCCOOMS-CS Rd, Rm, Rm OP #						
MVRsconds-Sp Rd, Rm OP Rs						
MVNconds-Ss Rd, Rm, #	BIC <cond><s> Rd, Rn, Rm OP Rs</s></cond>		0 0 0 1 1 1 0	S R	R	R 0 9 1 R
ADD-cond-SP Rd, Rn, #	MVN <cond><s> Rd, Rm OP #</s></cond>		0 0 0 1 1 1 1	S SB	R	# 0 R
DOR-cond-N-SP Rd, Rn, #	MVN <cond><s> Rd, Rm OP Rs</s></cond>		0 0 0 1 1 1 1	S SB	R	R 0 9 1 R
Subsconds-65				_		π
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B8Cccond> <s> Rd, Rn, # </s>						
STR-cond> Rn, #				_		
MSR.cond> CFSR f, #						
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CRNccond> Rn, #	MSR <cond> CPSR_f, #</cond>		0 0 1 1 0 0 1	0	SBO	#
MSRcconds SPSR f, # 0 0 1 1 0 1 1 0 SBO	CMP <cond> Rn, #</cond>		0 0 1 1 0 1 0	1 R	SB	#
DRRCCONd> <s> Rd, #</s>	CMN <cond> Rn, #</cond>			1 R		#
MOV.cond> <s> Rd, # BIC.cond><s> Rd, Rn, # MOV.cond><s> Rd, Rn, # BIC.cond><s> Rd, Rn, # BIC.cond><s #="" bic.cond="" rd,="" rn,=""><s #="" bic.cond="" rd,="" rn,=""> Rd, Rn, # BIC.cond> Rd, Rn, Rn, Rn, Rn, Rn, Rn, Rn, Rn, Rn, Rn</s></s></s></s></s></s></s></s></s></s>					SBO	#
BICCCOnd> <pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>S</pre>Rd, Rn, #</pre> <pre>BICCCOnd><pre>BICCCOnd><pre>S</pre>Rd, Rn, #</pre> <pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCOnd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BICCCONd><pre>BI</pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre></pre>	ORR <cond><s> Rd, Rn, #</s></cond>		0 0 1 1 1 0 0	D D		
MYN-cond> STR-cond> Rd, Rn, # LDR-cond> Rd, Rn, # Rd, Rn, # LDR-cond> Rd, Rn, # Rd, Rn, # LDR-cond> Rd, Rn, # Rd, Rn, #<			0 0 4 4		R	#
STR <cond> Rd, Rn, #</cond>	MOV <cond><s> Rd, #</s></cond>			S SB	R R	#
LDR <cond> Rd, Rn, # STR<cond>B Rd, Rn, # LDR<cond>B Rd, Rn, # LDR<cond>B Rd, Rn, # STR<cond>B Rd, Rn, # STR<cond>B Rd, Rn, # LDR<cond>B Rd, Rn, # STR<cond>B Rd, Rn, # LDR<cond>B Rd, Rn, # LDR<cond #="" b="" l<="" ldr<cond="" rd,="" rn,="" td=""><td>MOV<cond><s> Rd, # BIC<cond><s> Rd, Rn, #</s></cond></s></cond></td><td></td><td>0 0 1 1 1 1 0</td><td>S SB</td><td>R R R</td><td># #</td></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, #</s></cond></s></cond>		0 0 1 1 1 1 0	S SB	R R R	# #
STR.cond.bB Rd, Rn, #	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, #</s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 0 1 1 1 1 1 1	S SB S R S SB	R R R	# # # # #
LDR <cond>B Rd, Rn, # STR<cond>T Rd, Rn, # LDR<cond>P U 1 W 1 R R R # STR<cond>T Rd, Rn, # LDR<cond>P U 1 W 1 R R R # LDR<cond>T Rd, Rn, # LDR<cond>T Rd, Rn, # LDR<cond>B Rd, Rn, # LDR<cond #="" b="" ldr<cond="" rd,="" rn,="">B Rd, Rn, # LDR<cond #="" b="" ld<="" ldr="" ldr<cond="" rd,="" rn,="" td=""><td>MOV<cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, # STR<cond> Rd, #</cond></s></cond></s></cond></s></cond></td><td></td><td>0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 1 0 P U 0 W</td><td>S SB S R S SB O R</td><td>R R R R</td><td># # # #</td></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, # STR<cond> Rd, #</cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 1 0 P U 0 W	S SB S R S SB O R	R R R R	# # # #
LDR <cond>T Rd, Rn, #</cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, #</cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 1 0 P U 0 W 0 1 0 P U 0 W	S SB S R S SB O R	R R R R R	# # # # # # # # # # # # # # # # # # # #
STR <cond>BT Rd, Rn, #</cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, #</cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 1 0 P U 0 W 0 1 0 P U 0 W 0 1 0 P U 1 W	S SB S R S SB O R 1 R	R R R R R R R R R	# # # # # #
LDR <cond>BT Rd, Rn, #</cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Bd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, #</cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 1 0 1 0 P U 0 W 0 1 0 P U 1 W	S SB SB S SB S SB S SB S SB S SB S SB	R R R R R R R	# # # # # # # # # # # # # # # # # # #
STR <cond> Rd, Rn, #</cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> B Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, #</cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 1 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1	S SB S R S SB 0 R 1 R 0 R 1 R	R R R R R R R R	# # # # # # # # #
LDR <cond> Rd, Rn, # STR<cond>B Rd, Rn, # LDR<cond>B Rd, Rn, # LDR<cond>B Rd, Rn, # STR<cond>B Rd, Rn, # LDR<cond>B Rd, Rn, # LDR<cond #="" b="" l<="" ldr<cond="" rd,="" rn,="" td=""><td>MOV<cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond></td><td></td><td>0 0 1 1 1 1 0 0 0 1 1 1 1 1 1 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1</td><td>S SB S R S SB 0 R 1 R 0 R 1 R 0 R 1 R</td><td>R R R R R R R R</td><td># # # # # # # # # # # # # # # # # # #</td></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 1 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1	S SB S R S SB 0 R 1 R 0 R 1 R 0 R 1 R	R R R R R R R R	# # # # # # # # # # # # # # # # # # #
STR <cond>B Rd, Rn, #</cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Bd, Rn, # STR<cond> Rd, Rn, # STR<cond>TRd, Rn, # STR<cond>TRd, Rn, # LDR<cond>TRd, Rn, # LDR<cond>TRd, Rn, # LDR<cond>TRd, Rn, # LDR<cond>TRd, Rn, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1	S SB SB R S SB SB O R 1 R O R 1 R O R 1 R O R 1 R O R 1 R O R 1 R O R 1 R O R 1 R O R 1 R O R O	R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
LDR <cond>B Rd, Rn, #</cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> B Rd, Rn, # STR<cond>B Rd, Rn, # STR<cond>T Rd, Rn, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 1	S SBS RS RS SBS RS SBS RS SBS RS SBS RS	R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
STR <cond>T Rd, Rn, # LDR<cond>T Rd, Rn, # LDR<cond>T Rd, Rn, # LDR<cond>T Rd, Rn, # Do 1 1 0 U 0 1 1 R R R # 0 R R R # 0 R R R # 0 R R R # 0 R R R # 0 R R R R # 0 R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R</cond></cond></cond></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Ed, Rn, # STR<cond> Ed, Rn, # STR<cond> T Rd, Rn, # LDR<cond> T Rd, Rn, # LDR<cond> Rd, Rn, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 1 0 0 U 1 1 0 1 1 0 0 U 0 1	S SBS R R S SBS R R S SBS R R R R R R R	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
LDR <cond>T Rd, Rn, # STR<cond>BT Rd, Rn, # LDR<cond>T Rd, Rn, # LDR</cond>T Rd, Rn, Rn, Rn, * LDR</cond>T Rd, Rn, Rn, * LDR</cond>T Rd, Rn, Rn, Rn, * LDR</cond>T Rd, Rn, Rn, Rn, Rn, Rn, Rn, Rn, Rn, Rn, Rn</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 0 1	S SBS R R S SBS R R S SBS R R R R R R R	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
STR <cond>BT Rd, Rn, #</cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> B Rd, Rn, # STR<cond> T Rd, Rn, # LDR<cond> T Rd, Rn, # LDR<cond> T Rd, Rn, # LDR<cond> B Rd, Rn, # LDR<cond> B Rd, Rn, # LDR<cond> B Rd, Rn, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 0 0 U 0 0 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 1 W	S SBS R R SS SBS R R SS SBS R R R SS SBS R R R R	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
Undefined Instruction	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 1 W	S SBS R R S SBS R R S SBS R R R R R R R	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
STM <cond><addrmode> Rm<!-- -->, reg list</addrmode></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> B Rd, Rn, # STR<cond> B Rd, Rn, # STR<cond> B Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> T Rd, Rn, # LDR<cond> T Rd, Rn, # STR<cond> B Rd, Rn, # LDR<cond> B Rd, Rn, # LDR<cond> B Rd, Rn, # STR<cond> T Rd, Rn, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 P U 1 W	S SBS R R S SBS R R S SBS R R S SBS R R R R	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
DMccond>caddrmode> Rmc!>, reg list	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond>T Rd, Rn, # LDR<cond>T Rd, Rn, # LDR<cond>T Rd, Rn, # STR<cond>T Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 0 0 U 0 1 1 0 1 0 0 U 0 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 0 U 0 1	S SBS R R S SBS R R S SBS R R S SBS R R R R	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
STM <cond><addrmode> Rm, reg list^</addrmode></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # S</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 1 P U 1 W	S SBS R SBS SBS R SBS SBS R R SBS SBS R R SBS R R SBS R R SBS R R R SBS R R R SBS R R R R	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
UNPREDICTABLE LDM <cond><addrmode> Rm, reg list^ 1 0 0 P U 1 0 1 R 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</addrmode></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # S</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 1 P U 1 W	S SBS RS SBS RS SBS SBS RS SBS SBS RS SBS RS SBS RS SBS RS RS SBS RS	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
LDM <cond><addrmode> Rm, reg list^</addrmode></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MIV<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> T Rd, Rn, # LDR<cond> T Rd, Rn, # LDR<cond> T Rd, Rn, # STR<cond> T Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<sin s<="" str<sin="" td=""><td></td><td>0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 D U 1 U 1 U 1 U 1 U 1 U 1 U 1 U 1 U</td><td>S SBS R R SS R R SS SB R R SS SB R R SS SB R R SS R R SS R R R SS R R R R</td><td>R R R R R R R R R R R R R R R R R R R</td><td># # # # # # # # # # # # # # # # # # #</td></sin></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 D U 1 U 1 U 1 U 1 U 1 U 1 U 1 U 1 U	S SBS R R SS R R SS SB R R SS SB R R SS SB R R SS R R SS R R R SS R R R R	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
UNPREDICTABLE	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MVN<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<str<str<str<str<str<str<str<str<str<< td=""><td></td><td>0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 P U 1 W 0 1 1 P U 1 W 0 1 1 0 U 0 1 0 1 1 D U 1 1 1 0 1 1 0 U 0 1 0 1 1 D U 1 W 0 1 1 1 D U 1 W 0 1 1 1 D U 1 U 1 0 1 1 0 U 1 1 1 0 1 1 0 U 1 1 1 0 1 1 0 U 1 1 1 0 1 1 0 U 0 U 1 0 1 1 D U 0 U 1 1 0 1 1 D U 0 U 0 U 1 0 1 1 D U 0 U 0 U 0 U 0 U 0 U 0 U 0 U 0 U 0 U</td><td>S SBS R SB S SB S SB S SB S SB S SB S S</td><td>R R R R R R R R R R R R R R R R R R R</td><td># # # # # # # # # # # # # # # # # # #</td></str<str<str<str<str<str<str<str<str<<></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 P U 1 W 0 1 1 P U 1 W 0 1 1 0 U 0 1 0 1 1 D U 1 1 1 0 1 1 0 U 0 1 0 1 1 D U 1 W 0 1 1 1 D U 1 W 0 1 1 1 D U 1 U 1 0 1 1 0 U 1 1 1 0 1 1 0 U 1 1 1 0 1 1 0 U 1 1 1 0 1 1 0 U 0 U 1 0 1 1 D U 0 U 1 1 0 1 1 D U 0 U 0 U 1 0 1 1 D U 0 U 0 U 0 U 0 U 0 U 0 U 0 U 0 U 0 U	S SBS R SB S SB S SB S SB S SB S SB S S	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
LDM <cond><addrmode> Rm<!-- -->, reg list^</addrmode></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MINC<ond><s> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # Undefined Instruction STM<cond> Rd, Rn, # Undefined Only Rd, Rn, # Undefined Only Rd, Rn, # STM<cond> Rd, Rn, Rm< Rm<!-- --> reg list UNPREDICTABLE</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></ond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 1 0 P U 0 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 P U 1 W 1 P U 1 W 1 P U 1 W 1 P U 1 W	S SBS R SB	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
LDM <cond><addrmode> Rm<!-- -->, reg list^</addrmode></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MIVAcond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond #="" ldr<cond="" rd,="" rn,=""> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond #="" ldr<co<="" ldr<cond="" rd,="" rn,="" td=""><td></td><td>0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 1 P U 1 W 1 0 0 P U 1 0 W 1 0 0 P U 1 0 W</td><td>S SBS R S S SBS R S S SBS R S SBS R S S SBS R S S S S</td><td>R R R R R R R R R R R R R R R R R R R</td><td># # # # # # # # # # # # # # # # # # #</td></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 1 P U 1 W 1 0 0 P U 1 0 W 1 0 0 P U 1 0 W	S SBS R S S SBS R S S SBS R S SBS R S S SBS R S S S S	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
BL <cond> <target addr=""></target></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MINC<ond><s> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STM<cond> Rd, Rn, # Undefined Instruction STM<cond> Rd STM<cond> Rd STM<cond> Rd STM<cond> Rd STM<cond> Rm<!-- --> reg list UNPREDICTABLE LDM<cond> Rm, reg list UNPREDICTABLE STM<cond> Rm<!-- --> reg list</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></ond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 P U 1 W 0 1 1 0 U 1 1 0 1 1 0 U 1 1 1 0 0 P U 0 W	SB S	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
STC <cond> p<cp_num>, CRd, # 1 1 0 P U N W 0 R CR # LDC<cond> p<cpp_num>, CRd, En, CRm, CRm, CRm, CRm, CRm, CRm, CRm, CRm</cpp_num></cond></cp_num></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MIV<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rm<!-- -->, reg list STM<cond> Rd<rd<cond< td=""><td></td><td>0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 1 P U 1 W 1 0 1 1 0 U 1 1 0 1 1 0 U 1 1 1</td><td>SB SB S</td><td>R R R R R R R R R R R R R R R R R R R</td><td># # # # # # # # # # # # # # # # # # #</td></rd<cond<></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 1 P U 1 W 1 0 1 1 0 U 1 1 0 1 1 0 U 1 1 1	SB S	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
LDC <cond> p<cp_num>, CRd, #</cp_num></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MINC<ond><s> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> TRd, Rn, # Undefined Instruction STM<cond> Rm<!-- -->, reg list STM<cond> Rd STM<cond> Rm<!-- -->, reg list UNPREDICTABLE STM<cond> Rm<!-- -->, reg list UNPREDICTABLE STM<cond> Rm<!-- -->, reg list DM<cond> Caddrmode> Rm<!-- -->, reg list DM< Cond> Caddrmode> Rm<!-- -->, reg list</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></ond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 1	SB S	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
CDP <cond> p<cp#>,,CRd,CRn,CRm,<o2> 1 1 0 1 CR CR 2 0 CR MCR<cond> p<cp#>,,Rd,CRn,CRm,<o2> 1 1 1 0 1 0 CR R 2 1 CR MRC<cond> p<cp#>,,Rd,CRn,CRm,<o2> 1 1 1 0 1 1 CR R 2 1 CR</o2></cp#></cond></o2></cp#></cond></o2></cp#></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MINC<ond><s> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rm<!-- -->, reg list UNPREDICTABLE LDM<cond> caddrmode> Rm<!-- -->, reg list UNPREDICTABLE STM<cond> caddrmode> Rm<!-- -->, reg list LDM<cond> caddrmode> Rm<!-- -->, reg list LDM<cond> caddrmode> Rm<!-- -->, reg list EDM<cond> caddrmode> Rm<!-- -->, reg list EDM<cond< td=""><td></td><td>0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 0 U 1 W 0 1 1 0 U 1 1 1 0 1 1 0 U 1 1 1 1 0 0 P U 1 0 W 1 0 0 P U 1 0 W 1 0 0 P U 1 0 W 1 0 0 P U 1 U W 1 0 0 P U 1 U W 1 0 0 P U 1 U W</td><td>S S S S S S S S S S S S S S S S S S S</td><td>R R R R R R R R R R R R R R R R R R R</td><td># # # # # # # # # # # # # # # # # # #</td></cond<></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></ond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 0 U 1 W 0 1 1 0 U 1 1 1 0 1 1 0 U 1 1 1 1 0 0 P U 1 0 W 1 0 0 P U 1 0 W 1 0 0 P U 1 0 W 1 0 0 P U 1 U W 1 0 0 P U 1 U W 1 0 0 P U 1 U W	S S S S S S S S S S S S S S S S S S S	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
MCR <cond> p<cp#>,,Rd,CRn,CRm,</cp#></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MIV<cond><s> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> T Rd, Rn, # LDR<cond> T Rd, Rn, # STR<cond> T Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> T Rd, Rn, # LDR<cond #="" ldr<cond="" rd,="" rn,="" t=""> T Rd, Rn, # LDR<cond #="" ldr<cond="" r<="" rd,="" rn,="" t="" td=""><td></td><td>0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 0 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 1 0 U 1 1 0 1 1 0 U 1 1 0 1 1 0 U 1 1 0 1 1 0 U 1 U 1 U 1 0 1 1 0 U 1 U 1 U 1 0 1 1 0 U 1 U 1 U 1 0 1 0 0 P U 1 U W 1 0 0 P U 1 U W</td><td>S S S S S S S S S S S S S S S S S S S</td><td>R R R R R R R R R R R R R R R R R R R</td><td># # # # # # # # # # # # # # # # # # #</td></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></cond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 P U 1 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 0 0 U 0 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 1 0 U 1 1 0 1 1 0 U 1 1 0 1 1 0 U 1 1 0 1 1 0 U 1 U 1 U 1 0 1 1 0 U 1 U 1 U 1 0 1 1 0 U 1 U 1 U 1 0 1 0 0 P U 1 U W 1 0 0 P U 1 U W	S S S S S S S S S S S S S S S S S S S	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
MRC <cond> p<cp#>,,Rd,CRn,CRm,</cp#></cond>	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MINC<ond><s> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> T Rd, Rn, # STR<cond> Rm<!-- -->, reg list STM<cond> Rd STM<cond> Rm<!-- -->, reg list STM<cond> Rd STM<cond> Rm<!-- -->, reg list UNPREDICTABLE STM<cond> Rm<!-- -->, reg list UNPREDICTABLE STM<cond> Rm<!-- -->, reg list UNPREDICTABLE STM<cond> Rm<!-- -->, reg list UNPREDICTABLE STM<cond> caddrmode> Rm<!-- -->, reg list DM< cond> caddrmode> Rm<!-- -->, reg list STM<cond> caddrmode> Rm<!-- -->, reg list STM<cond> caddrmode> Rm<!-- -->, reg list STM<cond> caddrmode> Rm<!-- -->, reg list DM< cond> caddrmode> Rm<!-- -->, reg list STM<cond> caddrmode> Rm<!-- -->, reg list DM< cond> caddrmode> Rm<!-- -->, reg list B< cond> ctarget addr> BL< cond> ctarget addr> BL< cond> ctarget addr> BL< cond> ctarget addr> BL< cond> ccond> p< cp num>, CRd, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></ond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 0 1 1 1 1 1 0 0 0 1 1 1 1 1 1 0 0 0 1 0 1 1 1 1 0 0 0 0 0 1 0 1 1 1 0 0 0 0 0 0 1 1 1 0	S S S S S S S S S S S S S S S S S S S	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MINC<ond><s> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rm<!-- -->, reg list "UMPREDICTABLE STM<cond> RddTmode> Rm<!-- -->, reg list "BL<cond> ctarget addr> BL<cond> ctarget addr> BL<cond> ctarget addr> BL<cond> pccp num, CRd, # LDC<cond> pccp num, CRd, #</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></s></ond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 0 0 U 1 1 0 1 1 0 U 1 1 0 1 1 0 U 0 1 0 1 1 P U 1 W 0 1 1 1 P U 1 W 0 1 1 1 P U 1 W 0 1 1 1 0 U 1 1 1 0 1 0 0 P U 1 0 W 1 1 0 0 P U 1 W 1 1 0 0 P U N W 1 1 0 0 P U N W 1 1 1 0 P U N W 1 1 1 0 P U N W	SB S	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #
	MOV <cond><s> Rd, # BIC<cond><s> Rd, Rn, # MINC<ond>>S> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> T Rd, Rn, # LDR<cond> T Rd, Rn, # STR<cond> T Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> T Rd, Rn, # STR<cond> Rd, Rn, # STR<cond> Rd, Rn, # LDR<cond> T Rd, Rn, # LDM<cond> T Rd, Rn, reg list LDM<cond> Caddrmode> Rm<!-- -->, reg list LDC<cond> Cadget addr> STC<cond> pccp num>, CRd, # LDC<cond> pccp num>, CRd, # LDC<cond> pccp num>, CRd, Rd, Rd, Rd, Rd, Rd, Rd, Rd, Rd, Rd,</cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></cond></ond></s></cond></s></cond>		0 0 1 1 1 1 0 0 0 1 1 1 1 1 0 0 0 1 0 P U 0 W 0 1 0 P U 1 W 0 1 0 P U 1 W 0 1 0 0 U 0 1 0 1 0 0 U 1 1 0 1 1 P U 0 W 0 1 1 P U 1 W 0 1 1 1 P U 1 W 1 0 0 P U 1 W 1 1 1 0 P U N W 1 1 1 0 P U N W 1 1 1 0 P U N W	S S S S S S S S S S S S S S S S S S S	R R R R R R R R R R R R R R R R R R R	# # # # # # # # # # # # # # # # # # #

M	M	0	S F
E	EQ	0 0 0 0	= 1
N E	NE	0 0 0 1	= 0
C S	CS	0 0 1 0	C = 1
C C	CC	0 0 1 1	C = 0
U H S	HS	0 0 1 0	C = 1
U L	LO	0 0 1 1	C = 0
M /N	MI	0 1 0 0	N = 1
P /P	PL	0 1 0 1	N = 0
0	VS	0 1 1 0	V = 1
N O	VC	0 1 1 1	V = 0
U H	HI	1 0 0 0	C = 1, = 0
U L ₉ S	LS	1 0 0 1	C = 0, = 1
S G E	GE	1 0 1 0	N = V
S L	LT	1 0 1 1	N != V
S G	GT	1 1 0 0	= 0, N = V
S L E	LE	1 1 0 1	= 1, N != V
Α	AL	1 1 1 0	-
N 9	NE	1 1 1 1	-

FE EJECTEO ARM Reference

ARM Reference	-	
Opcode	Notes	ZCNV
ADC <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	-	s s s s
ADD <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	-	s s s s
AND <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	-	S S S
B <cond> <target_addr></target_addr></cond>	-	
BIC <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	-	s s s
BL <cond> <target_addr></target_addr></cond>	-	
BX <cond> Rm</cond>	-	
CDP <cond> p<cp#>,o1,CRd,CRn,CRm,o2</cp#></cond>	-	
CMN <cond> Rn, <sh_op></sh_op></cond>	-	x
CMP <cond> Rn, <sh_op></sh_op></cond>	-	x
EOR <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	-	s s s
LDC <cond> p<cp_num>, CRd, #</cp_num></cond>	-	
LDM <cond><adm> Rm, {reg list}^</adm></cond>		
LDM <cond><adm> Rm<!-- -->, {reg list}</adm></cond>	"!" K R V	
LDM <cond><adm> Rm<!-- -->, {reg list}^</adm></cond>	-	
LDR <cond> Rd, Rn, #</cond>	ĺ	
LDR <cond>B Rd, Rn, #</cond>	ĺ	
LDR <cond>BT Rd, Rn, #</cond>		
LDR <cond>H Rd, <address> LDR<cond>SB Rd, <address></address></cond></address></cond>	ĺ	
LDR <cond>SB Rd, <address> LDR<cond>SH Rd, <address></address></cond></address></cond>	ĺ	
LDR <cond>SH Rd, <address> LDR<cond>T Rd, Rn, #</cond></address></cond>	ĺ	
MCR <cond> p<cp#>,o1,Rd,CRn,CRm,o2</cp#></cond>	_	1
MLA <cond><s> Rd, Rm, Rs, Rn</s></cond>		s s s
MOV <cond><s> Rd, <sh_op></sh_op></s></cond>		SSS
noviconarios na, ibn_ops	R ≗ 15	3 3 3
MRC <cond> p<cp#>,o1,Rd,CRn,CRm,o2</cp#></cond>	10 - 15	* * * *
MRS <cond> Rd, CPSR</cond>	9	
MRS <cond> Rd, SPSR</cond>		
MSR <cond> CPSR <fields>, Rm</fields></cond>	_	
MSR <cond> CPSR f, #</cond>	_	
MSR <cond> SPSR_<fields>, Rm</fields></cond>	_	
MSR <cond> SPSR f, #</cond>	_ 9	
MUL <cond><s> Rd, Rm, Rs</s></cond>	-	s s s
MVN <cond><s> Rd, <sh_op></sh_op></s></cond>	-	s s s
ORR <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	-	s s s
RSB <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	9	s
RSC <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	=	s
SBC <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	-	s s s s
SMLAL <cond><s> RdLo, RdHi, Rm, Rs</s></cond>	64	s s s s
SMULL <cond><s> RdLo, RdHi, Rm, Rs</s></cond>	64	s s s s
STC <cond> p<cp_num>, CRd, #</cp_num></cond>	=	
STM <cond><adm> Rm, {reg list}^</adm></cond>		
STM <cond><adm> Rm<!-- -->, {reg list}</adm></cond>	"!" K R V	
STM <cond><adm> Rm<!-- -->, {reg list}^</adm></cond>	-	
STR <cond> Rd, Rn, #</cond>	ĺ	
STR <cond>B Rd, Rn, #</cond>	ĺ	
STR <cond>BT Rd, Rn, #</cond>	ĺ	
STR <cond>H Rd, <address></address></cond>	ĺ	
STR <cond>T Rd, Rn, #</cond>		
SUB <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	· -	s s s s
SWI <swi_number></swi_number>	-	
SWP <cond> Rd, Rm, [Rn]</cond>	-	
SWP <cond>B Rd, Rm, [Rn]</cond>	=	
TEQ <cond> Rn, <sh_op></sh_op></cond>	-	XXX
TST <cond> Rn, <sh op=""></sh></cond>	° - 64	x x x
UMLAL <cond><s> RdLo, RdHi, Rm, Rs</s></cond>	64 64	
UMULL <cond><s> RdLo, RdHi, Rm, Rs</s></cond>	U4	S S S S

Data Processing Opcode
Load/Store Opcode
Branching Opcode
Multiplication Opcode
Other Opcodes
CoProcessor Opcodes

Flag Settings
s - if flag set
x - always
* - special

Opcode	Operation
C <cond><s> Rd, Rn, <sh op=""></sh></s></cond>	R = R + < > + C
)D <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	R = R + < >
D <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	R = R & < >
cond> <target_addr></target_addr>	PC = PC + < >
C <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	R = R &!< >
<pre><cond> <target_addr></target_addr></cond></pre>	LR = PC+4; PC = PC + < >
<pre><cond> Rm</cond></pre>	PC = R ; M =THUMB
P <cond> p<cp#>,o1,CRd,CRn,CRm,o2</cp#></cond>	
N <cond> Rn, <sh_op></sh_op></cond>	< >=R +< >
P <cond> Rn, <sh_op></sh_op></cond>	< >=R -< >
R <cond><s> Rd, Rn, <sh_op></sh_op></s></cond>	R = R < >
C <cond> p<cp_num>, CRd, #</cp_num></cond>	#
M <cond><adm> Rm, {reg list}^</adm></cond>	special, see doc
M <cond><adm> Rm<!-- -->, {reg list}</adm></cond>	< >= R +=4
M <cond><adm> Rm<!-- -->, {reg list}^</adm></cond>	special, see doc
R <cond>B Rd, Rn, #</cond>	R = R +#
R <cond>BT Rd, Rn, #</cond>	R = R +#
R <cond>H Rd, <address></address></cond>	R = 9
R <cond>SB Rd, <address></address></cond>	R =
R <cond>SH Rd, <address></address></cond>	R = 9
R <cond>T Rd, Rn, #</cond>	R = R +#
R <cond> p<cp#>,o1,Rd,CRn,CRm,o2</cp#></cond>	- ARM
A <cond><s> Rd, Rm, Rs, Rn</s></cond>	R = R * R + R
V <cond><s> Rd, <sh_op></sh_op></s></cond>	R = < > ΔRM -
"Ceconds neco#s.ol.Rd.CRn.CRm.o2	APM -
S <cond> Rd, SPSR</cond>	R = SPSR
R <cond> CPSR <fields>, Rm</fields></cond>	CPSR = R ()
R <cond> CPSR < IlleIds>, Rm</cond>	CPSR = # ()
R <cond> CPSR_I, # R<cond> SPSR <fields>, Rm</fields></cond></cond>	,
R <cond> SPSR < IlleIds>, Rm</cond>	SPSR = R () SPSR = # ()
L <cond>SPSR_I, #</cond>	R = R * R
'N <cond><s> Rd, km, ks 'N<cond><s> Rd, <sh op=""></sh></s></cond></s></cond>	R = -< >
R <cond><s> Rd, <sn_op></sn_op></s></cond>	R = R < >
B <cond><s> Rd, Rn, <sh op=""></sh></s></cond>	R = < >-R
C <cond><s> Rd, Rn, <sh op=""></sh></s></cond>	R = < >-R + C
C <cond><s> Rd, Rn, <sh op=""></sh></s></cond>	R = R - < > + C
LAL <cond><s> RdLo, RdHi, Rm, Rs</s></cond>	R HR L = R *R +(R HR L)
	R HR L = R *R
ULL <cond><s> RdLo. RdH1. Rm. Re</s></cond>	P
ULL <cond><s> RdLo, RdHi, Rm, Rs</s></cond>	S P #
'C <cond> p<cp_num>, CRd, #</cp_num></cond>	S R # special see doc
C <cond> p<cp_num>, CRd, # M<cond><adm> Rm, {reg list}^</adm></cond></cp_num></cond>	special, see doc
<pre>'C<cond> p<cp num="">, CRd, # 'M<cond><adm> Rm, {reg list}^ 'M<cond><adm> Rm<!---->, {reg list}</adm></cond></adm></cond></cp></cond></pre>	special, see doc R +=4 =
<pre>'C<cond> p<cp num="">, CRd, # 'M<cond><adm> Rm, {reg list}^ 'M<cond><adm> Rm<!---->, {reg list} 'M<cond><adm> Rm<!---->, {reg list} 'M<cond><adm> Rm<!---->, {reg list}^</adm></cond></adm></cond></adm></cond></adm></cond></cp></cond></pre>	special, see doc R +=4 =
'C <cond> p<cp_num>, CRd, # 'M<cond><adm> Rm, {reg list}^ 'M<cond><adm> Rm<!-- -->, {reg list} 'M<cond><adm> Rm<!-- -->, {reg list}^ 'R<cond><adm> Rm<!-- -->, {reg list}^ 'R<cond> Rd, Rn, #</cond></adm></cond></adm></cond></adm></cond></adm></cond></cp_num></cond>	special, see doc R +=4 =
C <cond> p<cp num="">, CRd, # Mccond><adm> Rm, {reg list} Mccond><adm> Rm<1>, {reg list} Mccond><adm> Rm<1>, {reg list} Mccond><adm> Rm<1>, {reg list} Mccond> Rd, Rn, # R<cond> Rd, Rn, #</cond></adm></adm></adm></adm></cp></cond>	special, see doc R +=4 =
Cccond> p <cp num="">, CRd, # Mccond><adm> Rm, {reg list}^ Mccond><adm> Rmcl>, {reg list} Mccond><adm> Rmcl>, {reg list} Mccond><adm> Rmcl>, {reg list}^ Rccond> Rd, Rn, # Rccond>B Rd, Rn, # Rccond>B Rd, Rn, #</adm></adm></adm></adm></cp>	special, see doc R +=4 =
<pre>ccond> p<cp num="">, CRd, # /<cond><adm> Rm, {reg list}^ /<cond><adm> Emcl>, {reg list} /<cond><adm> Emcl>, {reg list} /<cond> Rd, Rn, # /<cond> Rd, Rn, #</cond></cond></adm></cond></adm></cond></adm></cond></cp></pre>	special, see doc R +=4 =