MF1049-01a

EPSON

CMOS 4-BIT SINGLE CHIP MICROCOMPUTER

E0C6S46 TECHNICAL MANUAL

E0C6S46 Technical Hardware

ENERGY SAVING EPSON

SEIKO EPSON CORPORATION

CONTENTS

CHAPTER 1 OUTLINE

The E0C6S46 is a microcomputer with a C-MOS 4-bit core CPU E0C6200 as main component, and ROM, RAM, dot matrix LCD driver, time base counter, clock synchronous serial interface, etc. built-in. Since the E0C6S46 can be driven with low voltage, it is suitable for portable equipment requiring dot matrix display functions.

The E0C6S46 is a smakker version of the E0C624A and except for external memory access function, it has the same functions as the E0C624A. Thus it can be used for applications of the E0C624A that do dot need external memory. Note the following structure and characteristics differences between the E0C6S46 and the E0C624A.

Pad size and layout: Size 100 μm Pitch 130 μm (Min.)

Electrical characteristics: External resistor value for CR oscillation (built-in capacitor is modified)
CR and ceramic oscillation start times
Low-level output current from output ports
Refer to Chapter 14, "Electrical Characteristics".

1.1 Features

Oscillation circuit	OSC1: 32.768 kHz (Typ.)	Crystal oscillation circuit		
	OSC3: 2 MHz (Max.)	CR or ceramic oscillation circuit (∗1)		
Instruction set	108 types			
Instruction execution time	32.768 kHz:	152.6 μsec	213.6 μsec	366.2 μsec
(differ depending on the instruction)	1 MHz:	5.0 μsec	7.0 μsec	12.0 μsec
	2 MHz:	2.5 μsec	3.5 μsec	6.0 μsec
ROM capacity	6,144 words × 12 bits			
RAM capacity	Data memory:	640 words × 4 bits		
	Display memory:	160 words × 4 bits		
Input port	8 bits (Pull-up resistors may be supplemented ∗1)			
Output port	20 bits (Buzzer and clock outputs are possible ∗1)			
I/O port	16 bits			
Serial interface	8-bit clock synchronous system × 1 ch.			
Dot matrix type LCD driver	40 segments × 16 or 8 commons (∗2)			
Time base counter	Clock timer, stopwatch timer			
Programmable timer	8-bit timer × 1 ch., with event counter and clock output functions			
Watchdog timer	Built-in			
Sound generator	8 programmable sounds (8 types of frequency) with envelope and 1-shot output functions			
Supply voltage detection (SVD)	-2.2, -2.5, -3.1, -4.2 V programmable (V_{DD} standard)			
External interrupt	Input port interrupt:	2 systems		
Internal interrupt	Clock timer interrupt:	1 system		
	Stopwatch timer interrupt:	1 system		
	Programmable timer interrupt:	1 system		
	Serial interface interrupt:	1 system		
Power supply voltage	2.2 V to 5.5 V (Min. 1.8 V when the OSC3 oscillation circuit is not used)			
Operating temperature range	-20°C to 70°C			
Current consumption (Typ.)	During HALT:	32.768 kHz (crystal oscillation), 3.0 V		2.5 μA
	During operation:	32.768 kHz (crystal oscillation), 3.0 V		6.5 μA
		2 MHz (CR oscillation), 3.0 V		1 mA
Package	QFP5-128pin (plastic) or chip			

∗1: Can be selected with mask option ∗2: Can be selected with software

1.2 Block Diagram

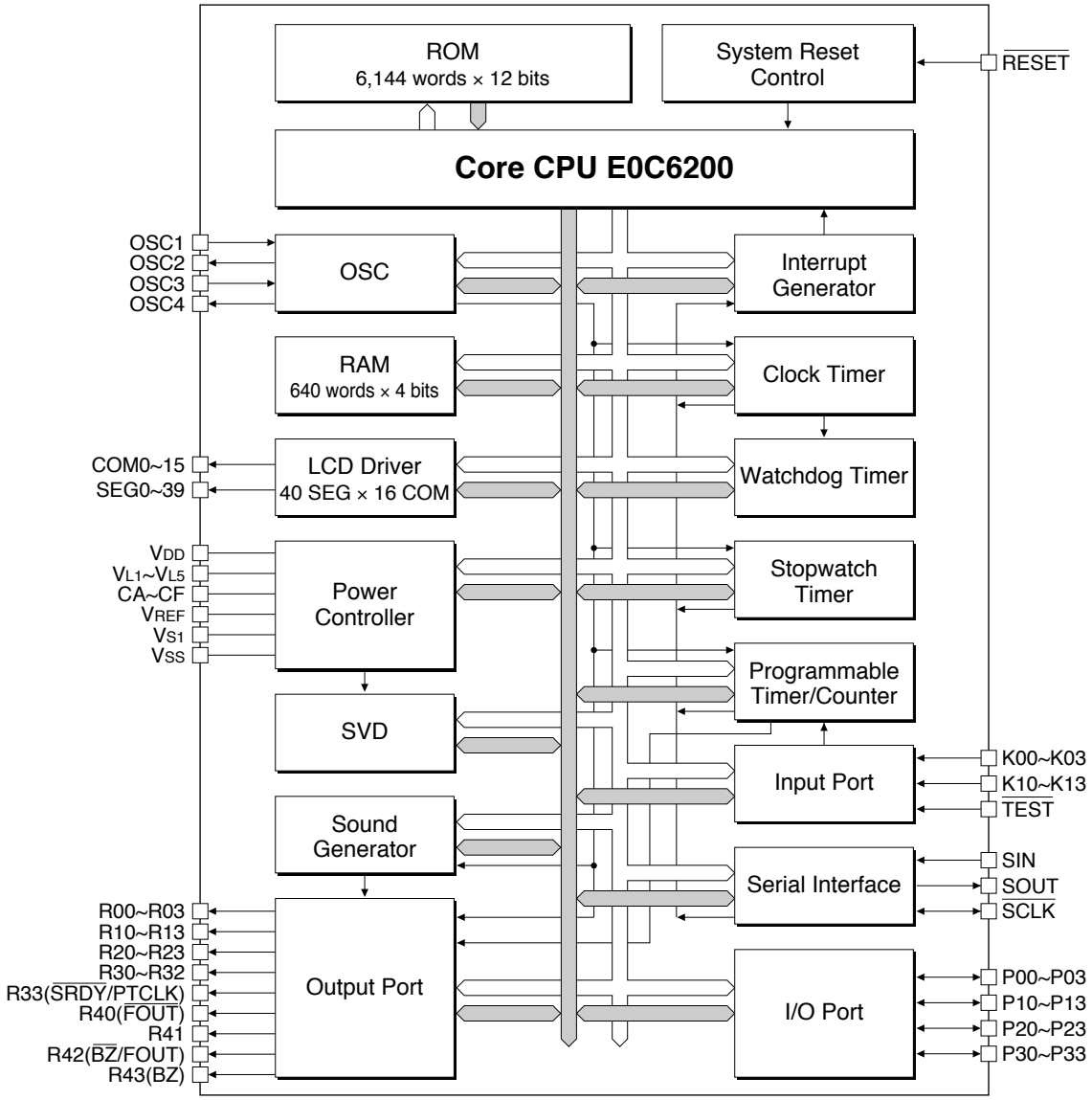
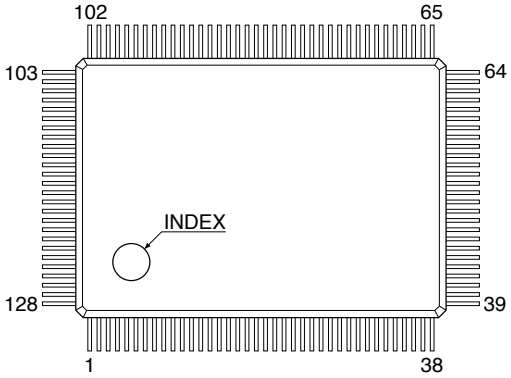


Fig. 1.2.1 Block diagram

1.3 Pin Layout Diagram

QFP5-128pin



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	V_{L3}	33	SEG33	65	SEG2	97	R42
2	V_{L4}	34	N.C.	66	SEG1	98	N.C.
3	V_{L5}	35	SEG32	67	SEG0	99	R41
4	CF	36	SEG31	68	$\overline{SCLK}$	100	R40
5	N.C.	37	SEG30	69	N.C.	101	R33
6	CE	38	SEG29	70	SOUT	102	R32
7	CD	39	SEG28	71	SIN	103	R31
8	CC	40	SEG27	72	K13	104	R30
9	CB	41	SEG26	73	K12	105	R23
10	CA	42	SEG25	74	K11	106	R22
11	COM0	43	SEG24	75	K10	107	R21
12	COM1	44	SEG23	76	K03	108	R20
13	COM2	45	SEG22	77	K02	109	R13
14	COM3	46	SEG21	78	K01	110	R12
15	COM4	47	SEG20	79	K00	111	R11
16	COM5	48	SEG19	80	P33	112	R10
17	COM6	49	SEG18	81	P32	113	R03
18	COM7	50	SEG17	82	P31	114	R02
19	COM8	51	SEG16	83	P30	115	R01
20	COM9	52	SEG15	84	P23	116	R00
21	COM10	53	SEG14	85	P22	117	V_{SS}
22	COM11	54	SEG13	86	P21	118	$\overline{RESET}$
23	COM12	55	SEG12	87	P20	119	$\overline{TEST}$
24	COM13	56	SEG11	88	P13	120	OSC4
25	COM14	57	SEG10	89	P12	121	OSC3
26	COM15	58	SEG9	90	P11	122	V_{S1}
27	SEG39	59	SEG8	91	P10	123	OSC2
28	SEG38	60	SEG7	92	P03	124	OSC1
29	SEG37	61	SEG6	93	P02	125	V_{DD}
30	SEG36	62	SEG5	94	P01	126	V_{REF}
31	SEG35	63	SEG4	95	P00	127	V_{L1}
32	SEG34	64	SEG3	96	R43	128	V_{L2}

N.C.: No Connection

Fig. 1.3.1 Pin layout diagram

1.4 Pin Description

Table 1.4.1 Pin description

Pin name	Pin No.	I/O	Function	
V_{DD}	125	–	Power supply (+)	
V_{SS}	117	–	Power supply (-)	
V_{S1}	122	–	Internal logic system/oscillation system regulated voltage output	
V_{L1}–V_{L5}	127, 128, 1–3	–	LCD system power supply 1/4 bias generated internally, 1/5 bias generated externally *1	
V_{REF}	126	O	LCD system power test pin *2	
CA–CF	10–6, 4	–	LCD system voltage booster condenser connecting pin	
OSC1	124	I	Crystal or CR oscillator input *1	
OSC2	123	O	Crystal or CR oscillator output *1, CD buiil-in	
OSC3	121	I	CR or ceramic oscillator input *1	
OSC4	120	O	CR or ceramic oscillator output *1	
COM0–COM15	11–26	O	LCD common output (1/8 duty or 1/16 duty is selected on software)	
SEG0–SEG39	67–35, 33–27	O	LCD segment output	
K00–K03	79–76	I	Input port (pull up resistor is available by mask option) *1	
K10–K13	75–72	I	Input port (pull up resistor is available by mask option) *1	
P00–P03	95–92	I/O	I/O port	Complementary output or
P10–P13	91–88	I/O	I/O port	Nch open drain output *1
P20–P23	87–84	I/O	I/O port	
P30–P33	83–80	I/O	I/O port or output port *1	
R00–R03	116–113	O	Output port	
R10–R13	112–109	O	Output port	
R20–R23	108–105	O	Output port	
R30–R32	104–102	O	Output port	
R33	101	O	Output port, $\overline{SRDY}$ output or PTCLK output *1	
R40	100	O	Output port or $\overline{FOUT}$ output *1	
R41	99	O	Output port	
R42	97	O	Output port, $\overline{BZ}$ output or FOUT output *1	
R43	96	O	Output port or BZ output *1	
SIN	71	I	Serial interface data input	
SOUT	70	O	Serial interface data output	
$\overline{SCLK}$	68	I/O	Serial interface clock input/output	
$\overline{RESET}$	118	I	Initial reset input terminal	
$\overline{TEST}$	119	I	Testing input terminal *3	

*1 Selected by mask option

*2 Leave the V_{REF} pin unconnected (N.C.).

*3 The $\overline{TEST}$ pin is used when the IC load is being detected. During ordinary operation be certain to connect this pin to V_{DD}.

CHAPTER 2 CPU AND BUILT-IN MEMORY

2.1 CPU and Instruction Set

The E0C6S46 uses the 4-bit core CPU E0C6200 for its CPU. It has almost the same register configurations, instructions, and other features as the other family devices which use the E0C6200/6200A/6200B, allowing full use of software assets. The instruction set of the E0C6S46 has 108 types of instructions, all consisting of one word (12 bits).

For detailed information on the CPU and the instruction set, refer to the "E0C6200/6200A Core CPU Manual".
Note, however, that because E0C6S46 does not assume SLEEP operation, the SLP instruction is not available in the E0C6200 instruction set.

The instruction list is shown in Tables 2.1.1(a)–(c).
The following lists the symbols used in the instruction list:

Symbols associated with registers and memory

A	A register
B	B register
X	XHL register (low order eight bits of index register IX)
Y	YHL register (low order eight bits of index register IY)
XH	XH register (high order four bits of XHL register)
XL	XL register (low order four bits of XHL register)
YH	YH register (high order four bits of YHL register)
YL	YL register (low order four bits of YHL register)
XP	XP register (high order four bits of index register IX)
YP	YP register (high order four bits of index register IY)
SP	Stack pointer SP
SPH	High-order four bits of stack pointer SP
SPL	Low-order four bits of stack pointer SP
MX, M(X)	Data memory whose address is specified with index register IX
MY, M(Y)	Data memory whose address is specified with index register IY
Mn, M(n)	Data memory address 000H–00FH (address specified with immediate data n of 00H–0FH)
M(SP)	Data memory whose address is specified with stack pointer SP
r, q	Two-bit register code r, q is two-bit immediate data; according to the contents of these bits, they indicate registers A, B, and MX and MY (data memory whose addresses are specified with index registers IX and IY)

r		q		Register
r1	r0	q1	q0	specified
0	0	0	0	A
0	1	0	1	B
1	0	1	0	MX
1	1	1	1	MY

Symbols associated with program counter

NBP	New bank pointer
NPP	New page pointer
PCB	Program counter bank
PCP	Program counter page
PCS	Program counter step
PCSH	Four high order bits of PCS
PCSL	Four low order bits of PCS

Symbols associated with flags

F	Flag register (I, D, Z, C)
C	Carry flag
Z	Zero flag
D	Decimal flag
I	Interrupt flag
↓	Flag reset
↑	Flag set
↕	Flag set or reset

Associated with immediate data

p	Five-bit immediate data or label 00H–1FH
s	Eight-bit immediate data or label 00H–0FFH
I	Eight-bit immediate data 00H–0FFH
i	Four-bit immediate data 00H–0FH

Associated with arithmetic and other operations

+	Add
-	Subtract
∧	Logical AND
∨	Logical OR
∀	Exclusive-OR
★	Add-subtract instruction for decimal operation when the D flag is set

Table 2.1.1(a) Instruction sets (1)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Branch instructions	PSET	p	1	1	1	0	0	1	0	p4	p3	p2	p1	p0					5	NBP ← p4, NPP ← p3~p0
	JP	s	0	0	0	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0
		C, s	0	0	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=1
		NC, s	0	0	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if C=0
		Z, s	0	1	1	0	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=1
		NZ, s	0	1	1	1	s7	s6	s5	s4	s3	s2	s1	s0					5	PCB ← NBP, PCP ← NPP, PCS ← s7~s0 if Z=0
	JPBA		1	1	1	1	1	1	1	0	1	0	0	0					5	PCB ← NBP, PCP ← NPP, PCSH ← B, PCSL ← A
	CALL	s	0	1	0	0	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← NPP, PCS ← s7~s0
	CALZ	s	0	1	0	1	s7	s6	s5	s4	s3	s2	s1	s0					7	M(SP-1) ← PCP, M(SP-2) ← PCSH, M(SP-3) ← PCSL+1 SP ← SP-3, PCP ← 0, PCS ← s7~s0
	RET		1	1	1	1	1	1	0	1	1	1	1	1					7	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3
	RETS		1	1	1	1	1	1	0	1	1	1	1	0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, PC ← PC+1
	RETD	*l*	0	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					12	PCSL ← M(SP), PCSH ← M(SP+1), PCP ← M(SP+2) SP ← SP+3, M(X) ← *l*3~*l*0, M(X+1) ← *l*7~*l*4, X ← X+2
System control instructions	NOP5		1	1	1	1	1	1	1	1	1	0	1	1					5	No operation (5 clock cycles)
	NOP7		1	1	1	1	1	1	1	1	1	1	1	1					7	No operation (7 clock cycles)
	HALT		1	1	1	1	1	1	1	1	1	0	0	0					5	Halt (stop clock)
Index operation instructions	INC	X	1	1	1	0	1	1	1	0	0	0	0	0					5	X ← X+1
		Y	1	1	1	0	1	1	1	1	0	0	0	0					5	Y ← Y+1
	LD	X, x	1	0	1	1	x7	x6	x5	x4	x3	x2	x1	x0					5	XH ← x7~x4, XL ← x3~x0
		Y, y	1	0	0	0	y7	y6	y5	y4	y3	y2	y1	y0					5	YH ← y7~y4, YL ← y3~y0
		XP, r	1	1	1	0	1	0	0	0	0	0	r1	r0					5	XP ← r
		XH, r	1	1	1	0	1	0	0	0	0	1	r1	r0					5	XH ← r
		XL, r	1	1	1	0	1	0	0	0	1	0	r1	r0					5	XL ← r
		YP, r	1	1	1	0	1	0	0	1	0	0	r1	r0					5	YP ← r
		YH, r	1	1	1	0	1	0	0	1	0	1	r1	r0					5	YH ← r
		YL, r	1	1	1	0	1	0	0	1	1	0	r1	r0					5	YL ← r
		r, XP	1	1	1	0	1	0	1	0	0	0	r1	r0					5	r ← XP
		r, XH	1	1	1	0	1	0	1	0	0	1	r1	r0					5	r ← XH
		r, XL	1	1	1	0	1	0	1	0	1	0	r1	r0					5	r ← XL
		r, YP	1	1	1	0	1	0	1	1	0	0	r1	r0					5	r ← YP
		r, YH	1	1	1	0	1	0	1	1	0	1	r1	r0					5	r ← YH
		r, YL	1	1	1	0	1	0	1	1	1	0	r1	r0					5	r ← YL
	ADC	XH, i	1	0	1	0	0	0	0	0	i3	i2	i1	i0			↕	↕	7	XH ← XH+i3~i0+C
		XL, i	1	0	1	0	0	0	0	1	i3	i2	i1	i0			↕	↕	7	XL ← XL+i3~i0+C
		YH, i	1	0	1	0	0	0	1	0	i3	i2	i1	i0			↕	↕	7	YH ← YH+i3~i0+C
		YL, i	1	0	1	0	0	0	1	1	i3	i2	i1	i0			↕	↕	7	YL ← YL+i3~i0+C

Table 2.1.1(b) Instruction sets (2)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Index operation instructions	CP	XH, i	1	0	1	0	0	1	0	0	i3	i2	i1	i0			↕	↕	7	XH-i3~i0
		XL, i	1	0	1	0	0	1	0	1	i3	i2	i1	i0			↕	↕	7	XL-i3~i0
		YH, i	1	0	1	0	0	1	1	0	i3	i2	i1	i0			↕	↕	7	YH-i3~i0
		YL, i	1	0	1	0	0	1	1	1	i3	i2	i1	i0			↕	↕	7	YL-i3~i0
Data transfer instructions	LD	r, i	1	1	1	0	0	0	r1	r0	i3	i2	i1	i0					5	r ← i3~i0
		r, q	1	1	1	0	1	1	0	0	r1	r0	q1	q0					5	r ← q
		A, Mn	1	1	1	1	1	0	1	0	n3	n2	n1	n0					5	A ← M(n3~n0)
		B, Mn	1	1	1	1	1	0	1	1	n3	n2	n1	n0					5	B ← M(n3~n0)
		Mn, A	1	1	1	1	1	0	0	0	n3	n2	n1	n0					5	M(n3~n0) ← A
		Mn, B	1	1	1	1	1	0	0	1	n3	n2	n1	n0					5	M(n3~n0) ← B
	LDPX	MX, i	1	1	1	0	0	1	1	0	i3	i2	i1	i0					5	M(X) ← i3~i0, X ← X+1
		r, q	1	1	1	0	1	1	1	0	r1	r0	q1	q0					5	r ← q, X ← X+1
	LDPY	MY, i	1	1	1	0	0	1	1	1	i3	i2	i1	i0					5	M(Y) ← i3~i0, Y ← Y+1
		r, q	1	1	1	0	1	1	1	1	r1	r0	q1	q0					5	r ← q, Y ← Y+1
	LBPX	MX, *l*	1	0	0	1	*l*7	*l*6	*l*5	*l*4	*l*3	*l*2	*l*1	*l*0					5	M(X) ← *l*3~*l*0, M(X+1) ← *l*7~*l*4, X ← X+2
Flag operation instructions	SET	F, i	1	1	1	1	0	1	0	0	i3	i2	i1	i0	↑	↑	↑	↑	7	F ← F∨i3~i0
	RST	F, i	1	1	1	1	0	1	0	1	i3	i2	i1	i0	↓	↓	↓	↓	7	F ← F∧i3~i0
	SCF		1	1	1	1	0	1	0	0	0	0	0	1				↑	7	C ← 1
	RCF		1	1	1	1	0	1	0	1	1	1	1	0				↓	7	C ← 0
	SZF		1	1	1	1	0	1	0	0	0	0	1	0			↑		7	Z ← 1
	RZF		1	1	1	1	0	1	0	1	1	1	0	1			↓		7	Z ← 0
	SDF		1	1	1	1	0	1	0	0	0	1	0	0		↑			7	D ← 1 (Decimal Adjuster ON)
	RDF		1	1	1	1	0	1	0	1	1	0	1	1		↓			7	D ← 0 (Decimal Adjuster OFF)
	EI		1	1	1	1	0	1	0	0	1	0	0	0	↑				7	I ← 1 (Enables Interrupt)
	DI		1	1	1	1	0	1	0	1	0	1	1	1	↓				7	I ← 0 (Disables Interrupt)
Stack operation instructions	INC	SP	1	1	1	1	1	1	0	1	1	0	1	1					5	SP ← SP+1
	DEC	SP	1	1	1	1	1	1	0	0	1	0	1	1					5	SP ← SP-1
	PUSH	r	1	1	1	1	1	1	0	0	0	0	r1	r0					5	SP ← SP-1, M(SP) ← r
		XP	1	1	1	1	1	1	0	0	0	1	0	0					5	SP ← SP-1, M(SP) ← XP
		XH	1	1	1	1	1	1	0	0	0	1	0	1					5	SP ← SP-1, M(SP) ← XH
		XL	1	1	1	1	1	1	0	0	0	1	1	0					5	SP ← SP-1, M(SP) ← XL
		YP	1	1	1	1	1	1	0	0	0	1	1	1					5	SP ← SP-1, M(SP) ← YP
		YH	1	1	1	1	1	1	0	0	1	0	0	0					5	SP ← SP-1, M(SP) ← YH
		YL	1	1	1	1	1	1	0	0	1	0	0	1					5	SP ← SP-1, M(SP) ← YL
		F	1	1	1	1	1	1	0	0	1	0	1	0					5	SP ← SP-1, M(SP) ← F
	POP	r	1	1	1	1	1	1	0	1	0	0	r1	r0					5	r ← M(SP), SP ← SP+1
		XP	1	1	1	1	1	1	0	1	0	1	0	0					5	XP ← M(SP), SP ← SP+1
		XH	1	1	1	1	1	1	0	1	0	1	0	1					5	XH ← M(SP), SP ← SP+1
		XL	1	1	1	1	1	1	0	1	0	1	1	0					5	XL ← M(SP), SP ← SP+1
		YP	1	1	1	1	1	1	0	1	0	1	1	1					5	YP ← M(SP), SP ← SP+1

Table 2.1.1(c) Instruction sets (3)

Classification	Mnemonic	Operand	Operation Code												Flag				Clock	Operation
			B	A	9	8	7	6	5	4	3	2	1	0	I	D	Z	C		
Stack operation instructions	POP	YH	1	1	1	1	1	1	0	1	1	0	0	0					5	YH← M(SP), SP ← SP+1
		YL	1	1	1	1	1	1	0	1	1	0	0	1					5	YL ← M(SP), SP ← SP+1
		F	1	1	1	1	1	1	0	1	1	0	1	0	↕	↕	↕	↕	5	F ← M(SP), SP ← SP+1
	LD	SPH, r	1	1	1	1	1	1	1	0	0	0	r1	r0					5	SPH ← r
		SPL, r	1	1	1	1	1	1	1	1	0	0	r1	r0					5	SPL ← r
		r, SPH	1	1	1	1	1	1	1	0	0	1	r1	r0					5	r ← SPH
		r, SPL	1	1	1	1	1	1	1	1	0	1	r1	r0					5	r ← SPL
Arithmetic instructions	ADD	r, i	1	1	0	0	0	0	r1	r0	i3	i2	i1	i0	★		↕	↕	7	r ← r+i3~i0
		r, q	1	0	1	0	1	0	0	0	r1	r0	q1	q0	★		↕	↕	7	r ← r+q
	ADC	r, i	1	1	0	0	0	1	r1	r0	i3	i2	i1	i0	★		↕	↕	7	r ← r+i3~i0+C
		r, q	1	0	1	0	1	0	0	1	r1	r0	q1	q0	★		↕	↕	7	r ← r+q+C
	SUB	r, q	1	0	1	0	1	0	1	0	r1	r0	q1	q0	★		↕	↕	7	r ← r-q
	SBC	r, i	1	1	0	1	0	1	r1	r0	i3	i2	i1	i0	★		↕	↕	7	r ← r-i3~i0-C
		r, q	1	0	1	0	1	0	1	1	r1	r0	q1	q0	★		↕	↕	7	r ← r-q-C
	AND	r, i	1	1	0	0	1	0	r1	r0	i3	i2	i1	i0			↕		7	r ← r∧i3~i0
		r, q	1	0	1	0	1	1	0	0	r1	r0	q1	q0			↕		7	r ← r∧q
	OR	r, i	1	1	0	0	1	1	r1	r0	i3	i2	i1	i0			↕		7	r ← r∨i3~i0
		r, q	1	0	1	0	1	1	0	1	r1	r0	q1	q0			↕		7	r ← r∨q
	XOR	r, i	1	1	0	1	0	0	r1	r0	i3	i2	i1	i0			↕		7	r ← r∀i3~i0
		r, q	1	0	1	0	1	1	1	0	r1	r0	q1	q0			↕		7	r ← r∀q
	CP	r, i	1	1	0	1	1	1	r1	r0	i3	i2	i1	i0			↕	↕	7	r-i3~i0
		r, q	1	1	1	1	0	0	0	0	r1	r0	q1	q0			↕	↕	7	r-q
	FAN	r, i	1	1	0	1	1	0	r1	r0	i3	i2	i1	i0			↕		7	r∧i3~i0
		r, q	1	1	1	1	0	0	0	1	r1	r0	q1	q0			↕		7	r∧q
	RLC	r	1	0	1	0	1	1	1	1	r1	r0	r1	r0			↕	↕	7	d3 ← d2, d2 ← d1, d1 ← d0, d0 ← C, C ← d3
	RRC	r	1	1	1	0	1	0	0	0	1	1	r1	r0			↕	↕	5	d3 ← C, d2 ← d3, d1 ← d2, d0 ← d1, C ← d0
	INC	Mn	1	1	1	1	0	1	1	0	n3	n2	n1	n0			↕	↕	7	M(n3~n0) ← M(n3~n0)+1
	DEC	Mn	1	1	1	1	0	1	1	1	n3	n2	n1	n0			↕	↕	7	M(n3~n0) ← M(n3~n0)-1
	ACPX	MX, r	1	1	1	1	0	0	1	0	1	0	r1	r0	★		↕	↕	7	M(X) ← M(X)+r+C, X ← X+1
	ACPY	MY, r	1	1	1	1	0	0	1	0	1	1	r1	r0	★		↕	↕	7	M(Y) ← M(Y)+r+C, Y ← Y+1
	SCPX	MX, r	1	1	1	1	0	0	1	1	1	0	r1	r0	★		↕	↕	7	M(X) ← M(X)-r-C, X ← X+1
	SCPY	MY, r	1	1	1	1	0	0	1	1	1	1	r1	r0	★		↕	↕	7	M(Y) ← M(Y)-r-C, Y ← Y+1
	NOT	r	1	1	0	1	0	0	r1	r0	1	1	1	1			↕		7	r ← $\overline{r}$

2.2 Program Memory (ROM)

The built-in ROM, a mask ROM for loading the program, has a capacity of 6,144 steps × 12 bits. The program area is two banks, each of 16 (0–15) pages × 256 (00H–FFH) steps. After initial reset, the program beginning address is set to bank 0, page 1, step 00H. The interrupt vector is allocated to page 1 of each bank, steps 02H–0CH.

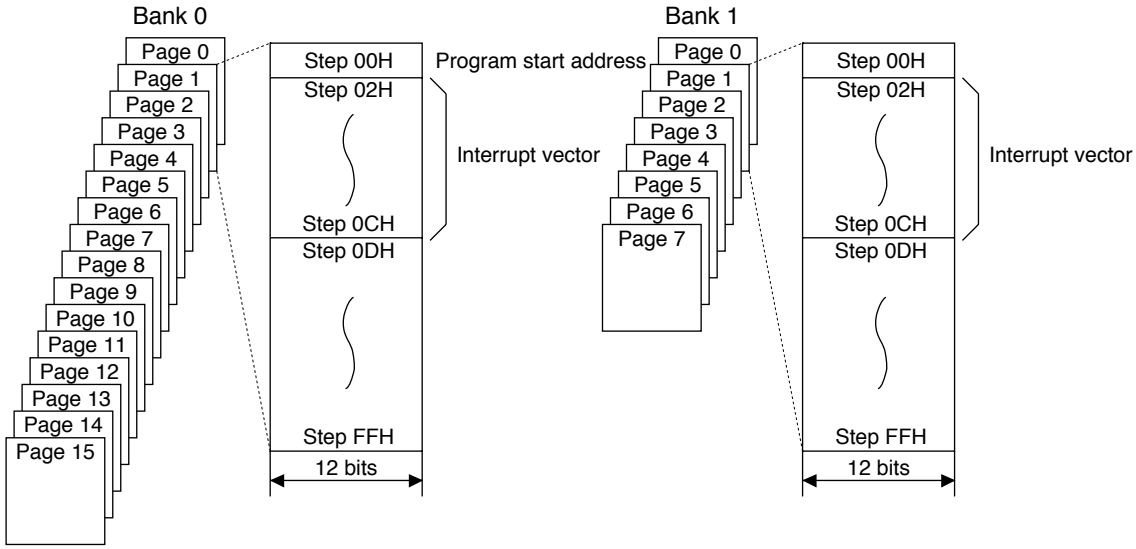


Fig. 2.2.1 Configuration of the built-in ROM

2.3 Data Memory (RAM)

The E0C6S46 built-in data memories are configured a general-purpose RAM, display data memory of the LCD, and I/O data memory which controls the peripheral circuit.

General-purpose RAM: 640 words × 4 bits (000H–27FH)
Display data memory: 160 words × 4 bits (E00H–E4FH, E80H–ECFH)
I/O memory: 48 words × 4 bits (F00H–F7EH)

During programming, take note of the following:

(1) Since the stack area is taken from the RAM area, take care that destruction of stack data due to data writing does not occur. Sub-routine calls or interrupts consume 3 words of the stack area.

(2) RAM address 000H–00FH are memory register areas that are addressed with register pointer RP.

The memory map of the built-in data memory (RAM) and details of the I/O data memory map are shown in Figure 2.3.1 and Tables 2.3.1(a)–(d), respectively.

Note: Memory is not mounted in unused area within the memory map and in memory area not indicated in this chapter. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9	MA	MB	MC	MD	ME	MF
	1	RAM (256 words x 4 bits) R/W															
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																
1	0	RAM (256 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																
	8																
	9																
	A																
	B																
	C																
	D																
	E																
	F																
2	0	RAM (128 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5																
	6																
	7																

Address Page	Low / High	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
E	0	Display data memory (80 words x 4 bits) R/W															
	1																
	2																
	3																
	4																
	5	Unused area															
	6																
	7																
	8	Display data memory (80 words x 4 bits) R/W															
	9																
	A																
	B																
	C																
	D	Unused area															
	E																
	F																
F	0	I/O memory															
	1																
	2																
	3	Unused area															
	4																
	5																
	6																
	7																
	8	Unused area															
	9																
	A																
	B																
	C																
	D																
	E																
	F																

Fig. 2.3.1 Memory map

Table 2.3.1(a) I/O data memory map (1)

Address	Register								Comment
	D3	D2	D1	D0	Name	Init *1	1	0	
F00H	IT1	IT2	IT8	IT32	IT1 *3	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2 *3	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8 *3	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32*3	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
F01H	0	0	ISW1	ISW0	0 *4	– *2			
					0 *4	– *2			
	R				ISW1*3	0	Yes	No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0*3	0	Yes	No	Interrupt factor flag (stopwatch 10 Hz)
F02H	0	0	0	IPT	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IPT *3	0	Yes	No	Interrupt factor flag (programmable timer)
F03H	0	0	0	ISIO	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					ISIO*3	0	Yes	No	Interrupt factor flag (serial interface)
F04H	0	0	0	IK0	0 *4	– *2			
					0 *4	– *2			
	R				0 *4	– *2			
					IK0 *3	0	Yes	No	Interrupt factor flag (K00–K03)
F05H	0	0	0	IK1	0 *3	– *2			
					0 *3	– *2			
	R				0 *3	– *2			
					IK1 *4	0	Yes	No	Interrupt factor flag (K10–K13)
F10H	EIT1	EIT2	EIT8	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
F11H	0	0	EISW1	EISW0	0 *3	– *2			
					0 *3	– *2			
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
F12H	0	0	0	EIPT	0 *3	– *2			
					0 *3	– *2			
	R			R/W	0 *3	– *2			
					EIPT	0	Enable	Mask	Interrupt mask register (programmble timer)
F13H	0	0	0	EISIO	0 *3	– *2			
					0 *3	– *2			
	R			R/W	0 *3	– *2			
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
F14H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
F15H	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (K13)
					EIK12	0	Enable	Mask	Interrupt mask register (K12)
	R/W				EIK11	0	Enable	Mask	Interrupt mask register (K11)
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
F20H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
F21H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)

∗1 Initial value following initial reset

∗2 Not set in the circuit

∗3 Reset (0) immediately after being read

∗4 Always "0" when being read

Table 2.3.1(b) I/O data memory map (2)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F22H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB Stopwatch timer 1/100 sec data (BCD) LSB
					SWL2	0			
					SWL1	0			
	R				SWL0	0			
F23H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB Stopwatch timer 1/10 sec data (BCD) LSB
					SWH2	0			
					SWH1	0			
	R				SWH0	0			
F24H	PT3	PT2	PT1	PT0	PT3	X *3			MSB Programmable timer data (low-order) LSB
					PT2	X *3			
					PT1	X *3			
	R				PT0	X *3			
F25H	PT7	PT6	PT5	PT4	PT7	X *3			MSB Programmable timer data (high-order) LSB
					PT6	X *3			
					PT5	X *3			
	R				PT4	X *3			
F26H	RD3	RD2	RD1	RD0	RD3	X *3			MSB Programmable timer reload data (low-order) LSB
					RD2	X *3			
					RD1	X *3			
	R/W				RD0	X *3			
F27H	RD7	RD6	RD5	RD4	RD7	X *3			MSB Programmable timer reload data (high-order) LSB
					RD6	X *3			
					RD5	X *3			
	R/W				RD4	X *3			
F30H	SD3	SD2	SD1	SD0	SD3	X *3			MSB Serial interface data register (low-order) LSB
					SD2	X *3			
					SD1	X *3			
	R/W				SD0	X *3			
F31H	SD7	SD6	SD5	SD4	SD7	X *3			MSB Serial interface data register (high-order) LSB
					SD6	X *3			
					SD5	X *3			
	R/W				SD4	X *3			
F40H	K03	K02	K01	K00	K03	– *2	High	Low	Input port (K00–K03)
					K02	– *2	High	Low	
					K01	– *2	High	Low	
	R				K00	– *2	High	Low	
F41H	DFK03	DFK02	DFK01	DFK00	DFK03	1	↓	↑	Input relation register (DFK00–DFK03)
					DFK02	1	↓	↑	
					DFK01	1	↓	↑	
	R/W				DFK00	1	↓	↑	
F42H	K13	K12	K11	K10	K13	– *2	High	Low	Input port (K10–K13)
					K12	– *2	High	Low	
					K11	– *2	High	Low	
	R				K10	– *2	High	Low	
F50H	R03	R02	R01	R00	R03	X *3	High	Low	Output port (R00–R03)
					R02	X *3	High	Low	
					R01	X *3	High	Low	
	R/W				R00	X *3	High	Low	
F51H	R13	R12	R11	R10	R13	X *3	High	Low	Output port (R10–R13)
					R12	X *3	High	Low	
					R11	X *3	High	Low	
	R/W				R10	X *3	High	Low	
F52H	R23	R22	R21	R20	R23	X *3	High	Low	Output port (R20–R23)
					R22	X *3	High	Low	
					R21	X *3	High	Low	
	R/W				R20	X *3	High	Low	

∗1 Initial value following initial reset

∗2 Not set in the circuit

∗3 Undefined

Table 2.3.1(c) I/O data memory map (3)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F53H	R33	R32	R31	R30	R33	X *2	High	Low	Output port (R33)
							Off	On	PTCLK output
	R/W						*3	*3	[$\overline{\text{SRDY}}$ (SIO READY)]
					R32	X *2	High	Low	Output port (R30–R32)
					R31	X *2	High	Low	
					R30	X *2	High	Low	
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT)
							*3	*3	[Buzzer inverted output ($\overline{\text{BZ}}$)]
					R41	1	High	Low	Output port (R41)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output ($\overline{\text{FOUT}}$)
F60H	P03	P02	P01	P00	P03	X *2	High	Low	I/O port (P00–P03)
					P02	X *2	High	Low	
	R/W				P01	X *2	High	Low	
					P00	X *2	High	Low	
F61H	P13	P12	P11	P10	P13	X *2	High	Low	I/O port (P10–P13)
					P12	X *2	High	Low	
	R/W				P11	X *2	High	Low	
					P10	X *2	High	Low	
F62H	P23	P22	P21	P20	P23	X *2	High	Low	I/O port (P20–P23)
					P22	X *2	High	Low	
	R/W				P21	X *2	High	Low	
					P20	X *2	High	Low	
F63H	P33	P32	P31	P30	P33	X *2	High	Low	I/O port / Dedicated output port (P33)
					P32	X *2	High	Low	I/O port / Dedicated output port (P32)
	R/W				P31	X *2	High	Low	I/O port / Dedicated output port (P31)
					P30	X *2	High	Low	I/O port / Dedicated output port (P30)
F70H	CLKCHG	OSCC	VSC1	VSC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VSC1	0			CPU operating voltage switch
					VSC0	0			
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
					ALON	0	All on	Normal	All LCD dots displayed control
	R/W				LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode
F72H	LC3	LC2	LC1	LC0	LC3	X *2			LCD contrast adjustment LC3–LC0 = 0 light : LC3–LC0 = 15 dark
					LC2	X *2			
	R/W				LC1	X *2			
					LC0	X *2			
F73H	SVDDT	SVDON	SVC1	SVC0	SVDDT	1 *4	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
	R	R/W			SVC1	X *2			SVD criteria voltage setting
					SVC0	X *2			
F74H	SHOTPW	BZFQ2	BZFQ1	BZFQ0	SHOTPW	0	62.5 ms	31.25 ms	1-shot buzzer pulse width
					BZFQ2	0			Buzzer frequency selection
	R/W				BZFQ1	0			
					BZFQ0	0			

∗1 Initial value following initial reset

∗2 Undefined

∗3 When selecting options enclosed in brackets [ ] as output option, the output register will function as register only and will not affect the individual outputs.

∗4 When SVD is off, "1" is read out.

Table 2.3.1(d) I/O data memory map (4)

Address	Register D3	D2	D1	D0	Name	Init *1	1	0	Comment
F75H	BZSHOT	ENVRST	ENVRT	ENVON	BZSHOT	0	Trigger	–	1-shot buzzer trigger (W)
							BUSY	READY	Status (R)
					ENVRST	Reset	Reset	–	Envelope reset
	W	W	R/W		ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection
	R				ENVON	0	On	Off	Envelope On/Off
F76H	0	0	TMRST	WDRST	0 *3	– *2			
					0 *3	– *2			
	R		W		TMRST *3	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset
F77H	0	0	SWRST	SWRUN	0 *3	– *2			
					0 *3	– *2			
	R		W	R/W	SWRST *3	Reset	Reset	–	Stopwatch timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop
F78H	0	0	PTRST	PTRUN	0 *3	– *2			
					0 *3	– *2			
	R		W	R/W	PTRST *3	Reset	Reset	–	Programmable timer reset
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
F79H	PTCOUT	PTC2	PTC1	PTC0	PTCOUT	0	On	Off	Programmable timer clock output
					PTC2	0			Programmable timer input clock selection
	R/W				PTC1	0			
					PTC0	0			
F7AH	SCTRG	SEN	SCS1	SCS0	SCTRG *3	–	Trigger	–	Serial interface clock trigger
					SEN	0	↰	↱	Serial interface clock edge selection
	W	R/W			SCS1	0			Serial interface clock mode selection
					SCS0	0			
F7BH	HZR3	HZR2	HZR1	HZR0	HZR3 *3	0	Output	High-Z	R30–R33 output high-impedance control
					HZR2	0	Output	High-Z	R20–R23 output high-impedance control
	R/W				HZR1	0	Output	High-Z	R10–R13 output high-impedance control
					HZR0	0	Output	High-Z	R00–R03 output high-impedance control
F7DH	IOC3	IOC2	IOC1	IOC0	IOC3	0	Output	Input	I/O control (P30–P33)
					IOC2	0	Output	Input	I/O control (P20–P23)
	R/W				IOC1	0	Output	Input	I/O control (P10–P13)
					IOC0	0	Output	Input	I/O control (P00–P03)
F7EH	PUP3	PUP2	PUP1	PUP0	PUP3	0	Off	On	I/O pull up resistor On/Off (P30–P33)
					PUP2	0	Off	On	I/O pull up resistor On/Off (P20–P23)
	R/W				PUP1	0	Off	On	I/O pull up resistor On/Off (P10–P13)
					PUP0	0	Off	On	I/O pull up resistor On/Off (P00–P03)

*1 Initial value following initial reset

*2 Not set in the circuit

*3 Always "0" when being read

CHAPTER 3 POWER SOURCE

3.1 Power Supply System

The E0C6S46 operating power voltage is as follows:

2.2–5.5 V (Min. 1.8 V, when OSC3 oscillation circuit is not used)

The E0C6S46 operates when a single power supply within the above range is applied between VDD and VSS. Even if the voltage is not within the above range necessary for the internal circuits, the IC itself can generate the following built-in power circuits.

Circuit	Power supply circuit	Output voltage
Oscillation circuit and internal circuits	Regulated voltage circuit	VS1
LCD driver	LCD system voltage circuit	VL1–VL5

Notes: • *VL3 is used only when the driving voltage of the LCD system will be supplied externally (1/5 bias); when using the internal LCD system voltage circuit (1/4 bias), it should be shorted with VL2.*

• *See "14 Electrical Characteristics" for voltage values.*

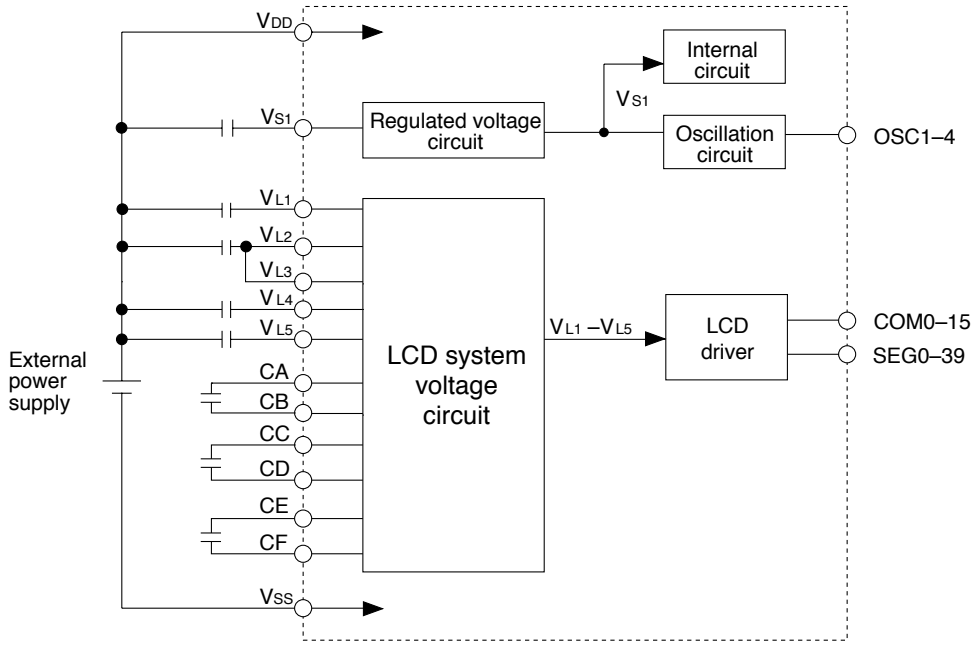


Fig. 3.1.1 Configuration of power supply

3.2 SVD (Supply Voltage Detection) Circuit

3.2.1 Configuration of SVD circuit

The E0C6S46 has a built-in SVD (supply voltage detection) circuit which allows detection of power voltage drop through software.
Turning the SVD operation on and off can be controlled through the software. Because the IC consumes a large amount of current during SVD operation, it is recommended that the SVD operation be kept OFF unless it is otherwise necessary.
Also, the SVD criteria voltage can be set by software. The criteria voltage can be set by matching to one of the 4 types of batteries below that can be used.

-2.2, -2.5, -3.1, -4.2 V (VDD reference voltage)

See "14 Electrical Characteristics" for the precision of the criteria voltage.

Figure 3.2.1.1 shows the configuration of the SVD circuit.

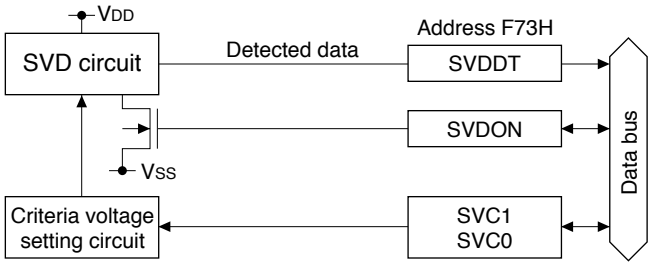


Fig. 3.2.1.1 Configuration of SVD circuit

3.2.2 Control of SVD circuit

The SVD operation control registers are explained below.

Table 3.2.2.1 Control registers of SVD circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
F73H	SVDDT	SVDON	SVC1	SVC0	SVDDT	1	Low	Normal	SVD evaluation data
					SVDON	0	On	Off	SVD circuit On/Off
	R	R/W			SVC1	X			SVD criteria voltage setting
					SVC0	X			

SVC0 and SVC1 (F73H [D0 and D1], R/W)
Criteria voltage for supply voltage detection is set as shown in Table 3.2.2.2.

Table 3.2.2.2 Criteria voltage for SVD circuit

SVC1	SVC0	Criteria voltage
0	0	-2.2 V
0	1	-2.5 V
1	0	-3.1 V
1	1	-4.2 V

The VDD reference voltage is used as the criteria voltage.
At initial reset, this register becomes undefined.

SVDON (F73H [D2], R/W)
Turns the SVD circuit ON and OFF.

When "1" is written: SVD circuit ON
When "0" is written: SVD circuit OFF
Reading: Valid

By writing "1" to the SVDON, the SVD circuit is turned ON, and determination of supply voltage is initiated. Likewise, by writing "0", it is turned OFF.
At initial reset, it is set to "0" (OFF).

Note: The SVD circuit should normally be turned OFF as the consumption current of the IC becomes large when it is ON.

SVDDT (F73H [D3], R)
This is the result of supply voltage determination.

When "0" is read: Criteria voltage ≤ Source voltage (V_{DD}–V_{SS})
When "1" is read: Criteria voltage > Source voltage (V_{DD}–V_{SS})
Writing: Invalid

If the SVD circuit is ON, when the voltage of the battery is detected to be lower than the criteria voltage set at SVC0 and SVC1, SVDDT is "1". If it is more than the criteria voltage, it is "0".
The SVDDT reading is valid when SVDON is "1" and is always "1" when SVDON is "0".

Note: To obtain a stable detection result, after setting SVDON to "1", provide at least 100 µs waiting time before performing SVDDT reading.

3.2.3 Programming notes

(1) The SVD circuit should normally be turned OFF (SVDON = "0") as the consumption current of the IC becomes large when it is ON (SVDON = "1").

(2) To obtain a stable detection result, after setting SVDON to "1", provide at least 100 µs waiting time before performing SVDDT reading.

3.3 Heavy Load Protection Mode

Because the load of the battery in the E0C6S46 becomes heavy due to the buzzer, lamp, and other features, it has been equipped with heavy load protection function in case of power voltage drop. This functions works in the heavy load protection mode.
Based on the workings of the heavy load protection function, the E0C6S46 realizes operation at 2.2 V (Min. 1.8 V, when OSC3 oscillation circuit is not used) source voltage.

During heavy load or when 2.2 V or below is detected by SVD, set it to heavy load protection mode. At the normal mode, the LCD system regulated voltage is created with V_{L2}; V_{L1} is 1/2 reduced V_{L2} voltage while V_{L4} and V_{L5} are created by boosting to 1.5 and 2 times voltages, respectively. On the other hand, at the heavy load protection mode, the regulated voltage is V_{L1}; V_{L2}, V_{L4}, and V_{L5} are created by boosting to 2, 3 and 4 times voltages. Because of this, the consumed current becomes greater than that in the normal mode, be careful not to set the heavy load protection unless necessary.
The LCD system voltage modes are shown in Table 3.3.1.

Table 3.3.1 LCD system voltage mode

LCD voltage	Normal mode	Heavy load protection mode
V_{L1}	1/2 V_{L2}	V_{L1} regulated voltage
V_{L2}	V_{L2} regulated voltage	2 V_{L1}
V_{L4}	3/2 V_{L2}	3 V_{L1}
V_{L5}	4/2 V_{L2}	4 V_{L1}

3.3.1 Control of heavy load protection mode

The control register for the heavy load protection mode are explained below.

Table 3.3.1.1 Control register for heavy load protection mode

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
					ALON	0	All on	Normal	All LCD dots displayed control
	R/W				LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode

HLMOD (F71H [D0], R/W)
Controls the heavy load protection mode.

When "1" is written: Heavy load protection mode is set
When "0" is written: Heavy load protection mode is released
Reading: Valid

Conversion to heavy load protection mode is done by writing "1" to HLMOD while cancellation of this mode is done by writing "0".
At initial reset, the mode is set to "0" (heavy load protection mode cancellation).

3.3.2 Programming notes

(1) During heavy load or when 2.2 V or below is detected by SVD, set it to heavy load protection mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) Perform heavy load driving only after setting up at least 1 ms wait time through the software, after switching to the heavy load protection mode. (See Figure 3.3.2.1.)

(3) When the heavy load protection mode is to canceled after completion of heavy load driving, set up at least 2 seconds wait time through the software. (See Figure 3.3.2.1.)

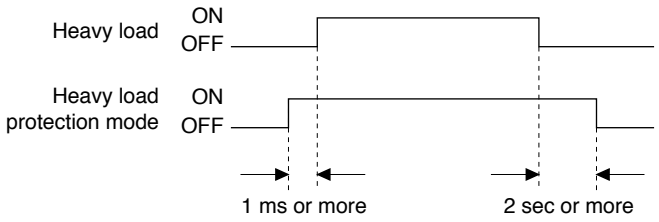


Fig. 3.3.2.1 Control timing for heavy load protection mode

3.4 CPU Operating Voltage Change

During operation, E0C6S46 can change OSC1 and OSC3 system clocks through the software, and operation at clock mode or high-speed mode is then possible. In this case, to obtain stable operating, operating voltage V_{S1} of the internal circuit is changed through the software. For details, see Chapter 5, "Oscillation Circuit".

CHAPTER 4 INITIAL RESET

4.1 Initial Reset Factors

The E0C6S46 requires initial reset function to initialize the circuits.
There are four types of initial reset factors:
(1) External reset through low level input to the $\overline{\text{RESET}}$ terminal
(2) External initial reset by simultaneous low level input of K00–K03 terminals (mask option)
(3) Initial reset by oscillation detector
(4) Initial reset by watchdog timer

Note: The E0C6S46 must be reset after turning power on using the initial reset factor (1) or (2).

Figure 4.1.1 shows the configuration of the initial reset circuit.

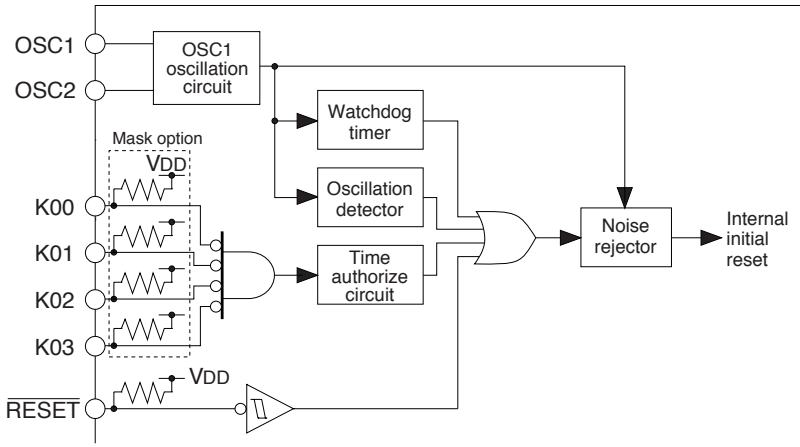


Fig. 4.1.1 Configuration of initial reset circuit

4.1.1 External initial reset by the $\overline{\text{RESET}}$ terminal

Initial resetting can be done externally by placing the reset terminal at low level. When the reset terminal goes high, the CPU will start operating.

Power-on reset

When turning the power on, the reset terminal should be set at a low level as in the timing shown in Figure 4.1.1.1.

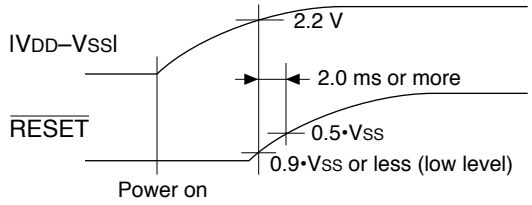


Fig. 4.1.1.1 Initial reset at power on

The reset terminal should be set to 0.9•VSS or less (low level) until the supply voltage becomes 2.2 V or more. After that, a level of 0.5•VSS or less should be maintained more than 2.0 ms.

Reset pulse

Because the initial reset circuit has noise rejector built-in, keep it at low level for at least 2 ms (in case oscillation frequency f_{OSC1} = 32.768 kHz).

4.1.2 External initial reset by simultaneous low level input of K00–K03 terminals

Initial reset may be done by simultaneously providing low level input externally to the input port (K00–K03) selected by mask option. Because the initial reset circuit has time authorize circuit built-in, keep the specified input port terminal at Low level for at least 2 seconds (in case oscillation frequency f_{OSC1} = 32.768 kHz). The input port combination which can be selected from the mask option are as follows:

- Not use
- K00∗K01
- K00∗K01∗K02
- K00∗K01∗K02∗K03

4.1.3 Initial reset by oscillation detector

The oscillation detector generates an initial reset signal until the crystal oscillation circuit (OSC1) starts oscillation during power charge.
However, depending on the power-on sequence (voltage rise timing), the circuit may not work properly. Therefore, use the reset terminal or reset by simultaneous low input to the input port (K00–K03) for initial reset after turning power on.

4.1.4 Initial reset by watchdog timer

If the CPU runs away for some reason, the watchdog timer will detect this situation and output an initial reset signal. See "4.2 Watchdog Timer" for details.

4.1.5 Internal register at initial resetting

The CPU is initialized by initial resetting as follows:

Table 4.1.5.1 Initial values

CPU Core			
Name	Symbol	Bit size	Initial value
Program counter step	PCS	8	00H
Program counter page	PCP	4	1H
Program counter bank	PCB	1	0
New page pointer	NPP	4	1H
New bank pointer	NBP	1	0
Stack pointer	SP	8	Undefined
Index register X	X	12	Undefined
Index register Y	Y	12	Undefined
Register pointer	RP	4	Undefined
General-purpose register A	A	4	Undefined
General-purpose register B	B	4	Undefined
Interrupt flag	I	1	0
Decimal flag	D	1	0
Zero flag	Z	1	Undefined
Carry flag	C	1	Undefined

Peripheral Circuits		
Name	Bit size	Initial value
RAM	640 × 4	Undefined
Display memory	160 × 4	Undefined
Other peripheral circuits	–	∗

∗ See Tables 2.3.1(a)–(d).

4.2 Watchdog Timer

4.2.1 Configuration of watchdog timer

E0C6S46 has a built-in watchdog timer with OSC1 (clock timer 1 Hz signal) basic oscillation. The watchdog timer needs to be reset periodically through the software, and if not reset within 3–4 seconds, it automatically generates an initial reset signal to the CPU.
Figure 4.2.1.1 shows the configuration of the watchdog timer.

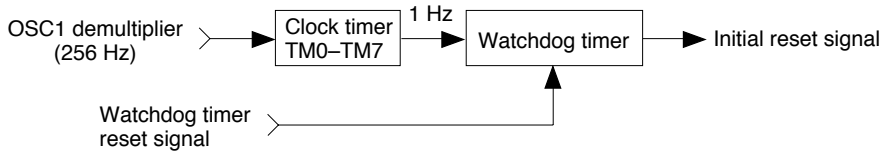


Fig. 4.2.1.1 Configuration of watchdog timer

By resetting the watchdog timer during the program's main routine, program runaways which do not pass the watchdog timer processing during main routine can be detected.
Note, however, that the watchdog timer operates even during HALT such that if the HALT condition continues for 3–4 seconds, it is re-initiated through initial resetting.

4.2.2 Control of watchdog timer

The control register of the watchdog timer is explained below.

Table 4.2.2.1 Control register of watchdog timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
F76H	0	0	TMRST	WDRST	0	–			
					0	–			
	R		W		TMRST	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset

WDRST (F76H [D0], W)
This bit resets the watchdog timer.

When "1" is written: Watchdog timer reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" on WDRST, the watchdog timer is reset, after which it is immediately restarted. Writing "0" will mean no operation.
Because this bit is only for writing, it is always set to "0" during reading.

4.2.3 Programming notes

(1) The watchdog timer must reset within 3-second cycles by the software.

(2) When the clock timer is reset (TMRST ← "1"), the watchdog timer is counted up; reset the watchdog immediately after if necessary.

CHAPTER 5 OSCILLATION CIRCUIT

5.1 Configuration of Oscillation Circuit

The E0C6S46 has two oscillation circuits (OSC1 and OSC3). OSC1 is a crystal oscillation circuit that supplies the operating clock to the CPU and peripheral circuits. OSC3 is either a CR or a ceramic oscillation circuit. When processing with the E0C6S46 requires high-speed operation, the CPU operating clock can be switched from OSC1 to OSC3 by the software. To stabilize operation of the internal circuits, the operating voltage V_{S1} must be switched according to the oscillation circuit to be used. Figure 5.1.1 is the block diagram of this oscillation system.

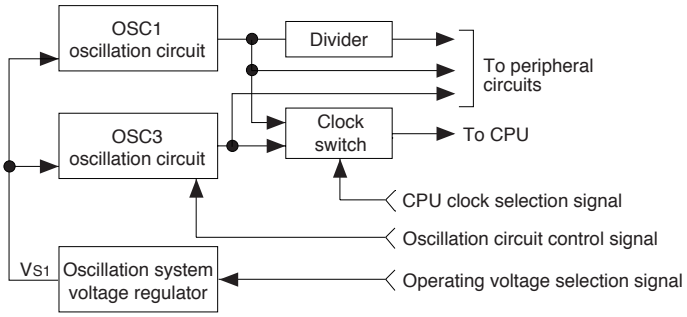


Fig. 5.1.1 Oscillation system block diagram

5.2 OSC1 Oscillation Circuit

The OSC1 oscillation circuit generates the main clock for the CPU and the peripheral circuits. Circuit type is a crystal oscillation circuit.
Figure 5.2.1 shows the configuration of the OSC1 oscillation circuit.

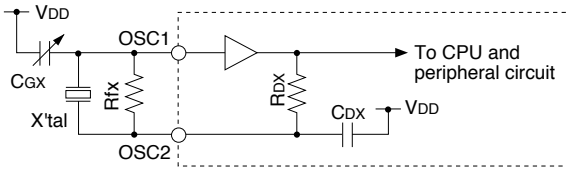
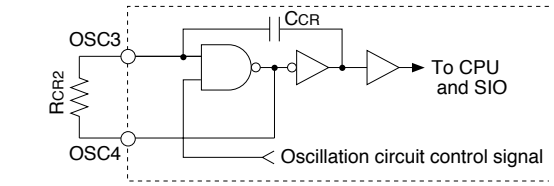


Fig. 5.2.1 OSC1 crystal oscillation circuit

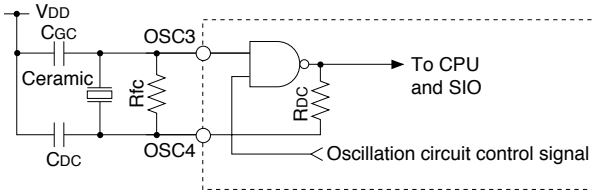
As shown in Figure 5.2.1, the crystal oscillation circuit can be configured simply by connecting the crystal oscillator (X'tal) of 32.768 kHz (Typ.) and the feedback resistor Rfx (10 MΩ) between the OSC1 and OSC2 terminals and the trimmer capacitor (C_{GX}) between the OSC1 and V_{DD} terminals.

5.3 OSC3 Oscillation Circuit

The E0C6S46 has built-in the OSC3 oscillation circuit that generates the CPU's sub-clock (Max. 2 MHz) for high speed operation. The mask option enables selection of either the CR or ceramic oscillation circuit. When CR oscillation is selected, only a resistance is required as an external element. When ceramic oscillation is selected, a ceramic oscillator and two capacitors (gate and drain capacitance) are required. Figure 5.3.1 shows the configuration of the OSC3 oscillation circuit.



(1) CR oscillation circuit



(2) Ceramic oscillation circuit

Fig. 5.3.1 OSC3 oscillation circuit

As shown in Figure 5.3.1, the CR oscillation circuit can be configured simply by connecting the resistor R_{CR2} between the OSC3 and OSC4 terminals when CR oscillation is selected. See "14 Electrical Characteristics" for resistance value of R_{CR2}.
When ceramic oscillation is selected, the ceramic oscillation circuit can be configured by connecting the ceramic oscillator (Max. 2 MHz) and the feedback resistor Rfc (about 1 MΩ) between the OSC3 and OSC4 terminals, capacitor C_{GC} between the OSC3 and OSC4 terminals, and capacitor C_{DC} between the OSC4 and V_{DD} terminals. For both C_{GC} and C_{DC}, connect capacitors that are about 100 pF. To reduce current consumption of the OSC3 oscillation circuit, oscillation can be stopped by the software (OSCC register).

When the OSC3 oscillation circuit is not used, connect the OSC3 terminal to V_{S1}.

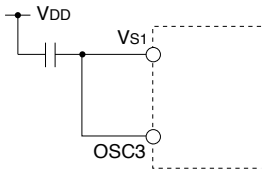


Fig. 5.3.2 Connection diagram when the OSC3 oscillation circuit is unused

5.4 Operating Voltage Change

E0C6S46 can change OSC1 and OSC3 system clocks through the software. In this case, to obtain stable operation, operating voltage V_{S1} of the internal circuit is changed through the software.
Likewise, when selecting OSC1 as the system clock, there is need to change operating voltage V_{S1} according to the value of the power voltage (V_{DD}–V_{SS}).
Oscillation frequency and the corresponding operating voltage V_{S1} are shown in Table 5.4.1.

Table 5.4.1 Oscillation frequency and operating voltage

Oscillation frequency	Oscillation circuit	Operating voltage V_{S1}
32.768 kHz	OSC1	-1.2 V or -2.1 V
1 MHz	OSC3	-2.1 V
2 MHz	OSC3	-3.0 V

The V_{DD} reference voltage is used as the operating voltage V_{S1}.
When OSC3 is to be used as the CPU system clock, change the operating voltage V_{S1} accordingly through the software and then turn the OSC3 oscillation ON and switch the clock frequency.
If the OSC3 oscillation frequency is to be fixed around 1 MHz, set the operating voltage to -2.1 V; at 2 MHz, set the operating voltage to -3.0 V.
Moreover, when the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage detected with the SVD circuit were less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the detected voltage were 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). However, it can be used fixed at -1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

Note: Switching V_{S1} when the power source voltage is lower than the set voltage may cause misoperation. Perform the operating voltage only after making sure that power voltage by SVD is more than the V_{S1} setting voltage (absolute value).

5.5 Clock Frequency and Instruction Execution Time

Table 5.5.1 shows the instruction execution time according to each frequency of the system clock.

Table 5.5.1 Clock frequency and instruction execution time

Clock frequency	Instruction execution time (μs)		
	5-clock instruction	7-clock instruction	12-clock instruction
32.768 kHz	152.6	213.6	366.2
1 MHz	5.0	7.0	12.0
2 MHz	2.5	3.5	6.0

5.6 Control of Oscillation Circuit

The control registers for the oscillation circuit are explained below.

Table 5.6.1 Control registers of oscillation circuit

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
F70H	CLKCHG	OSCC	VSC1	VSC0	CLKCHG	0	OSC3	OSC1	CPU system clock switch
					OSCC	0	On	Off	OSC3 oscillation On/Off
	R/W				VSC1	0			CPU operating voltage switch
					VSC0	0			

VSC0 and VSC1 (F70H [D0 and D1], R/W)

Switches the operating voltage of the internal circuit in accordance to the oscillation frequency and power source voltage.

The corresponding setting description is shown in Table 5.6.2.

Table 5.6.2 Corresponding between oscillation frequency, power source voltage, and operating voltage (V_{S1})

VSC1	VSC0	V_{S1}	Oscillation circuit	Oscillation frequency	Power source voltage (V_{DD}–V_{SS})
0	0	-1.2 V	OSC1	32.768 kHz	Under 3.1 V
0	1	-2.1 V	OSC1	32.768 kHz	3.1 V or more (∗)
0	1	-2.1 V	OSC3	1 MHz	2.2 V or more
1	×	-3.0 V	OSC3	2 MHz	3.1 V or more

The V_{DD} reference voltage is used as the operating voltage V_{S1}.

There is no need to set the (∗) state with regards to power whose initial value is 3.6 V or less as in lithium batteries.

VSC1 and VSC0 are set to "0" at initial reset.

Note: When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

(VSC1, VSC0) = (0, 0) → (0, 1) → 5 ms WAIT → (1, ×)
= (1, ×) → (0, 1) → 5 ms WAIT → (0, 0)

= (0, 0) → (1, ×) is prohibited
= (1, ×) → (0, 0) is prohibited

Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.

OSCC (F70H [D2], R/W)

Controls the oscillation of the OSC3 oscillation circuit.

When "1" is written: OSC3 oscillation ON
When "0" is written: OSC3 oscillation OFF
Reading: Valid

When high-speed operation of the CPU is required, OSCC is set to "1"; otherwise, set it to "0" to minimize power current consumption.

At initial reset, OSCC is set to "0".

Note: It takes 5 ms for the OSC3 oscillation circuit to stabilize after oscillation turns ON. Since oscillation stabilization time differs according to external oscillation terminal and usage conditions, set the stand-by time with enough allowance when switching the clock frequency.

CLKCHG (F70H [D3], R/W)

Selects the CPU operating clock.

When "1" is written: OSC3 clock is selected
When "0" is written: OSC1 clock is selected
Reading: Valid

When assigning OSC3 as the CPU operating clock, set CLKCHG to "1"; when assigning OSC1, set it to "0". At initial reset, CLKCHG is set to "0".

Note: When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.6.1 and then proceed with software processing.

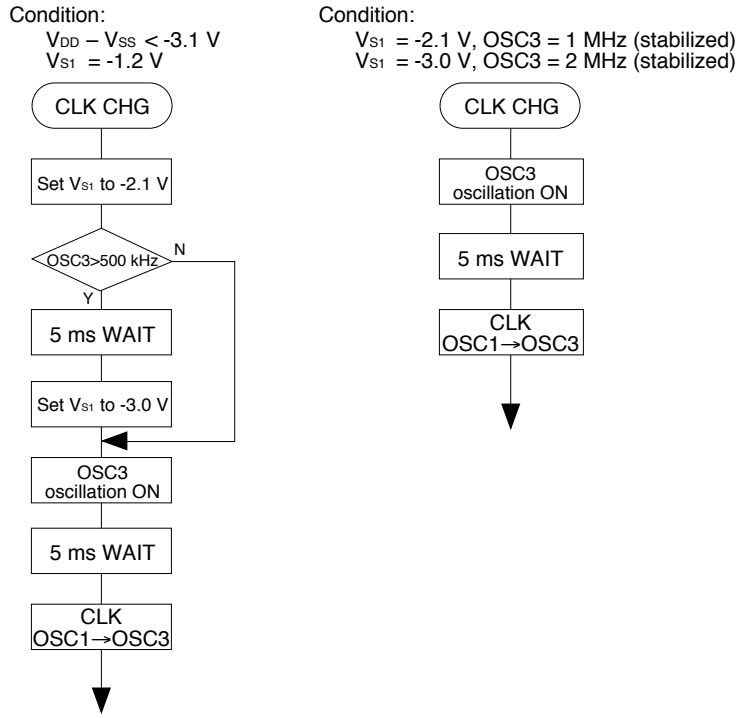


Fig. 5.6.1 CPU operating clock control flow

5.7 Programming Notes

(1) When high-speed operation of the CPU is not required, observe the following reminders to minimize power current consumption.

Set the CPU operating clock to OSC1.
Turn the OSC3 oscillation OFF.
Set the internal operating voltage (V_{S1}) to -1.2 V or -2.1 V.

(2) When the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage detected with the SVD circuit were less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the detected voltage were 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). Moreover, because -1.2 V will be set during initial reset, be sure to execute the previous process at the beginning of the initial routine. Note, however, that it can be used fixed at 1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

(3) When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

(VSC1, VSC0) = (0, 0) → (0, 1) → 5 ms WAIT → (1, ×)
= (1, ×) → (0, 1) → 5 ms WAIT → (0, 0)

= (0, 0) → (1, ×) is prohibited
= (1, ×) → (0, 0) is prohibited

Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.

(4) When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.6.1 and then proceed with software processing.

(5) Use separate instructions to switch the clock from OSC3 to OSC1 and turn the OSC3 oscillation OFF. Simultaneous processing with a single instruction may cause malfunction of the CPU.

CHAPTER 6 INPUT/OUTPUT PORTS

6.1 Input Port (Kxx)

6.1.1 Configuration of input ports

The E0C6S46 has 8 bits (4 bits × 2, K00–K03, K10–K13) general input ports built-in.
Figure 6.1.1.1 shows the configuration of the input port.

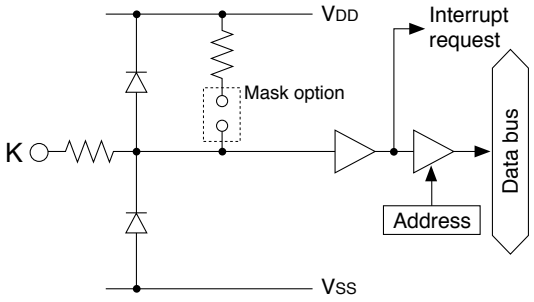


Fig. 6.1.1.1 Configuration of input port

The input port pin K03 is used as the clock input pins for the programmable timer. See "8.3 Programmable Timer" for details.

6.1.2 Mask option

The input ports (K00–K03 and K10–K13) are provided with built-in pull up resistor the use of which may be selected for every bit with the mask option.
Selection of "Pull up resistor enable" with the mask option suits input from the push switch, key matrix, and so forth. When changing the input port from low level to high level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 μs waiting time is required.
When "Pull up resistor disabled" is selected, the port can be used for slide switch input and interfacing with other LSIs. In this case, take care that floating state does not occur.

6.1.3 Interrupt function

All eight bits of the input ports K00–K03 and K10–K13 provide the interrupt function.
Whether to mask the interrupt function can be selected individually for all eight bits by the software.

Input interrupt (K00–K03) and input relation registers

The input ports K00–K03 are equipped with input relation registers. The condition for issuing an interrupt can be set by the software.
Figure 6.1.3.1 shows the configuration of the input (K00–K03) interrupt circuit.

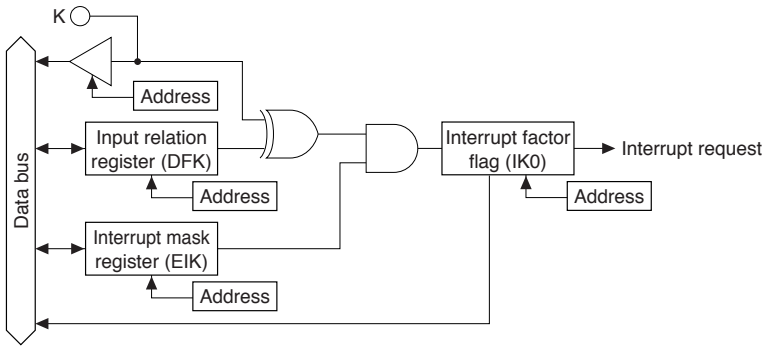


Fig. 6.1.3.1 Configuration of input (K00–K03) interrupt circuit

The input interrupt timing of K00–K03 can be set to generate interrupt at the rising edge or falling edge of the input by the setting of input relation registers DFK00–DFK03. Moreover, masking can be set individually to the interrupt of K00–K03. However, if the interrupt of any one of K00–K03 is enabled, interrupt will be generated when the content change from matched to no matched with the input relation register. When interrupt is generated, the interrupt factor flag IK0 is set to "1".
Figure 6.1.3.2 shows an example of an interrupt for K00–K03.

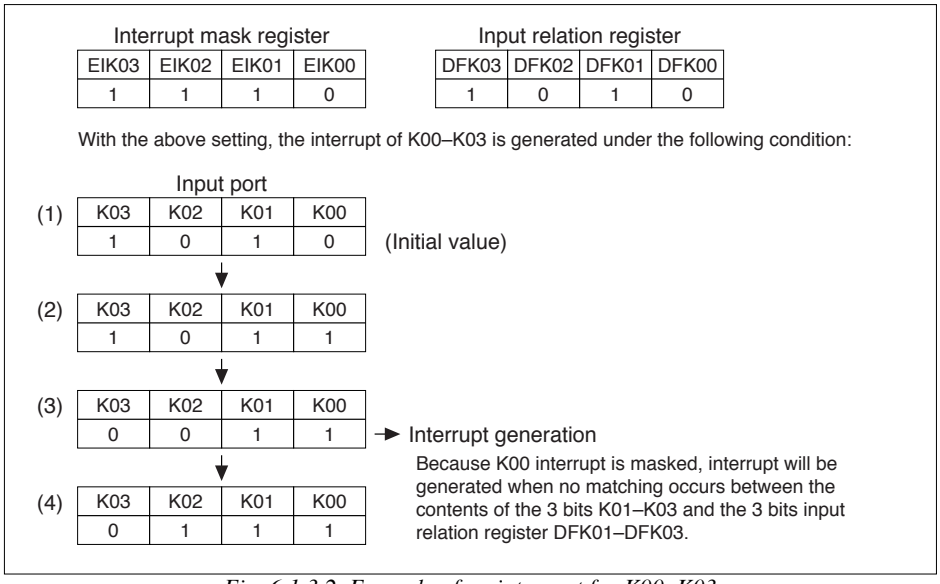


Fig. 6.1.3.2 Example of an interrupt for K00–K03

Because K00 is masked by an interrupt mask register (EIK00), interrupt will not be generated at the above step (2). Next, since K03 becomes "0" at step (3), interrupt is generated due to the no matching of the data of the terminal whose interrupt is enabled and the data of the input relation registers. No interrupt is generated from a no matched state to another no matched state as in step (4) because the condition for interrupt generation, as has been previously stated, is that the port data and the contents of the input relation registers must change from a matched state to a no matched one. Moreover, a terminal whose interrupt is masked will not affect the condition for interrupt generation.

Input interrupt (K10–K13)

Figure 6.1.3.3 shows the configuration of the input (K10–K13) interrupt circuit.

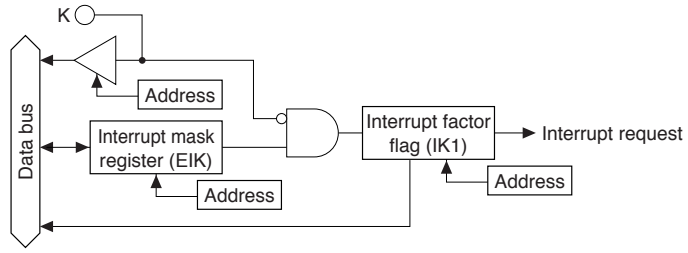


Fig. 6.1.3.3 Configuration of the input (K10–K13) interrupt circuit

There is no input relation registers for K10–K13, and interrupt is fixed to occur at the falling edge of input. The interrupt mask can be selected for each of the four pins with the interrupt mask register EIK10–EIK13. When all the enabled pins are "1", interrupt occurs when one or more of the pins changes to "0".

When interrupt is generated, the interrupt factor flag IK1 is set to "1".

Figure 6.1.3.4 shows an example of an interrupt for K10–K13.

Interrupt mask register

EIK13	EIK12	EIK11	EIK10
0	1	1	1

With the above setting, the interrupt of K10–K13 is generated under the following condition:

Input port

	K13	K12	K11	K10	
(1)	1	1	1	1	(Initial value)
(2)	0	1	1	1	
(3)	0	1	0	1	→ Interrupt generation
(4)	0	1	0	0	

Because K13 interrupt is masked, interrupt will be generated when one or more terminals among the 3 bits K10–K12 become "0" from a state where all terminals were "1".

Fig. 6.1.3.4 Example of an interrupt for K10–K13

The mask register (EIK13) masks the interrupt of K13, so an interrupt does not occur at (2). At (3), K11 becomes "0", so that an interrupt occurs if the interrupt enabled pins were all "1" and at least one pin then changes to "0". At (4), the conditions for interrupt are not established, so an interrupt does not occur. Further, pins that have been masked for interrupt do not affect the conditions for interrupt generation.

6.1.4 Control of input ports

The control registers for the input ports are explained below.

Table 6.1.4.1 Control registers of input ports

Address	Register D3	D2	D1	D0	Name	Init	1	0	Comment
F04H	0	0	0	IK0	0	–			
					0	–			
	R				0	–			
					IK0	0	Yes	No	Interrupt factor flag (K00–K03)
F05H	0	0	0	IK1	0	–			
					0	–			
	R				0	–			
					IK1	0		No	Interrupt factor flag (K10–K13)
F14H	EIK03	EIK02	EIK01	EIK00	EIK03	0	Enable	Mask	Interrupt mask register (K03)
					EIK02	0	Enable	Mask	Interrupt mask register (K02)
	R/W				EIK01	0	Enable	Mask	Interrupt mask register (K01)
					EIK00	0	Enable	Mask	Interrupt mask register (K00)
F15H	EIK13	EIK12	EIK11	EIK10	EIK13	0	Enable	Mask	Interrupt mask register (K13)
					EIK12	0	Enable	Mask	Interrupt mask register (K12)
	R/W				EIK11	0	Enable	Mask	Interrupt mask register (K11)
					EIK10	0	Enable	Mask	Interrupt mask register (K10)
F40H	K03	K02	K01	K00	K03	–	High	Low	Input port (K00–K03)
					K02	–	High	Low	
	R				K01	–	High	Low	
					K00	–	High	Low	
F41H	DFK03	DFK02	DFK01	DFK00	DFK03	1	⌐	⌙	Input relation register (DFK00–DFK03)
					DFK02	1	⌐	⌙	
	R/W				DFK01	1	⌐	⌙	
					DFK00	1	⌐	⌙	
F42H	K13	K12	K11	K10	K13	–	High	Low	Input port (K10–K13)
					K12	–	High	Low	
	R				K11	–	High	Low	
					K10	–	High	Low	

K00–K03, K10–K13 (F40H, F42H, R)

Input data of the input port terminal may be read out with these registers.

When "1" is read: High level
When "0" is read: Low level
Writing: Invalid

The terminal voltage of 8 bits input ports (K00–K03 and K10–K13) are each reading as "1" and "0" at high (V_{DD}) level and low (V_{SS}) level, respectively.
When these bits are used for reading only, writing operation becomes invalid.

DFK00–DFK03 (F41H, R/W)

These input relation registers which set the interrupt generating conditions of K00–K03.

When "1" is written: Falling edge
When "0" is written: Rising edge
Reading: Valid

When DFK0x is set to "1", the falling edge of the input becomes an interrupt generating condition, the rising edge when set to "0". DFK0x respectively correspond to input ports K0x and may be set in units of 1 bit.
At initial reset, these registers are all set to "1".

EIK00–EIK03, EIK10–EIK13 (F14H, F15H, R/W)

These are interrupt mask registers of the input ports.

When "1" is written: Enable
When "0" is written: Mask
Reading: Valid

EIK0x corresponds to input port K0x, and EIK1x corresponds to input port K1x. Whether to mask the interrupt function can be set in units of 1 bit.
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, these registers are all set to "0" (mask).

IK0, IK1 (F04H [D0], F05H [D0], R)

These are interrupt factor flags of the input ports.

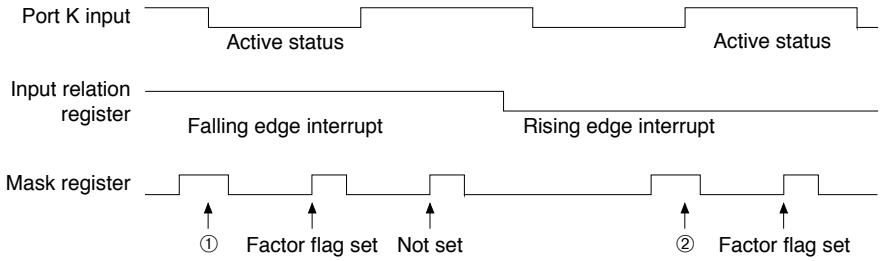
When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

The interrupt factor flags IK0 and IK1 are associated with K00–K03 and K10–K13, respectively. From the status of these flags, the software can decide whether an input interrupt has occurred.
These flags will not be set even if the input conditions are established if, for every terminal series, the interrupt mask registers (EIKxx) are all set to "0" (i.e., EIK00–EIK03, or EIK10–EIK13 are all set to "0", or all are individually set to "0").
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, these flags are set to "0".

6.1.5 Programming notes

(1) When changing the input port from low level to high level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 μs waiting time is required.

(2) Input interrupt programming related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 6.1.5.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set. Therefore, when using the input interrupt, the active status of the input terminal implies

input terminal = low status, when the falling edge interrupt is effected and
input terminal = high status, when the rising edge interrupt is effected.

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 6.1.5.1. However, when clearing the content of the mask register with the input terminal kept in the low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case. When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (high status).

When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 6.1.5.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the low status.

In addition, when the mask register = "1" and the content of the input relation register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input relation register in the mask register = "0" status.

(3) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(4) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

6.2 Output Port (Rxx)

6.2.1 Configuration of output ports

The E0C6S46 has 20 bits (4 bits × 5, R00–R03, R10–R13, R20–R23, R30–R33, and R40–R43) general output ports built-in.
Figure 6.2.1.1 shows the configuration of the output port.

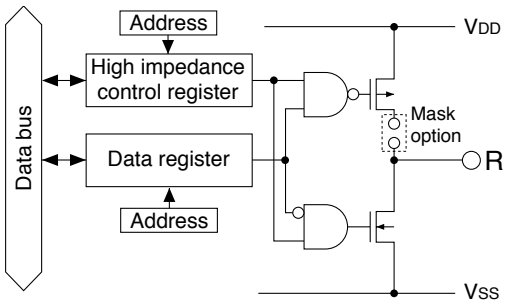


Fig. 6.2.1.1 Configuration of output port

6.2.2 Mask option

The output ports may be selected for the following by mask option.

(1) Output specification of output ports

The output specification of the output ports may be selected as listed below. Two types of output specification may be selected: complementary output and N channel (Nch) open drain output. However, even if Nch open drain is selected, application on the terminal of voltage exceeding the power current voltage is not permitted.

R00–R03: Complementary or Nch open drain (selected with the 4 bits group)
R10–R13: Complementary or Nch open drain (selected with the 4 bits group)
R20–R22: Complementary or Nch open drain (selected with the 3 bits group)
R23: Complementary or Nch open drain
R30–R33: Complementary or Nch open drain (select in units of 1 bit)
R40–R43: Complementary or Nch open drain (select in units of 1 bit)

(2) Special output

Output ports R33, R40, R42 and R43 may be selected, in addition to DC output, as special output port as follows:

R33: SIO Ready ($\overline{\text{SRDY}}$) or programmable timer operating clock output (PTCLK)
R40: Clock inverted output ($\overline{\text{FOUT}}$)
R42: Buzzer inverted output ($\overline{\text{BZ}}$) or clock output (FOUT)
R43: Buzzer output (BZ)

Buzzer outputs BZ (R43) and $\overline{BZ}$ (R42)

Through mask option selection, R43 and R42 may be assigned as buzzer outputs. BZ and $\overline{BZ}$ are buzzer signal outputs for driving piezo-electric buzzers, the buzzer signal being created by the division of fOSC1. Moreover, digital envelope may be added to the buzzer signal.
See Chapter 10, "Sound Generator" for details.

Buzzer output BZ and $\overline{BZ}$ can be controlled simultaneously by register R43. Note, however, that register R42 at $\overline{BZ}$ output selection may be used as a 1-bit general register in which Read/Write operation is possible, and the data of said register will not affect $\overline{BZ}$ (output from the R42 terminal).

Notes: • *The BZ and $\overline{BZ}$ output signals could generate hazards during ON/OFF switching.*

• *When output port R43 is set to DC output, output port R42 may not be set to $\overline{BZ}$ output.*

Figure 6.2.2.1 shows the output waveform of BZ and $\overline{BZ}$.

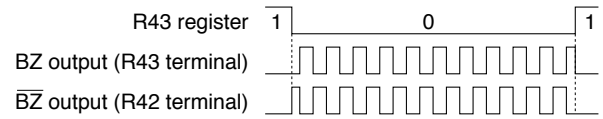


Fig. 6.2.2.1 Output waveform of BZ and $\overline{BZ}$

SIO Ready $\overline{SRDY}$ (R33)

When output port R33 is selected as $\overline{SRDY}$ output, it will generate a Ready signal which will indicate whether the serial interface is available to transmit or receive signals. See Chapter 9, "Serial Interface" for details.

PTCLK (R33)

The operating clock for the programmable timer is output externally from this port. In this case, the clock output ON or OFF may be controlled from the R33 register by setting PTCOUT (F79H [D3]) to "1". The clock frequency is selected by the 3 bits register of PTC0–PTC2.
Moreover, when PTCOUT is set to "0", output port R33 becomes DC output.
Because of the above functions, PTCLK output and DC output belong to a common option selection item. Refer to "8.3 Programmable Timer" regarding selection of clock frequency.

Control of R33 output

3 states output or 2 states output for output port R33 may be selected with the mask option.
When $\overline{SRDY}$ is selected for R33, 2 states output is ordinarily selected in compliance with it.
Moreover, although 2 states output may be selected even during the selection of DC output and PTCLK output, caution is required as output becomes undefined (i.e., it will not be initially reset) when power is supplied.

Clock outputs FOUT (R42), $\overline{FOUT}$ (R40)

When R40 and R42 are selected to clock output, it outputs the clock of fOSC3, fOSC1 or the demultiplied fOSC1. R40 ($\overline{FOUT}$) output generates an antiphase clock in relation to R42 (FOUT). Figure 6.2.2.2 shows the output waveform of FOUT and $\overline{FOUT}$. The clock frequency is selectable with the mask options, from the frequencies listed in Table 6.2.2.1.

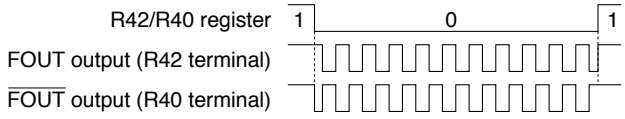


Fig. 6.2.2.2 Output waveform of FOUT and $\overline{FOUT}$

Note: Clock output signal could generate hazards during ON/OFF switching.

Table 6.2.2.1 FOUT clock frequency

Setting	Clock frequency (Hz)
fOSC3	OSC3 oscillation frequency
fOSC1/ 1	32,768
fOSC1/ 2	16,384
fOSC1/ 4	8,192
fOSC1/ 8	4,096
fOSC1/ 16	2,048
fOSC1/ 32	1,024
fOSC1/ 64	512
fOSC1/128	256

6.2.3 High impedance control

The terminal output state of output ports R00–R03, R10–R13, R20–R23, and R30–R33, may be selected for high impedance state through the software in 4 bits groups. Control is done with the high impedance control registers (HZR0–HZR3).

6.2.4 Control of output ports

The control registers for the output ports are explained below.

Table 6.2.4.1 Control registers of output ports

Address	Register D3	D2	D1	D0	Name	Init	1	0	Comment
F50H	R03	R02	R01	R00	R03	X	High	Low	Output port (R00–R03)
					R02	X	High	Low	
	R/W				R01	X	High	Low	
					R00	X	High	Low	
F51H	R13	R12	R11	R10	R13	X	High	Low	Output port (R10–R13)
					R12	X	High	Low	
	R/W				R11	X	High	Low	
					R10	X	High	Low	
F52H	R23	R22	R21	R20	R23	X	High	Low	Output port (R20–R23)
					R22	X	High	Low	
	R/W				R21	X	High	Low	
					R20	X	High	Low	
F53H	R33	R32	R31	R30	R33	X	High	Low	Output port (R33)
							Off	On	PTCLK output
	R/W								[$\overline{\text{SRDY}}$ (SIO READY)]
					R32	X	High	Low	Output port (R30–R32)
					R31	X	High	Low	
					R30	X	High	Low	
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT)
									[Buzzer inverted output ($\overline{\text{BZ}}$)]
					R41	1	High	Low	Output port (R41)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output ($\overline{\text{FOUT}}$)
F7BH	HZR3	HZR2	HZR1	HZR0	HZR3	0	Output	High-Z	R30–R33 output high-impedance control
					HZR2	0	Output	High-Z	R20–R23 output high-impedance control
	R/W				HZR1	0	Output	High-Z	R10–R13 output high-impedance control
					HZR0	0	Output	High-Z	R00–R03 output high-impedance control

HZR0–HZR3 (F7BH, R/W)
Controls high impedance loading to output ports R00–R03, R10–13, R20–R23 and R30–R33 in units of 4 bits groups.

When "1" is written: Data output
When "0" is written: High impedance
Reading: Valid

By writing "1" in the control registers (HZR0–HZR3) corresponding to the groups, the output register data is generated in the terminal; writing "0" will generate high impedance state.
During initial reset, these registers are set to "0" and the ports acquire high impedance state.

When DC output is selected

R00–R03, R10–R13, R20–R23, R30–R33, R40–R43 (F50H, F51H, F52H, F53H, F54H, R/W)
Sets the output data for the output ports.

When "1" is written: High level
When "0" is written: Low level
Reading: Valid

Output port terminals will generate the data written into the corresponding registers (R00–R03, .. R40–R43) as it is. The output port terminal goes high (V_{DD}) when "1" is written to the register, and goes low (V_{SS}) when "0" is written.
At initial reset, only R40–R43 are set to "1" and the other output registers become undefined.

When special output is selected

R43 (F54H [D3], R/W) when BZ and $\overline{BZ}$ output is selected
Performs the output control of buzzer signal (BZ, $\overline{BZ}$).

When "0" is written: Buzzer signal output
When "1" is written: Low level (DC)
Reading: Valid

When "0" is set on R43, BZ signal is generated from R43 terminal; at the same time, $\overline{BZ}$ signal (BZ inverted signal) is generated from R42 terminal if R42 is set to $\overline{BZ}$ output.
When "1" is set on R43, R43 terminal (and R42 terminal too, when $\overline{BZ}$ output is selected) output goes low (V_{SS}).
Note, however, that R42 at $\overline{BZ}$ output selection may be used as a 1-bit general register in which Read / Write operation is possible, and the data of said register will not affect $\overline{BZ}$ (R42 terminal output).
At initial reset, R43 and R42 are set to "1".

R33 (F53H [D3], R/W) when PTCLK (DC) output is selected
Controls the output of the programmable timer operating clock (PTCLK).

When "0" is written: Clock output
When "1" is written: High level (DC)
Reading: Valid

With "1" written on PTCOUT (F79H [D3]), the operating clock of the programmable timer may be generated externally by writing "0" on R33 register. Moreover, the output will go high (V_{DD}) by writing "1". However, when PTCOUT is "0", the output becomes regular DC output.
Because this register is not initialized during initial reset, R33 terminal becomes undefined when 2 states output is selected with mask option.

R40, R42 (F54H [D0, D2], R/W) when FOUT and $\overline{\text{FOUT}}$ output is selected

Controls the FOUT and $\overline{\text{FOUT}}$ (clock) output.

When "0" is written: Clock output
When "1" is written: High level (DC)
Reading: Valid

When R42 is set to FOUT output, clock with the specified frequency is generated from R42 terminal by writing "0" on R42 register.
By writing "1", the R42 terminal will go high (V_{DD}).
The same applies to R40. The clock phase when $\overline{\text{FOUT}}$ signal is output from R40 is antiphase to that of R42.
At initial reset, R40 and R42 are set to "1".

6.2.5 Programming notes

(1) When BZ, $\overline{\text{BZ}}$, FOUT, $\overline{\text{FOUT}}$, and PTCLK (DC) are selected by mask option, a hazard may be observed in the output waveform when the data of the output register changes.

(2) Because the R00–R03, R10–R13, R20–R23, and R30–R32 (R33) ports gain high impedance during initial reset, be careful when using them as interface with external devices and the like.

(3) When R33 port is selected for 2 states and DC (PTCLK) output by mask option, R33 terminal becomes undefined at initial reset.

6.3 I/O Port (Pxx)

6.3.1 Configuration of I/O ports

The E0C6S46 has 16 bits (4 bits × 4, P00–P03, P10–P13, P20–P23, and P30–P33) general I/O ports built-in. Figure 6.3.1.1 shows the configuration of the I/O port.

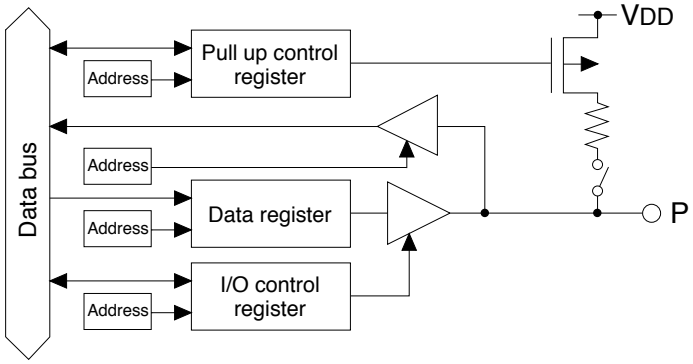


Fig. 6.3.1.1 Configuration of I/O port

6.3.2 Mask option

The following by mask option may be selected for the I/O ports P00–P03, P10–P13, P20–P23, P30–P33.

(1) Output specification during output mode

Output specification (during output) for each I/O port may be selected as listed below. Two types of output specification may be selected: complementary output and N channel (Nch) open drain output. However, even if Nch open drain is selected, application on the terminal of voltage exceeding the power current voltage is not permitted.

P00–P03: Complementary or Nch open drain (selected with the 4 bits group)
P10–P13: Complementary or Nch open drain (selected with the 4 bits group)
P20–P22: Complementary or Nch open drain (select in units of 1 bit)
P30–P33: Complementary or Nch open drain (select in units of 1 bit)

(2) Dedicated output port

The I/O ports P30–P33 may be set with the mask option as dedicated output ports.
This selection may be conducted by 1 bit.

6.3.3 I/O control register and input/output mode

When using an I/O port as Pxx (x = 0 to 3), input/output direction may be set by group, with 4 bits each of Px0 to Px3 (x = 0 to 3) considered as one group. Modes can be set by writing input/output direction data to the I/O control register corresponding I/O port group.

To set the input mode, "0" is written to the I/O control register. When an I/O port is set to input mode, it becomes high impedance state and works as an input port.

The output mode is set when "1" is written to the I/O control register. When an I/O port set to output mode works as an output port, it outputs a high level (V_{DD}) when the data of output register is "1", and a low level (V_{SS}) when the data of output register is "0".

Setting of the I/O control register is not effective for the ports set as dedicated output through the mask option.

6.3.4 Pull up resistor

The common input/output ports can be selected through the software to apply pull up resistor in 4 bits groups.
Selection of pull up resistor application is done by writing data to the pull up resistor control registers (PUP0–PUP3).

6.3.5 Control of I/O ports

The control registers for the I/O ports are explained below.

Table 6.3.5.1 Control register of I/O ports

Address	Register D3	D2	D1	D0	Name	Init	1	0	Comment
F60H	P03	P02	P01	P00	P03	X	High	Low	I/O port (P00–P03)
					P02	X	High	Low	
					P01	X	High	Low	
	R/W				P00	X	High	Low	
F61H	P13	P12	P11	P10	P13	X	High	Low	I/O port (P10–P13)
					P12	X	High	Low	
					P11	X	High	Low	
	R/W				P10	X	High	Low	
F62H	P23	P22	P21	P20	P23	X	High	Low	I/O port (P20–P23)
					P22	X	High	Low	
					P21	X	High	Low	
	R/W				P20	X	High	Low	
F63H	P33	P32	P31	P30	P33	X	High	Low	I/O port / Dedicated output port (P33)
					P32	X	High	Low	I/O port / Dedicated output port (P32)
					P31	X	High	Low	I/O port / Dedicated output port (P31)
	R/W				P30	X	High	Low	I/O port / Dedicated output port (P30)
F7DH	IOC3	IOC2	IOC1	IOC0	IOC3	0	Output	Input	I/O control (P30–P33)
					IOC2	0	Output	Input	I/O control (P20–P23)
					IOC1	0	Output	Input	I/O control (P10–P13)
	R/W				IOC0	0	Output	Input	I/O control (P00–P03)
F7EH	PUP3	PUP2	PUP1	PUP0	PUP3	0	Off	On	I/O pull up resistor On/Off (P30–P33)
					PUP2	0	Off	On	I/O pull up resistor On/Off (P20–P23)
					PUP1	0	Off	On	I/O pull up resistor On/Off (P10–P13)
	R/W				PUP0	0	Off	On	I/O pull up resistor On/Off (P00–P03)

IOC0, IOC1, IOC2, IOC3 (F7DH, R/W)

Input/output direction of I/O ports are set in units of 4 bits groups.

When "1" is written: Output mode
When "0" is written: Input mode
Reading: Valid

IOCx (I/O control register) and port group correspondence are as follows:

IOC0: P00–P03
IOC1: P10–P13
IOC2: P20–P23
IOC3: P30–P33

By writing "1" to IOCx (x = 0 to 3), the I/O ports in the corresponding group are placed in the output mode, while writing "0" place them in the input mode.
At initial reset, IOCx are set to "0" and the I/O ports are all in the input mode.

PUP0, PUP1, PUP2, PUP3 (F7EH, R/W)

Whether the I/O ports will be pulled up or not is set in units of 4 bits groups.

When "0" is written: Pull up ON
When "1" is written: Pull up OFF
Reading: Valid

PUPx and port group correspondence are the same as that of the IOCx.
By writing "0" to PUPx (x = 0 to 3), the I/O ports in the corresponding group are pulled up, while writing "1" turns the pull up function OFF.
At initial reset, PUPx are set at "0", and all I/O ports are pulled up.

P00–P03, P10–P13, P20–P23, P30–P33 (F60H, F61H, F62H, F63H, R/W)

- **During writing operation**

  When "1" is written: High level
  When "0" is written: Low level

  When the I/O port is set at output port, the data written is generated on the I/O port terminal as it is. When "1" is written as port data, the port terminal goes high (V_{DD}) and goes low (V_{SS}) when "0" is written.
  This is the same when P30–P33 are set as dedicated output ports through the mask option.
  Note, however, that even at input mode, port data writing is also possible.

- **During reading operation**

  When "1" is read: High level
  When "0" is read: Low level

  Reading the I/O port terminal voltage level. When the I/O port is at input mode, voltage level input of the port terminal is read; when set at output mode, output voltage level is read. When the terminal voltage is at high (V_{DD}) level, port data reading is "1"; at low (V_{SS}) level, it is "0".

6.3.6 Programming notes

(1) When the I/O port is set at output mode, and low impedance load is connected to the port terminal, the data written and read may differ.

(2) If the state of the I/O port meets all of the following 4 conditions, the reading data will be undefined:
- The input/output mode is set at output mode
- Output specification is set at Nch open drain
- The content of the data register is "1"
- The pull up resistor turned is OFF

(3) When P30–P33 has been set as the output exclusive in the mask option, a pull up resistor cannot be added even if the pull up resistor control register PUP3 has been made "0".

CHAPTER 7 LCD DRIVER

The E0C6S46 has 16 common terminals and 40 segment terminals and can drive a maximum of 640 (40 × 16) dots (8 characters × 2 lines) LCD.
This LCD driver performs the following control through the software.

- Drive duty can be set to 1/16 or 1/8 duty.
- LCD contrast can be adjusted through a 16 steps range.
- All dots of the LCD panel can be switched ON and OFF.

7.1 Drive Duty

Because the power for LCD driving is generated by the internal circuit of the CPU, there is no need to provide for it externally. Driving is done by 1/16 duty or 1/8 duty dynamic drive through 4 electric potentials (1/4 bias) : V_{L1}, V_{L2}, V_{L4}, and V_{L5}. The 5 electric potentials are entered in V_{L1}, V_{L2}, V_{L3}, V_{L4} and V_{L5} terminals and 1/5 bias driving may then be set.
Drive duty may be selected from the software. Dot number differences due to the selected duty are shown in Table 7.1.1.

Table 7.1.1 Differences due to selected duty

Duty	Common terminal in use	Maximum dot number	Frame frequency *
1/16	COM0–15	640 dots	32 Hz
1/8	COM0–7	320 dots	32 Hz

* Frame frequency = f_{OSC1}/1,024

Figure 7.1.1 shows the drive waveform for 1/16 duty (1/5 bias), and Figure 7.1.2 shows the drive waveform for 1/8 duty (1/4 bias).

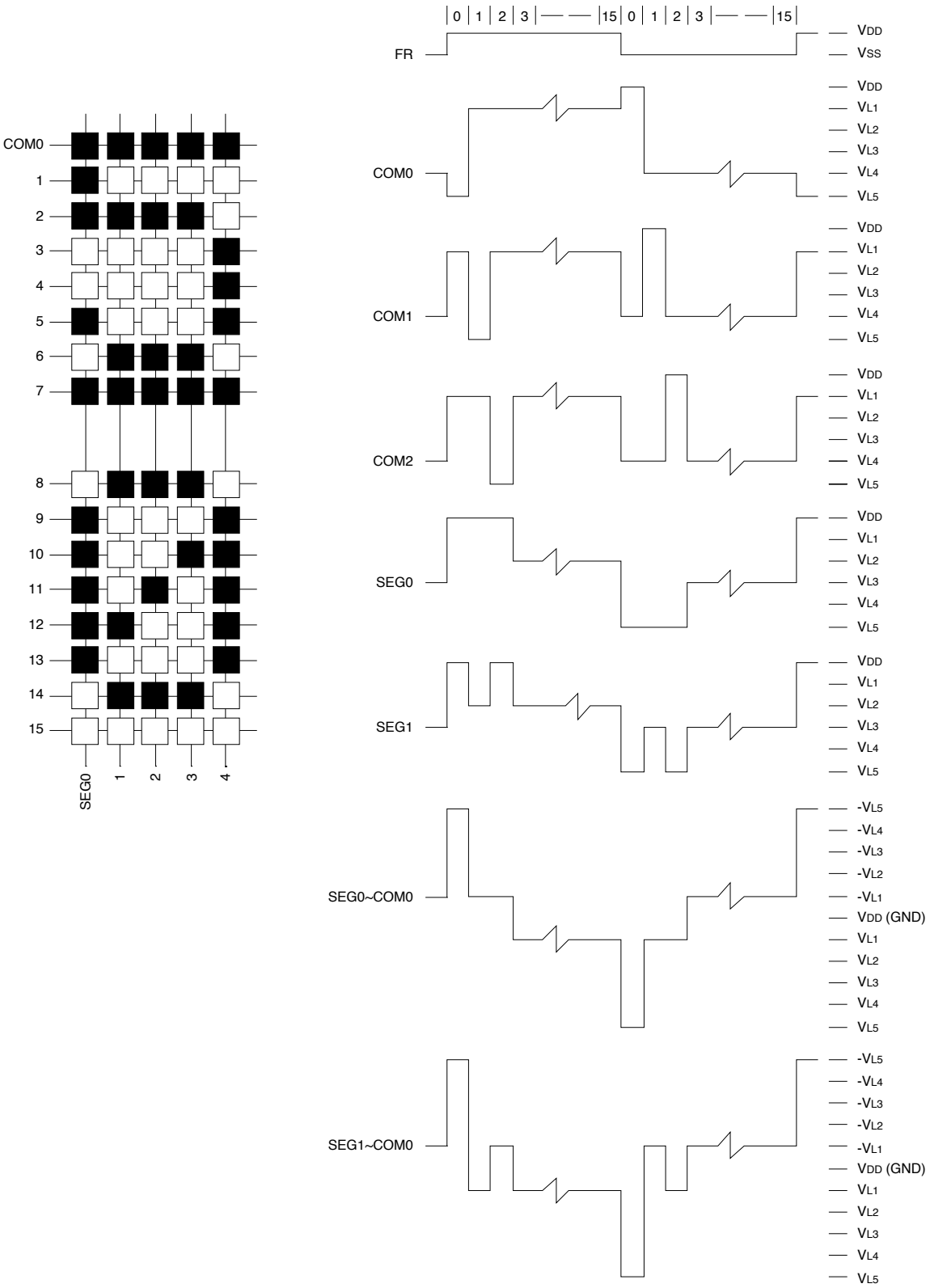


Fig. 7.1.1 Drive waveform for 1/16 duty (1/5 bias)

Note: 1/5 bias may only be utilized when power for LCD driving is supplied externally; when internal power circuit is used, 1/4 bias is utilized.

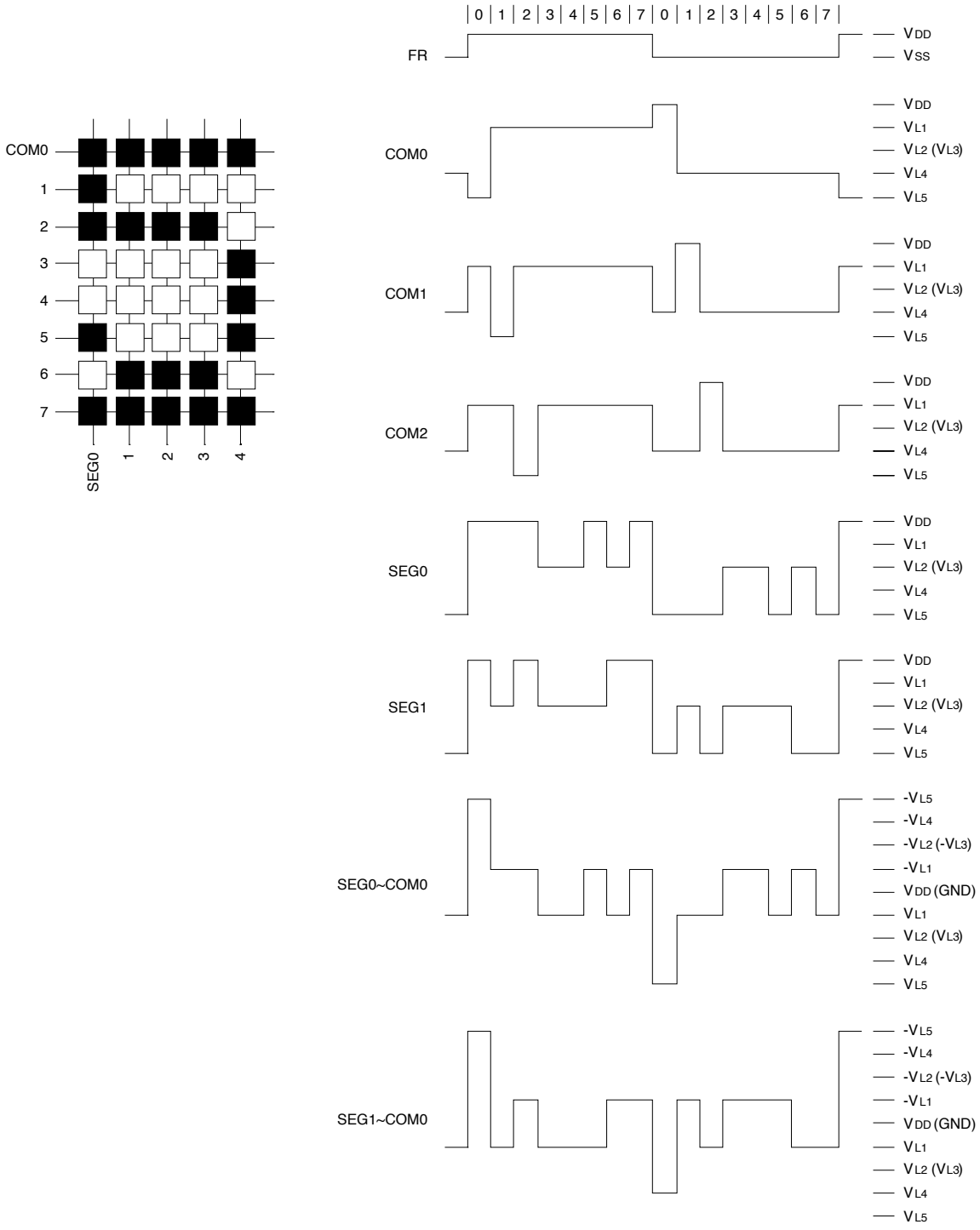


Fig. 7.1.2 Drive waveform for 1/8 duty (1/4 bias)

7.2 Mask Option

Disconnecting the internal power for LCD driving will enable electric potentials to be supplied externally. In such case, the 5 electric potentials are entered in V_{L1}, V_{L2}, V_{L3}, V_{L4} and V_{L5} terminals and 1/5 bias driving may then be set. Since 1/5 bias driving provides better display quality, when low power current consumption is not required (i.e., when power is supplied from AC outlet), select external power mode. However, note that in order to maintain a stable display, power source must be one which will remain stable even when heavy load such as buzzer, etc. is driven.
Moreover, in the external power mode, the contrast adjustment function cannot be used. Accommodate this limitation by utilizing the external circuit as necessary.

A sample circuit of external power for LCD driving when power is supplied externally is shown in Figure 7.2.1.

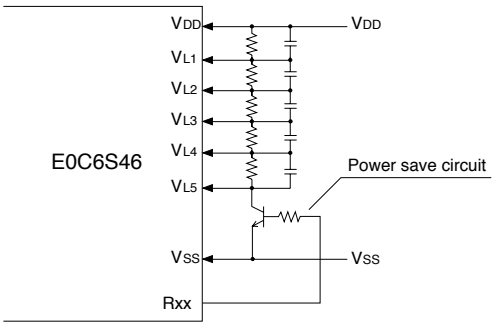


Fig. 7.2.1 Sample circuit of external power for LCD driving when power is supplied externally

7.3 Display Data Memory

The display data memory of the E0C6S46 is allocated to the built-in RAM addresses E00H–E4FH and E80H–ECFH.
Figure 7.3.1 shows the correspondence between the display data memory and the LCD dot matrix.

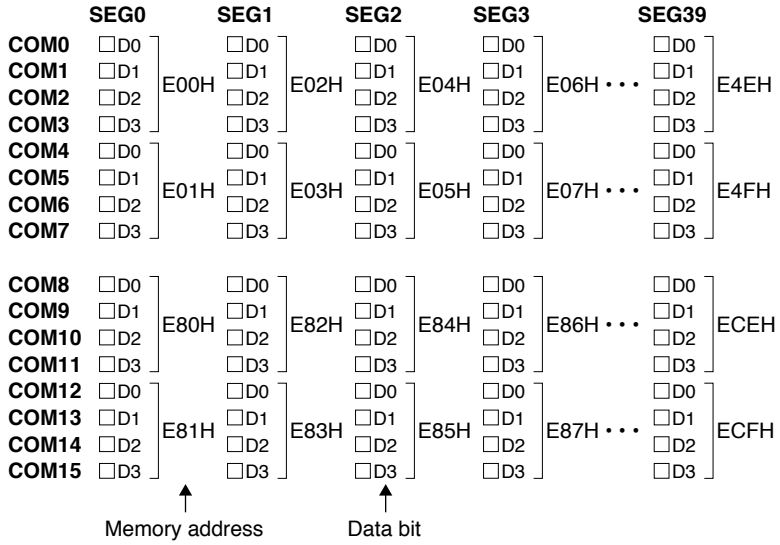


Fig. 7.3.1 LCD dot matrix and segment memory correspondence

When the segment memory bit is assigned as "1", the corresponding LCD dot lights up, and when assigned as "0", the dot dies out. At 1/16 duty drive and 1/8 duty drive, COM0 to COM15 lines and COM0 to COM7 lines light up, respectively.
At initial reset, the display data memory content becomes undefined and hence, there is need to initialize by software.

7.4 Control of LCD Driver

The control registers for the LCD driver are explained below.

Table 7.4.1 Control registers of LCD driver

Address	Register D3	D2	D1	D0	Name	Init	1	0	Comment
F71H	ALOFF	ALON	LDUTY	HLMOD	ALOFF	1	All off	Normal	All LCD dots fade out control
					ALON	0	All on	Normal	All LCD dots displayed control
	R/W				LDUTY	0	1/8	1/16	LCD drive duty switch
					HLMOD	0	HLMOD	Normal	Heavy load protection mode
F72H	LC3	LC2	LC1	LC0	LC3	X			LCD contrast adjustment LC3–LC0 = 0 light : LC3–LC0 = 15 dark
	R/W				LC2	X			
					LC1	X			
					LC0	X			

LDUTY (F71H [D1], R/W)

Sets the LCD drive duty.

When "1" is written: 1/8 duty
When "0" is written: 1/16 duty
Reading: Valid

Writing "1" or "0" on LDUTY will set is to 1/8 duty or 1/16 duty, respectively.
At initial reset, LDUTY is set at "0".

ALON (F71H [D2], R/W)

Displays the all LCD dots on.

When "1" is written: All LCD dots displayed
When "0" is written: Normal operation
Reading: Valid

Writing "1" to ALON will display all the LCD dots on; writing "0" will set the LCD display back to normal. LCD panel testing may be conducted with this function.
Total LCD displaying at ALON = "1" is a static operation and does not affect the content of the display data memory.
ALON precedes ALOFF.
At initial reset, ALON is set at "0".

ALOFF (F71H [D3], R/W)

Fade outs the all LCD dots.

When "1" is written: All LCD dots fade out
When "0" is written: Normal operation
Reading: Valid

When "1" is written on ALOFF, all LCD dots will fade out; writing "0" will set it back to normal.
All fading out of LCD at ALOFF = "1" is due to light out signals and does not affect the content of the display data memory.
Flashing of the entire LCD panel is performed by this function.
At initial reset, ALOFF is set to "1".

LC0, LC1, LC2, LC3 (F72H, R/W)
Will adjust the LCD contrast.
Contrast may be adjusted to 16 levels as shown in Table 7.4.2.

Table 7.4.2 LCD contrast

	LC3	LC2	LC1	LC0	Contrast
0	0	0	0	0	light
1	0	0	0	1	↑
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
A	1	0	1	0	
B	1	0	1	1	
C	1	1	0	0	
D	1	1	0	1	
E	1	1	1	0	↓
F	1	1	1	1	dark

At room temperature, use setting number 7 or 8 as standard.
The voltage of the LCD system power terminals V_{L1}, V_{L2}, V_{L4} and V_{L5} changes through this function (only when the voltage is generated by the internal power supply circuit).
Because at initial reset, the contents of LC0–LC3 are undefined, initialize it by the software.

7.5 Programming Note

Because at initial reset, the contents of display data memory and LC0–LC3 are undefined, there is need to initialize by software.

CHAPTER 8 TIMERS

8.1 Clock Timer

8.1.1 Configuration of clock timer

The E0C6S46 has a clock timer with OSC1 (crystal oscillation) as basic oscillation built-in. The clock timer is configured with an 8 bits binary counter with 256 Hz signal divided from OSC1 as input clock, allowing 128 Hz–1 Hz of data to be read by the software. Figure 8.1.1.1 shows the configuration of the clock timer.

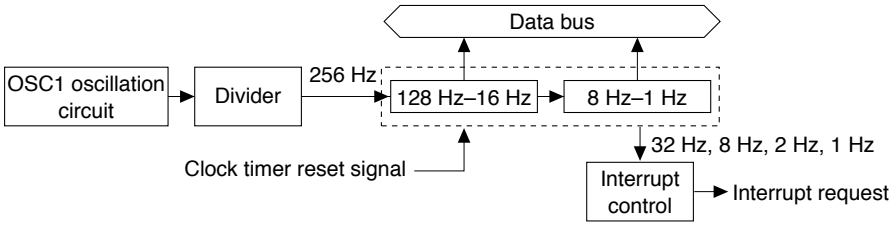


Fig. 8.1.1.1 Configuration of clock timer

8.1.2 Interrupt function

The clock timer has interrupt capability, and interrupt is generated by the falling edge of 32 Hz, 8 Hz, 2 Hz, and 1 Hz signals.
Figure 8.1.2.1 shows the timing chart of the clock timer.

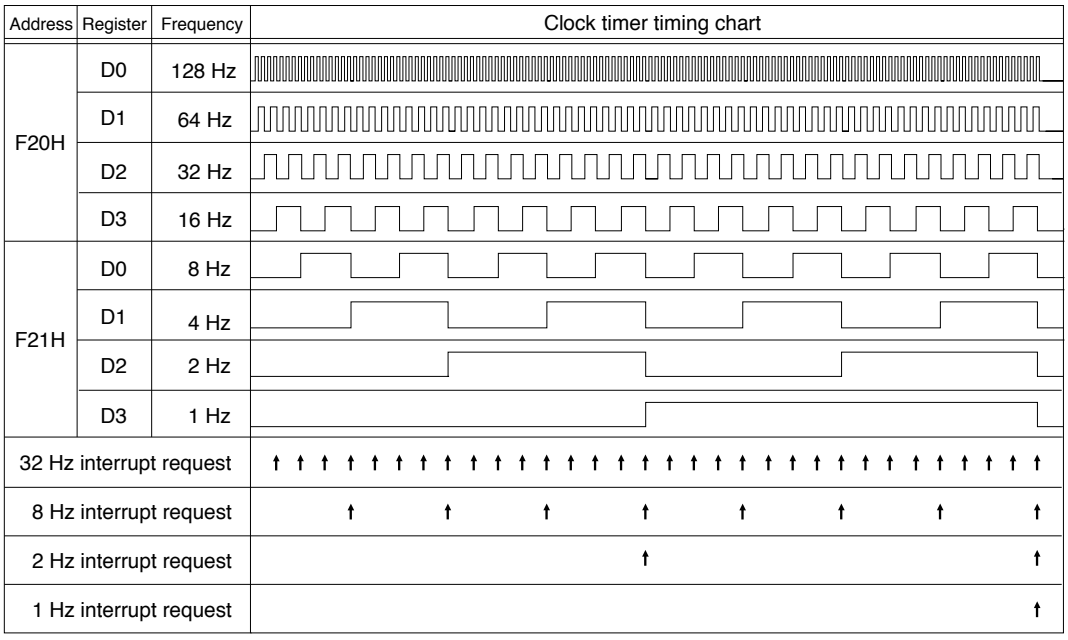


Fig. 8.1.2.1 Timing chart of clock timer

The clock timer interrupt is generated at the falling edge of the frequencies (32 Hz, 8 Hz, 2 Hz, and 1 Hz). At this time, the corresponding interrupt factor flag (IT32, IT8, IT2, and IT1) is set to "1". Selection of whether to mask the separate interrupts can be made with the interrupt mask registers (EIT32, EIT8, EIT2, and EIT1). However, regardless of the interrupt mask register setting, the interrupt factor flag is set to "1" at the falling edge of the corresponding signal.

8.1.3 Control of clock timer

The control registers for the clock timer are explained below.

Table 8.1.3.1 Control registers of clock timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
F00H	IT1	IT2	IT8	IT32	IT1	0	Yes	No	Interrupt factor flag (clock timer 1 Hz)
					IT2	0	Yes	No	Interrupt factor flag (clock timer 2 Hz)
	R				IT8	0	Yes	No	Interrupt factor flag (clock timer 8 Hz)
					IT32	0	Yes	No	Interrupt factor flag (clock timer 32 Hz)
F10H	EIT1	EIT2	EIT8	EIT32	EIT1	0	Enable	Mask	Interrupt mask register (clock timer 1 Hz)
					EIT2	0	Enable	Mask	Interrupt mask register (clock timer 2 Hz)
	R/W				EIT8	0	Enable	Mask	Interrupt mask register (clock timer 8 Hz)
					EIT32	0	Enable	Mask	Interrupt mask register (clock timer 32 Hz)
F20H	TM3	TM2	TM1	TM0	TM3	0			Clock timer data (16 Hz)
					TM2	0			Clock timer data (32 Hz)
	R				TM1	0			Clock timer data (64 Hz)
					TM0	0			Clock timer data (128 Hz)
F21H	TM7	TM6	TM5	TM4	TM7	0			Clock timer data (1 Hz)
					TM6	0			Clock timer data (2 Hz)
	R				TM5	0			Clock timer data (4 Hz)
					TM4	0			Clock timer data (8 Hz)
F76H	0	0	TMRST	WDRST	0	–			
					0	–			
	R		W		TMRST	Reset	Reset	–	Clock timer reset
					WDRST	Reset	Reset	–	Watchdog timer reset

TMRST (F76H [D1], W)

This bit resets the clock timer.

When "1" is written: Clock timer reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" on TMRST, the clock timer is reset and all timer data are set to "0".
Because this bit is only for writing, it is always "0" during reading.

TM0–TM7 (F20H, F21H, R)

Will read the data of the clock timer.
TMx (x = 0–7) and frequency correspondence are as follows:

F20H	F21H
TM0 (D0): 128 Hz	TM4 (D0): 8 Hz
TM1 (D1): 64 Hz	TM5 (D1): 4 Hz
TM2 (D2): 32 Hz	TM6 (D2): 2 Hz
TM3 (D3): 16 Hz	TM7 (D3): 1 Hz

The above 8 bits are only for reading and render writing operation invalid.
At initial reset, timer data is initialized to "0".

EIT32, EIT8, EIT2, EIT1 (F10H, R/W)

There are the interrupt mask registers of the clock timer.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

EIT32, EIT8, EIT2, and EIT1 correspond to 32 Hz, 8 Hz, 2 Hz, and 1 Hz timer interrupts, respectively.
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI).
Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, these registers are all set to "0" (mask).

IT32, IT8, IT2, IT1 (F00H, R)

There are the interrupt factor flags of the clock timer.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

IT32, IT8, IT2, and IT1 correspond to 32 Hz, 8 Hz, 2 Hz, and 1 Hz timer interrupts, respectively.
The occurrence of clock timer interrupt can be determined by the software through these flags. However, regardless of interrupt masking, these flags are set to "1" due to the falling edge of the corresponding signal.
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, these flags are set to "0".

8.1.4 Programming notes

(1) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(2) Because the watchdog timer counts up during reset as in the above (1), reset the watchdog timer as necessary.

(3) When the low-order digits (TM0–TM3) and high-order digits (TM4–TM7) are consecutively read, proper reading may not be obtained due to the carry from the low-order digits into the high-order digits (when the reading of the low-order digits and high-order digits span the timing of the carry). For this reason, perform multiple reading of timer data, make comparisons and use matching data as result.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

8.2 Stopwatch Timer

8.2.1 Configuration of stopwatch timer

The E0C6S46 has 1/100 sec unit (SWL) and 1/10 sec unit (SWH) stopwatch timer built-in. The stopwatch timer is configured with a 2 levels 4 bits BCD counter which has an input clock approximating 100 Hz signal (signal divided from OSC1 to the closest 100 Hz) and data can be read in units of 4 bits by software.
Figure 8.2.1.1 shows the configuration of the stopwatch timer.

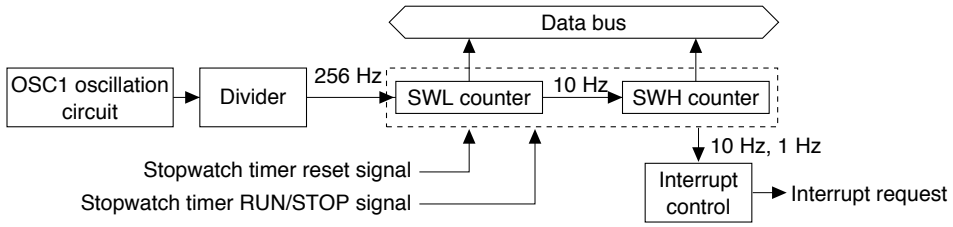


Fig. 8.2.1.1 Configuration of stopwatch timer

The stopwatch timer can be used as a separate timer from the clock timer. In particular, digital watch stopwatch functions can be realized easily with software.

8.2.2 Count-up pattern

The stopwatch timer is configured of 4 bits BCD counters SWL and SWH.
The counter SWL, at the stage preceding the stopwatch timer, has an approximated 100 Hz signal for the input clock. It counts up every 1/100 sec, and generates an approximated 10 Hz signal. The counter SWH has an approximated 10 Hz signal generated by the counter SWL for the input clock. In count-up every 1/10 sec, and generated 1 Hz signal.
Figure 8.2.2.1 shows the count-up pattern of the stopwatch timer.

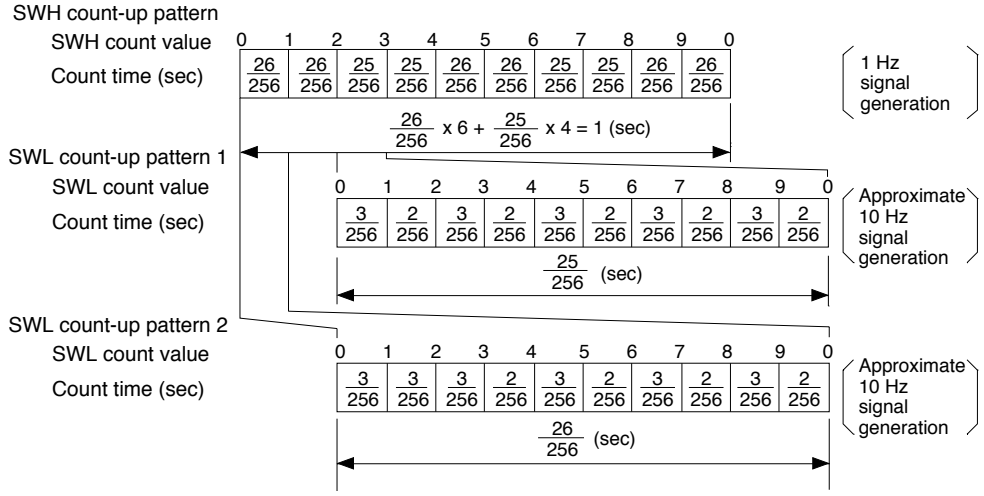


Fig. 8.2.2.1 Count-up pattern of stopwatch timer

SWL generates an approximated 10 Hz signal from the basic 256 Hz signal. The count-up intervals are 2/256 sec and 3/256 sec, so that finally two patterns are generated: 25/256 sec and 26/256 sec intervals. Consequently, these patterns do not amount to an accurate 1/100 sec.
SWH counts the approximated 10 Hz signals generated by the 25/256 sec and 26/256 sec intervals in the ratio of 4 : 6, to generate a 1 Hz signal. The count-up intervals are 25/256 sec and 26/256 sec, which do not amount to an accurate 1/10 sec.

8.2.3 Interrupt function

Stopwatch timers SWL and SWH, through their respective overflows, can generate 10 Hz (approximate 10 Hz) and 1 Hz interrupts.
Figure 8.2.3.1 shows the timing chart for the stopwatch timer.

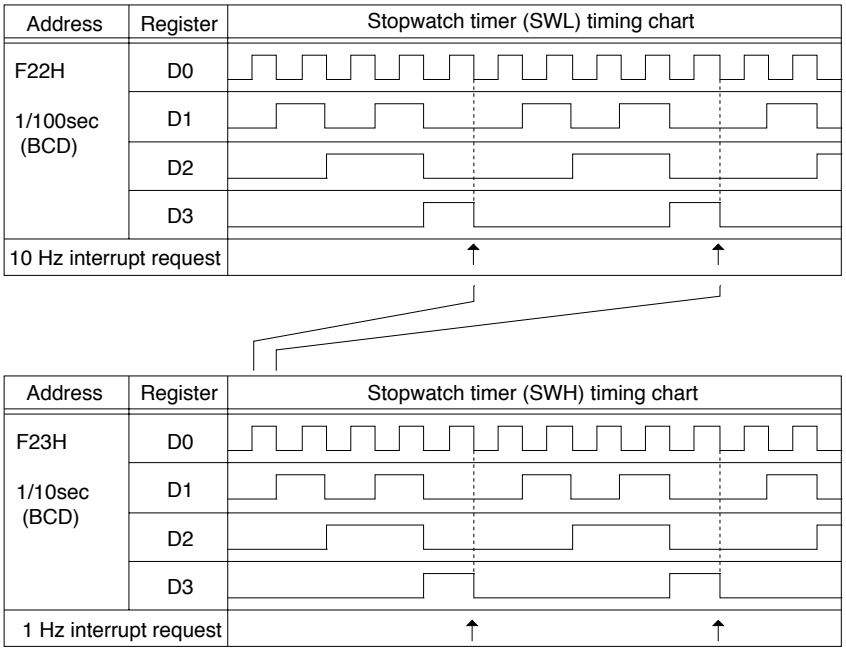


Fig. 8.2.3.1 Timing chart for stopwatch timer

The stopwatch interrupts are generated by the overflow of their respective counters SWL and SWH (changing "9" to "0"). At this time, the corresponding interrupt factor flags (ISW0 and ISW1) are set to "1". The respective interrupts can be masked separately through the interrupt mask registers (EISW0 and EISW1). However, regardless of the setting of the interrupt mask registers, the interrupt factor flags are set to "1" by the overflow of their corresponding counters.

8.2.4 Control of stopwatch timer

The control registers for the stopwatch timer are explained below.

Table 8.2.4.1 Control registers of stopwatch timer

Address	Register								Comment
	D3	D2	D1	D0	Name	Init	1	0	
F01H	0	0	ISW1	ISW0	0	–			
					0	–			
	R				ISW1	0		No	Interrupt factor flag (stopwatch 1 Hz)
					ISW0	0		No	Interrupt factor flag (stopwatch 10 Hz)
F11H	0	0	EISW1	EISW0	0	–			
					0	–			
	R		R/W		EISW1	0	Enable	Mask	Interrupt mask register (stopwatch 1 Hz)
					EISW0	0	Enable	Mask	Interrupt mask register (stopwatch 10 Hz)
F22H	SWL3	SWL2	SWL1	SWL0	SWL3	0			MSB
					SWL2	0			Stopwatch timer
	R				SWL1	0			1/100 sec data (BCD)
					SWL0	0			LSB
F23H	SWH3	SWH2	SWH1	SWH0	SWH3	0			MSB
					SWH2	0			Stopwatch timer
	R				SWH1	0			1/10 sec data (BCD)
					SWH0	0			LSB
F77H	0	0	SWRST	SWRUN	0	–			
					0	–			
	R		W	R/W	SWRST	Reset	Reset	–	Stopwatch timer reset
					SWRUN	0	Run	Stop	Stopwatch timer Run/Stop

SWRST (F77H [D1], W)

This bit resets the stopwatch timer.

When "1" is written: Stopwatch timer reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" on SWRST, the stopwatch timer is reset. All timer data is set to "0".
When the stopwatch timer is reset in the RUN mode, it will re-start counting immediately after the reset and at STOP mode, the reset data is maintained.
Because this bit is for writing only, it is always "0" during reading.

SWRUN (F77H [D0], R/W)

This register controls RUN/STOP of the stopwatch timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

By writing "1" on SWRUN, the stopwatch timer performs counting operation. Writing "0" will make the stopwatch stop counting.
Even if the stopwatch is stopped, the timer data at that point is kept.
When data of the counter is read at run mode, proper reading may not be obtained due to the carry from low-order digits (SWL) into high-order digits (SWH) (i.e., in case SWL and SWH reading span the timing of the carry). To avoid this occurrence, perform the reading after suspending the counter once and then set the SWRUN to "1" again.
Moreover, it is required that the suspension period not exceed 976 μs (1/4 cycle of 256 Hz).
At initial reset, SWRUN is set to "0".

SWL0–SWL3 (F22H, R)
Will read the stopwatch timer data to the 1/100 sec digits (BCD).
Since these bits are for reading only, writing operation is invalidated.
At initial reset, timer data is set to "0".

SWH0–SWH3 (F23H, R)
Will read the stopwatch timer data to the 1/10 sec digits (BCD).
Since these bits are for reading only, writing operation is invalidated.
At initial reset, timer data is set to "0".

EISW0, EISW1 (F11H [D0, D1], R/W)
There are the interrupt mask registers of the stopwatch timer.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

EISW0 and EISW1 correspond to 10 Hz and 1 Hz stopwatch timer interrupts, respectively.
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, these registers are all set to "0" (mask).

ISW0, ISW1 (F01H [D0, D1], R)
There are the interrupt factor flags of the stopwatch timer.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

ISW0 and ISW1 correspond to 10 Hz and 1 Hz stopwatch timer interrupts, respectively.
The occurrence of stopwatch timer interrupt can be determined by the software through these flags. However, regardless of interrupt masking, these flags are set to "1" by the overflow of the corresponding counters.
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, these flags are set to "0".

8.2.5 Programming notes

(1) When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 μs (1/4 cycle of 256 Hz).

(2) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(3) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

8.3 Programmable Timer

8.3.1 Configuration of programmable timer

The E0C6S46 has a programmable timer with OSC1 (crystal oscillation) as basic oscillation built-in. The programmable timer is configured with an 8 bits pre-settable down counter and it has been down-count at initial value by 256 Hz–8,192 Hz signal or by the input signal of input port K03.
The initial value of count data can be set by software to the reload register; at the point where the down-counter value is "0", the programmable timer reloads the initial value and continues to down-count.
The down-counter data may be read through the software. Moreover, the input clock being selected may be generated to output port R33.
Figure 8.3.1.1 shows the configuration of the programmable timer.

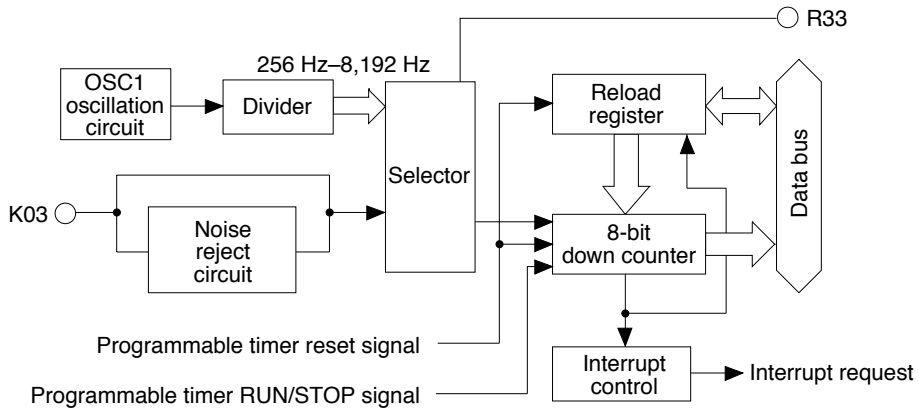


Fig. 8.3.1.1 Configuration of programmable timer

One input clock may be selected by software from any of the following 8 types:

(1) K03 input (with noise rejector)
(2) K03 input (direct)
(3) 256 Hz
(4) 512 Hz
(5) 1,024 Hz
(6) 2,048 Hz
(7) 4,096 Hz
(8) 8,192 Hz

Note, however, that down-count is done at falling edges of the input signal as shown in Figure 8.3.1.2.

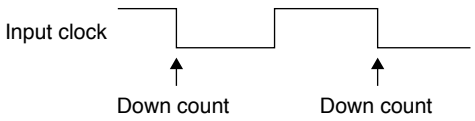


Fig. 8.3.1.2 Timing of down-counts

Type (1) K03 input (with noise rejector) is for counting by key entry, the input signal from which passes the 256 Hz sampling noise reject circuit. With this, no more than 2 ms of chattering is purged, and at least 4 ms signal is received.

8.3.2 Interrupt function

The programmable timer generates interrupt after the down-count from the initial setting is completed and the content of the down-counter indicates 00H.
After interrupt generation, the programmable timer reloads the initial count value into the down-counter and resumes counting.
Figure 8.3.2.1 shows the timing chart of the programmable timer.

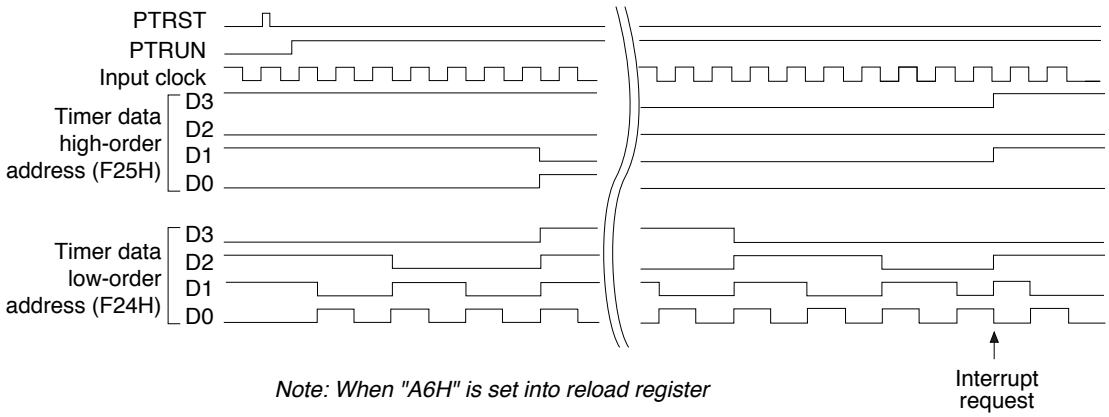


Fig. 8.3.2.1 Timing chart of programmable timer

When the down-counter values PT0–PT7 have become 00H the interrupt factor flag IPT is set to "1" and an interrupt is generated. The interrupt can be masked through the interrupt mask register EIPT. However, regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" when the down-counter equals 00H.

8.3.3 Control of programmable timer

The control registers for the programmable timer are explained below.

Table 8.3.3.1 Control registers of programmable timer

Address	Register D3	D2	D1	D0	Name	Init	1	0	Comment
F02H	0	0	0	IPT	0	–			
					0	–			
	R				0	–			
					IPT	0	Yes	No	Interrupt factor flag (programmable timer)
F12H	0	0	0	EIPT	0	–			
					0	–			
	R			R/W	0	–			
					EIPT	0	Enable	Mask	Interrupt mask register (programmble timer)
F24H	PT3	PT2	PT1	PT0	PT3	X			MSB
					PT2	X			Programmable timer data (low-order)
	R				PT1	X			
					PT0	X			LSB
F25H	PT7	PT6	PT5	PT4	PT7	X			MSB
					PT6	X			Programmable timer data (high-order)
	R				PT5	X			
					PT4	X			LSB
F26H	RD3	RD2	RD1	RD0	RD3	X			MSB
					RD2	X			Programmable timer
	R/W				RD1	X			reload data (low-order)
					RD0	X			LSB
F27H	RD7	RD6	RD5	RD4	RD7	X			MSB
					RD6	X			Programmable timer
	R/W				RD5	X			reload data (high-order)
					RD4	X			LSB
F78H	0	0	PTRST	PTRUN	0	–			
					0	–			
	R		W	R/W	PTRST	Reset	Reset	–	Programmable timer reset
					PTRUN	0	Run	Stop	Programmable timer Run/Stop
F79H	PTCOUT	PTC2	PTC1	PTC0	PTCOUT	0	On	Off	Programmable timer clock output
					PTC2	0			
	R/W				PTC1	0			Programmable timer input clock selection
					PTC0	0			

PTC0, PTC1, PTC2 (F79H [D0–D2], R/W)

Selects the input clock.

The PTC0–PTC2 setting and input clock correspondence is shown in Table 8.3.3.2.

Table 8.3.3.2 Input clock setting

PTC2	PTC1	PTC0	Input clock
0	0	0	K03 input (with noise rejector)
0	0	1	K03 input (direct)
0	1	0	256 Hz
0	1	1	512 Hz
1	0	0	1,024 Hz
1	0	1	2,048 Hz
1	1	0	4,096 Hz
1	1	1	8,192 Hz

PTCOUT (F79H [D3], R/W)

Generates the input clock being selected to output port R33.

Refer to Section 6.2, "Output Port" regarding control methods.

RD0–RD3, RD4–RD7 (F26H, F27H, R/W)

These are reload registers for setting the initial value of the timer.
Sets the low-order 4 bits of the 8 bits timer data to RD0–RD3, and the high-order 4 bits to RD4–RD7.
The set timer data is loaded to the down-counter when the programmable timer is reset or when the content of the down-counter is 00H.
When data of reload registers is set at "00H", the down-counter becomes a 256-value counter.
At initial reset, this register will be undefined.

PTRST (F78H [D1], W)

This bit resets the programmable timer.

When "1" is written: Programmable timer reset
When "0" is written: No operation
Reading: Always "0"

By writing "1" on PTRST, the programmable timer is reset.
The contents set in RD0–RD7 are loaded into the down-counter.
When the programmable timer is reset in the RUN mode, it will re-start counting immediately after loading and at STOP mode, the load data is maintained.
Because this bit is only for writing, it is always "0" during reading.

PTRUN (F78H [D0], R/W)

This register controls RUN/STOP of the programmable timer.

When "1" is written: RUN
When "0" is written: STOP
Reading: Valid

By writing "1" on PTRUN, the programmable timer performs counting operation. Writing "0" will make the programmable timer stop counting.
Even if the programmable timer is stopped, the timer data at that point is kept.
When data of the counter is read at the RUN mode, proper reading may not be obtained due to the carry from the low-order digits (PT0–PT3) into the high-order digits (PT4–PT7) (when the reading of the low-order digits and high-order digits span the timing of the carry). To avoid this occurrence, perform the reading after suspending the programmable timer once, and set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty).
At initial reset, PTRUN is set to "0".

PT0–PT3, PT4–PT7 (F24H, F25H, R)

Will read the data from the down-counter of the programmable timer.
Will read the low-order 4 bits of the 8 bits counter data PT0–PT3, and the high-order 4 bits PT4–PT7.
Because these 8 bits are only for reading, writing operation is rendered invalid.
At initial reset, timer data will be undefined.

EIPT (F12H [D0], R/W)

This is the interrupt mask register of the programmable timer.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI).
Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, this register is set to "0" (mask).

IPT (F02H [D0], R)

This is the interrupt factor flag of the programmable timer.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

From the status of this flag, the software can decide whether the programmable timer interrupt. Note, however, that even if the interrupt is masked, this flag will be set to "1" by the counter value will become "00H".
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, this flag is set to "0".

8.3.4 Programming notes

(1) When initiating programmable timer count, perform programming by the following steps:

1. Set the initial data to RD0–RD7.
2. Reset the programmable timer by writing "1" to PTRST.
3. Start the down-count by writing "1" to PTRUN.

(2) When the reload register (RD0–RD7) value is set at "00H", the down-counter becomes a 256-value counter.

(3) When data of the timer is read consecutively in 8 bits in the RUN mode, perform the reading after suspending the timer once and then set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty). Accordingly, when the input clock is a fast clock faster than a 256 Hz, high speed processing by OSC3 is required.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

CHAPTER 9 SERIAL INTERFACE

9.1 Configuration of Serial Interface

The E0C6S46 has a synchronous clock type 8 bits serial interface built-in.
The configuration of the serial interface is shown in Figure 9.1.1.
The CPU, via the 8 bits shift register, can read the serial input data from the SIN terminal. Moreover, via the same 8 bits shift register, it can convert parallel data to serial data and output it to the SOUT terminal.
The synchronous clock for serial data input/output may be set by selecting by software any one of 3 types of master mode (internal clock mode: when the E0C6S46 is to be the master for serial input/output) and a type of slave mode (external clock mode: when the E0C6S46 is to be the slave for serial input/output).
Also, when the serial interface is used at slave mode, $\overline{\text{SRDY}}$ (SIO READY) signal which indicates whether or not the serial interface is available to transmit or receive can be output to output port R33 by mask option.

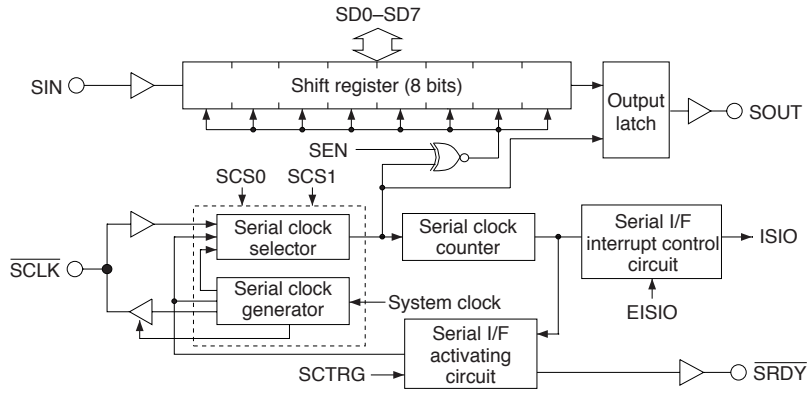


Fig. 9.1.1 Configuration of serial interface

9.2 Mask Option

The serial interface may be selected for the following by mask option.

(1) Whether or not the SIN terminal will use built-in pull up resistor may be selected.
If the use of no pull up resistor is selected, take care that floating state does not occur at the SIN terminal.

(2) Either complementary output or N channel (Nch) open drain as output specification for the SOUT terminal may be selected.
However, even if Nch open drain has been selected, application of voltage exceeding power source voltage to the SOUT terminal will be prohibited.

(3) Whether or not the $\overline{\text{SCLK}}$ terminal will use pull up resistor which is turned ON during input mode (external clock) may be selected. If the use of no pull up resistor is selected, take care that floating state does not occur at the $\overline{\text{SCLK}}$ terminal during input mode.
Normally, the use of pull up resistor should be selected.

(4) As output specification during output mode, either complementary output or N channel (Nch) open drain output may be selected for the $\overline{\text{SCLK}}$ terminal. However, even if the same Nch open drain as that of the SOUT terminal is selected, application of voltage exceeding the power current voltage is not permitted.

(5) LSB first or MSB first as input/output permutation of serial data may be selected.

(6) Output port R33 may be assigned as $\overline{\text{SRDY}}$ output terminal which will indicate whether the serial interface is available to transmit or receive signals.

9.3 Master Mode and Slave Mode of Serial Interface

The serial interface of the E0C6S46 has two types of operation mode: master mode and slave mode.
In the master mode, it uses an internal clock as synchronous clock of the built-in shift register, generates this internal clock at the $\overline{SCLK}$ terminal and controls the external (slave side) serial interface.
In the slave mode, the synchronous clock output from the external (master side) serial device is input from the $\overline{SCLK}$ terminal and uses it as the synchronous clock to the built- in shift register.
The master mode and slave mode are selected through registers SCS0 and SCS1; when the master mode is selected, a synchronous clock may be selected from among 3 types as shown in Table 9.3.1.

Table 9.3.1 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	CLK
1	0		CLK/2
0	1		CLK/4
0	0	Slave mode	External clock

CLK : CPU system clock

At initial reset, the slave mode (external clock mode) is selected.
Moreover, the synchronous clock, along with the input/output of the 8 bits serial data, is controlled as follows:

- At master mode, after output of 8 clocks from the $\overline{SCLK}$ terminal, clock output is automatically suspended and $\overline{SCLK}$ terminal is fixed at high level.
- At slave mode, after input of 8 clocks to the $\overline{SCLK}$ terminal, subsequent clock inputs are masked.

Note: When using the serial interface in the master mode, CPU system clock is used as the synchronous clock. Accordingly, when the serial interface is operating, system clock switching ($f_{OSC1} \leftrightarrow f_{OSC3}$) should not be performed.

A sample basic serial input/output portion connection is shown in Figure 9.3.1.

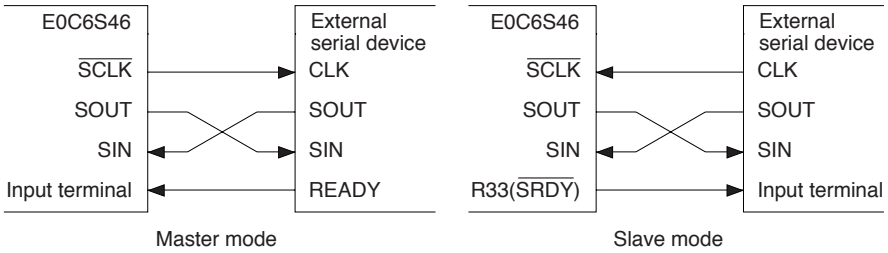


Fig. 9.3.1 Sample basic connection of serial input/output section

9.4 Data Input/Output and Interrupt Function

The serial interface of E0C6S46 can input/output data via the internal 8 bits shift register. The shift register operates by synchronizing with either the synchronous clock output from $\overline{SCLK}$ terminal (master mode), or the synchronous clock input to $\overline{SCLK}$ (slave mode).
The serial interface generates interrupt on completion of the 8 bits serial data input/output. Detection of serial data input/output is done by the counting of the synchronous clock ($\overline{SCLK}$); the clock completes input/output operation when 8 counts (equivalent to 8 cycles) have been made and then generates interrupt.
The serial data input/output procedure data is explained below:

(1) Serial data output procedure

The E0C6S46 serial interface is capable of outputting parallel data as serial data, in units of 8 bits. By setting the parallel data to data registers SD0–SD3 and SD4–SD7 individually and writing "1" to SCTRG (F7AH [D3]), it synchronizes with the synchronous clock and serial data is output at the SOUT terminal. The synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{\text{SCLK}}$ terminal while in the slave mode, external clock which is input from the $\overline{\text{SCLK}}$ terminal. The serial output of the SOUT terminal changes with the falling edge of the clock that is input or output from the $\overline{\text{SCLK}}$ terminal.

When the output of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after output of the 8 bits data.

(2) Serial data input procedure

The E0C6S46 serial interface is capable of inputting serial data as parallel data, in units of 8 bits. By writing "1" to SCTRG, the serial data is input from the SIN terminal, synchronizes with the synchronous clock, and is sequentially read in the 8 bits shift register. As in the above item (1), the synchronous clock used here is as follows: in the master mode, internal clock which is output to the $\overline{\text{SCLK}}$ terminal while in the slave mode, external clock which is input from the $\overline{\text{SCLK}}$ terminal. The serial data to the built-in shift register is read with the falling edge of the $\overline{\text{SCLK}}$ signal when SEN bit is "1" and is read with the rising edge of the $\overline{\text{SCLK}}$ signal when SEN bit is "0". Moreover, the shift register is sequentially shifted as the data is fetched.

When the input of the 8 bits data from SD0 to SD7 is completed, the interrupt factor flag ISIO is set to "1" and interrupt is generated. Moreover, the interrupt can be masked by the interrupt mask register EISIO. Note, however, that regardless of the setting of the interrupt mask register, the interrupt factor flag is set to "1" after input of the 8 bits data.

Also, the data input in the shift register can be read from data registers SD0–SD7 by software.

(3) Serial data input/output permutation

The E0C6S46 allow the input/output permutation of serial data to be selected by mask option as to either LSB first or MSB first. The block diagram showing input/output permutation in case of LSB first and MSB first is provided in Figure 9.4.1.

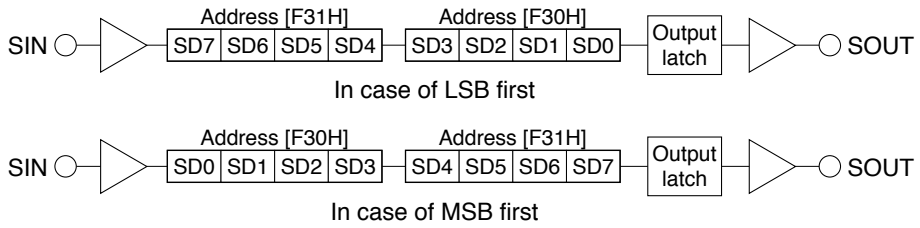


Fig. 9.4.1 Serial data input/output permutation

(4) $\overline{\text{SRDY}}$ signal

When the E0C6S46 serial interface is used in the slave mode (external clock mode), $\overline{\text{SRDY}}$ is used to indicate whether the internal serial interface is available to transmit or receive data for the master side (external) serial device. $\overline{\text{SRDY}}$ signal is generated from output port R33 by mask option.
$\overline{\text{SRDY}}$ signal becomes "0" (low) when the E0C6S46 serial interface becomes available to transmit or receive data; normally, it is at "1" (high).
$\overline{\text{SRDY}}$ signal changes from "1" to "0" immediately after "1" is written to SCTRG and returns from "0" to "1" when "0" is input to $\overline{\text{SCLK}}$ terminal (i.e., when the serial input/output begins transmitting or receiving data).
Moreover, when data is read from or written to SD4–SD7, the $\overline{\text{SRDY}}$ signal returns to "1".
The operating state (wait state or transmitting/receiving state) of the serial interface may be checked by connecting output port R33 ($\overline{\text{SRDY}}$) to input port (Kxx) or I/O port (Pxx) and performing reading.

(5) Timing chart

The E0C6S46 serial interface timing chart is shown in Figure 9.4.2.

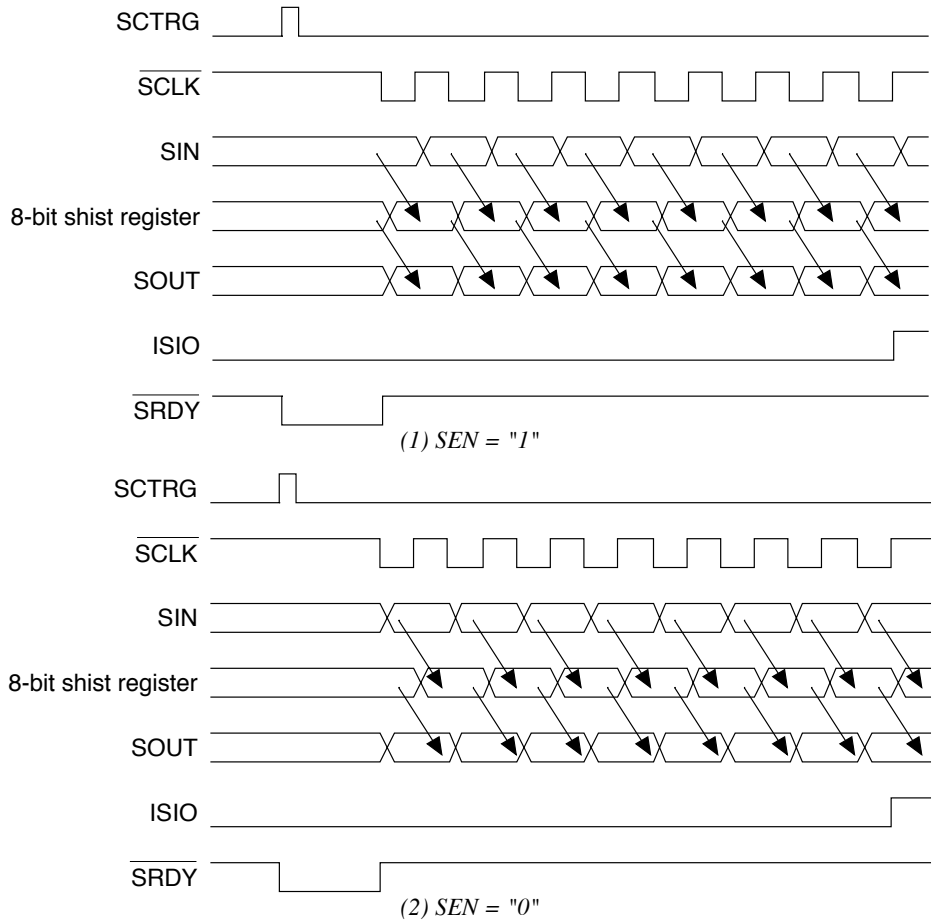


Fig. 9.4.2 Serial interface timing chart

9.5 Control of Serial Interface

The control registers for the serial interface are explained below.

Table 9.5.1 Control registers of serial interface

Address	Register D3	D2	D1	D0	Name	Init	1	0	Comment
F03H	0	0	0	ISIO	0	–			
					0	–			
					0	–			
	R				ISIO	0	Yes	No	Interrupt factor flag (serial interface)
F13H	0	0	0	EISIO	0	–			
					0	–			
	R			R/W	0	–			
					EISIO	0	Enable	Mask	Interrupt mask register (serial interface)
F30H	SD3	SD2	SD1	SD0	SD3	X			MSB
					SD2	X			Serial interface
					SD1	X			data register (low-order)
	R/W				SD0	X			LSB
F31H	SD7	SD6	SD5	SD4	SD7	X			MSB
					SD6	X			Serial interface
					SD5	X			data register (high-order)
	R/W				SD4	X			LSB
F7AH	SCTRG	SEN	SCS1	SCS0	SCTRG	–	Trigger	–	Serial interface clock trigger
					SEN	0	⌐	⌙	Serial interface clock edge selection
	W	R/W			SCS1	0			
					SCS0	0			Serial interface clock mode selection

SD0–SD3, SD4–SD7 (F30H, F31H, R/W)

This is the data register of the serial interface.

- **During writing operation**

  When "1" is written: High level
  When "0" is written: Low level

  Writes serial data will be output to SOUT terminal. From the SOUT terminal, the data converted to serial data as high (V_{DD}) level bit for bits set at "1" and as low (V_{SS}) level bit for bits set at "0".
  Perform data writing only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).
  At initial reset, these registers will be undefined.

- **During reading operation**

  When "1" is read: High level
  When "0" is read: Low level

  The serial data input from the SIN terminal can be read by this register.
  The data converted to parallel data, as high (V_{DD}) level bit "1" and as low (V_{SS}) level bit "0" input from SIN terminal. Perform data reading only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).
  At initial reset, these registers will be undefined.

SCS1, SCS0 (F7AH [D1, D0], R/W)
Selects the synchronous clock for the serial interface ($\overline{SCLK}$).

Table 9.5.2 Synchronous clock selection

SCS1	SCS0	Mode	Synchronous clock
1	1	Master mode	CLK
1	0		CLK/2
0	1		CLK/4
0	0	Slave mode	External clock

CLK : CPU system clock

Synchronous clock ($\overline{SCLK}$) is selected from among the above 4 types: 3 types of internal clock and external clock.
At initial reset, external clock is selected.

SEN (F7AH [D2], R/W)
Selects the timing for reading in the serial data input.

When "1" is written: Falling edge of $\overline{SCLK}$
When "0" is written: Rising edge of $\overline{SCLK}$
Reading: Valid

Selects whether the fetching for the serial input data to registers (SD0–SD7) at the falling edge (at "1" writing) or rising edge (at "0" writing) of the $\overline{SCLK}$ signal.
The input data fetching timing may be selected but output timing for output data is fixed at $\overline{SCLK}$ falling edge.
At initial reset, rising edge of $\overline{SCLK}$ (SEN = "0") is selected.

SCTRG (F7AH [D3], W)
This is a trigger to start input/output of synchronous clock.

When "1" is written: Trigger
When "0" is written: No operation
Reading: Always "0"

When this trigger is supplied to the serial interface activating circuit, the synchronous clock ($\overline{SCLK}$) input/output is started.
As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.)
Supply trigger only once every time the serial interface is placed in the RUN state.
Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

EISIO (F13H [D0], R/W)
This is the interrupt mask register of the serial interface.

When "1" is written: Enabled
When "0" is written: Masked
Reading: Valid

Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, this register is set to "0" (mask).

ISIO (F03H [D0], R)

This is the interrupt factor flag of the serial interface.

When "1" is read: Interrupt has occurred
When "0" is read: Interrupt has not occurred
Writing: Invalid

From the status of this flag, the software can decide whether the serial interface interrupt. Note, however, that even if the interrupt is masked, this flag will be set to "1" after the 8 bits data input/output.
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, this flag is set to "0".

9.6 Programming Notes

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock $\overline{SCLK}$ is external clock, start to input the external clock after the trigger.

(4) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

CHAPTER 10 SOUND GENERATOR

10.1 Configuration of Sound Generator

The E0C6S46 is capable of generating buzzer signals (BZ and $\overline{BZ}$) to drive a piezo-electric buzzer.
The buzzer signal frequency may be selected by software from 8 types of signal divided from fOSC1 (32.768 kHz).
Also, digital envelope which is duty ratio controlled may be added to the buzzer signal.
In addition, 1-shot output circuit is built-in to output key operation check sound, and the like.
Figure 10.1.1 shows the sound generator configuration. Figure 10.1.2 shows the sound generator timing chart.

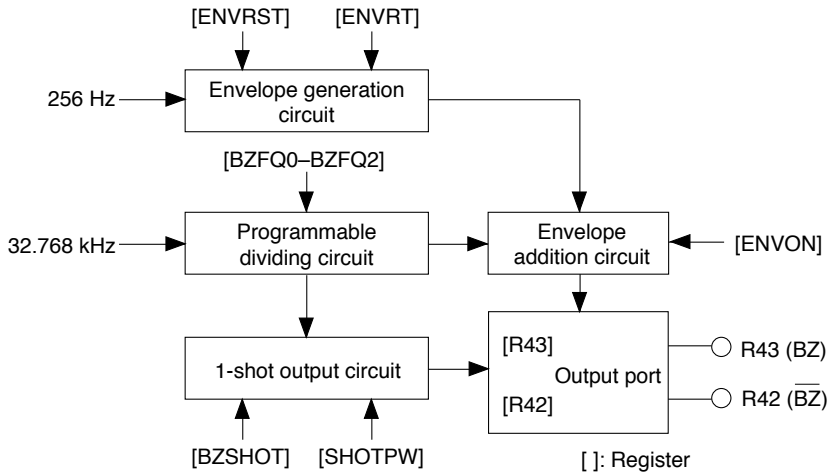


Fig. 10.1.1 Configuration of sound generator

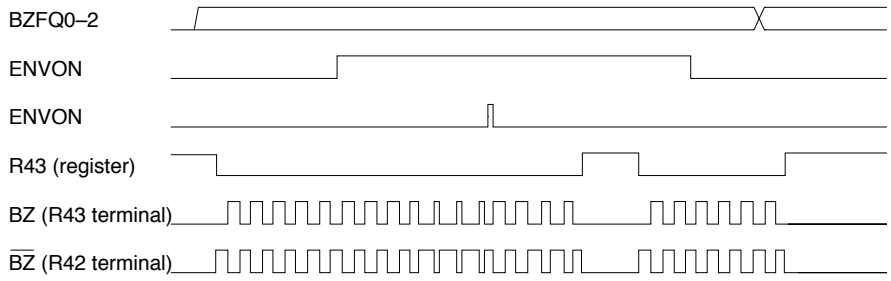


Fig. 10.1.2 Timing chart of sound generator

10.2 Mask Option

(1) Selection can be made whether to output the BZ signal from the R43 terminal.

(2) Selection can be made whether to output the $\overline{BZ}$ signal from the R42 terminal.
However, if the BZ signal is not output the $\overline{BZ}$ signal cannot be output.

See Section 6.2, "Output Port" for details of the above mask option.

10.3 Frequency Setting

The frequencies of the buzzer signals (BZ, $\overline{BZ}$) are set by writing data to registers BZFQ0–BZFQ2.
Table 10.3.1 lists the register setting values and the frequencies that can be set.

Table 10.3.1 Setting of frequencies of buzzer signals

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4,096.0
0	0	1	3,276.8
0	1	0	2,730.7
0	1	1	2,340.6
1	0	0	2,048.0
1	0	1	1,638.4
1	1	0	1,365.3
1	1	1	1,170.3

Note: A hazard may be observed in the output waveform of the buzzer signals when switches the buzzer frequency while the buzzer signals being output.

10.4 Digital Envelope

A duty ratio control data envelope (with duty ratio change in 8 steps) can be added to the buzzer signal (BZ, $\overline{BZ}$).
Duty ratio refers to the ratio of pulse width to the pulse cycle; given that high level output time is TH, and low level output time is TL, BZ output becomes TH/(TH+TL).
$\overline{BZ}$ output becomes TL/(TH+TL) owing to the inverted output of the BZ output. Moreover, care is necessary as the duty ratio differs according to the buzzer frequency.
Envelope addition is performed by writing "1" to ENVON; when "0" is written, the duty ratio is fixed at the maximum (1/2 duty). Moreover, when envelope is added, writing "1" to ENVRST will cause the BZ signal duty ratio to be returned to maximum.
The decay time of the envelope (time for the duty ratio to change) can be selected with the register ENVRT. This time is 62.5 ms (16 Hz) when "0" is written, and 125 ms (8 Hz) when "1" is written. However, a maximum difference of 4 ms is taken from envelope-ON until the first change.
Table 10.4.1 lists the duty ratio and buzzer frequencies.
Figure 10.4.1 shows the digital envelope timing chart.

Table 10.4.1 Duty ratio and buzzer frequencies

Duty ratio	Buzzer frequencies			
	4,096.6 2,048.0	3,276.8 1,638.4	2,730.7 1,365.3	2,340.6 1,170.3
Level 1 (max.)	8/16	8/20	12/24	12/28
Level 2	7/16	7/20	11/24	11/28
Level 3	6/16	6/20	10/24	10/28
Level 4	5/16	5/20	9/24	9/28
Level 5	4/16	4/20	8/24	8/28
Level 6	3/16	3/20	7/24	7/28
Level 7	2/16	2/20	6/24	6/28
Level 8 (min.)	1/16	1/20	5/24	5/28

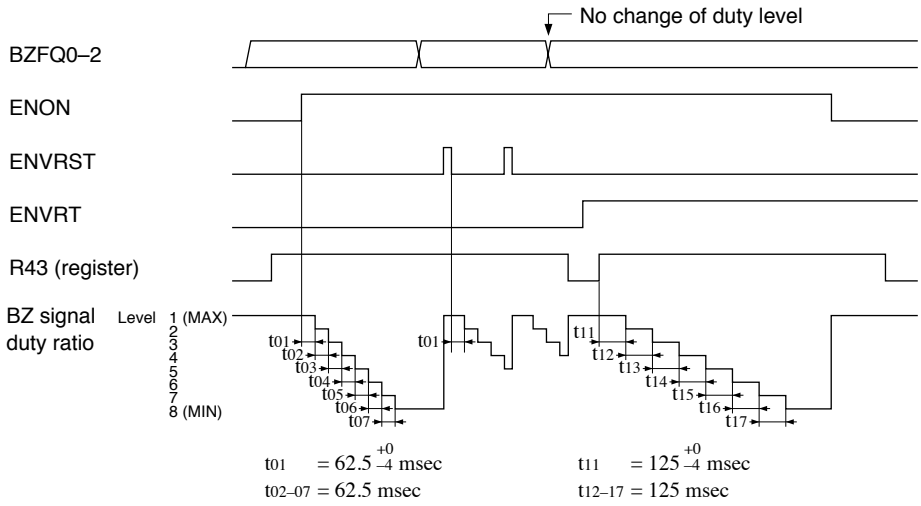


Fig. 10.4.1 Digital envelope timing chart

10.5 1-shot Output

In order to cause the buzzer to ring in a short period of time as in the case of key operation check sound, 1-shot output function is built-in. The time duration for buzzer signal to be output (BZ and $\overline{BZ}$) may be selected by SHOTPW; when "0" is written on SHOTPW, it is set to 31.25 ms and to 62.5 ms when "1" written.

Actual output operation is performed by writing "1" on BZSHOT; after performing the previously described writing operation, it synchronizes with the internal 256 Hz signal and buzzer signal is output in output port R43 (R42).

Moreover, after the set time has lapsed, it synchronizes with the same 256 Hz previously described and the buzzer signal is automatically turned off. Also, by reading BZSHOT, whether the 1-shot circuit is in operation or not may be determined with the software.

Figure 10.5.1 shows the timing chart of the 1-shot output.

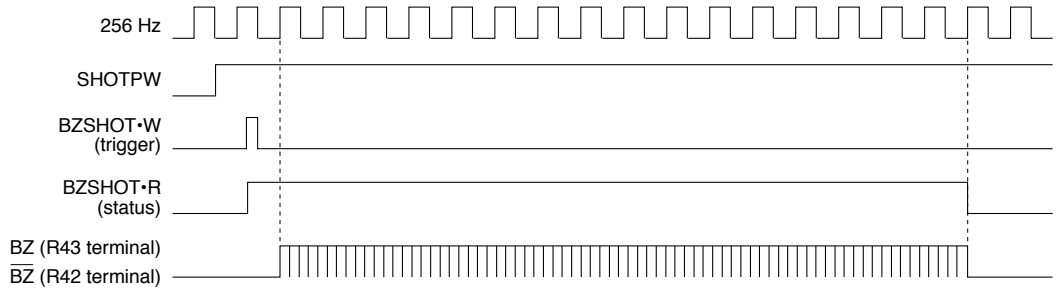


Fig. 10.5.1 Timing chart of 1-shot output

10.6 Control of Sound Generator

The control registers for the sound generator are explained below.

Table 10.6.1 Control registers of sound generator

Address	Register D3	D2	D1	D0	Name	Init	1	0	Comment
F54H	R43	R42	R41	R40	R43	1	High	Low	Output port (R43)
							Off	On	Buzzer output (BZ)
	R/W				R42	1	High	Low	Output port (R42)
							Off	On	Clock output (FOUT)
									[Buzzer inverted output ($\overline{BZ}$)]
					R41	1	High	Low	Output port (R41)
					R40	1	High	Low	Output port (R40)
							Off	On	Clock inverted output ($\overline{FOUT}$)
F74H	SHOTPW	BZFQ2	BZFQ1	BZFQ0	SHOTPW	0	62.5 ms	31.25 ms	1-shot buzzer pulse width
	R/W				BZFQ2	0			Buzzer frequency selection
					BZFQ1	0			
					BZFQ0	0			
F75H	BZSHOT	ENVRST	ENVRT	ENVON	BZSHOT	0	Trigger	–	1-shot buzzer trigger (W)
							BUSY	READY	Status (R)
					ENVRST	Reset	Reset	–	Envelope reset
	W / R	W	R/W		ENVRT	0	1.0 sec	0.5 sec	Envelope cycle selection
					ENVON	0	On	Off	Envelope On/Off

BZFQ0–BZFQ2 (F74H [D0, D1, D2], R/W)

Will select the buzzer signal frequency.

Table 10.6.2 Setting of frequencies of buzzer signals

BZFQ2	BZFQ1	BZFQ0	Buzzer frequency (Hz)
0	0	0	4,096.0
0	0	1	3,276.8
0	1	0	2,730.7
0	1	1	2,340.6
1	0	0	2,048.0
1	0	1	1,638.4
1	1	0	1,365.3
1	1	1	1,170.3

At initial reset, 4,096 Hz is selected.

ENVRST (F75H [D2], W)

This is the reset input to make the duty ratio of the buzzer signal the maximum.

When "1" is written: Reset input
When "0" is written: No operation
Reading: Always "0"

When envelope is added to the buzzer signal, by writing "1" on ENVRST, the envelope is reset and duty ratio becomes maximum. When envelope is not added, or when buzzer signal is not being output, reset operation is ineffective.

ENVON (F75H [D0], R/W)
This controls adding the envelope to the buzzer signal.

When "1" is written: Envelope added (ON)
When "0" is written: No envelope (OFF)
Reading: Valid

By writing "1" on ENVON, envelope is added to the buzzer signal. Writing "0" means envelope will not be added.
At initial reset, ENVON is set to "0" and envelope OFF will be selected.

ENVRT (F75H [D1], R/W)
Selects the attenuation time of the envelope added to the buzzer signal.

When "1" is written: 1.0 sec (125 ms × 7 = 875 ms)
When "0" is written: 0.5 sec (62.5 ms × 7 = 437.5 ms)
Reading: Valid

The attenuation time of digital envelopes is determined by the time change for duty ratio. When "1" is written on ENVRT, attenuation time is set in 125 ms (8 Hz) units (125 ms × 7 = 875 ms), and in 62.5 ms (16 Hz) unit (62.5 ms × 7 = 437.5 ms) when "0" is written.
However, there is a maximum error of 4 ms from envelope ON to the first change in both cases.
At initial reset, ENVRT is set to "0".

R43, R42 (F54H [D3, D2], R/W)
Controls the output of the buzzer signals (BZ, $\overline{BZ}$).

When "0" is written: Buzzer signal output
When "1" is written: Low level (DC)
Reading: Valid

When "0" is set on R43, BZ signal is generated from R43 terminal, and if R42 is set to $\overline{BZ}$ output, $\overline{BZ}$ signal (inverted signal of BZ) is generated at the same time.
When "1" is set on R43, R43 terminal (R42 too, if $\overline{BZ}$ output is selected) becomes of low (V_{SS}) level output.
However, R42 with $\overline{BZ}$ output selected, may be used as a 1-bit general register capable of read/write function, the data of which register does not affect $\overline{BZ}$ (R42 terminal output).
At initial reset, both R43 and R42 are set to "1".

Note: BZ and $\overline{BZ}$ output signals may produce hazards during ON/OFF switching.

SHOTPW (F74H [D3], R/W)
Sets the output time duration of the 1-shot buzzer.

When "1" is written: 62.5 ms
When "0" is written: 31.25 ms
Reading: Valid

Output time duration is set to 62.5 ms or 31.25 ms by writing "1" or "0", respectively, on SHOTPW.
At initial reset, SHOTPW is set to "0".

BZSHOT (F75H [D3], W, R)
Controls the output of the 1-shot buzzer.

- **During writing operation**
  When "1" is written: Trigger
  When "0" is written: No operation

  When "1" is written on BZSHOT, the 1-shot circuit operates and the buzzer signal (BZ and $\overline{BZ}$) is output.
  The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "0") state and writing to BZSHOT becomes invalid in the ON (R43 = "1") state.

- **During reading operation**
  When "1" is read: Busy
  When "0" is read: Ready

  The BZSHOT reads "1" when the 1-shot buzzer is ringing and "0" when it is not ringing. The period of "1" is from the time of the trigger until the buzzer output is turned OFF.
  At initial reset, "0" is read.

10.7 Programming Notes

(1) The BZ and $\overline{BZ}$ signals may generate hazards in the following cases:

- When the content of R43 register is changed, BZ and $\overline{BZ}$ signals are switched ON or OFF.
- When the contents of buzzer frequency selection registers (BZFQ0–BZFQ2) while the buzzer signal (BZ and $\overline{BZ}$) is being output.

(2) The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "0") state and writing to BZSHOT becomes invalid in the ON (R43 = "1") state.

CHAPTER 11 INTERRUPT AND HALT

The E0C6S46 has the following interrupt functions built-in, and masking is possible for each one.

External interrupt
- Input interrupt (2 systems)

Internal interrupt
- Clock timer interrupt (3 systems)
- Stopwatch timer interrupt (2 systems)
- Programmable timer interrupt (1 system)
- Serial interface interrupt (1 system)

To allow the interrupt to function, it is necessary that the interrupt mask register of the required system be set to "1" (enable) and, at the same time, the interrupt flag be set to "1" (EI).
When interrupt occurs, the interrupt flag is automatically reset to "0" (DI), prohibiting the any consequent interrupts.

The CPU stops the operating clock when a HALT instruction is executed and then enters the HALT state. Re-running the CPU from the HALT state requires issuance of interrupt request.
If return through interrupt request is not effective, return is effected from initial reset by the watchdog timer.

Figure 11.1 shows the configuration of the interrupt circuit.

See the explanations of the relevant circuits for interrupt details.

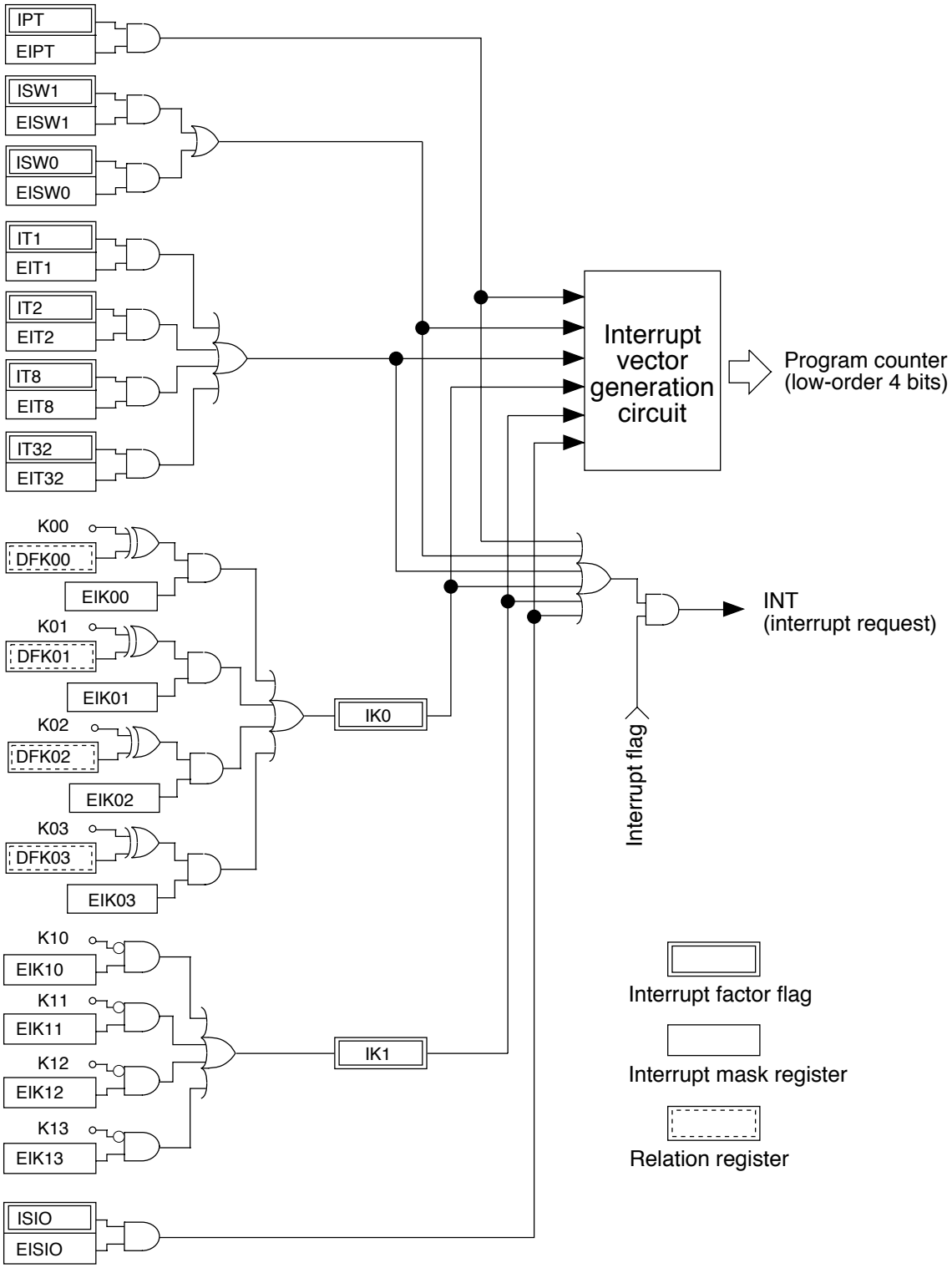


Fig. 11.1 Configuration of interrupt circuit

11.1 Interrupt Factor Flag and Interrupt Mask

The corresponding interrupt factor flag is set to "1" with the individual interrupt element.
If the following conditions exist, interrupt for the CPU occurs when the interrupt factor flag is set to "1".

- The corresponding interrupt mask register is set at "1" (enable).
- The interrupt flag is set at "1" (EI).

The interrupt factor flag is reset to "0" at the read-only register by reading the data.
Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.
At initial reset, the interrupt factor flag is reset to "0".

The interrupt can be masked by the corresponding interrupt mask register.
The interrupt mask register is a register capable of read/write operation; by writing "1", it is enabled (interrupt is allowed) and by writing "0", it is masked (interrupt is prohibited).
Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.
At initial reset, the interrupt mask register is set to "0".

The interrupt factor flag is set to "1" by interrupt factor even if the interrupt is masked. (The input interrupt factor flags IK0 and IK1 will be eliminated.)

Table 11.1.1 shows the correspondence between interrupt factor flags and interrupt mask registers.

Table 11.1.1 Interrupt factor flags and interrupt mask registers

Interrupt factor	Interrupt factor flag	Interrupt mask register
Falling edge of clock timer (1 Hz)	IT1 (F00H [D3])	EIT1 (F10H [D3])
Falling edge of clock timer (2 Hz)	IT2 (F00H [D2])	EIT2 (F10H [D2])
Falling edge of clock timer (8 Hz)	IT8 (F00H [D1])	EIT8 (F10H [D1])
Falling edge of clock timer (32 Hz)	IT32 (F00H [D0])	EIT32 (F10H [D0])
Overflow of stopwatch timer (SWH) (1 Hz)	ISW1 (F01H [D1])	EISW1 (F11H [D1])
Overflow of stopwatch timer (SWL) (10 Hz)	ISW0 (F01H [D0])	EISW0 (F11H [D0])
No matching between input ports (K00–K03) and input relation registers (DFK00–DFK03)	IK0 (F04H [D0])	EIK03 (F14H [D3]) EIK02 (F14H [D2]) EIK01 (F14H [D1]) EIK00 (F14H [D0])
Falling edge of input ports (K10–K13)	IK1 (F05H [D0])	EIK13 (F15H [D3]) EIK12 (F15H [D2]) EIK11 (F15H [D1]) EIK10 (F15H [D0])
Data (8 bits) input/output of serial interface has completed	ISIO (F03H [D0])	EISIO (F13H [D0])
Counter value of programmable timer = 00H	IPT (F02H [D0])	EIPT (F12H [D0])

11.2 Interrupt Vector

When an interrupt request is issued to the CPU, the CPU starts interrupt processing.
Interrupt processing is accomplished by the following steps after the instruction being executed is completed.

① The address (value of the program counter) of the program which should be run next is saved in the stack area (RAM).

② The vector address (1 page 02H–0CH) for each interrupt request is set to the program counter.

③ Branch instruction written to the vector is effected (branch to software interrupt processing routine).

Time equivalent to 12 cycles of CPU system clock is required for steps ① and ②.

The interrupt request and interrupt vector correspondence is shown in Table 11.2.1.

Table 11.2.1 Interrupt request and interrupt vectors

Interrupt vector (PCP and PCS)	Interrupt request	Priority
102H	Clock timer interrupt	Low
104H	Stopwatch timer interrupt	↑
106H	Input (K00–K03) interrupt	
108H	Input (K10–K13) interrupt	
10AH	Serial interface interrupt	↓
10CH	Programmable timer interrupt	High

When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

11.3 Programming Notes

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register. Note, however, that the input interrupt factor flags (IK0 and IK1) will be eliminated.

(2) When an interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI status. After completion of the interrupt processing, set to the EI status through the software as needed.
Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

(3) The interrupt factor flags must always be reset before setting the EI status. When the interrupt mask register has been set to "1", the same interrupt will occur again if the EI status is set unless of resetting the interrupt factor flag.

(4) The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

(6) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(7) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

(8) If an interrupt occurs while the CPU is processing some other interrupt request of which the priority is lower than the new one but the CPU has not fetched the interrupt vector, the CPU may shift to a vector address (one of among 102H, 104H, 106H, 10AH and 10EH) that is different from the new interrupt.
Therefore, make sure the interrupt factor flag has been set immediately after the branch instruction stored in the vector address is executed and quit the interrupt processing if it has not been set.
Furthermore, place a branch instruction for executing the interrupt processing routine in the vector address 10EH because the CPU may shift to that address. By setting the start address of the programmable timer interrupt processing routine as the branch destination, the priority level by hardware can be maintained.
If the program does not have the individual processing routine for each interrupt (for example, in the case of all interrupts using the same processing routine in which the type of interrupt is judged by reading the interrupt flags, or in the case of the main routine checking all the interrupt flags by branching the flow the RET instruction stored in all the vector address), place the instruction the same as the other interrupt vectors in address 10EH.
When the interrupt function is not used, it is not necessary to pay attention to the above mentioned precautions.

CHAPTER 12 SUMMARY OF NOTES

12.1 Notes for Low Current Consumption

The E0C6S46 contains control registers for each of the circuits so that current consumption can be lowered. These control registers lower the current consumption through programs that operate the circuits at the minimum levels.
The following text explains the circuits that can control operation and their control registers. Refer to these when putting programs together.

Table 12.1.1 Circuits and control registers

Circuits (and Items)	Control registers	Order of consumed current
CPU	HALT instruction	See electrical characteristics (Chapter 14)
CPU operation frequency	CLKCHG, OSCC	See electrical characteristics (Chapter 14)
Internal regulated voltage	VSC0, VSC1	See electrical characteristics (Chapter 14)
Heavy load protection mode	HLMOD	See electrical characteristics (Chapter 14)
SVD circuit	SVDON	Several tens μA

Below are the circuit status at initial reset.

CPU: Operating
CPU operating frequency: OSC1 side (CLKCHG = "0"), OSC3 oscillation circuit is stooped (OSCC = "0")
Internal regulated voltage: -1.2 V (VSC0, VSC1 = "0")
Heavy load protection mode: Normal operating mode (HLMOD = "0")
SVD circuit: OFF (SVDON = "0")

Also, be careful about panel selection because the current consumption can differ by the order of several μA on account of the LCD panel characteristics.

12.2 Summary of Notes by Function

Here, the cautionary notes are summed up by function category. Keep these notes well in mined when programming.

Memory

Memory is not mounted in unused area within the memory map and in memory area not indicated in this manual. For this reason, normal operation cannot be assured for programs that have been prepared with access to these areas.

SVD (Supply voltage detection) circuit

(1) The SVD circuit should normally be turned OFF (SVDON = "0") as the consumption current of the IC becomes large when it is ON (SVDON = "1").

(2) To obtain a stable detection result, after setting SVDON to "1", provide at least 100 μs waiting time before performing SVDDT reading.

Heavy load protection mode

(1) During heavy load or when 2.2 V or below is detected by SVD, set it to heavy load protection mode. Unless it is necessary, be careful not to set the heavy load protection mode with the software.

(2) Perform heavy load driving only after setting up at least 1 ms wait time through the software, after switching to the heavy load protection mode. (See Figure 3.3.2.1.)

(3) When the heavy load protection mode is to canceled after completion of heavy load driving, set up at least 2 seconds wait time through the software. (See Figure 3.3.2.1.)

Watchdog timer

(1) The watchdog timer must reset within 3-second cycles by the software.

(2) When clock timer resetting (TMRST ← "1") is performed, the watchdog timer is counted up; reset the watchdog immediately after if necessary.

Oscillation circuit

(1) When high-speed operation of the CPU is not required, observe the following reminders to minimize power current consumption.

Set the CPU operating clock to OSC1.
Turn the OSC3 oscillation OFF.
Set the internal operating voltage (V_{S1}) to -1.2 V or -2.1 V.

(2) When the CPU is to be operated with OSC1, set the operating voltage to -1.2 V if the power voltage detected with the SVD circuit were less than 3.1 V (V_{DD}–V_{SS} < 3.1 V); set the operating voltage to -2.1 V if the detected voltage were 3.1 V or more (V_{DD}–V_{SS} ≥ 3.1 V). Moreover, because -1.2 V will be set during initial reset, be sure to execute the previous process at the beginning of the initial routine. Note, however, that it can be used fixed at 1.2 V (at OSC1 operation) for power whose initial value is 3.6 V or less as in lithium batteries.

(3) When switching V_{S1} from -1.2 V (for OSC1 crystal oscillation circuit) to -3.0 V (for OSC3 oscillation circuit), or vice versa, be sure to hold the -2.1 V setting for more than 5 ms first for power voltage stabilization.

(VSC1, VSC0) = (0, 0) → (0, 1) → 5 ms WAIT → (1, ×)
= (1, ×) → (0, 1) → 5 ms WAIT → (0, 0)

= (0, 0) → (1, ×) is prohibited
= (1, ×) → (0, 0) is prohibited

Furthermore, perform the switch after making sure that power voltage by SVD is more than the V_{S1} (absolute value) set voltage. Switching V_{S1} when the power source voltage is lower than the set voltage may cause malfunction.

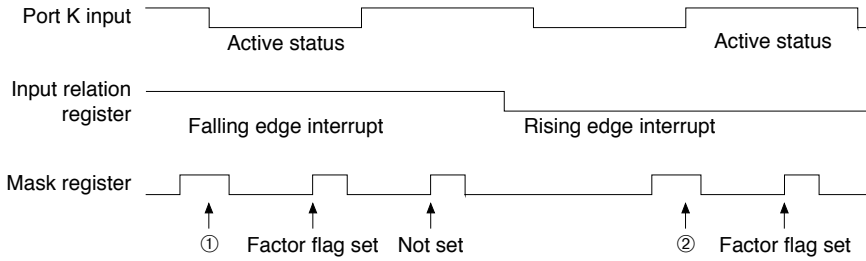
(4) When switching the CPU operating clock from OSC1 to OSC3, follow the flow chart shown in Figure 5.5.1 and then proceed with software processing.

(5) Use separate instructions to switch the clock from OSC3 to OSC1 and turn the OSC3 oscillation OFF. Simultaneous processing with a single instruction may cause malfunction of the CPU.

Input port (Kxx)

(1) When changing the input port from Low level to High level with a pull up resistor, a delay in the waveform rise time will occur depending on the time constant of the pull up resistor and input gate capacity. Hence, when reading data from the input port, set an appropriate waiting time. Care is particularly required for key matrix configuration scanning. For reference, approximately 500 μs waiting time is required.

(2) Input interrupt programming related precautions



When the content of the mask register is rewritten, while the port K input is in the active status. The input interrupt factor flags are set at ① and ②, ① being the interrupt due to the falling edge and ② the interrupt due to the rising edge.

Fig. 12.2.1 Input interrupt timing

When using an input interrupt, if you rewrite the content of the mask register, when the value of the input terminal which becomes the interrupt input is in the active status, the factor flag for input interrupt may be set. Therefore, when using the input interrupt, the active status of the input terminal implies

input terminal = Low status, when the falling edge interrupt is effected and
input terminal = High status, when the rising edge interrupt is effected.

When an interrupt is triggered at the falling edge of an input terminal, a factor flag is set with the timing of ① shown in Figure 12.2.1. However, when clearing the content of the mask register with the input terminal kept in the Low status and then setting it, the factor flag of the input interrupt is again set at the timing that has been set.

Consequently, when the input terminal is in the active status (Low status), do not rewrite the mask register (clearing, then setting the mask register), so that a factor flag will only set at the falling edge in this case.

When clearing, then setting the mask register, set the mask register, when the input terminal is not in the active status (High status).

When an interrupt is triggered at the rising edge of the input terminal, a factor flag will be set at the timing of ② shown in Figure 12.2.1. In this case, when the mask registers cleared, then set, you should set the mask register, when the input terminal is in the Low status.

In addition, when the mask register = "1" and the content of the input relation register is rewritten in the input terminal active status, an input interrupt factor flag may be set. Thus, you should rewrite the content of the input relation register in the mask register = "0" status.

Output port (Rxx)

(1) When BZ, $\overline{BZ}$, FOUT, $\overline{FOUT}$, and PTCLK (DC) are selected by mask option, a hazard may be observed in the output waveform when the data of the output register changes.

(2) Because the R00–R03, R10–R13, R20–R23, and R30–R32 (R33) ports gain high impedance during initial reset, be careful when using them as interface with external devices and the like.

(3) When R33 port is selected for 2 states and DC (PTCLK) output by mask option, R33 terminal becomes undefined at initial reset.

I/O port (Pxx)

(1) When the I/O port is set at output mode, and low impedance load is connected to the port terminal, the data written and read may differ.

(2) If the state of the I/O port meets all of the following 4 conditions, the reading data will be undefined:
- The input/output mode is set at output mode
- Output specification is set at Nch open drain
- The content of the data register is "1"
- The pull up resistor turned is OFF

(3) When P30–P33 has been set as the output exclusive in the mask option, a pull up resistor cannot be added even if the pull up resistor control register PUP3 has been made "0".

LCD driver

Because at initial reset, the contents of segment data memory and LC0–LC3 are undefined, there is need to initialize by software.

Clock timer

(1) When the clock timer has been reset, the interrupt factor flag (IT) may sometimes be set to "1". Consequently, perform flag read (reset the flag) as necessary at reset.

(2) Because the watchdog timer counts up during reset as in the above (1), reset the watchdog timer as necessary.

(3) When the low-order digits (TM0–TM3) and high-order digits (TM4–TM7) are consecutively read, proper reading may not be obtained due to the carry from the low-order digits into the high-order digits (when the reading of the low-order digits and high-order digits span the timing of the carry). For this reason, perform multiple reading of timer data, make comparisons and use matching data as result.

Stopwatch timer

When data of the counter is read at run mode, perform the reading after suspending the counter once and then set SWRUN to "1" again. Moreover, it is required that the suspension period not exceed 976 μs (1/4 cycle of 256 Hz).

Programmable timer

(1) When initiating programmable timer count, perform programming by the following steps:
1. Set the initial data to RD0–RD7.
2. Reset the programmable timer by writing "1" to PTRST.
3. Start the down-count by writing "1" to PTRUN.

(2) When the reload register (RD0–RD7) value is set at "00H", the down-counter becomes a 256-value counter.

(3) When data of the timer is read consecutively in 8 bits in the RUN mode, perform the reading after suspending the timer once and then set the PTRUN to "1" again. Moreover, it is required that the suspension period be within 1/4 cycle of the input clock (in case of 1/2 duty). Accordingly, when the input clock is a fast clock faster than 256 Hz, high speed processing by OSC3 is required.

Serial interface (SIN, SOUT, and $\overline{\text{SCLK}}$)

(1) When using the serial interface in the master mode, the synchronous clock uses the CPU system clock. Accordingly, do not change the system clock ($f_{OSC1} \leftrightarrow f_{OSC3}$) while the serial interface is operating.

(2) Perform data writing/reading to data registers SD0–SD7 only while the serial interface is halted (i.e., the synchronous clock is neither being input or output).

(3) As a trigger condition, it is required that data writing or reading on data registers SD0–SD7 be performed prior to writing "1" to SCTRG. (The internal circuit of the serial interface is initiated through data writing/reading on data registers SD0–SD7.) Supply trigger only once every time the serial interface is placed in the RUN state. Moreover, when the synchronous clock $\overline{\text{SCLK}}$ is external clock, start to input the external clock after the trigger.

Sound generator

(1) The BZ and $\overline{\text{BZ}}$ signals may generate hazards in the following cases:
- When the content of R43 register is changed, BZ and $\overline{\text{BZ}}$ signals are switched ON or OFF.
- When the contents of buzzer frequency selection registers (BZFQ0–BZFQ2) while the buzzer signal (BZ and $\overline{\text{BZ}}$) is being output.

(2) The 1-shot buzzer operates only when the regular buzzer output is in the OFF (R43 = "0") state and writing to BZSHOT becomes invalid in the ON (R43 = "1") state.

Interrupt

(1) The interrupt factor flag is set when the interrupt conditions are established, regardless of the setting of the interrupt mask register. Note, however, that the input interrupt factor flags (IK0 and IK1) will be eliminated.

(2) When an interrupt occurs, the interrupt flag will be reset by the hardware and it will become DI status. After completion of the interrupt processing, set to the EI status through the software as needed.
Moreover, the nesting level may be set to be programmable by setting to the EI state at the beginning of the interrupt processing routine.

(3) The interrupt factor flags must always be reset before setting the EI status. When the interrupt mask register has been set to "1", the same interrupt will occur again if the EI status is set unless of resetting the interrupt factor flag.

(4) The interrupt factor flag will be reset by reading through the software. Because of this, when multiple interrupt factor flags are to be assigned to the same address, perform the flag check after the contents of the address has been stored in the RAM. Direct checking with the FAN instruction will cause all the interrupt factor flag to be reset.

(5) Be sure that the interrupt factor flag reading is done with the interrupt in the DISABLE state (DI). Reading the interrupt factor flag while in the ENABLE state (EI) may cause malfunction.

(6) Be sure that writing to the interrupt mask register is done with the interrupt in the DISABLE state (DI). Writing to the interrupt mask register while in the ENABLE state (EI) may cause malfunction.

(7) When multiple interrupts simultaneously occur, the high priority vector address is set to the program counter.

(8) If an interrupt occurs while the CPU is processing some other interrupt request of which the priority is lower than the new one but the CPU has not fetched the interrupt vector, the CPU may shift to a vector address (one of among 102H, 104H, 106H, 10AH and 10EH) that is different from the new interrupt.

Therefore, make sure the interrupt factor flag has been set immediately after the branch instruction stored in the vector address is executed and quit the interrupt processing if it has not been set. Furthermore, place a branch instruction for executing the interrupt processing routine in the vector address 10EH because the CPU may shift to that address. By setting the start address of the programmable timer interrupt processing routine as the branch destination, the priority level by hardware can be maintained.
If the program does not have the individual processing routine for each interrupt (for example, in the case of all interrupts using the same processing routine in which the type of interrupt is judged by reading the interrupt flags, or in the case of the main routine checking all the interrupt flags by branching the flow the RET instruction stored in all the vector address), place the instruction the same as the other interrupt vectors in address 10EH.
When the interrupt function is not used, it is not necessary to pay attention to the above mentioned precautions.

12.3 Precautions on Mounting

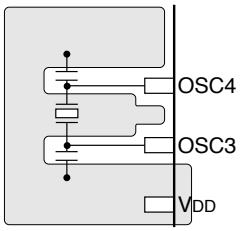
Oscillation Circuit

- Oscillation characteristics change depending on conditions (board pattern, components used, etc.). In particular, when a ceramic oscillator or crystal oscillator is used, use the oscillator manufacturer's recommended values for constants such as capacitance and resistance.
- Disturbances of the oscillation clock due to noise may cause a malfunction. Consider the following points to prevent this:

  (1) Components which are connected to the OSC1 (OSC3) and OSC2 (OSC4) terminals, such as oscillators, resistors and capacitors, should be connected in the shortest line.

  (2) As shown in the figure, make a V_{DD} pattern as large as possible at circumscription of the OSC1 (OSC3) and OSC2 (OSC4) terminals and the components connected to these terminals.
  Furthermore, do not use this V_{DD} pattern for any purpose other than the oscillation system.

Sample V_{DD} pattern (OSC3)



- In order to prevent unstable operation of the oscillation circuit due to current leak between OSC1 (OSC3) and V_{SS}, please keep enough distance between OSC3 and V_{SS} or other signals on the board pattern.

Reset Circuit

- The power-on reset signal which is input to the $\overline{RESET}$ terminal changes depending on conditions (power rise time, components used, board pattern, etc.).
  Decide the time constant of the capacitor and resistor after enough tests have been completed with the application product.
  When using the built-in pull-up resistor of the $\overline{RESET}$ terminal, take into consideration dispersion of the resistance for setting the constant.
- In order to prevent any occurrences of unnecessary resetting caused by noise during operating, components such as capacitors and resistors should be connected to the $\overline{RESET}$ terminal in the shortest line.

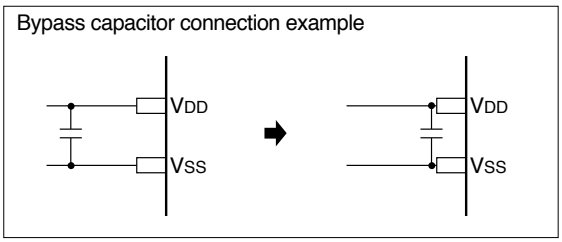
Power Supply Circuit

- Sudden power supply variation due to noise may cause malfunction. Consider the following points to prevent this:

  (1) The power supply should be connected to the V_{DD} and V_{SS} terminal with patterns as short and large as possible.
  Furthermore, similar consideration is necessary when V_{L1}–V_{L5} are supplied from outside the IC.

  (2) When connecting between the V_{DD} and V_{SS} terminals with a bypass capacitor, the terminals should be connected as short as possible.

Bypass capacitor connection example

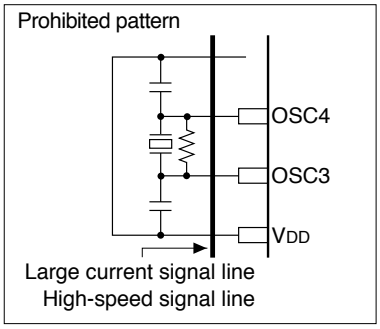


  (3) Components which are connected to the V_{S1}, V_{L1}–V_{L5} terminals, such as capacitors and resistors, should be connected in the shortest line.
  In particular, the V_{L1}–V_{L5} voltages affect the display quality.

- Do not connect anything to the V_{L1}–V_{L5} terminals when the LCD driver is not used.

Arrangement of Signal Lines

- In order to prevent generation of electromagnetic induction noise caused by mutual inductance, do not arrange a large current signal line near the circuits that are sensitive to noise such as the oscillation unit.
- When a signal line is parallel with a high-speed line in long distance or intersects a high-speed line, noise may generated by mutual interference between the signals and it may cause a malfunction. Do not arrange a high-speed signal line especially near circuits that are sensitive to noise such as the oscillation unit.



Precautions for Visible Radiation (when bare chip is mounted)

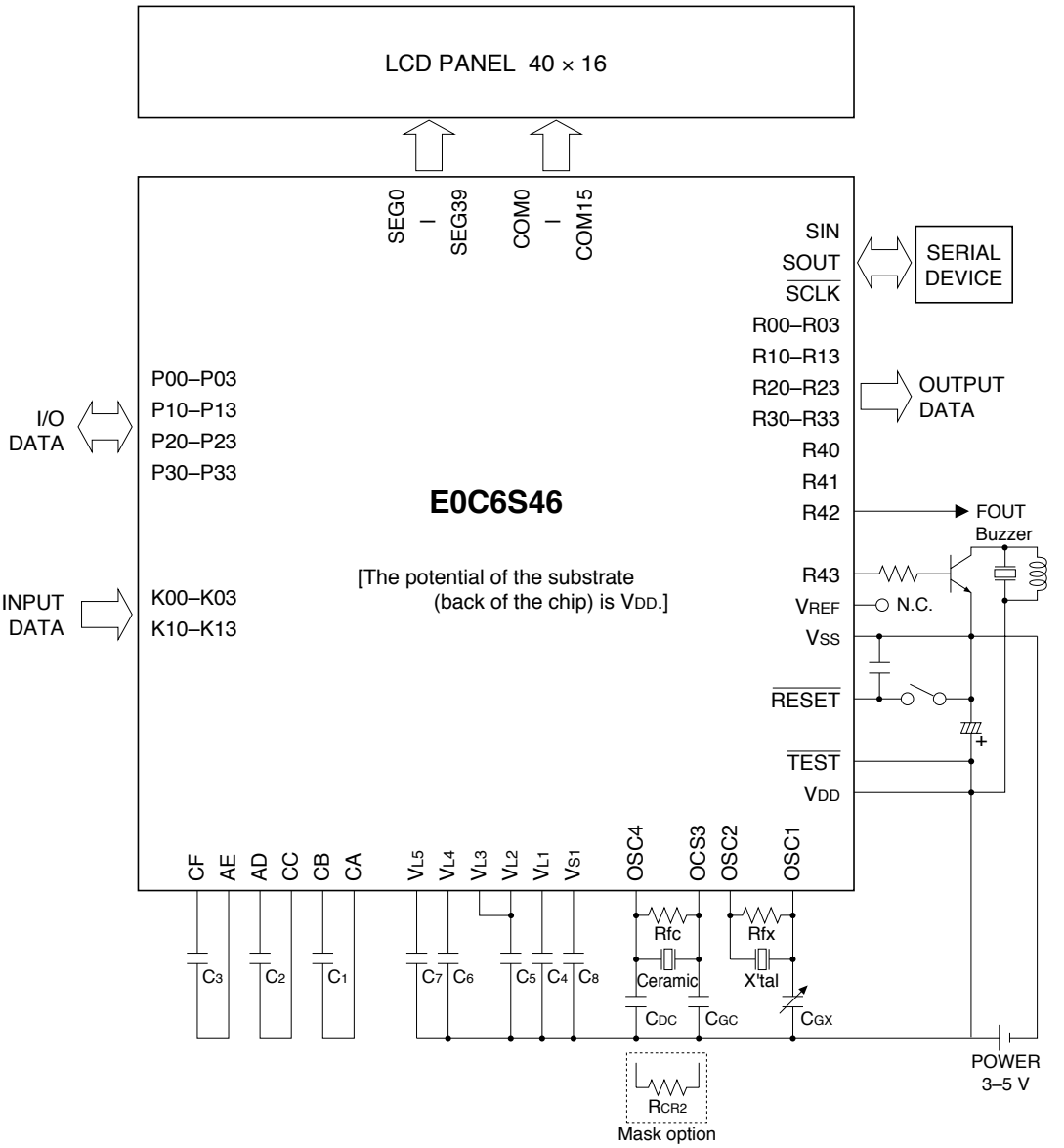
- Visible radiation causes semiconductor devices to change the electrical characteristics. It may cause this IC to malfunction. When developing products which use this IC, consider the following precautions to prevent malfunctions caused by visible radiation.

  (1) Design the product and implement the IC on the board so that it is shielded from visible radiation in actual use.

  (2) The inspection process of the product needs an environment that shields the IC from visible radiation.

  (3) As well as the face of the IC, shield the back and side too.

CHAPTER 13 BASIC EXTERNAL CONNECTION DIAGRAM



X'tal	Crystal oscillator	32.768 kHz, CI(Max)=35 kΩ
Rfx	Feedback resistor	10 MΩ
CGX	Trimmer capacitor	5–25 pF
Ceramic	Ceramic oscillator	500 kHz–2 MHz
Rfc	Feedback resistor	1 MΩ
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
(RCR2)	Resistor for OSC3 CR oscillation	20 kΩ–100 kΩ (VSC=2) 40 kΩ–100 kΩ (VSC=1)

C1	Booster capacitor (1)	0.1µF ∗1
C2	Booster capacitor (2)	0.1µF ∗1
C3	Booster capacitor (3)	0.1µF ∗1
C4	Capacitor between VDD and VL1	0.1µF ∗1
C5	Capacitor between VDD and VL2	0.1µF ∗1
C6	Capacitor between VDD and VL4	0.1µF ∗1
C7	Capacitor between VDD and VL5	0.1µF ∗1
C8	Capacitor between VDD and VS1	0.1µF

∗1 When the load on the liquid crystal system is large, increase the capacitance of the voltage booster capacitors (C1–C3) and the capacitors between VDD and liquid crystal system power (C4–C7).

Note: The above table is simply an example. Refer to Chapter 14, "Electrical Characteristics", for detailed characteristics.

CHAPTER 14 ELECTRICAL CHARACTERISTICS

14.1 Absolute Maximum Rating

(V_{DD}=0V)

Item	Symbol	Rated value	Unit
Supply voltage	V_{SS}	-7.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW
Electrostatic proof pressure	V_E	EIAJ test method (C=200pF) 150V or more MIL test method (C=100pF, R=1.5kΩ) 900V or more	V

*1 The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pin (or is drawn in).

*2 In case of plastic package.

14.2 Recommended Operating Conditions

(Ta=-20 to 70°C)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	VSC="0"	-3.8	-3.0	-1.8	V
			VSC="1"	-5.5	-3.0	-2.2	V
			VSC="2"	-5.5	-5.0	-3.5	V
Oscillation frequency (1)	f_{OSC1}			20	32.768	50	kHz
Oscillation frequency (2)	f_{OSC3}	VSC="1"		50	1,000	1,200	kHz
Oscillation frequency (3)	f_{OSC3}	VSC="2"		50	2,000	2,300	kHz
Voltage booster capacitor (1)	C_1				0.1		µF
Voltage booster capacitor (2)	C_2				0.1		µF
Voltage booster capacitor (3)	C_3				0.1		µF
Capacitor between V_{DD} and V_{L1}	C_4				0.1		µF
Capacitor between V_{DD} and V_{L2}	C_5				0.1		µF
Capacitor between V_{DD} and V_{L4}	C_6				0.1		µF
Capacitor between V_{DD} and V_{L5}	C_7				0.1		µF
Capacitor between V_{DD} and V_{S1}	C_8				0.1		µF

14.3 DC Characteristics

Conditions unless otherwise specified:

V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32.768kHz, f_{OSC3}=1MHz, Ta=25°C, C_1–C_8=0.047µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
High-level input voltage (1)	V_{IH1}	V_{SS}=-2.2 to -5.5V Ta=25°C	K00–03, K10–13, P00–03, P10–13, P20–23, P30–33, SIN, $\overline{SCLK}$	0.2·V_{SS}		0	V
Low-level input voltage (1)	V_{IL1}			V_{SS}		0.8·V_{SS}	V
High-level input voltage (2)	V_{IH2}	V_{SS}=-2.2 to -5.5V Ta=25°C	$\overline{RESET}$	-0.2		0	V
Low-level input voltage (2)	V_{IL2}			V_{SS}		V_{SS}+0.2	V
High-level input current	I_{IH}	V_{SS}=-3.0V, V_{IH}=0V	K00–03, K10–13, P00–03,	0		0.5	µA
Low-level input current (1)	I_{IL1}	V_{SS}=-3.0V, V_{IL1}=V_{SS} With Pull-up resistor	P10–13, P20–23, P30–33, SIN, $\overline{SCLK}$, $\overline{RESET}$	-45		-15	µA
Low-level input current (2)	I_{IL2}	V_{SS}=-3.0V, V_{IL2}=V_{SS} No Pull-up resistor		-0.5		0	µA
High-level output current (1)	I_{OH1}	V_{SS}=-2.2V V_{OH1}=-0.5V	P00–03, P10–13, P20–23, P30–33, R00–03, R10–13,			-1.0	mA
Low-level output current (1)	I_{OL1}	V_{SS}=-2.2V, V_{OL1}=V_{SS}+0.5V	R20–23, R30–33, R40, R41, SOUT, $\overline{SCLK}$	2.0			mA
High-level output current (2)	I_{OH2}	V_{SS}=-2.2V V_{OH2}=-0.5V	R42, R43			-2.0	mA
Low-level output current (2)	I_{OL2}	V_{SS}=-2.2V, V_{OL2}=V_{SS}+0.5V		4.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–15			-30	µA
	I_{OL3}	V_{OL3}=V_{L5}+0.05V		30			µA
Segment output current	I_{OH4}	V_{OH4}=-0.05V	SEG0–39			-10	µA
	I_{OL4}	V_{OL4}=V_{L5}+0.05V		10			µA

14.4 Analog Circuit Characteristics and Consumed Current

Conditions unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32.768kHz, f_{OSC3}=1MHz, Ta=25°C, C_1–C_8=0.047µF

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (Normal mode)	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)		1/2·V_{L2} -0.1		1/2·V_{L2} ×0.95	V
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)	LC="0"	Typ. ×1.12	-1.80	Typ. ×0.88	V
			LC="1"		-1.85		
			LC="2"		-1.90		
			LC="3"		-1.95		
			LC="4"		-2.01		
			LC="5"		-2.06		
			LC="6"		-2.11		
			LC="7"		-2.17		
			LC="8"		-2.22		
			LC="9"		-2.27		
			LC="10"		-2.32		
			LC="11"		-2.38		
			LC="12"		-2.43		
			LC="13"		-2.48		
			LC="14"		-2.53		
			LC="15"		-2.59		
	V_{L4}	Connects a 1MΩ load resistance between V_{DD} and V_{L4} (No panel load)		3/2·V_{L2}		3/2·V_{L2} ×0.95	V
	V_{L5}	Connects a 1MΩ load resistance between V_{DD} and V_{L5} (No panel load)		2·V_{L2}		2·V_{L2} ×0.95	V
LCD drive voltage (Heavy load protection mode)	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)	LC="0"	Typ. ×1.12	-0.92	Typ. ×0.88	V
			LC="1"		-0.95		
			LC="2"		-0.97		
			LC="3"		-1.00		
			LC="4"		-1.03		
			LC="5"		-1.05		
			LC="6"		-1.08		
			LC="7"		-1.11		
			LC="8"		-1.13		
			LC="9"		-1.16		
			LC="10"		-1.18		
			LC="11"		-1.21		
			LC="12"		-1.24		
			LC="13"		-1.26		
			LC="14"		-1.29		
			LC="15"		-1.32		
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)		2·V_{L1}		2·V_{L1} ×0.90	V
	V_{L4}	Connects a 1MΩ load resistance between V_{DD} and V_{L4} (No panel load)		3·V_{L1}		3·V_{L1} ×0.90	V
	V_{L5}	Connects a 1MΩ load resistance between V_{DD} and V_{L5} (No panel load)		4·V_{L1}		4·V_{L1} ×0.90	V
SVD voltage	V_{SVD0}	SVC="0"		-2.35	-2.20	-2.05	V
	V_{SVD1}	SVC="1"		-2.70	-2.50	-2.30	V
	V_{SVD2}	SVC="2"		-3.30	-3.10	-2.90	V
	V_{SVD3}	SVC="3"		-4.50	-4.20	-3.90	V
SVD circuit response time	t_{SVD}					100	µs
Current consumption *1 (OSC1/crystal oscillation)	I_{hlt}	During HALT (VSC="0", OSCC="0")			2.5	5.0	µA
	I_{EX1}	During operation at 32kHz (VSC="0", OSCC="0")			6.5	9.0	µA
	I_{EX2}	During operation at 1MHz (VSC="1")			400	600	µA
	I_{EX3}	During operation at 2MHz (VSC="2", V_{SS}=-5.0V)			1,000	1,500	µA

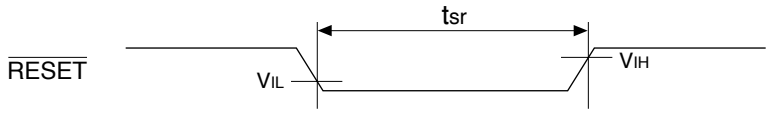
*1 No panel loard. The SVD circuit is in OFF status.

14.5 AC Characteristics

14.5.1 $\overline{\text{RESET}}$ input

Condition: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{IH}=0.5V_{SS}, V_{IL}=0.9V_{SS}

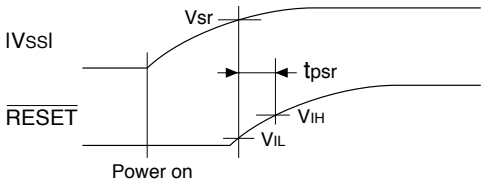
Item	Symbol	Min.	Typ.	Max.	Unit
$\overline{\text{RESET}}$ input time	tsr	2.0			ms

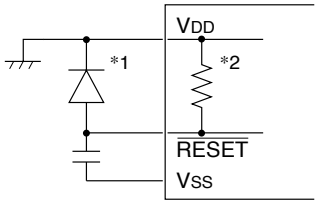


14.5.2 Power-on reset

Condition: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit
Operating power voltage	Vsr	-2.2			V
$\overline{\text{RESET}}$ input time	tpsr	2.0			ms





*1 Because the potential of the $\overline{\text{RESET}}$ terminal not reached V_{DD} level or higher.

*2 Built-in pull-up resistor

14.6 Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 crystal oscillation characteristics

Conditions unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R(C_I=35kΩ), C_{GX}=25pF, C_{DX}=built-in, Rfx=10MΩ, Ta=25°C, VSC="0"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			5	s
Built-in drain capacitance	C_D	Package as assembled		20		pF
		Bare chip		19		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustable range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{SS})			-5.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{S1}	200			MΩ

OSC3 CR oscillation characteristics 1

Conditions unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="1"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}	R_{CR2}=60kΩ	Typ. ×70%	1,000	Typ. ×130%	kHz
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			10	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-5		+5	%

OSC3 CR oscillation characteristics 2

Conditions unless otherwise specified:
V_{DD}=0V, V_{SS}=-5.0V, Ta=25°C, VSC="2"

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}	R_{CR2}=30kΩ	Typ. ×70%	2.0	Typ. ×130%	MHz
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			10	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-3.5 to -5.5V	-5		+5	%

OSC3 ceramic oscillation characteristics 1

Conditions unless otherwise specified:
V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="1", Ceramic oscillator: CSB 1000J *1 (1MHz), C_{GC}=C_{DC}=100pF, Rfc=1MΩ

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			10	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-3		+3	%

*1 Made by Murata Mfg. Co.

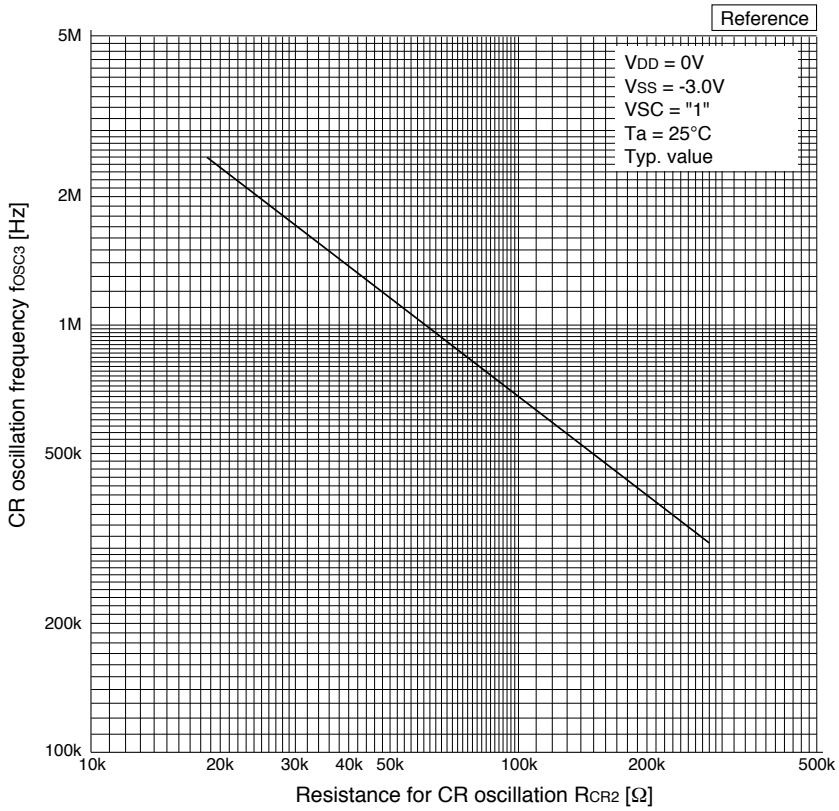
OSC3 ceramic oscillation characteristics 2

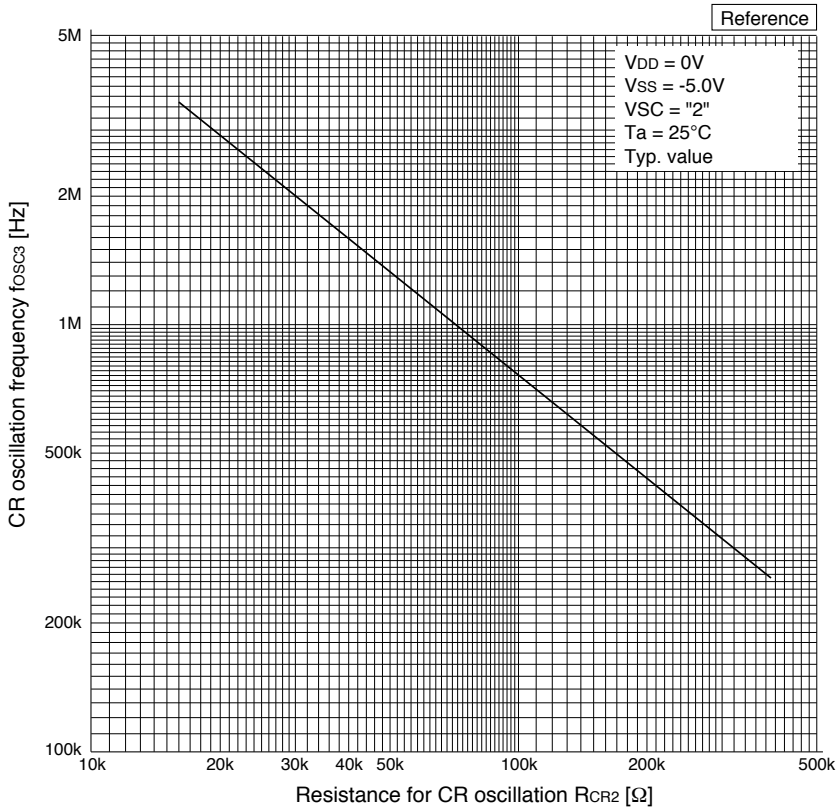
Conditions unless otherwise specified:
V_{DD}=0V, V_{SS}=-5.0V, Ta=25°C, VSC="2", Ceramic oscillator: CSA 2.00MG *1 (2MHz), C_{GC}=C_{DC}=100pF, Rfc=1MΩ

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			10	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-3.5 to -5.5V	-3		+3	%

*1 Made by Murata Mfg. Co.

OSC3 CR oscillation frequency - resistance characteristic



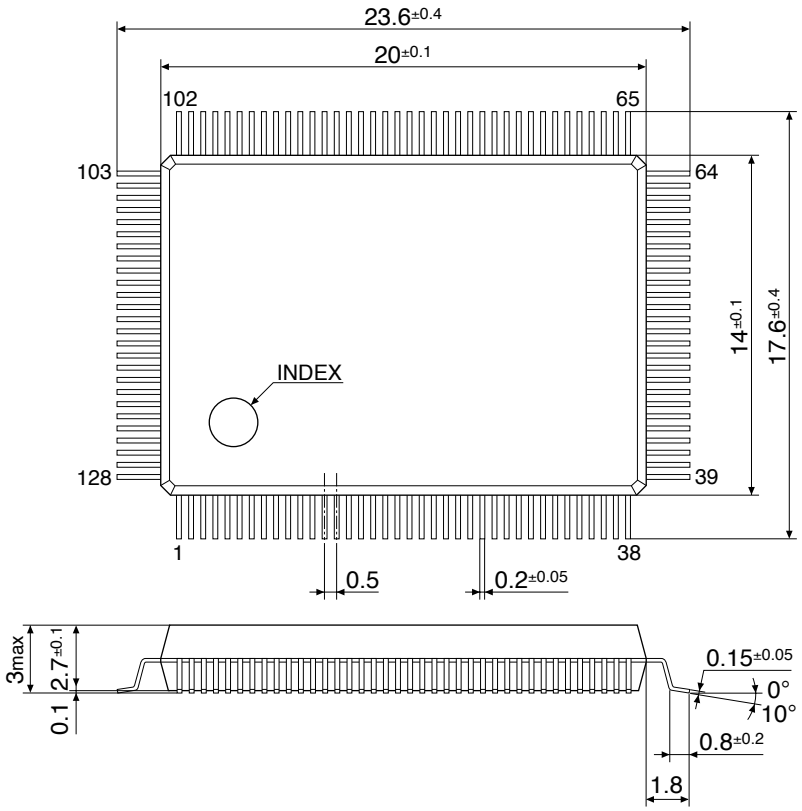


CHAPTER 15 PACKAGE

15.1 Plastic Package

QFP5-128pin

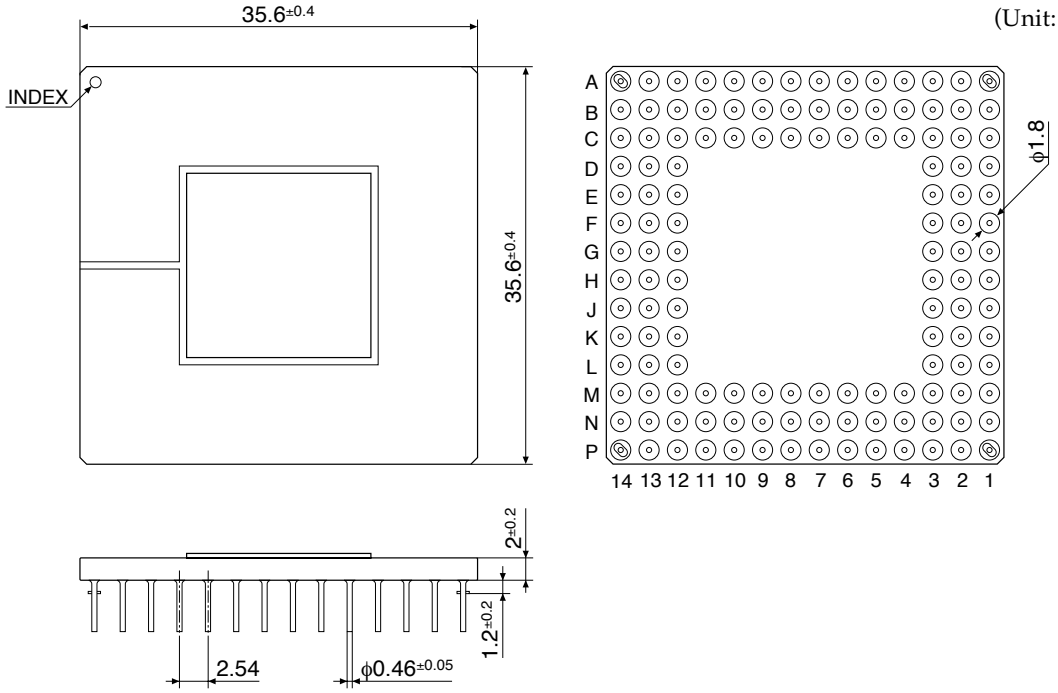
(Unit: mm)



15.2 Ceramic Package for Test Samples

PGA-132pin

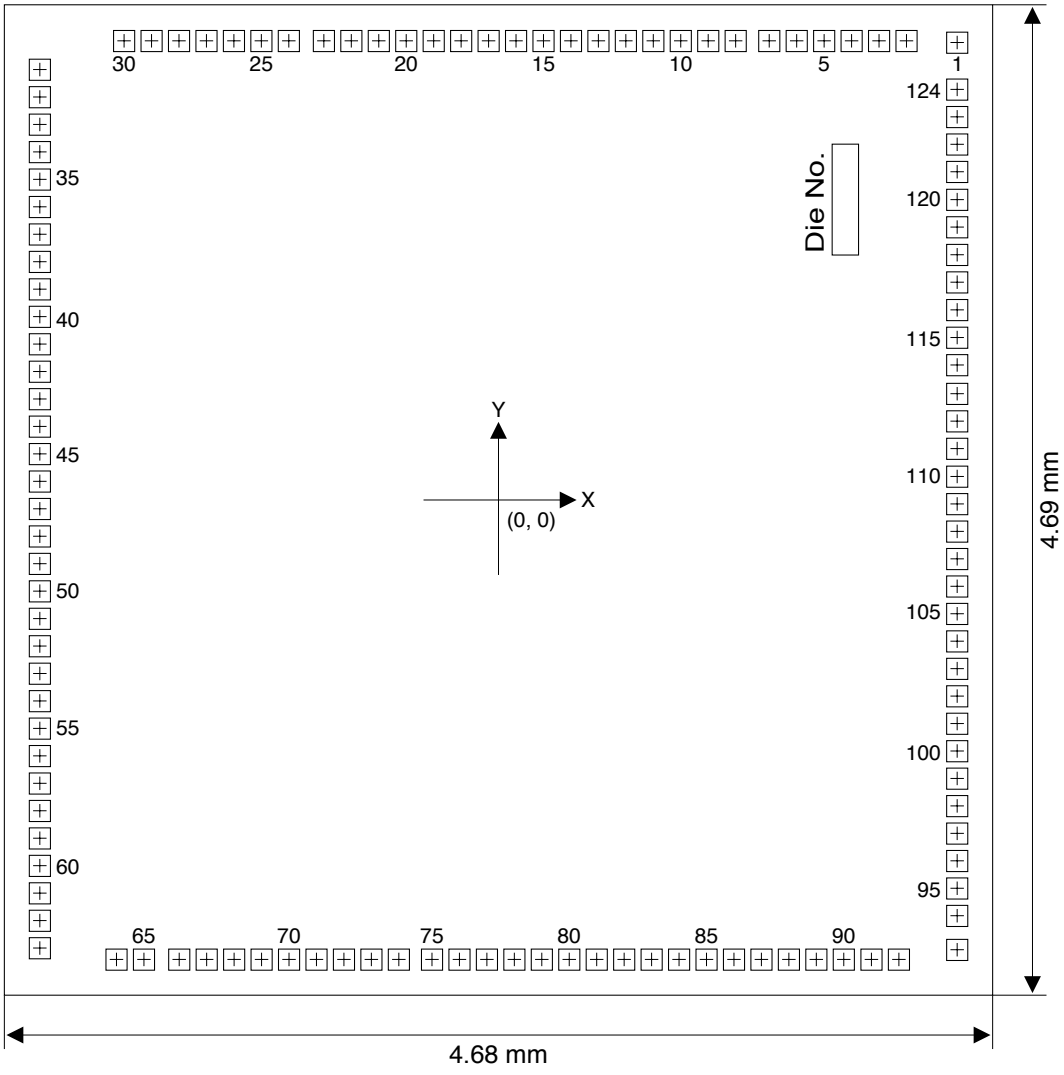
(Unit: mm)



No.	Coordinate	Name	No.	Coordinate	Name	No.	Coordinate	Name	No.	Coordinate	Name
1	C3	V_{L5}	34	M3	SEG32	67	M12	N.C.	100	C12	N.C.
2	A1	CF	35	P1	SEG31	68	P14	N.C.	101	A14	R41
3	D3	CE	36	M4	SEG30	69	L12	$\overline{SCLK}$	102	C11	R40
4	C2	CD	37	N3	SEG29	70	M13	SOUT	103	B12	R33
5	B1	CC	38	P2	SEG28	71	N14	SIN	104	A13	R32
6	C1	CB	39	P3	SEG27	72	M14	K13	105	A12	R31
7	E3	CA	40	M5	SEG26	73	K12	K12	106	C10	R30
8	D2	COM0	41	N4	SEG25	74	L13	K11	107	B11	R23
9	D1	COM1	42	P4	SEG24	75	L14	K10	108	A11	R22
10	E2	COM2	43	N5	SEG23	76	K13	K03	109	B10	R21
11	F3	COM3	44	M6	SEG22	77	J12	K02	110	C9	R20
12	E1	COM4	45	P5	SEG21	78	K14	K01	111	A10	R13
13	F2	COM5	46	N6	SEG20	79	J13	K00	112	B9	R12
14	F1	COM6	47	P6	SEG19	80	J14	P33	113	A9	R11
15	G3	COM7	48	M7	SEG18	81	H12	P32	114	C8	R10
16	G2	COM8	49	N7	SEG17	82	H13	P31	115	B8	R03
17	G1	COM9	50	P7	SEG16	83	H14	P30	116	A8	R02
18	H1	COM10	51	P8	SEG15	84	G14	P23	117	A7	R01
19	H2	COM11	52	N8	SEG14	85	G13	P22	118	B7	R00
20	H3	COM12	53	M8	SEG13	86	G12	P21	119	C7	V_{SS}
21	J1	COM13	54	P9	SEG12	87	F14	P20	120	A6	$\overline{RESET}$
22	J2	COM14	55	N9	SEG11	88	F13	P13	121	B6	$\overline{TEST}$
23	K1	COM15	56	P10	SEG10	89	E14	P12	122	A5	OSC4
24	J3	SEG39	57	M9	SEG9	90	F12	P11	123	C6	OSC3
25	K2	SEG38	58	N10	SEG8	91	E13	P10	124	B5	V_{S1}
26	L1	SEG37	59	P11	SEG7	92	D14	P03	125	A4	OSC2
27	L2	SEG36	60	N11	SEG6	93	D13	P02	126	B4	OSC1
28	K3	SEG35	61	M10	SEG5	94	E12	P01	127	C5	V_{DD}
29	M1	SEG34	62	P12	SEG4	95	C14	P00	128	A3	V_{REF}
30	N1	SEG33	63	P13	SEG3	96	B14	R43	129	A2	V_{L1}
31	M2	N.C.	64	N12	SEG2	97	C13	R42	130	B3	V_{L2}
32	L3	N.C.	65	M11	SEG1	98	D12	N.C.	131	C4	V_{L3}
33	N2	N.C.	66	N13	SEG0	99	B13	N.C.	132	B2	V_{L4}

CHAPTER 16 PAD LAYOUT

16.1 Diagram of Pad Layout



Chip size: 4.68 mm × 4.69 mm
Pad size: 0.1 mm × 0.1 mm

16.2 Pad Coordinates

(unit: μm)

Pad		Coordinate		Pad		Coordinate		Pad		Coordinate	
No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	V_{L5}	2,172	2,167	43	SEG20	-2,172	479	85	P11	985	-2,175
2	CF	1,932	2,175	44	SEG19	-2,172	349	86	P10	1,115	-2,175
3	CE	1,802	2,175	45	SEG18	-2,172	219	87	P03	1,245	-2,175
4	CD	1,672	2,175	46	SEG17	-2,172	89	88	P02	1,375	-2,175
5	CC	1,542	2,175	47	SEG16	-2,172	-41	89	P01	1,505	-2,175
6	CB	1,412	2,175	48	SEG15	-2,172	-171	90	P00	1,635	-2,175
7	CA	1,282	2,175	49	SEG14	-2,172	-301	91	R43	1,766	-2,175
8	COM0	1,123	2,175	50	SEG13	-2,172	-431	92	R42	1,896	-2,175
9	COM1	993	2,175	51	SEG12	-2,172	-561	93	R41	2,172	-2,129
10	COM2	863	2,175	52	SEG11	-2,172	-691	94	R40	2,172	-1,968
11	COM3	733	2,175	53	SEG10	-2,172	-821	95	R33	2,172	-1,838
12	COM4	603	2,175	54	SEG9	-2,172	-951	96	R32	2,172	-1,708
13	COM5	473	2,175	55	SEG8	-2,172	-1,081	97	R31	2,172	-1,578
14	COM6	343	2,175	56	SEG7	-2,172	-1,211	98	R30	2,172	-1,448
15	COM7	213	2,175	57	SEG6	-2,172	-1,341	99	R23	2,172	-1,318
16	COM8	83	2,175	58	SEG5	-2,172	-1,471	100	R22	2,172	-1,188
17	COM9	-47	2,175	59	SEG4	-2,172	-1,601	101	R21	2,172	-1,058
18	COM10	-177	2,175	60	SEG3	-2,172	-1,731	102	R20	2,172	-928
19	COM11	-307	2,175	61	SEG2	-2,172	-1,861	103	R13	2,172	-798
20	COM12	-437	2,175	62	SEG1	-2,172	-1,991	104	R12	2,172	-668
21	COM13	-567	2,175	63	SEG0	-2,172	-2,121	105	R11	2,172	-538
22	COM14	-697	2,175	64	$\overline{SCLK}$	-1,809	-2,175	106	R10	2,172	-408
23	COM15	-827	2,175	65	SOUT	-1,679	-2,175	107	R03	2,172	-278
24	SEG39	-993	2,175	66	SIN	-1,512	-2,175	108	R02	2,172	-148
25	SEG38	-1,123	2,175	67	K13	-1,382	-2,175	109	R01	2,172	-18
26	SEG37	-1,253	2,175	68	K12	-1,252	-2,175	110	R00	2,172	112
27	SEG36	-1,383	2,175	69	K11	-1,122	-2,175	111	V_{SS}	2,172	244
28	SEG35	-1,513	2,175	70	K10	-992	-2,175	112	$\overline{RESET}$	2,172	374
29	SEG34	-1,643	2,175	71	K03	-862	-2,175	113	$\overline{TEST}$	2,172	504
30	SEG33	-1,773	2,175	72	K02	-732	-2,175	114	OSC4	2,172	640
31	SEG32	-2,172	2,039	73	K01	-602	-2,175	115	OSC3	2,172	770
32	SEG31	-2,172	1,909	74	K00	-472	-2,175	116	V_{S1}	2,172	901
33	SEG30	-2,172	1,779	75	P33	-315	-2,175	117	OSC2	2,172	1,032
34	SEG29	-2,172	1,649	76	P32	-185	-2,175	118	OSC1	2,172	1,162
35	SEG28	-2,172	1,519	77	P31	-55	-2,175	119	V_{DD}	2,172	1,293
36	SEG27	-2,172	1,389	78	P30	75	-2,175	120	V_{REF}	2,172	1,423
37	SEG26	-2,172	1,259	79	P23	205	-2,175	121	V_{L1}	2,172	1,555
38	SEG25	-2,172	1,129	80	P22	335	-2,175	122	V_{L2}	2,172	1,685
39	SEG24	-2,172	999	81	P21	465	-2,175	123	V_{L3}	2,172	1,815
40	SEG23	-2,172	869	82	P20	595	-2,175	124	V_{L4}	2,172	1,945
41	SEG22	-2,172	739	83	P13	725	-2,175				
42	SEG21	-2,172	609	84	P12	855	-2,175				

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