EPSON

E0C6S46

4-bit Single Chip Microcomputer

Wide Voltage Operation Products

- Core CPU Architecture
- Dot Matrix LCD Driver
- Programmable SVD Circuit/Sound Generator

■ DESCRIPTION

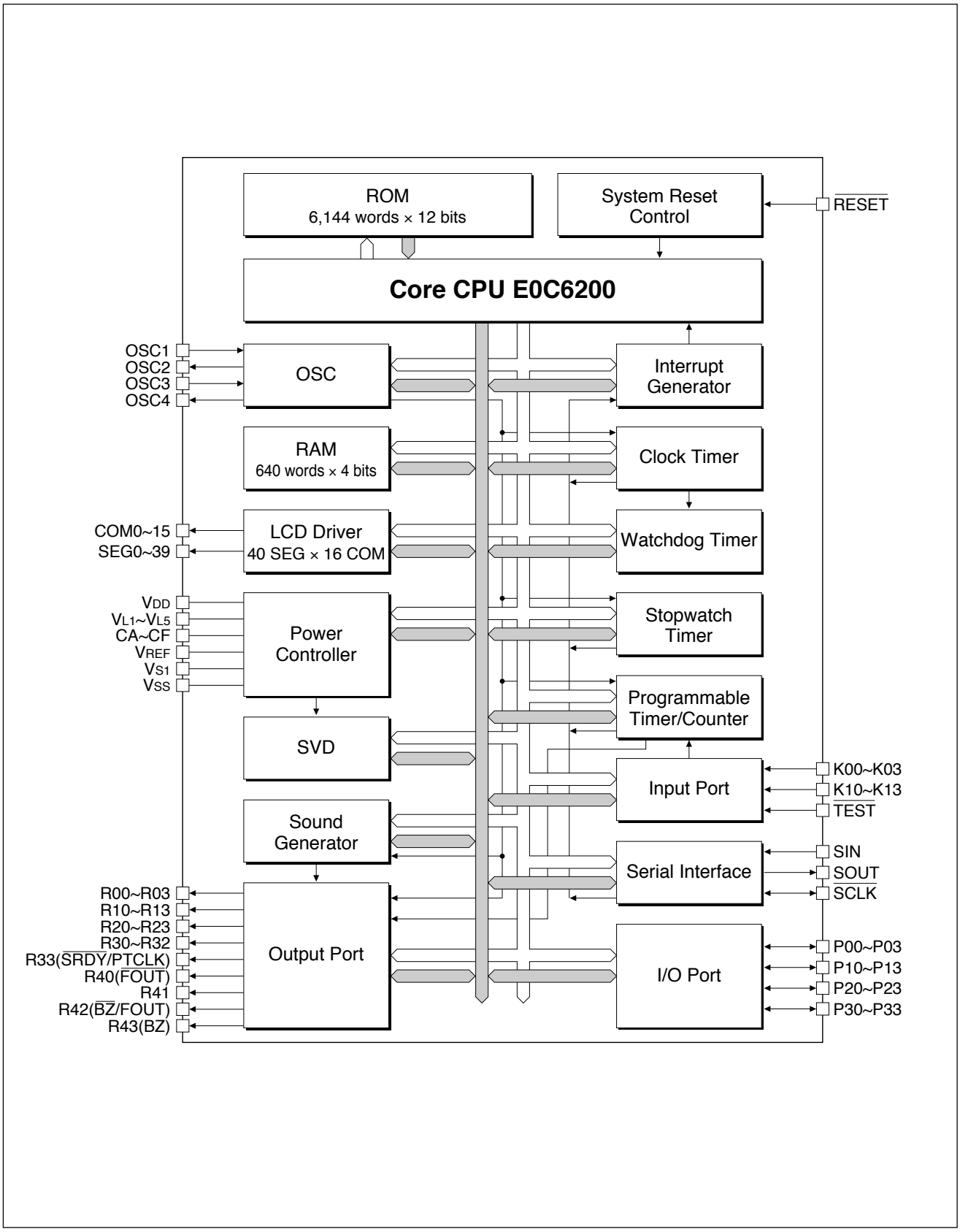
The E0C6S46 is an advanced single-chip CMOS 4-bit microcomputer consisting of the E0C6200 4-bit core CPU. The chip contains the ROM, RAM, dot matrix LCD driver, programmable SVD circuit, time base counter and clock synchronous serial port. The E0C6S46 can be applied to any system requiring large memory such as schedule reminder, and dot matrix display function.

■ FEATURES

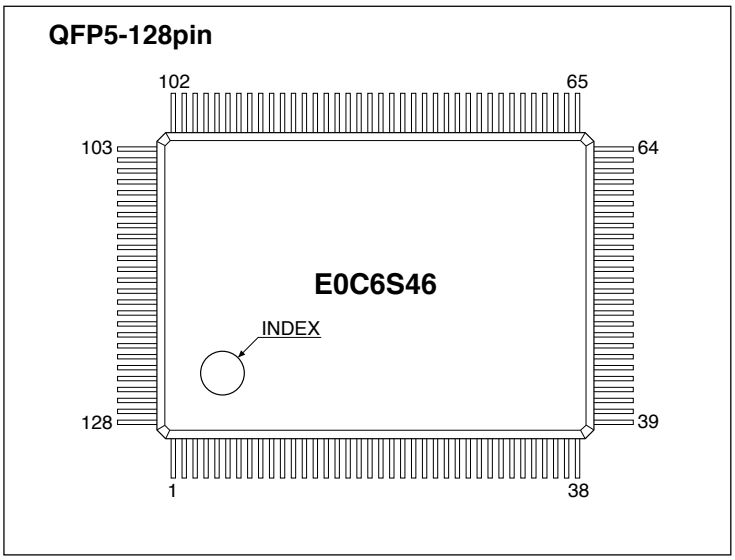
- CMOS LSI 4-bit parallel processing
- Oscillation circuit ..... OSC1 : 32.768kHz (Typ.) Crystal oscillation circuit
  OSC3 : 2MHz (Max.) CR or ceramic oscillation circuit (∗1)
- Instruction set ..... 108 instructions
- Instruction execution time ..... 32.768kHz : 152.6μsec, 213.6μsec, 366.2μsec
  (depending on the instruction) 1MHz : 5.0μsec, 7.0μsec, 12.0μsec
  2MHz : 2.5μsec, 3.5μsec, 6.0μsec
- ROM capacity ..... 6,144 words × 12 bits
- RAM capacity ..... Data memory : 640 words × 4 bits
  Display memory : 160 words × 4 bits
- Input port ..... 8 bits (pull-up resistors may be supplemented ∗1)
- Output port ..... 20 bits (buzzer and clock outputs are possible ∗1)
- I/O port ..... 16 bits
- Serial interface ..... 8-bit clock synchronous system × 1 ch.
- Dot matrix type LCD driver ..... 40 segments × 16 or 8 commons (∗2)
- Time base counter ..... Clock timer, stopwatch timer
- Programmable timer ..... 8-bit timer × 1 ch., with event counter and clock output functions
- Watchdog timer ..... Built-in
- Sound generator ..... 8 programmable sounds (8 types of frequency)
  with envelope and 1-shot output functions
- Supply voltage detection (SVD) ..... -2.2, -2.5, -3.1, -4.2V programmable (V_{DD} standard)
- Interrupts ..... External : Input port interrupt 2 systems
  Internal : Clock timer interrupt 1 system
  Stopwatch timer interrupt 1 system
  Programmable timer interrupt 1 system
  Serial interface interrupt 1 system
- Power supply voltage ..... 2.2V to 5.5V (Min. 1.8V when the OSC3 oscillation circuit is not used)
- Operating temperature range ..... -20°C to 70°C
- Current consumption (Typ.) ..... HALT mode : 32.768kHz (crystal oscillation), 3.0V 2.5μA
  OPERATING mode : 32.768kHz (crystal oscillation), 3.0V 6.5μA
  2MHz (CR oscillation), 3.0V 1mA
- Package ..... QFP5-128pin (plastic) or chip

∗1: Can be selected with mask option ∗2: Can be selected with software

■ BLOCK DIAGRAM



■ PIN CONFIGURATION



No.	Pin name	No.	Pin name	No.	Pin name	No.	Pin name
1	V_{L3}	33	SEG33	65	SEG2	97	R42
2	V_{L4}	34	N.C.	66	SEG1	98	N.C.
3	V_{L5}	35	SEG32	67	SEG0	99	R41
4	CF	36	SEG31	68	$\overline{SCLK}$	100	R40
5	N.C.	37	SEG30	69	N.C.	101	R33
6	CE	38	SEG29	70	SOUT	102	R32
7	CD	39	SEG28	71	SIN	103	R31
8	CC	40	SEG27	72	K13	104	R30
9	CB	41	SEG26	73	K12	105	R23
10	CA	42	SEG25	74	K11	106	R22
11	COM0	43	SEG24	75	K10	107	R21
12	COM1	44	SEG23	76	K03	108	R20
13	COM2	45	SEG22	77	K02	109	R13
14	COM3	46	SEG21	78	K01	110	R12
15	COM4	47	SEG20	79	K00	111	R11
16	COM5	48	SEG19	80	P33	112	R10
17	COM6	49	SEG18	81	P32	113	R03
18	COM7	50	SEG17	82	P31	114	R02
19	COM8	51	SEG16	83	P30	115	R01
20	COM9	52	SEG15	84	P23	116	R00
21	COM10	53	SEG14	85	P22	117	V_{SS}
22	COM11	54	SEG13	86	P21	118	$\overline{RESET}$
23	COM12	55	SEG12	87	P20	119	$\overline{TEST}$
24	COM13	56	SEG11	88	P13	120	OSC4
25	COM14	57	SEG10	89	P12	121	OSC3
26	COM15	58	SEG9	90	P11	122	V_{S1}
27	SEG39	59	SEG8	91	P10	123	OSC2
28	SEG38	60	SEG7	92	P03	124	OSC1
29	SEG37	61	SEG6	93	P02	125	V_{DD}
30	SEG36	62	SEG5	94	P01	126	V_{REF}
31	SEG35	63	SEG4	95	P00	127	V_{L1}
32	SEG34	64	SEG3	96	R43	128	V_{L2}

N.C. = No Connection

■ PIN DESCRIPTION

Pin name	Pin No.	I/O	Function	
V_{DD}	125	–	Power supply (+)	
V_{SS}	117	–	Power supply (-)	
V_{S1}	122	–	Internal logic system/oscillation system regulated voltage output	
V_{L1}–V_{L5}	127, 128, 1–3	–	LCD system power supply 1/4 bias generated internally, 1/5 bias generated externally *1	
V_{REF}	126	O	LCD system power test pin *2	
CA–CF	10–6, 4	–	LCD system voltage booster condenser connecting pin	
OSC1	124	I	Crystal oscillator input	
OSC2	123	O	Crystal oscillator output, C_D buiil-in	
OSC3	121	I	CR or ceramic oscillator input *1	
OSC4	120	O	CR or ceramic oscillator output *1	
COM0–COM15	11–26	O	LCD common output (1/8 duty or 1/16 duty is selected on software)	
SEG0–SEG39	67–35, 33–27	O	LCD segment output	
K00–K03	79–76	I	Input port (pull up resistor is available by mask option) *1	
K10–K13	75–72	I	Input port (pull up resistor is available by mask option) *1	
P00–P03	95–92	I/O	I/O port	Complementary output or
P10–P13	91–88	I/O	I/O port	Nch open drain output *1
P20–P23	87–84	I/O	I/O port	
P30–P33	83–80	I/O	I/O port or output port *1	
R00–R03	116–113	O	Output port	
R10–R13	112–109	O	Output port	
R20–R23	108–105	O	Output port	
R30–R32	104–102	O	Output port	
R33	101	O	Output port, $\overline{SRDY}$ output or PTCLK output *1	
R40	100	O	Output port or $\overline{FOUT}$ output *1	
R41	99	O	Output port	
R42	97	O	Output port, $\overline{BZ}$ output or FOUT output *1	
R43	96	O	Output port or BZ output *1	
SIN	71	I	Serial interface data input	
SOUT	70	O	Serial interface data output	
$\overline{SCLK}$	68	I/O	Serial interface clock input/output	
$\overline{RESET}$	118	I	Initial reset input terminal	
$\overline{TEST}$	119	I	Testing input terminal *3	

*1 Selected by mask option

*2 Leave the V_{REF} pin unconnected (N.C.).

*3 The $\overline{TEST}$ pin is used when the IC load is being detected. During ordinary operation be certain to connect this pin to V_{DD}.

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{DD}=0V)

Rating	Symbol	Value	Unit
Supply voltage	V_{SS}	-7.0 to 0.5	V
Input voltage (1)	V_I	V_{SS} - 0.3 to 0.5	V
Input voltage (2)	V_{IOSC}	V_{S1} - 0.3 to 0.5	V
Permissible total output current *1	ΣI_{VSS}	10	mA
Operating temperature	Topr	-20 to 70	°C
Storage temperature	Tstg	-65 to 150	°C
Soldering temperature / time	Tsol	260°C, 10sec (lead section)	–
Permissible dissipation *2	P_D	250	mW
Electrostatic proof pressure	V_E	EIAJ test method (C=200pF) 150V or more MIL test method (C=100pF, R=1.5kΩ) 900V or more	V

*1: The permissible total output current is the sum total of the current (average current) that simultaneously flows from the output pins (or is draw in).
*2: In case of plastic package.

● Recommended Operating Conditions

(Ta=-20 to 70°C)

Condition	Symbol	Remark		Min.	Typ.	Max.	Unit
Supply voltage	V_{SS}	V_{DD}=0V	VSC="0"	-3.8	-3.0	-1.8	V
			VSC="1"	-5.5	-3.0	-2.2	V
			VSC="2"	-5.5	-5.0	-3.5	V
Oscillation frequency (1)	f_{OSC1}			20	32.768	50	kHz
Oscillation frequency (2)	f_{OSC3}	VSC="1"		50	1,000	1,200	kHz
Oscillation frequency (3)	f_{OSC3}	VSC="2"		50	2,000	2,300	kHz
Voltage booster capacitor (1)	C_1				0.1		µF
Voltage booster capacitor (2)	C_2				0.1		µF
Voltage booster capacitor (3)	C_3				0.1		µF
Capacitor between V_{DD} and V_{L1}	C_4				0.1		µF
Capacitor between V_{DD} and V_{L2}	C_5				0.1		µF
Capacitor between V_{DD} and V_{L4}	C_6				0.1		µF
Capacitor between V_{DD} and V_{L5}	C_7				0.1		µF
Capacitor between V_{DD} and V_{S1}	C_8				0.1		µF

● DC Characteristics

(Unless otherwise specified: V_{DD}=0V,V_{SS}=-3.0V,V_{L1}=-1.0V,V_{L2}=-2.0V,V_{L4}=-3.0V,V_{L5}=-4.0V,f_{OSC1}=32.768kHz,f_{OSC3}=1MHz,Ta=25°C,C_1–C_8=0.047µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
High level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V	K00–03•10–13, P00–03•10–13	0.2•V_{SS}		0	V
Low level input voltage	V_{LIN}	Ta=25°C	P20–P23•30–33, SIN, $\overline{SCLK}$	V_{SS}		0.8•V_{SS}	V
High level input voltage	V_{HIN}	V_{SS}=-2.2 to -5.5V	$\overline{RESET}$	-0.2		0	V
Low level input voltage	V_{LIN}	Ta=25°C		V_{SS}		V_{SS}+0.2	V
High level input current	I_{IH}	V_{SS}=-3.0V V_{IH}=0V	K00–03•10–13, P00–03•10–13 P20–P23•30–33, SIN, $\overline{SCLK}$ $\overline{RESET}$	0		0.5	µA
Low level input current (1)	I_{IL1}	V_{SS}=-3.0V V_{IL1}=V_{SS} With pull-up resistor	K00–03•10–13, P00–03•10–13 P20–P23•30–33, SIN, $\overline{SCLK}$ $\overline{RESET}$	-45		-15	µA
Low level input current (2)	I_{IL2}	V_{SS}=-3.0V V_{IL2}=V_{SS} No pull-up resistor	K00–03•10–13, P00–03•10–13 P20–P23•30–33, SIN, $\overline{SCLK}$ $\overline{RESET}$	-0.5		0	µA
High level output current (1)	I_{OH1}	V_{SS}=-2.2V V_{OH1}=-0.5V	P00–03•10–13•20–23•30–33 R00–03•10–13•20–23•30–33 R40•41, SOUT, $\overline{SCLK}$			-1.0	mA
Low level output current (1)	I_{OL1}	V_{SS}=-2.2V V_{OL1}=V_{SS}+0.5V	P00–03•10–13•20–23•30–33 R00–03•10–13•20–23•30–33 R40•41, SOUT, $\overline{SCLK}$	2.0			mA
High level output current (2)	I_{OH2}	V_{SS}=-2.2V V_{OH2}=-0.5V	R42•43			-2.0	mA
Low level output current (2)	I_{OL2}	V_{SS}=-2.2V V_{OL1}=V_{SS}+0.5V	R42•43	4.0			mA
Common output current	I_{OH3}	V_{OH3}=-0.05V	COM0–15			-30	µA
	I_{OL3}	V_{OL3}=V_{L5}+0.05V		30			µA
Segment output current	I_{OH4}	V_{OH4}=-0.05V	SEG0–39			-10	µA
	I_{OL4}	V_{OL4}=V_{L5}+0.05V		10			µA

● Analog Circuit Characteristics and Current Consumption

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, V_{L1}=-1.0V, V_{L2}=-2.0V, V_{L4}=-3.0V, V_{L5}=-4.0V, f_{OSC1}=32.768kHz, f_{OSC3}=1MHz, Ta=25°C, C_1–C_8=0.047µF)

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
LCD drive voltage (Normal mode)	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)		1/2·V_{L2} -0.1		1/2·V_{L2} ×0.95	V
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)	LC="0"	Typ. ×1.12	-1.80	Typ. ×0.88	V
			LC="1"		-1.85		
			LC="2"		-1.90		
			LC="3"		-1.95		
			LC="4"		-2.01		
			LC="5"		-2.06		
			LC="6"		-2.11		
			LC="7"		-2.17		
			LC="8"		-2.22		
			LC="9"		-2.27		
			LC="10"		-2.32		
			LC="11"		-2.38		
			LC="12"		-2.43		
			LC="13"		-2.48		
			LC="14"		-2.53		
			LC="15"		-2.59		
	V_{L4}	Connects a 1MΩ load resistance between V_{DD} and V_{L4} (No panel load)		3/2·V_{L2}		3/2·V_{L2} ×0.95	V
	V_{L5}	Connects a 1MΩ load resistance between V_{DD} and V_{L5} (No panel load)		2·V_{L2}		2·V_{L2} ×0.95	V
LCD drive voltage (Heavy load protection mode)	V_{L1}	Connects a 1MΩ load resistance between V_{DD} and V_{L1} (No panel load)	LC="0"	Typ. ×1.12	-0.92	Typ. ×0.88	V
			LC="1"		-0.95		
			LC="2"		-0.97		
			LC="3"		-1.00		
			LC="4"		-1.03		
			LC="5"		-1.05		
			LC="6"		-1.08		
			LC="7"		-1.11		
			LC="8"		-1.13		
			LC="9"		-1.16		
			LC="10"		-1.18		
			LC="11"		-1.21		
			LC="12"		-1.24		
			LC="13"		-1.26		
			LC="14"		-1.29		
			LC="15"		-1.32		
	V_{L2}	Connects a 1MΩ load resistance between V_{DD} and V_{L2} (No panel load)		2·V_{L1}		2·V_{L1} ×0.90	V
	V_{L4}	Connects a 1MΩ load resistance between V_{DD} and V_{L4} (No panel load)		3·V_{L1}		3·V_{L1} ×0.90	V
	V_{L5}	Connects a 1MΩ load resistance between V_{DD} and V_{L5} (No panel load)		4·V_{L1}		4·V_{L1} ×0.90	V
SVD voltage	V_{SVD0}	SVC="0"		-2.35	-2.20	-2.05	V
	V_{SVD1}	SVC="1"		-2.70	-2.50	-2.30	V
	V_{SVD2}	SVC="2"		-3.30	-3.10	-2.90	V
	V_{SVD3}	SVC="3"		-4.50	-4.20	-3.90	V
SVD circuit response time	t_{SVD}					100	µs
Current consumption *1 (OSC1/crystal oscillation)	I_{Halt}	During HALT (VSC="0", OSCC="0")			2.5	5.0	µA
	I_{EX1}	During operation at 32kHz (VSC="0", OSCC="0")			6.5	9.0	µA
	I_{EX2}	During operation at 1MHz (VSC="1")			400	600	µA
	I_{EX3}	During operation at 2MHz (VSC="2", V_{SS}=-5.0V)			1,000	1,500	µA

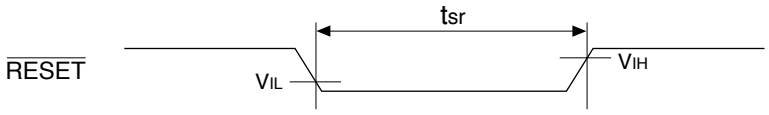
*1: No panel loard. The SVD circuit is in OFF status.

● AC Characteristics

$\overline{\text{RESET}}$ Input

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C, V_{IH}=0.5V_{SS}, V_{IL}=0.9V_{SS})

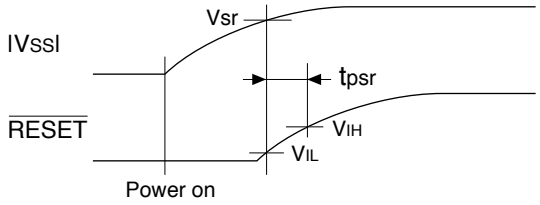
Characteristic	Symbol	Min.	Typ.	Max.	Unit
$\overline{\text{RESET}}$ input time	tsr	2.0			ms

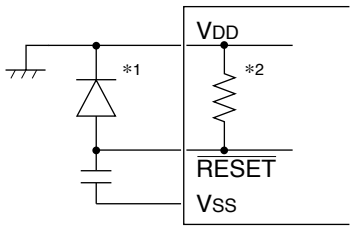


Power-on Reset

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, f_{OSC1}=32.768kHz, Ta=25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Operating power voltage	Vsr	-2.2			V
$\overline{\text{RESET}}$ input time	tpsr	2.0			ms





*1 Because the potential of the $\overline{\text{RESET}}$ terminal not reached V_{DD} level or higher.

*2 Built-in pull-up resistor

● Oscillation Characteristics

The oscillation characteristics change depending on the conditions (components used, board pattern, etc.). Use the following characteristics as reference values.

OSC1 Crystal Oscillation Circuit

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Crystal: C-002R(C_I=35kΩ), C_{GX}=25pF, C_{DX}=built-in, Rfx=10MΩ, Ta=25°C, VSC="0")

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			5	s
Built-in drain capacitance	C_D	Package as assembled		20		pF
		Bare chip		19		pF
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V			5	ppm
Frequency/IC deviation	∂f/∂IC		-10		10	ppm
Frequency adjustable range	∂f/∂C_G	C_G=5 to 25pF	35	45		ppm
Harmonic oscillation start voltage	V_{hho}	C_G=5pF (V_{SS})			-5.5	V
Permitted leak resistance	R_{leak}	Between OSC1 and V_{DD}, V_{S1}	200			MΩ

OSC3 CR Oscillation Circuit (1)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="1")

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}	R_{CR2}=60kΩ	Typ. ×70%	1,000	Typ. ×130%	kHz
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			10	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-5		+5	%

OSC3 CR Oscillation Circuit (2)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-5.0V, Ta=25°C, VSC="2")

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation frequency	f_{OSC3}	R_{CR2}=30kΩ	Typ. ×70%	2.0	Typ. ×130%	MHz
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			10	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-3.5 to -5.5V	-5		+5	%

OSC3 Ceramic Oscillation Circuit (1)

(Unless otherwise specified: V_{DD}=0V, V_{SS}=-3.0V, Ta=25°C, VSC="1", Ceramic oscillator: CSB 1000J *1 (1MHz), C_{GC}=C_{DC}=100pF, Rfc=1MΩ)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-2.2 to -5.5V			10	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-2.2 to -5.5V	-3		+3	%

*1: Made by Murata Mfg. Co.

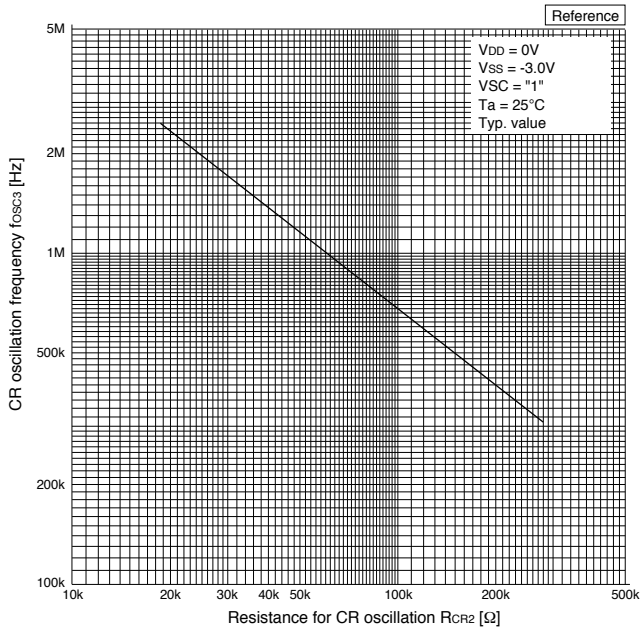
OSC3 Ceramic Oscillation Circuit (2)

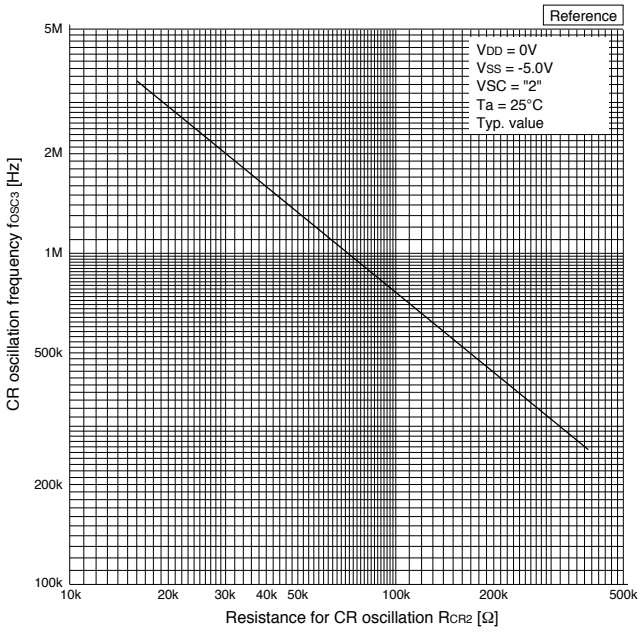
(Unless otherwise specified: V_{DD}=0V, V_{SS}=-5.0V, Ta=25°C, VSC="2", Ceramic oscillator: CSA 2.00MG *1 (2MHz), C_{GC}=C_{DC}=100pF, Rfc=1MΩ)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Oscillation start time	tsta	V_{SS}=-3.5 to -5.5V			10	ms
Frequency/voltage deviation	∂f/∂V	V_{SS}=-3.5 to -5.5V	-3		+3	%

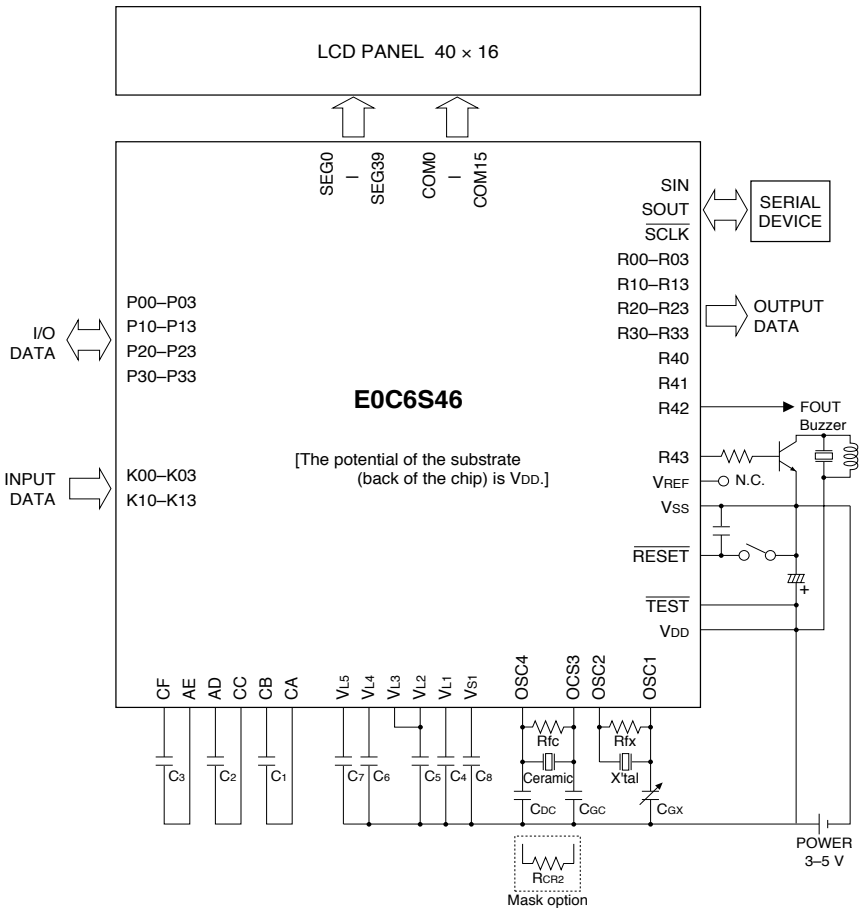
*1: Made by Murata Mfg. Co.

OSC3 CR oscillation frequency - reference characteristics





■ BASIC EXTERNAL CONNECTION DIAGRAM



X'tal	Crystal oscillator	32.768 kHz, CI(Max)=35 kΩ
Rfx	Feedback resistor	10 MΩ
CGX	Trimmer capacitor	5–25 pF
Ceramic	Ceramic oscillator	500 kHz–2 MHz
Rfc	Feedback resistor	1 MΩ
CGC	Gate capacitor	100 pF
CDC	Drain capacitor	100 pF
(RCR2)	Resistor for OSC3 CR oscillation	20 kΩ–100 kΩ (VSC=2) 40 kΩ–100 kΩ (VSC=1)

C1	Booster capacitor (1)	0.1µF ∗1
C2	Booster capacitor (2)	0.1µF ∗1
C3	Booster capacitor (3)	0.1µF ∗1
C4	Capacitor between VDD and VL1	0.1µF ∗1
C5	Capacitor between VDD and VL2	0.1µF ∗1
C6	Capacitor between VDD and VL4	0.1µF ∗1
C7	Capacitor between VDD and VL5	0.1µF ∗1
C8	Capacitor between VDD and VS1	0.1µF

∗1 When the load on the liquid crystal system is large, increase the capacitance of the voltage booster capacitors (C1–C3) and the capacitors between VDD and liquid crystal system power (C4–C7).

Note: The above table is simply an example, and is not guaranteed to work.

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