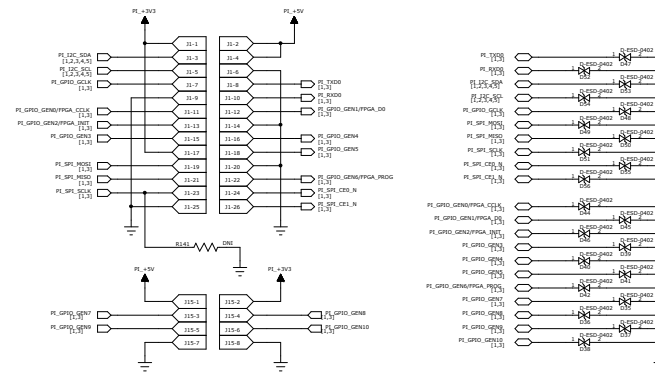
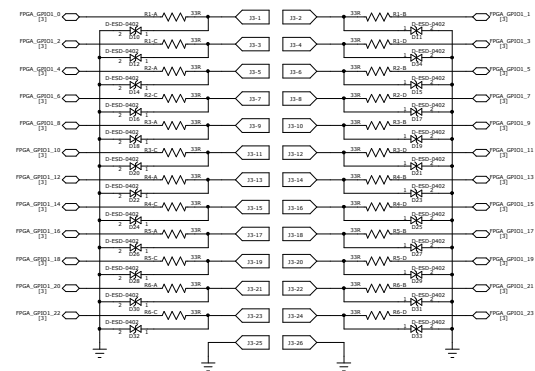


RASPBERRY PI INTERFACE

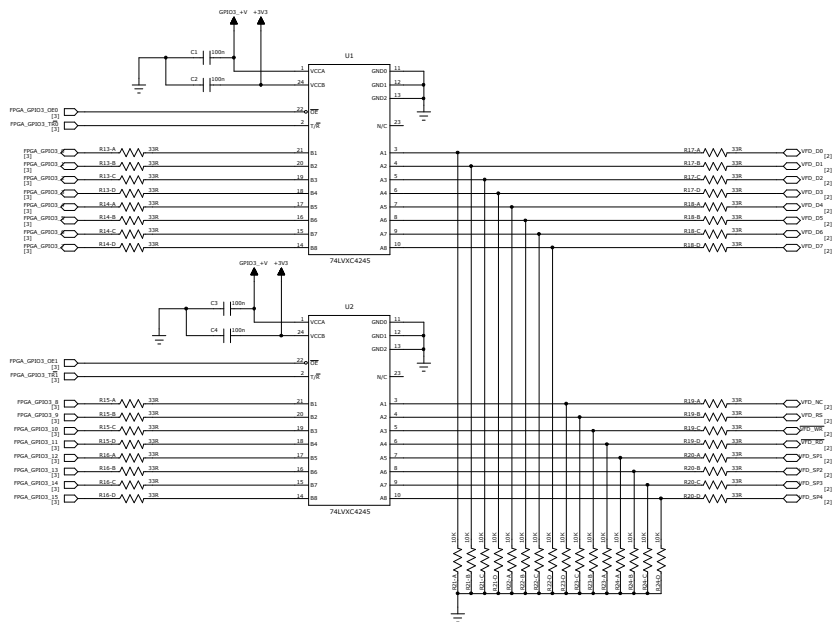


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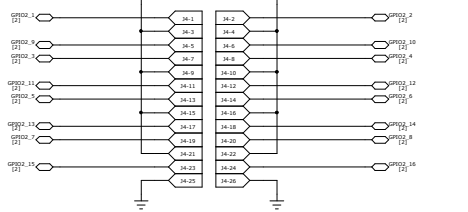
GPIO1 Connector (3V GPIO)



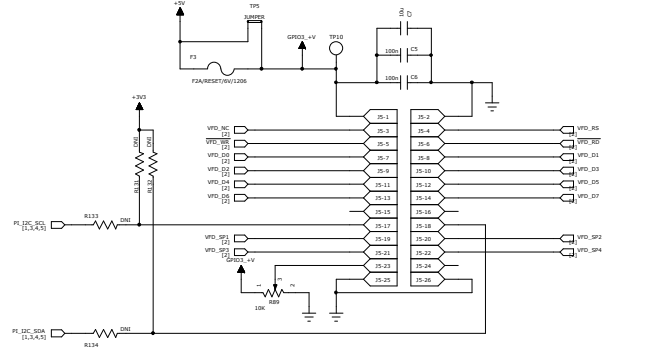
GPIO3 / LCD / VACUUM FLORESCENT DISPLAY (5V GPIO)



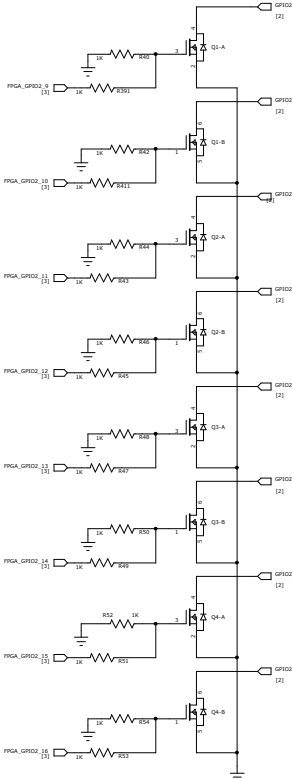
GPIO2 Connector (5V or 3.3V O-C Outputs)



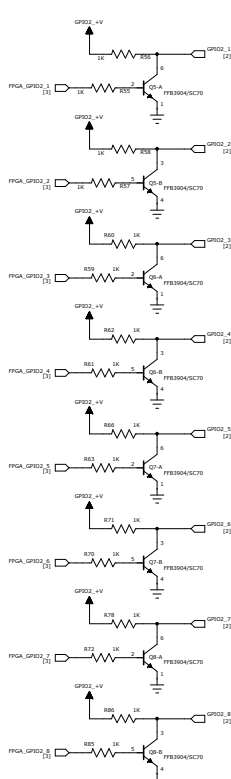
GPIO3 Connector (VFD / LCD / 5V GPIO)



5V (2A) / O-C GPIO



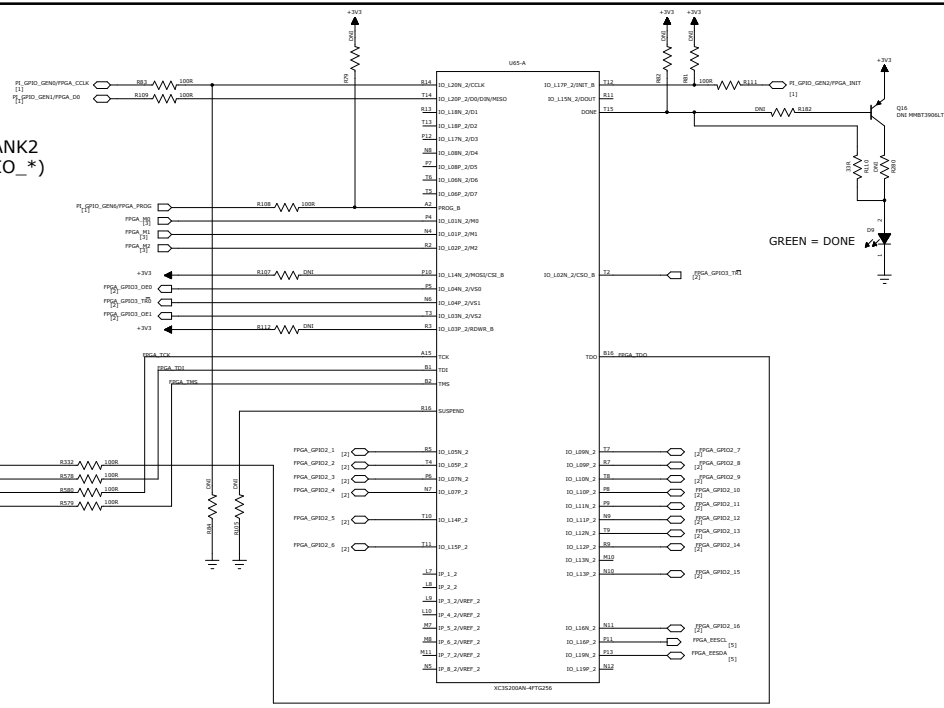
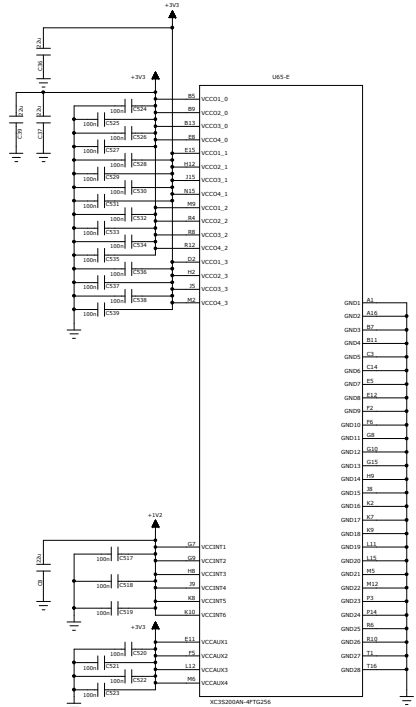
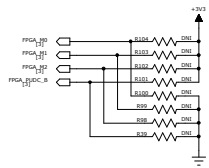
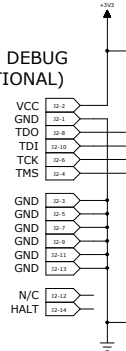
5V / O-C GPIO



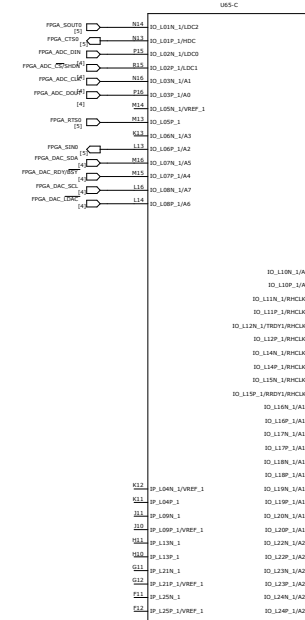
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Bank2 (Bottom) User IOs
GPIO2* Fully swappable within BANK2
(DO NOT USE Pins IP_*, use only IO_*)

JTAG DEBUG
(OPTIONAL)

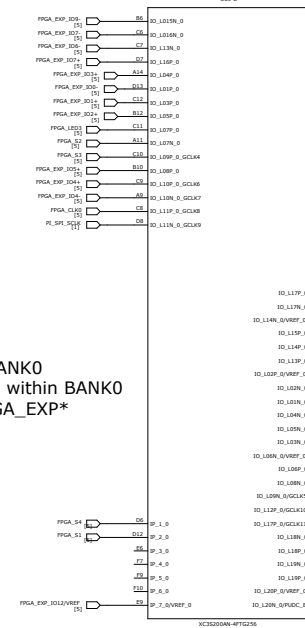


Bank1 (Right) User IOs
PI_* fully swappable within BANK0
Do not move PI_SPI_SCLK
Do not move PI_GPIO_GCLK
Do not move FPGA_CLK0

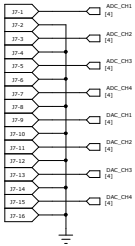
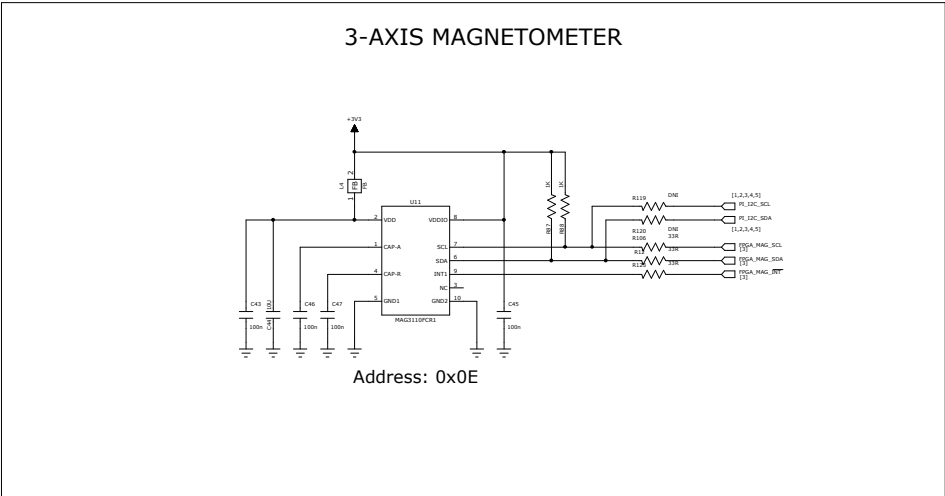
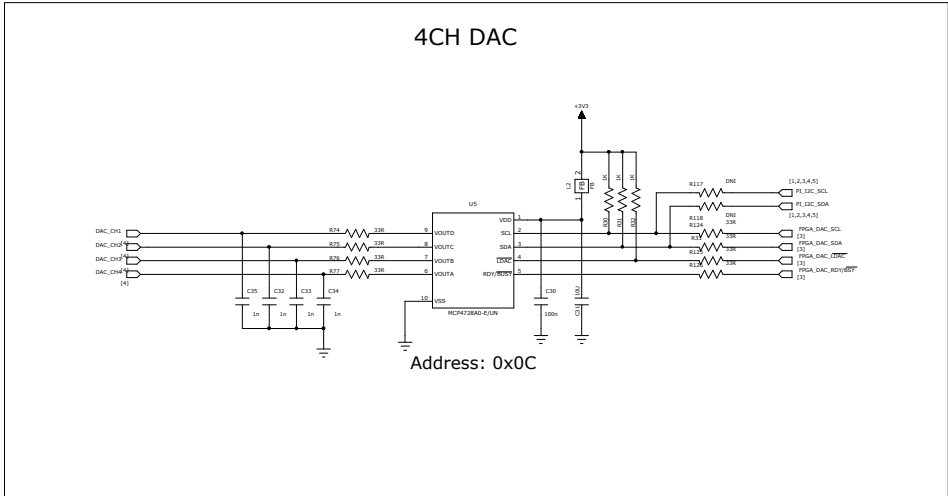
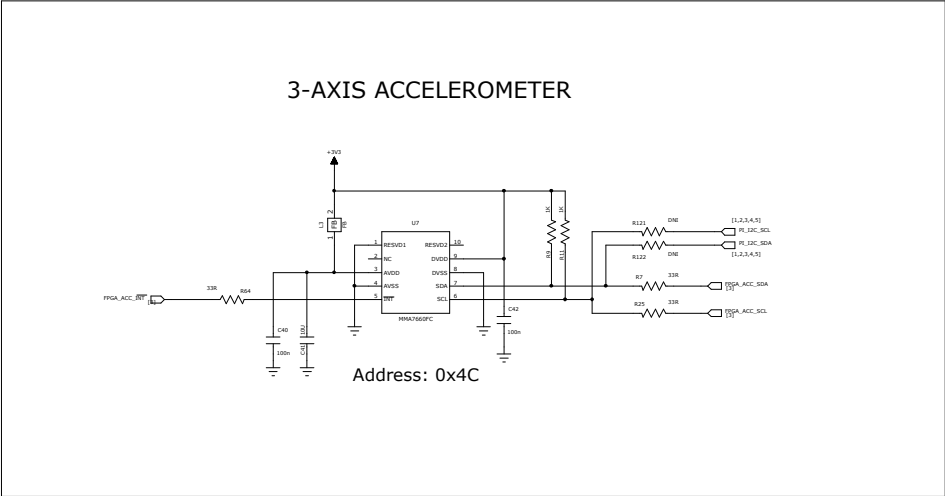
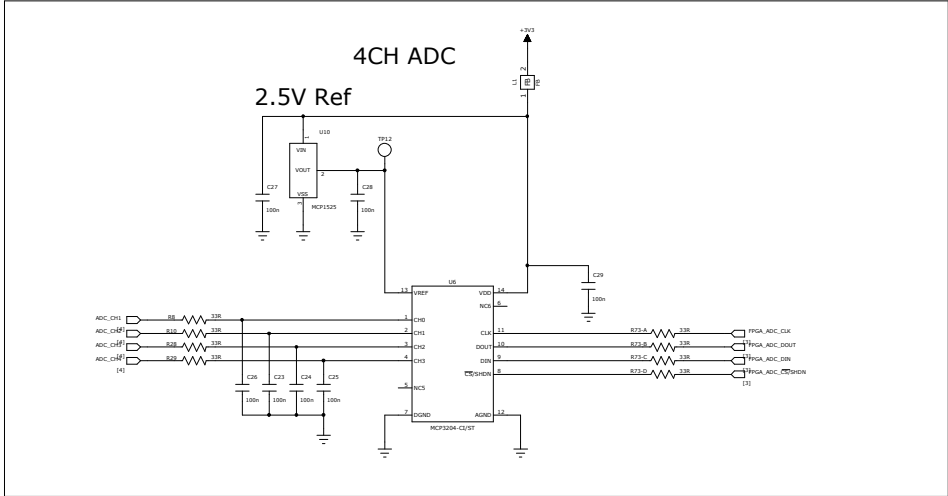


Bank3 (Left) User IOs
GPIO3 fully swappable within BANK2
Do not use IP_* pins

Bank0 (Top) User IOs
SW* Fully swappable within BANK0
FPGA_EXP_IO* Fully swappable in pairs within BANK0
Do not interchange SW* with FPGA_EXP*



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The diagram illustrates an I2C interface circuit. On the left, an FPGA provides two I2C master outputs: `FFGA_FESCL [15]` and `FFGA_FESDA [15]`. These signals pass through 8113 and 8114 pull-up resistors, respectively, to a common I2C bus. The bus is also connected to the `SCL` and `SDA` pins of two EEPROMs: an `AT24C02B-1R` (labeled USB) and an `AT24C02A-2.7` (labeled USB). Both EEPROMs have their `VCC` pins connected to a +3.3V supply and their `GND` pins connected to ground. The `CS` (chip select) pins of both EEPROMs are connected to ground. The `CS` pin of the `AT24C02A-2.7` is also connected to a 10k pull-up resistor to the +3.3V supply. The I2C address for both devices is 0x0A, as indicated by the text "I2C Address: 0x0A".

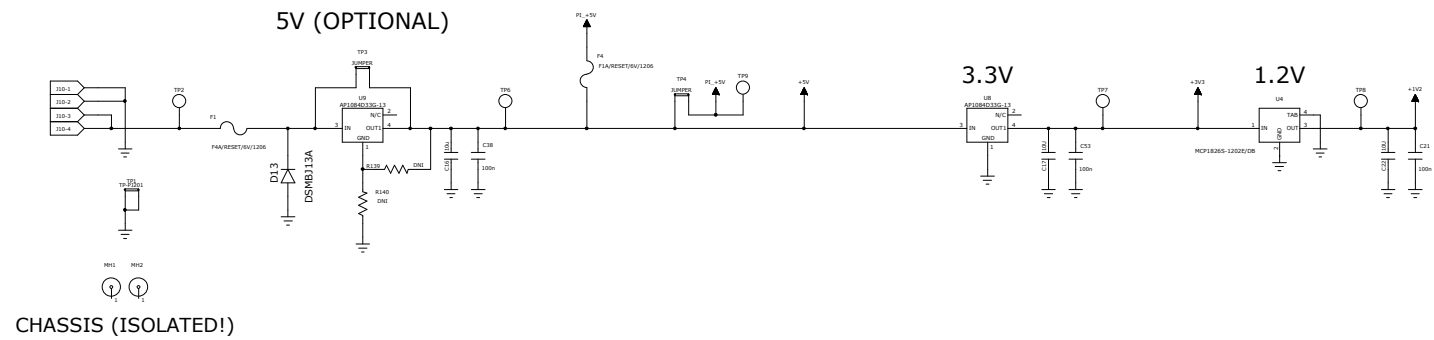
33MHZ OSCILLATOR

The diagram shows a 33MHz oscillator circuit. A crystal oscillator module (X1, 33.333MHz) is connected to a 33pF capacitor (C4) and a 10k resistor (R69). The oscillator is powered by a 3.3V supply and grounded to GND. The output of the oscillator is connected to the FPGA_CLK0 pin of the FPGA device.

SWITCHES

The diagram shows a 4-bit digital-to-analog converter circuit. It features four input lines, each labeled with a component name and a value in brackets: FPGA_51 (1), FPGA_52 (1), FPGA_53 (1), and FPGA_54 (1). Each input line is connected to a switch. The switches are controlled by resistors: FPGA_51 has a 330k resistor, FPGA_52 has a 33k resistor, FPGA_53 has a 330k resistor, and FPGA_54 has a 33k resistor. The other end of each resistor is connected to a common ground. The switches are connected to a common output line that leads to a +5V supply. The output line is also connected to a 10k resistor, which is connected to ground. The output line is labeled '1' in brackets.

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