AND				
	а	b	output	
	0	0	0	
	0	1	0	
	1	0	0	
	1	1	1	
NOT				
	in	out		
	1	0		
	0	1		
OR				
	а	b	out	
	0	0	0	
	1	0	1	
	0	1	1	
	1	1	1	
XOR				
	а	b	out	
	0	0	0	
	1	0	1	
	0	1	1	
	1	1	0	
MUX		_	_	
	а	b	sel	out
	0	0	0	0
	0	0	1	0
	0	1	0	0
	0	1	1	1
	1	0	0	1
	1	0	1	0
	1	1	0	1
	1	1	1	1
DMIN				
DMUX	•	1	_	
	in	sel	a	b
	0	0	0	0
	0	1	0	0
	1	0	1	0
	1	1	0	1