Ahsanullah University of Science & Technology
Department of Computer Science & Engineering
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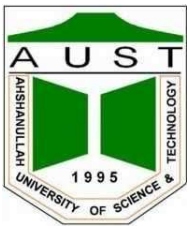

Digital System Design Lab

CSE 3110

Submitted By:

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Introduction:

An arithmetic and logic unit (ALU) is a combinational digital electronics circuit that performs arithmetical and logical operations on integer binary numbers. In this given experiment, we have built a 4-bit ALU.

Problem Statement:

Group V

Design the following 4-bit ALU (Arithmetic Logic Unit):

S2	S1	S0	Output	Function
1	0	1	Ai-Bi	Subtract
0	1	1	Ai + Bi + 1	Add with Carry
1	1	1	Ai + Bi	Add
0	0	1	Ai + 1 + 1	Transfer A with Carry
1	X	0	Ai I Bi	OR
0	X	0	Ai xor Bi	XOR

Function Generation:

S2	S1	S0	Output	X_i	Y_i	Z_i
1	0	1	$A_i - B_i$ (subtract)	A_i	$\overline{B_i}$	1
0	1	1	$A_i + B_i + 1$ (Add with Carry)	A_i	B_i	1
1	1	1	$A_i + B_i$ (Add)	A_i	B_i	0
0	0	1	$A_i + 1 + 1$ (Transfer w/ Carry)	A_i	1	1
1	X	0	A_i I B_i (OR)	$A_i + B_i$	0	0
0	X	0	$A_i \oplus B_i$ (XOR)	$A_i \oplus B_i$	0	0

$$X_i = \begin{cases} A_i & \text{when } S0 = 1 \\ A_i \oplus B_i & \text{when } S0 = 0 \text{ ; } S2 = 0 \\ A_i + B_i & \text{when } S0 = 0 \text{ ; } S2 = 1 \end{cases}$$

$$= A_i S0 + (A_i \oplus B_i)\,\overline{S0}\,\overline{S2} + (A_i + B_i)\,\overline{S0}\,S2$$

$$Y_i = \begin{cases} \overline{B_i} & \text{when } S0 = 1 \text{ ; } S1 = 0 \text{ ; } S2 = 1 \\ B_i & \text{when } S0 = 1 \text{ ; } S1 = 1 \\ 1 & \text{when } S0 = 1 \text{ ; } S1 = 0 \text{ ; } S2 = 0 \end{cases}$$

$$= \overline{B_i}\, S0 \overline{S1} \overline{S2} + B_i S_0 S_1 + 1 \cdot S_0 \overline{S_1}\, \overline{S_2}$$

$$Y_i = \overline{B_i}\, S0\, \overline{S_1} S_2 + B_i S_0 S_1 + S_0 \overline{S_1}\, \overline{S_2}$$

$$Z_i = S_2 \overline{S_1} S_0 + \overline{S_2} S_1 S_0 + \overline{S_2}\, \overline{S_1} S_0$$

$$= S_0 (S_2 \overline{S_1} + \overline{S_2} S_1 + \overline{S_2}\, \overline{S_1})$$

$$= S_0 (S_2 \overline{S_1} + \overline{S_2})$$

$$Z_i = S_0 (\overline{S_2} + \overline{S_1})$$

$$[A + \bar{A}B = A + B]$$

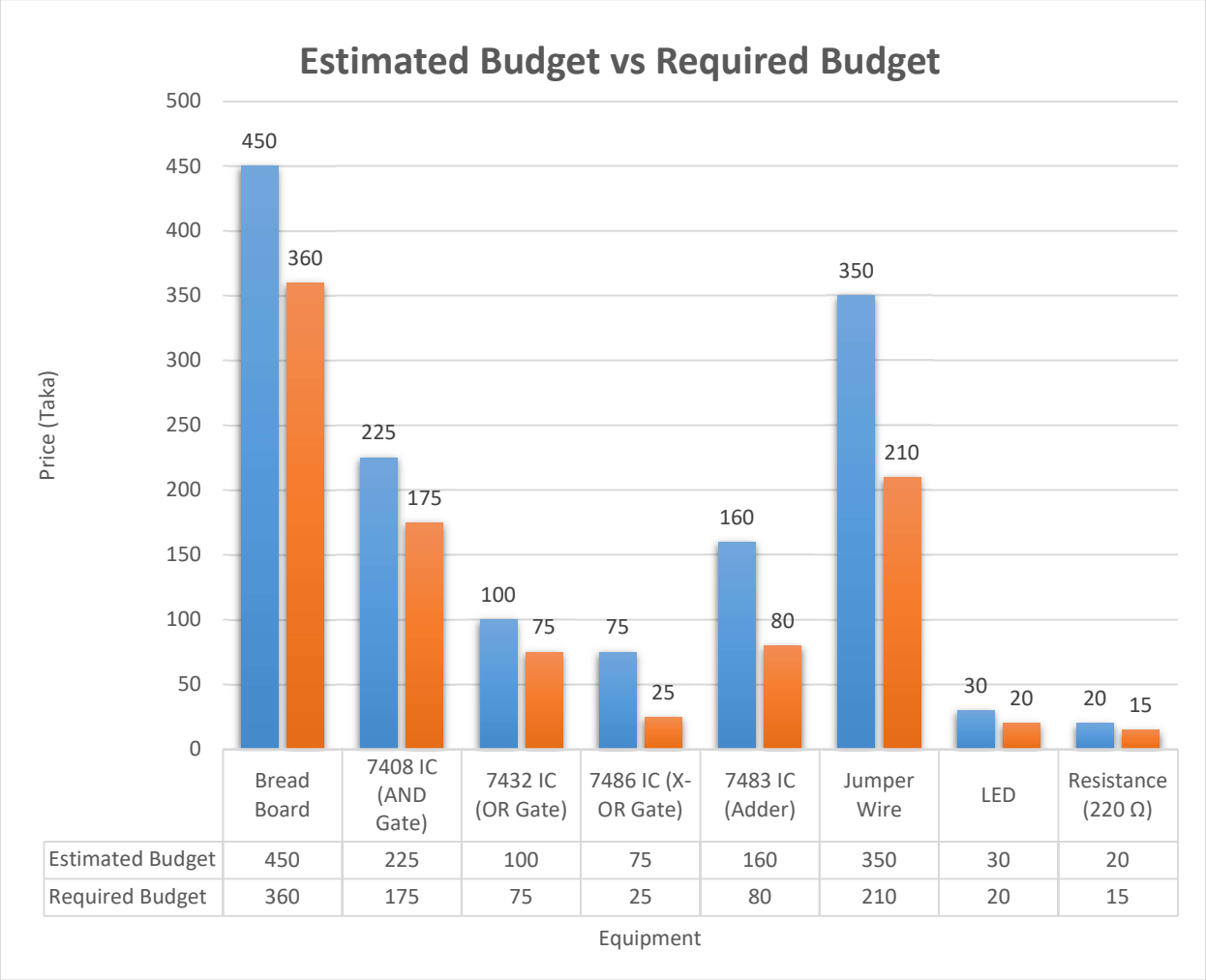
$$= (A_i \oplus B_i)\,\overline{S_0}\,\overline{S_2} + A_i S_0 + A_i \overline{S_0} S_2 + B_i \overline{S_0} S_2$$

$$= (A_i \oplus B_i)\,\overline{S_0}\,\overline{S_2} + A_i (S_0 + \overline{S_0} S_2) + B_i \overline{S_0} S_2$$

$$X_i = (A_i \oplus B_i)\,\overline{S_0}\,\overline{S_2} + A_i (S_0 + S_2) + B_i \overline{S_0} S_2$$

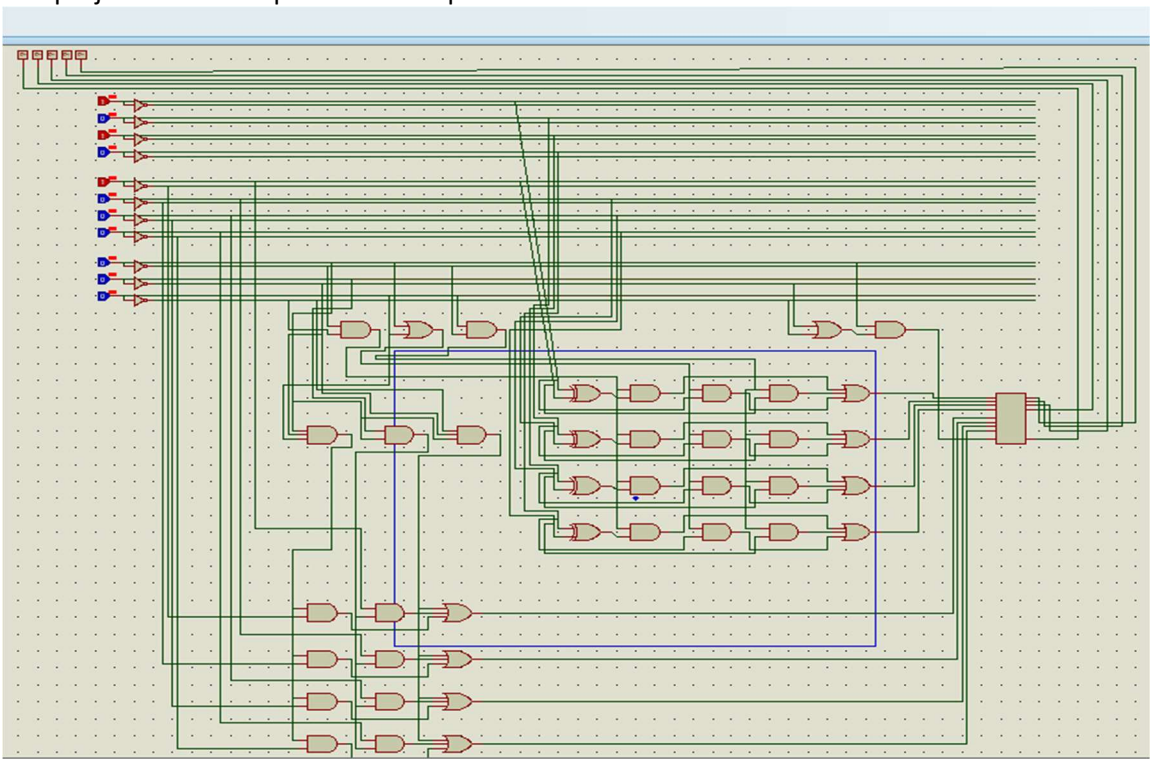
Equipment and Budget Comparison:

For this project required equipment are:
7408 IC (AND Gate) – 8 pieces
7404 IC (NOT Gate) – 2 pieces
7432 IC (OR Gate) – 2pieces
7486 IC (X-OR Gate) – 1piece
7483 IC (ADDER) – 1piece



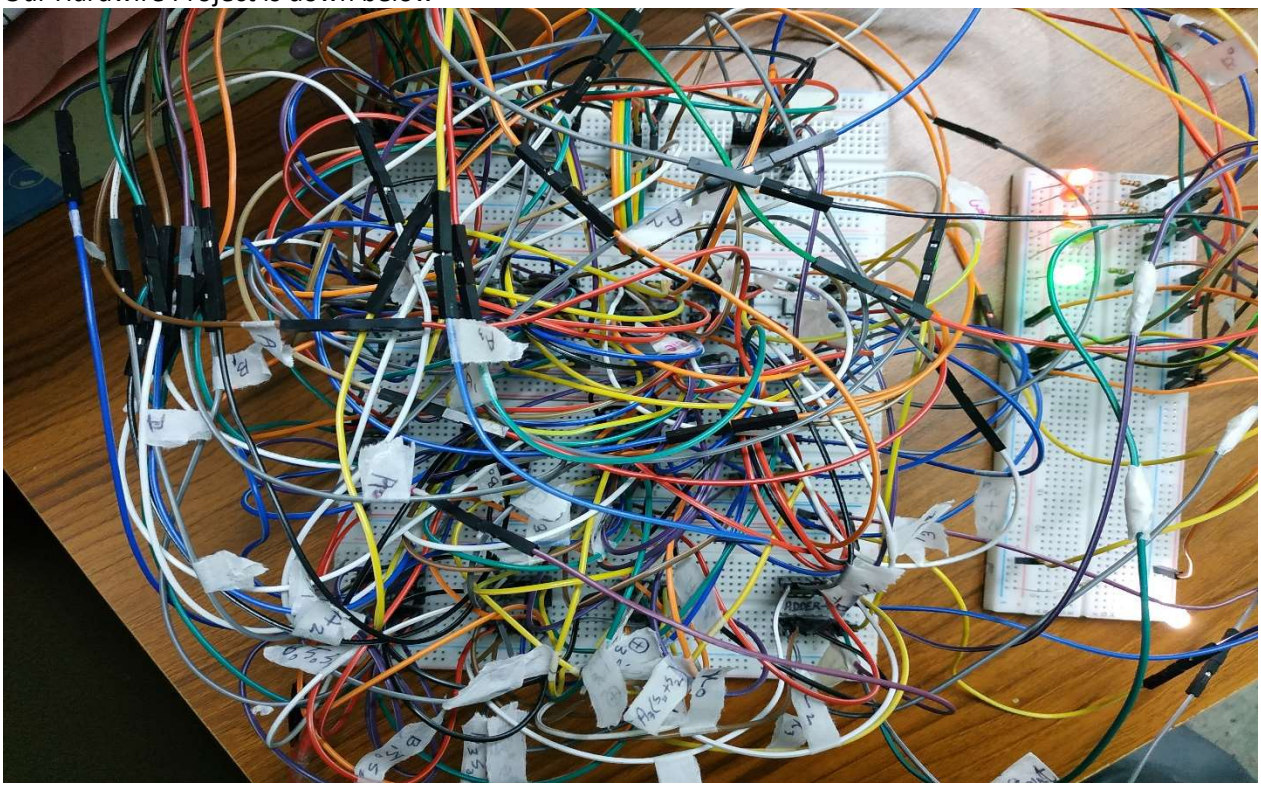
Simulation:

The project that we implemented on proteus is down below



Implementation:

Our Hardwire Project is down below



Result:

By Fixing the value of A= 1010 and B=0101, we get the following output

S2	S1	S0	Output	Cout	F3	F2	F1	F0
1	0	1	Sub	1	0	1	0	1
0	1	1	Add w C	1	0	0	0	0
1	1	1	Add	0	1	1	1	1
0	0	1	Transfer w C	1	1	0	1	0
1	X	0	OR	0	1	1	1	1
0	X	0	XOR	0	1	1	1	1

Conclusion:

At first, we implemented functions from the given table. Then we have done the experiment in Proteus software. We found an error in XOR operation and have fixed it. Then we implemented the experiment in hardware. Finally, we are able to complete our experiment without any error.