

# Robert French

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Summary	I have an eclectic set of interests that has led me through 30 years of experience with software development, management, and business development, 6 years of experience as a flight instructor and commercial pilot, 17 years of experience as a challenge-level square dance caller, and that is now leading me into a new career in research astronomy. During my careers I have written more than 1,000,000 lines of code, founded a highly successful startup, taught many people to fly, and traveled around the world performing on stage. I am experienced and comfortable in roles as an individual contributor, team lead, manager, educator, and public speaker. My goal is to make significant contributions to my fields of endeavor while working on cool projects with intelligent and motivated people.		
Astronomy-Related Professional Experience	2008 – present	The SETI Institute	Mountain View, CA
	<ul style="list-style-type: none"><li>Working with researcher Mark Showalter to perform photometry of Saturn's F Ring using images from the Cassini and Voyager spacecraft.</li></ul>		
Aviation-Related Professional Experience	2003 - 2007	Sundance Flying Club	Palo Alto, CA
	2004 - present	West Valley Flying Club	Palo Alto, CA
	2007 - 2009	Advantage Aviation	Palo Alto, CA
	<ul style="list-style-type: none"><li>Airline Transport Pilot-rated pilot (airplane single- and multi-engine land and sea)</li><li>FAA Gold Seal Flight Instructor (airplane single- and multi-engine and instrument)</li><li>FAA Certified Ground Instructor (advanced and instrument)</li><li>4,100 hours total flight time; 2,600 hours flight instruction given; 1,800 hours ground instruction given</li><li>Previous owner of two aircraft (11 years total ownership)</li><li>Taught 21 students to become private, instrument, or commercial pilots (&gt; 95% first-time pass).</li><li>Nominated as Flight Instructor of the Year for the San Jose region.</li></ul>		
Computer-Related Professional Experience	1996 – 2000	Silicon Spice, Inc.	Mountain View, CA
	2000 – 2001	Broadcom Corporation	Mountain View, CA
	<ul style="list-style-type: none"><li>Silicon Spice produced a high-performance communications processor based on a proprietary reconfigurable processor architecture. The chip was targeted at the carrier-class voice and remote access server market and was capable of delivering hundreds of channels of voice or modem processing in a small, low-power package. Silicon Spice provided a complete system solution: packaged silicon, development tools, reference boards, embedded host software, and voice and modem application stacks.</li><li>As Co-Founder of Silicon Spice, was responsible for all aspects of company development. Raised over \$90M in venture funding in five rounds. Involved in hiring over 60 of the 130 employees, including a world-class CEO and executive staff. Actively participated in customer visits and demos at all levels. Provided vision for the product and the company culture.</li><li>As Director of Software Development, was responsible for building and managing groups including: retargetable compiler, debugger/IDE, chip simulation, embedded real-time OS, embedded host software, voice and modem applications, quality assurance, release engineering, ITS, and documentation. Provided vision and direction for the software development process, including the extensive use of testing automation. Delivered 18 high-quality software releases.</li><li>Participated in the architectural design of two generations of chips.</li><li>Was issued 17 patents on software and architecture (additional patents still pending).</li><li>Silicon Spice was sold to Broadcom Corporation in October, 2000 for \$1.25 billion.</li></ul>		

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| 2007 – present | Veloxdat, Inc. | Sunnyvale, CA |
| 2002 – present | Stretch, Inc.  | Sunnyvale, CA |
- Member of the Technical Advisory Board. Provide analysis and advice for marketing, applications, and silicon and software technology.
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| 1992 – 1996 | Silicon Graphics, Inc. | Mountain View, CA |
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- In charge of the global and local optimizers for the MIPSpro 6.0 compiler. Implemented a wide variety of new optimizations and achieved record-breaking Nullstone benchmark results.
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| 1991 | Carnegie Mellon University | Pittsburgh, PA |
|------|----------------------------|----------------|
- Designed and implemented an optimizing code generator for the Intel/CMU iWarp parallel processing system. The code generator interfaced with the Stanford SUIF compiler system and provided software pipelining and support for efficient inter-processor communication. The compiler significantly outperformed the Intel production compiler.
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|-------------|---------------------|--------------|
| 1990 – 1996 | Stanford University | Stanford, CA |
|-------------|---------------------|--------------|
- Co-developer of the SUIF compiler infrastructure, a publicly available research platform used by hundreds of companies and universities. Designed and implemented significant portions of the SUIF library, ANSI C front end, and C back end. Investigated methods for compilation and fast simulation of hardware description languages, especially Verilog.
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| 1989 – 1993 | ComputerVision | Cambridge, MA |
|-------------|----------------|---------------|
- Solely responsible for porting *DesignView*, a pioneering graphical constraint-based mechanical engineering design system consisting of more than 340,000 lines of C code, from Windows 3.x to UNIX-X11-Motif.
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| 1986 – 1989 | MIT Project Athena | Cambridge, MA |
|-------------|--------------------|---------------|
- Member of the team that developed Zephyr, a network-based, distributed, secure notice multicast system for personal and system messages (today known as instant messaging). Zephyr is considered the first such system, predating ICQ and AOL IM by eight years. Aided in the design of the Zephyr protocol and implemented the client library and all client applications. Zephyr is still in use at MIT today.
  - Ported GNU Emacs to X11. It was the first fully functional X11 application.
  - Developed a distributed, fault-tolerant database application for document submission.
  - Implemented or improved various UNIX system applications (such as login and mount) to work in a highly distributed secure processing environment.
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| 1979 – 1986 | Various Companies | Louisville, KY |
|-------------|-------------------|----------------|
- Implemented accounting and inventory software for several companies. Managed a small programming department at a mail-order company. Developed a new BASIC interpreter that was sold with a color graphics board for the TRS-80. Developed dozens of utilities and games for the TRS-80 that were sold commercially. Developed some of the first shareware for the Amiga, including a well-regarded Mandelbrot set exploration system. Tutored students in programming concepts.

Square  
Dance-  
Related  
Professional  
Experience

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| 1992 - present | Challenge-Level Square Dance Caller | Various locations |
|----------------|-------------------------------------|-------------------|
- One of the top C4-level callers in the United States.
  - Called many square dance weekends throughout the United States, Canada, Sweden, Germany, and Japan.
  - Taught many full-length (6-9 month) and accelerated (2-3 week) square dance classes at all levels from beginners through C3A.
  - Co-author of the book *Mental Image Mechanics*, a treatise on set theory applied to square dance calls.

Education	2008 – present	Swinburne University of Technology	Melbourne, Australia
	M.S. in Astronomy (in progress)		
	<ul style="list-style-type: none"> <li>Course emphasis on cosmology and astrophysics.</li> </ul>		
	1990 – 1996	Stanford University	Stanford, CA
	Ph.D. candidate in Computer Science, advisor: Monica Lam		
	M.S. in Computer Science		
	<ul style="list-style-type: none"> <li>Teaching assistant for <i>Topics in Parallelizing Compilers, Advanced Compiling Techniques, and Programming Languages</i>.</li> <li>Awarded Intel Foundation Graduate Fellowship, 1995-1996.</li> </ul>		
	1986 – 1990	MIT	Cambridge, MA
	B.S. in Computer Science		
	<ul style="list-style-type: none"> <li>Course emphasis on computer architecture, compiler and programming language theory, and VLSI design. Thesis examined the use of simulated annealing in the optimization of programs on fine-grained parallel computers.</li> </ul>		
Patents and publications	U.S. Patent #7,428,593: System and method of processing data flow in multi-channel, multi-service environment by dynamically allocating a socket		
	U.S. Patent #7,266,672: Method and apparatus for retiming in a network of multiple context processing elements.		
	U.S. Patent #7,249,351: System and method for preparing software for execution in a dynamically configurable hardware environment.		
	U.S. Patent #7,188,192: Controlling multiple context processing elements based on transmitted message containing configuration data, address mask, and destination identification.		
	U.S. Patent #7,032,103: System and method for executing hybridized code on a dynamically configurable hardware environment.		
	U.S. Patent #6,990,566: Multi-channel bi-directional bus network with direction sideband bit for multiple contact processing elements.		
	U.S. Patent #6,912,576: System and method of processing data flow in multi-channel, multi-service environment by dynamically allocating a socket.		
	U.S. Patent #6,892,324: Multi-channel, multi-service debug.		
	U.S. Patent #6,751,722: Local control of multiple context processing elements with configuration contexts.		
	U.S. Patent #6,745,317: Three level direct communication connections between neighboring multiple context processing elements.		
	U.S. Patent #6,675,289: System and method for executing hybridized code on a dynamically configurable hardware environment.		
	U.S. Patent #6,553,479: Local control of multiple context processing elements with major contexts and minor contexts.		
	U.S. Patent #6,526,498: Method and apparatus for retiming in a network of multiple context processing elements.		

U.S. Patent #6,457,116: Method and apparatus for controlling contexts of multiple context processing elements in a network of multiple context processing elements.

U.S. Patent #6,122,719: Method and apparatus for retiming in a network of multiple context processing elements.

U.S. Patent #6,108,760: Method and apparatus for position independent reconfiguration in a network of multiple context processing elements.

U.S. Patent #5,915,123: Method and apparatus for controlling configuration memory contexts of processing elements in a network of multiple context processing elements.

Amarasinghe, S. P., *et al.* *The Multiprocessor as a General-Purpose Processor: A Software Perspective*. IEEE Micro, June 1996.

Amarasinghe, S. P., *et al.* *Breakthroughs in Parallelizing Compilers and Their Architectural Implications*. HOT Chips VII, August 1995.

French, Robert S., *et al.* *A General Method for Compiling Event-Driven Simulations*. Proceedings of the 32nd Design Automation Conference. June 1995, pp. 151-156.

Wilson, Robert P., *et al.* *SUIF: An Infrastructure for Research on Parallelizing and Optimizing Compilers*. ACM SIGPLAN Notices, December 1994, pp. 31-37.

Lam, Monica S., *et al.* *SUIF: A Parallelizing & Optimizing Research Compiler*. Stanford Computer Systems Laboratory Technical Report No. CSL-TR-94-620, May 1994.

Williams, Nick, *et al.* *The Educational On-Line System*. European UNIX User's Group Proceedings. April 1990, pp. 125-131.

French, Robert S. *A Simple Placement and Routing Algorithm for a Two-Dimensional Computational Origami Architecture*. Papers of the MIT-ACM Undergraduate Computer Science Conference, April 1989.

DellaFera, C. Anthony, *et al.* *The Zephyr Notification Service*. Usenix Conference Proceedings, February 1988, pp. 213-219.

Operating  
System and  
Language  
Experience

#### Operating Systems

- UNIX versions: LINUX, Solaris, IRIX, SysV, 4.3 BSD, ULTRIX, HP/UX
- MULTICS, VAX/VMS, RSTS/E, RT-11, TOPS-10, TOPS-20
- Windows 3.0 through XP, MSDOS, AmigaOS, Apple DOS, TRS-DOS, CP/M-80

#### Programming and Scripting Languages

- BASIC, C, C++, CLU, COBOL, FORTH, FORTRAN, IDL, LISP, Mathematica, PASCAL, PERL, PL/I, PostScript, Prolog, RPG II, Scheme, Verilog
- Assembly languages: 8088, 8086, Z-80, 6809, 68000, MIPS R3000 through R10000, SPARC, XTensa, KL10