Internship / Thesis Proposal – 4 to 6 months

Title:

**Development of IonSat Interfaces and Electrical Architecture**

Context of the internship

The Centre Spatial de l'École polytechnique (Space center of École polytechnique, CSEP), created in 2010, proposes and supervises space projects for École polytechnique students. It is at the origin of one of the first French student nanosatellites, X-CubeSat, launched into orbit in 2017. The CSEP brings together and coordinates, through its projects, students, teacher-researchers, industrialists and French and European space agencies. It is financially and operationally supported by the education patronage program *Espace, science et défis du Spatial (*Space, Science and Challenges), led by Professor Pascal Chabert.

IonSat is an ongoing 6U nanosatellite project equipped with an electric propulsion engine, dedicated to demonstrating the feasibility of nanosatellite missions in very low orbit (300 km). It is at the frontier of space applications, with a strong educational vocation. The project is currently led by twenty students, supported by numerous space actors: industries (Thalès Alenia Space), agencies (CNES, Onera).

Internship description

The objective of this internship is to participate in the development of the IonSat electronic architecture and communication buses. The IonSat Platform receives commands from the ground via a RF link in two bands. The commands are transmitted through the common bus to the main on-board computer (OBC). The OBC executes the commands and, in parallel, it requests information to the payloads carried by the satellite. Such information, together with the status of the satellite measured by different sensors, is sent back to the ground segment.
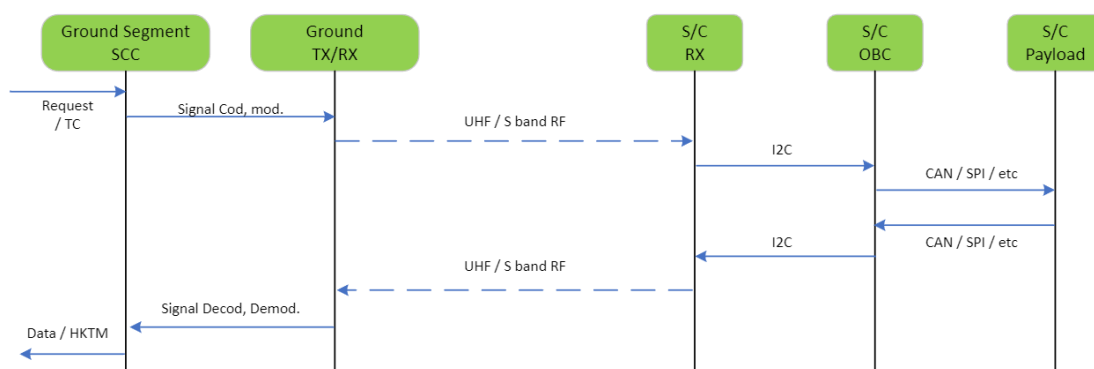
Message Sequence Diagram

According to the philosophy of low-cost missions, most subsystems in the satellite are Components-Off-The-Shelf (COTS) obtained from different providers. The communication between such components is made through common electrical interfaces, such as data bus or power lines managed by a common electronic board.

At state-of-the-art, the IonSat team has defined the different sub-systems composing the satellite. The next step of the project is to define the electronic architecture of the satellite and, in particular, how all the sub-systems shall be integrated.

In this context, the internship will focus on the design, the development, the integration and the validation of the VHDL IPs protocols required for the flight software. In particular, the student will:

1) Familiarize himself with the topic by performing bibliographic studies;
2) Develop the architecture of the electrical interfaces of the satellite. This means that the student will analyze in detail the characteristics of the On-Board electronics and identify the most efficient way to power and control the sub-systems of the satellite;
3) Implement the identified optimize architecture by coding the On-Board electronics (FPGA included);
4) Validation of the implementation with numerical simulations and/or experimental tests.

Note that to achieve such objectives the student might be required to implement communication protocols for specific components of the satellite.

All the above topics will be the subject of documentations that the student will prepare during the internship.

The intern will be supervised by a full-time engineer of the CSEP. If needed, the student will also interact with engineers working in the space team of the Laboratory of Plasmas Physics (LPP) that is specialized in conception of space-ready magnetometers and on-board electronics.

During the internship, the IonSat team (included the intern student) will have frequent interactions with experts from both the major French aerospace agencies (CNES and ONERA) and French companies (Thalès Alenia Space and ThrustMe) which are partners of the IonSat Project.

Technical Requirements

- M1 or M2 level in electrical/electronic engineering, software engineering, or related domains.
- Experience in C/C++ or FPGA (VHL) programming.
- Knowledge of communication buses (I2C, CAN, RS422, etc.).
- Knowledge of Xilinx design tools.
- Knowledge in CubeSat subsystems.
- Knowledge in UNIX like systems.
- Good English profficiency.

Behavioural Requirements

- Self Motivation and autonomy.
- Communication and teamwork.

Internship duration: between 4 and 6 months, from February 2023.

If you are interested, send your CV and a cover letter, clearly indicating your motivation and availability dates.

Contacts:

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