Temperature Control of Diffusion/CVD Furnaces Using Robust Multivariable Loop-Shaping Techniques

Kostas Tsakalis, ASU

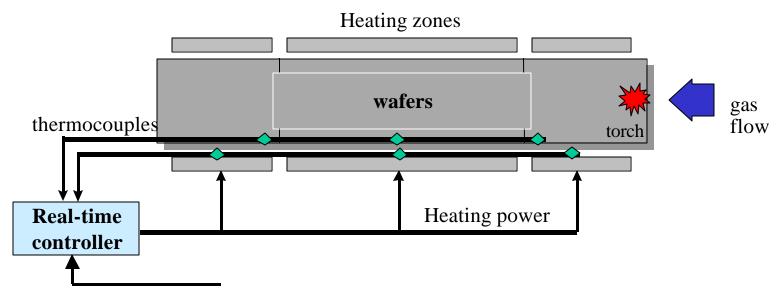
Jose-Job Flores-Godoy ASU

Kevin Stoddard SEMY Eng. Inc.



- Tight temperature control
- Quick design turnaround (for retrofitting apps)

Introduction I

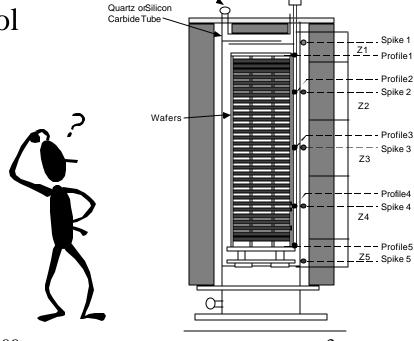


Time, Temperature set-points

- Temperature uniformity, fast stabilization, disturbance attenuation,...
- Quick design, minimal iterations (furnace down-time)
- Low expertise requirements

Introduction II

- Standard Practice:
 - Spike PID, Profile table look-up
 - Periodic Profiling, Disturbances, Stabilization, Uniformity
- Model-based multivariable control
 - Modeling (nominal+uncertainty)
 - Controller design (loop-shaping)
 - Implementation
 - Multiple operating points



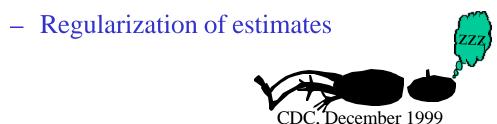
ProfileTC

Modeling I

- System Identification
- Control-Oriented ID: Uncertainty description compatible with the controller design method.
 - Our choice: Loop-Shaping (available insight, computations) based on sensitivity and complementary sensitivity targets.
 - Nominal Model: MISO equation error, yielding a linear estimation model

$$y = N(\theta)[u] + D(\theta)[y] + e = w^T\theta$$

- Estimated parameters include initial conditions; this is important to handle short input-output sets that begin on a transient.
- Continuous time model.



Modeling II

- Coprime Factor Description of the Uncertainty
- Robust Stability Condition: σ [C S D⁻¹] σ [Δ _N] + σ [S D⁻¹] σ [Δ _D] < 1
- CS~P-1T: Relates uncertainty to target loop properties (controller independent).
- Uncertainty estimate + Target selection: Minimize RSC
- Effective closed loop uncertainty estimate: (for outer loop design)

$$\begin{split} & \delta_{M,e} < \{\sigma \, [\, S \, D^{\text{--}1} \,] \, \sigma \, [\, C \, S \,] \, \sigma \, [\, T^{\text{--}1} \,] \, \sigma \, [\Delta_N] + \sigma \, [S \, D^{\text{--}1} \,] \, \sigma \, [\Delta_D] \, \} \, \alpha \\ & \alpha = (1 - \sigma \, [C \, S \, D^{\text{--}1}] \, \sigma \, [\Delta_N] + \sigma \, [S \, D^{\text{--}1} \,] \, \sigma \, [\Delta_D] \,)^{\text{--}1} \end{split}$$



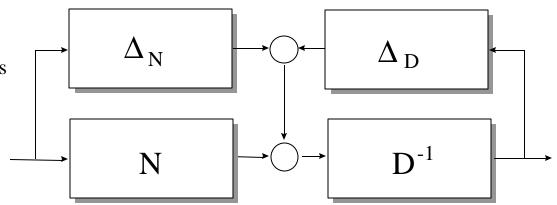
Interpretation:

 $\Delta_{\rm N}$ => compl. sensitivity constraints

(high frequencies)

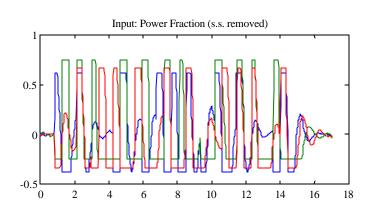
 $\Delta_{\rm D} =>$ sensitivity constraints

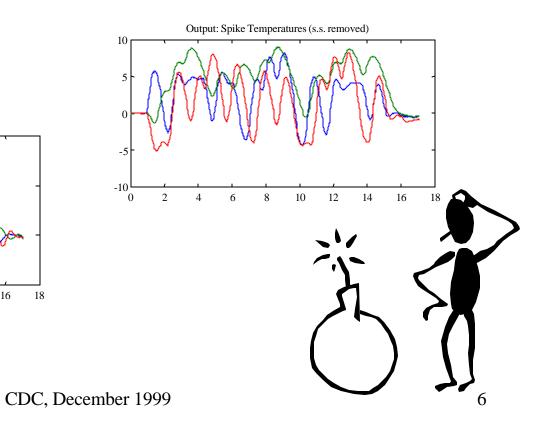
(low frequencies)



Modeling III

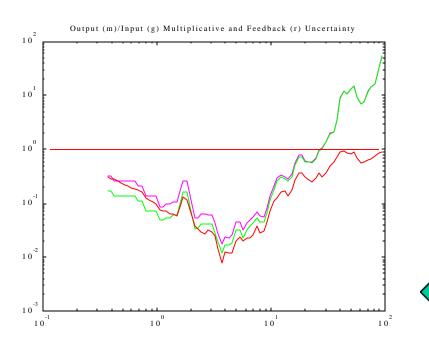
- Identification Experiment:
 - ~20 min test (net time at the operating conditions)
 - Target bandwidth ~5 rad/min

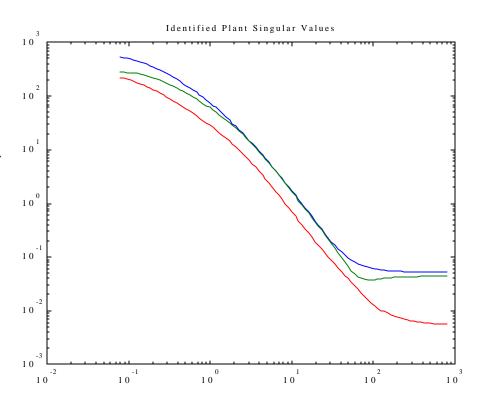




Inner Loop (Spike Subsystem) Modeling

 Power to spike temperature.
 Very high and uncertain low frequency gain. (but good model around the intended crossover)

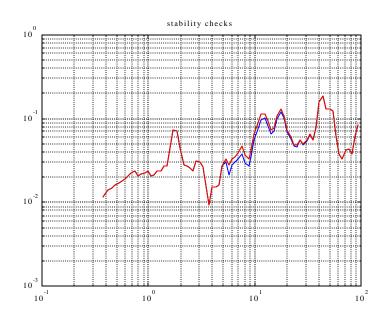


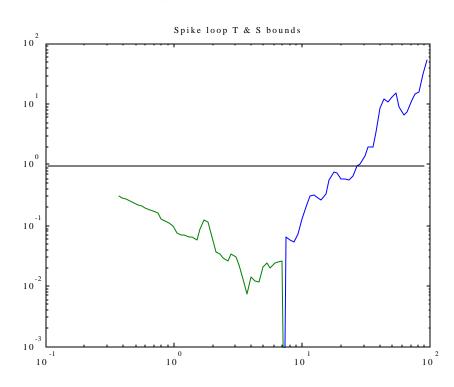


"Raw" uncertainty data expressed as inverse S&T bounds (|fft(e)|/|fft(u)|, |fft(e)|/|fft(y)|) show asymptotic behavior.

Spike Model Uncertainty

• After the split, the high frequency uncertainty is expressed as an inverse T constraint and the low frequency as an inverse S constraint.

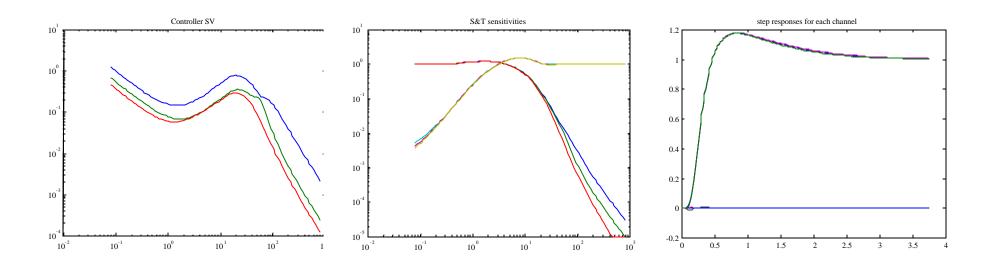




- Rare limitations from RHP zeros
- Small RSC => Confidence in the design

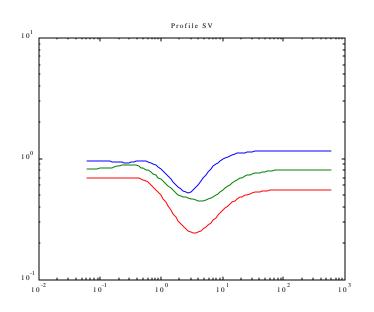
Spike Controller Design

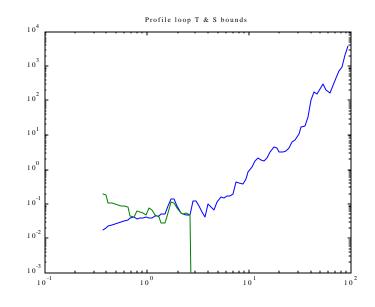
- Target loop => weighted H-infinity sensitivity optimization
- The approach yields excellent matching properties with minimal iterations in the weight selection.
- Simple weights => Automation, Low expertise requirements.



Outer Loop (Profile Subsystem)

- The profile subsystem (spike to profile temperatures) is identified in a similar manner.
- Target loop constraints: profile subsystem uncertainty, nominal inner closed-loop, effective inner closed-loop uncertainty.
- The profile controller is designed for the combined profile/inner-loop system. Typically a straightforward design.

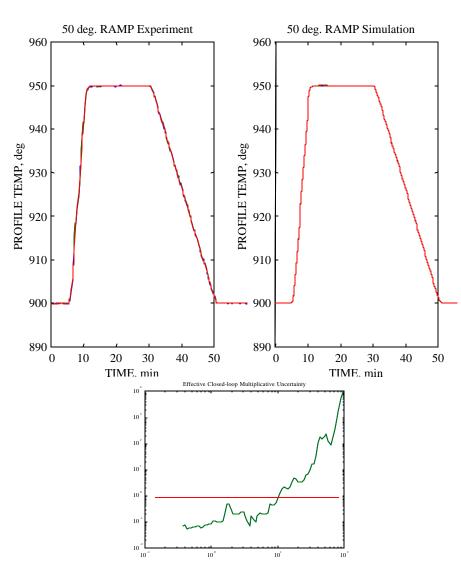




Controller Implementation and Testing



- After reduction, the controller is discretized and augmented with anti-windup mechanisms.
- Excellent and predictable performance in the typical ramp-up/ramp-down operations



More Results

• "Temperature no longer variable of concern" Source: M. Yelverton, et. al., AEC/APC XI, 1999. (AMD)



1998

Editors'

Process Results:

- Decreased cycle time (faster controlled ramps, faster stabilization). Time-to-process reduced by as much as 50%
- Increased process indices (Cp, Cpk by as much as 250%)
- Increased tool utilization (no need for profiling)

Source: Tucker, Valdez, Tsakalis, Warren and Stoddard, AEC/APC X, 1988. (Motorola, Mesa)

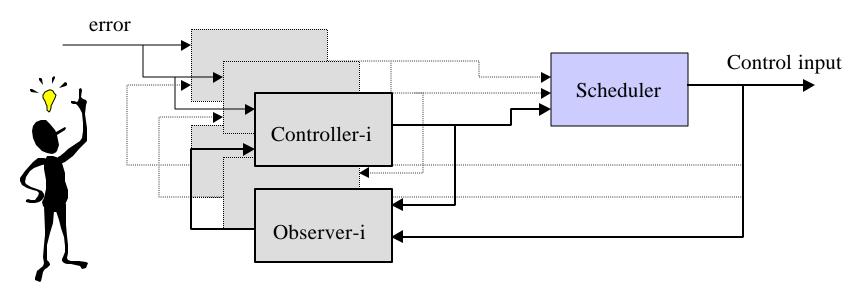


Semiconductor Intl, Best Product Award, 1988



Controller Scheduling

- Handling multiple operating conditions
- Modeling and controller design at different steady-states
- Scheduling with bumpless transfer techniques
 - In general, models and controllers will have different order; simple interpolation is not enough.

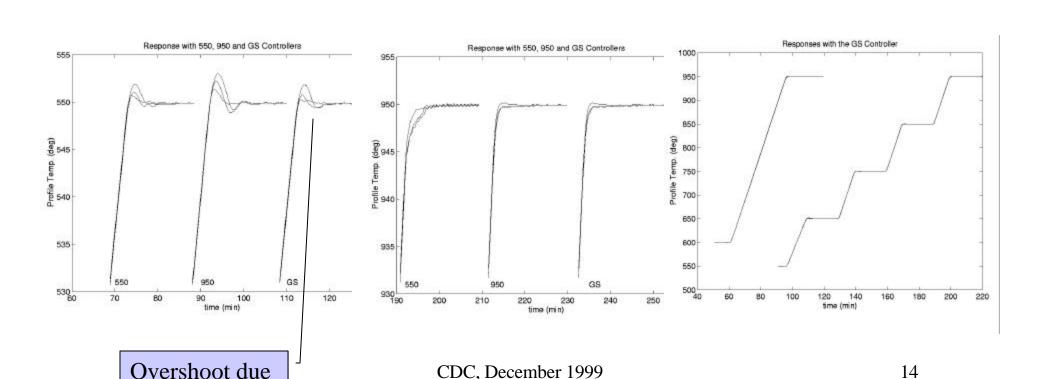


Scheduled Controller Tests

Higher -but manageable- complexity

to saturation

- 3 controllers covering the range 500-1000 deg.C
- Scheduled controller has good performance in the entire range and transfers are fairly smooth





Concluding Remarks

- Integrated method to design high-performance temperature controllers
- Quick and reliable designs; low expertise requirements
- Excellent success record
- Controller scheduling to handle wide-range operations
- Future work:
 - Tech-transfer to other processes
 - Nonlinear modeling and uncertainty descriptions

