Problem: includes were’nt set up correctly

Fm\_shell confirms correct synthesis

Gonna tighten constraints to initial utilization 0.4 and clock frequency at

Problem: did synthesis with clock constraint at 250Mhz. Gonna apply higher frequency to check for slack violations.

Slack too tight at 0.12 setup and -0.3 hold. Will solve hold in routing

Problem: virtual pad placement is completely wrong. Gonna have to redo.

Added possibly way too many virtual pads – fixed and still met 2% drop threshold

Max routing layer constraints were wrong. Corrected 6-10 for power 1-5 for routing

Problem: error when analyzingfprail no pads were connected. Redid them now everything is okay. Still meeting.

Optimizing for dynamic power

Problem: can’t find tap cells

Problem: clk wasn’t showing. Ran get\_ports found clk, reran Get\_clock clk it came back. Weird

Clkskew within target

Used clock to fix hold violations. Utilization jumped from 0.25 to 0.5. hold violations still there but need to increase significant digits.

Post clk routing utilization 56%. And hold time is 0.01 violated and setup time is 0.79

Removed filler cells , legalized placement then ran route\_zrt\_eco it worked

Fm\_shell has a problem with linking the cells in the no pg Verilog file with the library. Can’t do formal verification.

Fixed by exporting Verilog file with the following settings via gui.

Gds file only outputs one metal layer in icwbeve

Exported through gui worked fine.

Grg.gds swapped

Drc check in caliber reveals a lot of errors in metal 4.1?

Lvs in caliber refuses to compare due to different number of ports, power and ground not found

Spice model has them , but apparently gds 2 file doesn’t

Skipped starxtract

Fixed hold time violation in prime\_time under cmin