# Low-Power High-Speed Multiplier For Error-Tolerant Application

Khaing Yin Kyaw, Wang Ling Goh*, and Kiat Seng Yeo
School of Electrical and Electronic Engineering
Nanyang Technological University
Singapore
*ewlgoh@ntu.edu.sg

*Abstract*—**In this paper, a new design concept that engaged accuracy as a design parameter is proposed. By introducing accuracy as a design parameter, the bottleneck of conventional digital IC design techniques can be breakthrough to improve on the performances of power consumption and speed. The aim is to fulfill the need for high performance basic sequential elements with low-power dissipation which is steadily growing.**

***Keywords - Multiplier, truncated, error-tolerant, low power, high speed integrated circuits, CMOS technology***

## I. INTRODUCTION

With the ever-increasing quest for greater computing power on battery-operated mobile devices, there is a migration of design emphasis from conventional delay and area optimization to power dissipation minimization, while preserving the desired performance. One common technique for energy efficiency CMOS circuits is the reduction of the supply voltage. However, there are two drawbacks: first is the increase in the gates delay. To overcome this problem, the threshold voltage to be scaled down; and the other drawback is the degradation of noise immunity of the circuits [1]. Hence, the increasing noise sensitivity has become an important concern in the design of devices, circuits and systems [2].

The data processed by many digital systems may in actual fact have already contained errors [3]. Because of the advances in VLSI scaling and the near emergence of billion transistor chips, the results of noise, process variations and spot defects will dictate that few such chips will be error-free. And unlike the conventional method, a completely new design style for an ultra-low power multiplier is proposed in this paper. In addition to the power consumption and speed, *accuracy* is used as a new parameter for the upcoming nano-regime.

With an innovative and novel multiplication method adopted, an ultra-low-power and high-speed multiplier for Error Tolerant application is introduced in this paper and we name our new design, the Error Tolerant Multiplier (ETM). The novel ETM can achieve enormous improvements on speed performance and power consumption at a trade-off-it cannot always maintain 100% accuracy as the conventional multipliers do. However, because of its outstanding advantages in power consumption and speed performance, this ETM has many potential applications in the domains where ultra-low power and/or super-high speed is required while the accuracy is not the main concern. [4-5].

The rest of the paper is organized as follows: section II describes the concept of ETM in both its theoretical and implementation aspects, section III shows the experimental result of a 12-bit ETM compared against the standard parallel multiplier. The quality measurements adopted to analyze all the multipliers discussed are also provided, and lastly, a brief conclusion is given in section IV.

## II. ERROR TOLERANT MULTIPLIER

The definitions of the key terminologies used in this paper are given as follows [3]:

- *Overall error, OE* = $|R_c - R_e|$, where $R_c$ denotes the correct result and $R_e$ is the result obtained by the proposed multiplier (all results are represented as decimal numbers).
- *Accuracy, ACC* = $(1 - OE / R_c) \times 100\%$. Its value ranges from 0% to 100%.
- *Minimum acceptance accuracy* (*MAA*) is the threshold value of the results derived from the proposed multiplier. If they are higher than the minimum acceptance accuracy (*MAA*), they are called accepted results and is often defined by the customers/designers according to the specific applications.
- *Acceptance probability* (*AP*) is the probability that the accuracy of a multiplier is higher than minimum acceptance accuracy (*MAA*). It can be expressed as $AP = P(ACC > MAA)$ and its value ranges from 0 to 1.

For maximum area reduction, an n × n multiplier generates only n times of the most significant product bits and truncates the least significant half of the partial products in order to produce a final product with reduced precision. To achieve a lower average error, and truncation of the partial product bits, an error compensation circuit with an area overhead that is much lower than the truncated part is usually added [6]. Such circuit is widely used in current digital signal processing applications such as the finite-impulse response (FIR) filtering and the discrete cosine transform (DCT) transforms [7-9].

### A. Proposed Mutliplication Algorithm for ETM

This new multiplication algorithm can be illustrated via an example shown in Fig. 1. First, the input operands are split into two parts: a multiplication part that includes a number of higher order bits and a non-multiplication part that is made up of the remaining lower order bits. The length of each part need

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not necessary be equal. The multiplication process begins at the point where the bits split and move simultaneously towards the two opposite directions till all bits are taken care of. In the example of Fig. 1, the two 12-bit input operands, the multiplicand "101110011011" (2971) and the multiplier "010011001001" (1225), are divided into two equal-sized parts, and each of which contains 6 input bits.

As for the lower order bits of the input operands (non-multiplication part), a special mechanism is applied - no partial product will be generated and the carry propagation path has been removed. Every bit position from left to right (MSB to LSB) of the non-multiplication part is checked and if either or both of the two operand bits are "1", the checking process is brought to an end and from that bit onwards, all the bit positions are set to "1". In the event that both operand bits are "0", the corresponding product bit is set to "0". In this way, the overall error generated due to the elimination of partial-products can be minimized. In the example, at the sixth position, the two input bits are both equal to "0". Hence, the corresponding result bit is set to "0". At the fifth LSB bit ($2^{nd}$ position from the starting point), as the multiplicand bit is "1", the corresponding result bit is set to "1" and all the remaining resultant bits to its right are also set to "1".

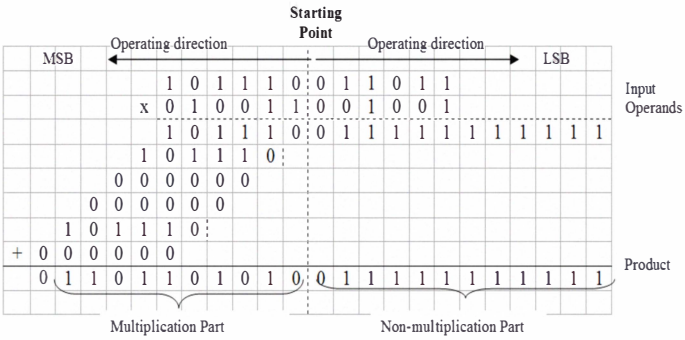


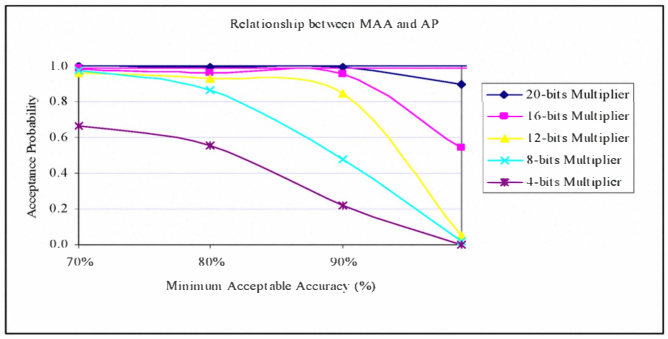

Figure 1 Multiplication algorithms of ETM.

For the higher order bits of the input operands that fall into the multiplication part, the operation is conducted as per in normal multiplication operation, from right to left (LSB to MSB). Its circuit is hence constructed in the conventional way. We retained the conventional topology here since the higher order bits have greater weightage than the lower order bits. By eliminating the partial products and the carry propagation path in the non-multiplication part (LSBs) and performing the multiplication of the MSBs simultaneously, the overall delay time is greatly reduced and so is the power consumption.

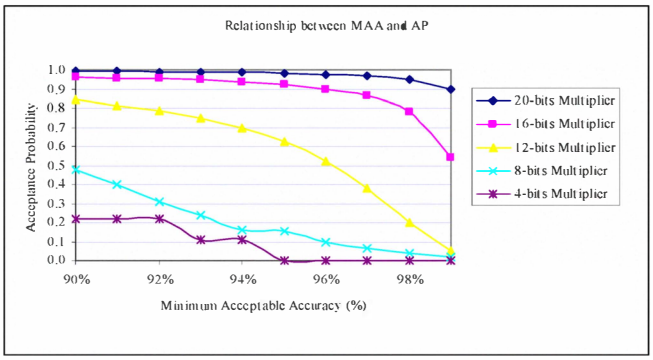
### B. *Relationships between* AP, MAA, *Dividing Strategy and Size of Multiplier*

Upon further evaluation of the proposed multiplication algorithm, it can also be seen that the accuracy of the ETM is closely related to the input pattern. The relationships between the *MAA*, the *AP*, the dividing strategy and the size of multiplier had been investigated using MATLAB program. In Fig. 2, the five curves represent five different sizes of multipliers and they are associated with different *MAA*'s - 70%, 80% and 90% ~ 99%, respectively.

Over 65,000 inputs were randomly selected from all possible input patterns in the evaluation of the 20-bit multipliers. As for the rest of the multipliers, over 6,500 input patterns were selected randomly. It can be deduced that the lower the *MAA* set, the higher the *AP* for the multiplier. This means that if some degree of error can be tolerated, the chances of getting acceptable results will be very high and the likelihood increases when the size of the multiplier increases. When the size of the multiplier becomes larger, the *AP* value will also increase. Therefore, the proposed ETM works better in larger multipliers especially those of 16-bits, 20-bits or even higher.




(a)




(b)

Figure 2 Comparison of ETM with different bit sizes: (a) *AP* comparison for *MAA* 70%, 80%, 90% and 99%, and (b) *AP* comparison for *MAA* 90% to 99%.

### C. *Hardware Implementation*

The block diagram of the 12-bit ETM is depicted in Fig. 3. In the proposed design, inputs A and B are each divided into two 6-bit blocks. The control block is first used for detecting the logic "1" in the MSB position of the inputs, (A11 ~ A6 and B11 ~ B6). When logic "1" is found, the "CTRL" signal will be activated and the input operands are high enough to operate in the ETM mode, which consists of two major blocks: (i) non-multiplication part to give the lower order bits of the final output and (ii) multiplication part to generate the higher order bits of the product.

In the non-multiplication part, it is made up of six cascading PGCs. The PGC circuit consists of one NOR gate and two transistors, M1 and M2. Each PGC is used to generate the lower output digits (P0 ~ P11). When both of the input

patterns A and B are "0", the product bit will be set to "0". When either of the input bits $A_i$ or $B_i$ is "1" or the previous product bit $P_{i+1}$ is "1", the output signal $P_i$ will be set to high. In this way, the high signal will be propagated to all the bit positions on its right.

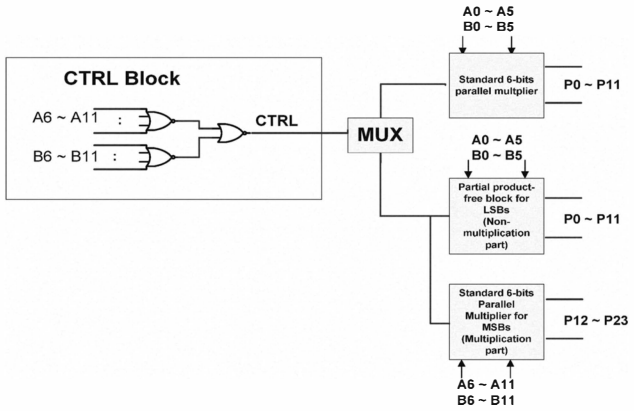



Figure 3 Architecture and implementation of the proposed 12-bits ETM.

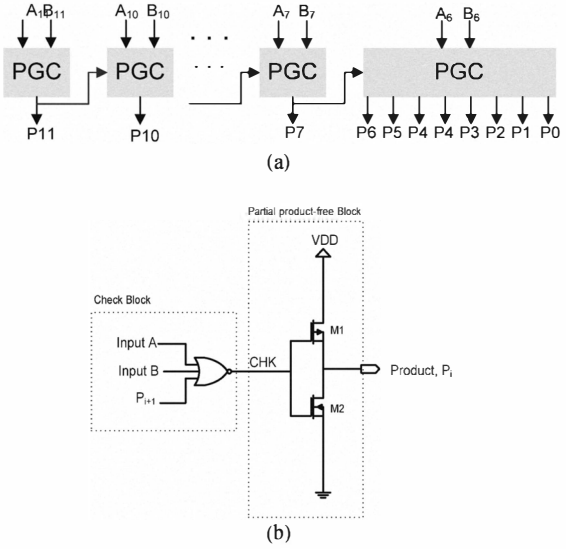



Figure 4 Non-multiplication part: (a) overall architecture and (b) schematic diagram of a PGC.

In the multiplication part, the standard 6-bits parallel multiplier is employed to produce the next higher order 12-bits product, P12 ~ P23, as illustrated in Fig. 5. If the higher order bits are checked and there is no logic "1" detected by the control block, the MUX selects 6-bits conventional multiplier and gives the final result, P0 ~ P11. In standard N × N parallel multiplier, the $N^2$ bit products are generated whereas, in the proposed ETM, only N-bit products need to be produced by two N-bit inputs.

After the input patterns are divided into two parts and the higher orders checked by the control block, the 12-bit multiplier becomes redundant. Since there is no logic "1" located in higher order half of the operands, only 6-bit multiplier is necessary to generate the final product (P0 ~ P11). By omitting the carry signal traveling through the adder arrays, the proposed ETM is able to achieve a reduction in the delay, power saving and reduction of silicon area which translate to saving in hardware cost when compared to the traditional 12-bits multiplier.

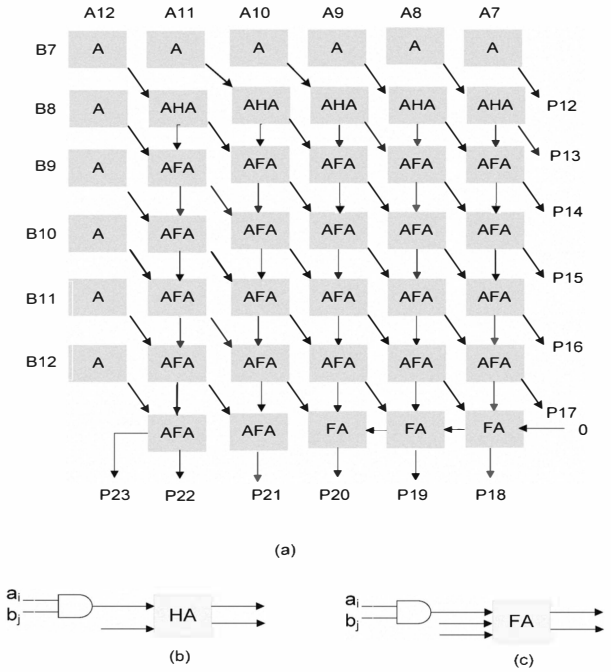



Figure 5 A 6 × 6 multiplication using parallel multipliers where A, HA and FA are the AND, half-adder and full-adder cells, respectively. (a) Multiplier block diagram, (b) AHA cell, and (c) AFA cell [7].

To demonstrate the functionality of the proposed ETM, five different input patterns were randomly selected and simulated. These five data, with corresponding results and accuracies are listed in Table I (note that for convenience, all the numbers were written in HEX format). It is obvious that the accuracy of the 12-bits multiplier falls in an acceptable range. This is because the unacceptable results are distributed across the entire product, ranging from 0 to 23 bits, instead of "squeezing" in small number ranges.

TABLE I. FIVE INPUT PATTERNS AND THEIR CORRESPONDING RESULTS AND ACCURACIES

| A | B | CORRECT RESULT | OBTAINED RESULT BY ETM | ACCURACY |
|---|---|---|---|---|
| 0E01 | 0A1C | 8D 921C | 8C 07FF | 98% |
| 08F1 | 06A8 | 3B 8428 | 38 EFFF | 96% |
| 000A | 0006 | 00 003C | 00 003C | 100% |
| 0FF0 | 010A | 10 8F60 | 0F CFFF | 95% |
| 0888 | 0111 | 09 1908 | 08 87FF | 94% |

## *D. Simulation*

In this work, all the circuits were designed and simulated based on Chartered Semiconductor Manufacturing Limited 0.18-μm CMOS process technology. Simulations were performed at a temperature of 25°C and a supply voltage of 1.8 V. Each circuit drives an output load of 10 fF and all simulation was performed at a clock frequency of 10 MHz, for the conventional and proposed multipliers. The propagation delay and the power consumption during difference switching

activities were measured for the proposed ETM. Besides, a 12 × 12 standard parallel multiplier was also constructed for the purpose of performance comparison. Note that when compared to the 6-bit multiplier of Fig. 5, additional blocks of AND gate, half-adder and full-adder are required in the standard 12-bits multiplier.

## III. Performance Discussion

As provided in Table II and Fig. 6, the difference in the power-delay product (PDP) of the conventional and proposed 12-bit multiplier is compared in order to determine the merit of the proposed ETM. As is evident from Fig. 6, the power dissipation is noted to decrease drastically, from 50% to 96%, depending on the input switching activities.

TABLE II. SIMULATION RESULTS OF 12-BIT ETM AND STANDARD PARALLEL MULTIPLIER

| | A | B | Power (uW) | Delay (nsec) | PDP (fJ) |
|---|---|---|---|---|---|
| **Proposed 12-bits ETM** | 0E01 | 0A1C | 45.47 | 0.76 | 34.56 |
| | 08F1 | 06A8 | 59.54 | 0.62 | 36.86 |
| | 000A | 0006 | 20.35 | 0.76 | 15.45 |
| | 0FF0 | 010A | 59.54 | 0.77 | 45.85 |
| | 0888 | 0111 | 18.29 | 0.93 | 16.92 |
| **Conventional 12-bits Multiplier** | 0E01 | 0A1C | 180.40 | 0.75 | 135.30 |
| | 08F1 | 06A8 | 254.00 | 0.65 | 165.10 |
| | 000A | 0006 | 31.20 | 0.94 | 29.45 |
| | 0FF0 | 010A | 255.00 | 2.34 | 596.70 |
| | 0888 | 0111 | 96.40 | 0.95 | 91.58 |

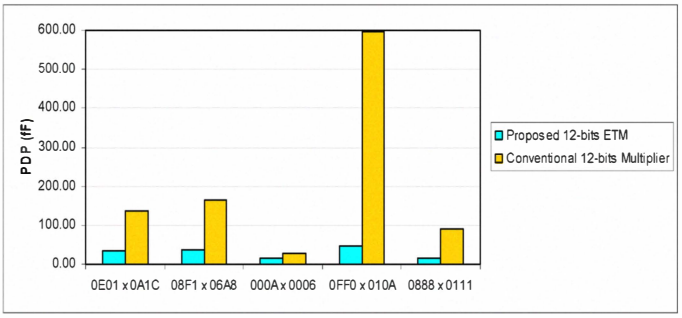



Figure 6 Performance comparisons of ETM and a conventional 12 × 12 parallel multiplier.

The power consumption break-ups of the multipliers for different input activities are depicted in Fig. 7. When compared to standard multiplier, the power dissipation of the proposed ETM dropped from 75% to 90%. This is a very significant power dissipation reduction for the maximum data switching activities.

The 12-bits ETM permits effective area-saving by reducing the high area cost in the summation of partial products. While maintaining the lower average error from the conventional method, the proposed ETM achieves an impressive savings of more than 50% for a 12 × 12 fixed-width multiplication, as indicated in Table III.

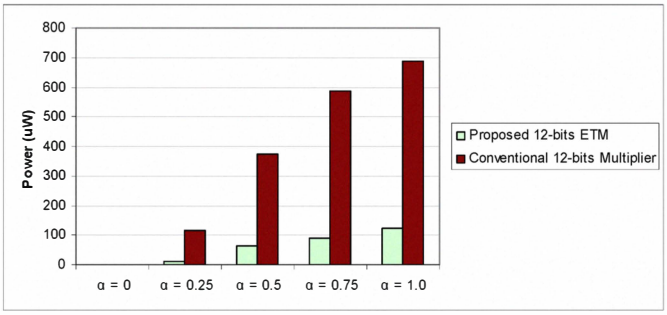



Figure 7 Power consumption versus switching activity.

TABLE III. AREA OF ETM AND STANDARD PARALLEL MULTIPLIER

| | Conventional 12-bits Multiplier | Proposed 12-bits ETM |
|---|---|---|
| Area ($\mu m^2$) | 1028 | 491 |

## IV. Conclusion

In the proposed design strategy, the multiplier circuit is redesigned into two different parts – the multiplication part is implemented using conventional method to ensure a greater accuracy in the higher order bits while the non-multiplication part is constructed in a novel method that permits certain amount of errors. Such errors will be a value that is acceptable to the circuit designer/customer, for attaining savings in power and also enhancement in speed of operation. These multipliers are widely used in application specific data paths in multimedia and wireless communication applications where some degree of saturation error within the dynamic range of interest is tolerable depending of the level of perceptual quality and signal-to-noise degradation it induced.

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