NCT6796D

Nuvoton LPC/eSPI SI/O

Date: July 6th, 2017 Revision 0.6

Table of Contents –

1. GENERAL DESCRIPTION 1

2. FEATURES 2

3. BLOCK DIAGRAM 5

4. PIN LAYOUT 6

5. PIN DESCRIPTION 7

5.1 LPC INTERFACE 8
5.2 ESPI INTERFACE 8
5.3 MULTI-MODE PARALLEL PORT 8
5.4 SERIAL PORT INTERFACE 10
5.5 KBC INTERFACE 11
5.6 CIR INTERFACE 11
5.7 HARDWARE MONITOR INTERFACE 12
5.8 INTEL® PECI INTERFACE 14
5.9 ADVANCED CONFIGURATION & POWER INTERFACE 14
5.10 ADVANCED SLEEP STATE CONTROL CONTROL 15
5.11 PORT 80 MESSAGE DISPLAY & LED CONTROL 16
5.12 SMBUS INTERFACE 16
5.13 POWER PINS 17
5.14 AMD SB-TSI INTERFACE 17
5.15 DSW 17
5.16 IR 18
5.17 MEMORY OK 18
5.18 INTEL POWER FAULT 18
5.19 DDR4 POWER SEQUENCE 18
5.20 GENERAL PURPOSE I/O PORT 18
5.20.1 GPIO-0 Interface 18
5.20.2 GPIO-1 Interface 19
5.20.3 GPIO-2 Interface 20
5.20.4 GPIO-3 Interface 21
5.20.5 GPIO-4 Interface 21
5.20.6 GPIO-5 Interface 22
5.20.7 GPIO-6 Interface 23
5.20.8 GPIO-7 Interface 24
5.20.9 GPIO-8 Interface 24
5.21 STRAPPING PINS 25
5.22 INTERNAL PULL-UP, PULL-DOWN PINS 26
5.23 STRAPPING AND MULTI FUNCTION PIN CONTROL 27

6. GLUE LOGIC 29

6.1 ACPI GLUE LOGIC 29
6.2 3VSBSW# 32
6.3 PSON# BLOCK DIAGRAM 33
6.4 EXTEND PSON# AFTER POWER OFF 34
6.5 DDR4PWR 35
6.6 PSIN# 36
6.6.1 PSIN# Block Diagram (S5 -> S0) 36
6.6.2 PSIN# Block 1sec Diagram (S0 -> S5) 36
6.6.3 PSIN# 4sec Status Diagram 36
6.6.4 Disable PSIN# to PSOUT# Diagram 37
6.6.5 Enable PSOUT# Delay Diagram 38
6.7 PWROK 38
6.8 FRONT PANEL LEDS 40

6.8.1 Automatic Mode 40
6.8.2 Manual Mode 41
6.8.3 S0~S5 LED Blink Block Diagram 42
6.8.4 LED Pole (LED_POL) 42
6.8.5 Deeper Sleeping State Detect Function 43
6.9 ADVANCED SLEEP STATE CONTROL (ASSC) FUNCTION 45
6.9.1 When ASSC is disabled 45
6.9.2 When ASSC is enabled (Enter into Deeper Sleeping State) 46
6.9.3 When ASSC is enabled (Exit Deeper Sleeping State) 46
6.9.4 SLP_S5#_LATCH Control Function 47
6.10 INTEL DSW FUNCTION 48
6.10.1 Enter DSW State timing diagram 48
6.10.2 Exit DSW State timing diagram 49
6.10.3 Application Circuit 49
6.11 THERMTRIP FUNCTION 50

7. CONFIGURATION REGISTER ACCESS PROTOCOL 51

7.1 CONFIGURATION SEQUENCE 52
7.1.1 Enter the Extended Function Mode 52
7.1.2 Configure the Configuration Registers 52
7.1.3 Exit the Extended Function Mode 53
7.1.4 Software Programming Example 53

8. HARDWARE MONITOR 54

8.1 GENERAL DESCRIPTION 54
8.2 ACCESS INTERFACES 54
8.3 LPC INTERFACE 54
8.4 ESPI INTERFACE 56
8.5 I²C INTERFACE 57
8.6 ANALOG INPUTS 58
8.6.1 Voltages Over 2.048 V or Less Than 0 V 59
8.6.2 Voltage Data Format 59
8.6.3 Temperature Data Format 60
8.6.4 ADC Conversion Time and Cycle Time 62
8.7 PECI 62
8.7.1 PECI Calibration 64
8.8 FAN SPEED MEASUREMENT AND CONTROL 66
8.8.1 Fan Speed Reading 66
8.8.2 Fan Speed Calculation by Fan Count Reading 66
8.8.3 Fan Speed Calculation by Fan RPM Reading 66
8.8.4 Fan Speed Control 66
8.8.5 SMART FAN™ Control 68
8.8.6 Temperature Source & Reading for Fan Control 69
8.9 SMART FAN™ I 69
8.9.1 Thermal Cruise Mode 69
8.9.2 Speed Cruise Mode 71
8.10 SMART FAN™ IV & CLOSE LOOP FAN CONTROL MODE 74
8.10.1 Step Up Time / Step Down Time 79
8.10.2 Fan Output Step 79
8.10.3 Revolution Pulse Selection 80
8.10.4 Weight Value Control 80
8.10.5 DTS2.0 82
8.11 ALERT AND INTERRUPT 84
8.11.1 SMI# Interrupt Mode 85
8.11.2 Voltage SMI# Mode 85
8.11.3 Fan SMI# Mode 86

8.11.4 Temperature SMI# Mode 86
8.11.5 OVT# Interrupt Mode 91
8.11.6 Caseopen Detection 92

9. HARDWARE MONITOR REGISTER SET 94

9.1 ADDRESS PORT (PORT X5H) 94
9.2 DATA PORT (PORT X6H) 94
9.3 SYSFANOUT PWM OUTPUT FREQUENCY CONFIGURATION REGISTER – INDEX 00H (BANK 0) 95
9.4 SYSFANOUT OUTPUT VALUE SELECT REGISTER – INDEX 01H (BANK 0) 96
9.5 CPUFANOUT PWM OUTPUT FREQUENCY CONFIGURATION REGISTER – INDEX 02H (BANK 0) 96
9.6 CPUFANOUT OUTPUT VALUE SELECT REGISTER – INDEX 03H (BANK 0) 97
9.7 SYSFANOUT CONFIGURATION REGISTER I – INDEX 04H (BANK 0) 97
9.8 AUXFANOUT0 PWM OUTPUT FREQUENCY CONFIGURATION REGISTER – INDEX 10H (BANK 0) 98
9.9 AUXFANOUT0 OUTPUT VALUE SELECT REGISTER – INDEX 11H (BANK 0) 99
9.10 AUXFANOUT1 PWM OUTPUT FREQUENCY CONFIGURATION REGISTER – INDEX 12H (BANK 0) 99
9.11 AUXFANOUT1 OUTPUT VALUE SELECT REGISTER – INDEX 13H (BANK 0) 100
9.12 AUXFANOUT2 PWM OUTPUT FREQUENCY CONFIGURATION REGISTER – INDEX 14H (BANK 0) 100
9.13 AUXFANOUT2 OUTPUT VALUE SELECT REGISTER – INDEX 15H (BANK 0) 101
9.14 AUXFANOUT3 PWM OUTPUT FREQUENCY CONFIGURATION REGISTER – INDEX 16H (BANK 0) 102
9.15 AUXFANOUT3 OUTPUT VALUE SELECT REGISTER – INDEX 17H (BANK 0) 103
9.16 AUXFANOUT4 PWM OUTPUT FREQUENCY CONFIGURATION REGISTER – INDEX 28H (BANK 0) 103
9.17 AUXFANOUT4 OUTPUT VALUE SELECT REGISTER – INDEX 29H (BANK 0) 104
9.18 OVT# CONFIGURATION REGISTER – INDEX 18H (BANK 0) 104
9.19 VALUE RAM — INDEX 27H ~ 3FH (BANK 0) 105
9.20 CONFIGURATION REGISTER – INDEX 40H (BANK 0) 105
9.21 INTERRUPT STATUS REGISTER 1 – INDEX 41H (BANK 0) 106
9.22 INTERRUPT STATUS REGISTER 2 – INDEX 42H (BANK 0) 107
9.23 SMI# MASK REGISTER 1 – INDEX 43H (BANK 0) 107
9.24 SMI# MASK REGISTER 2 – INDEX 44H (BANK 0) 107
9.25 INTERRUPT STATUS REGISTER 4 – INDEX 45H (BANK 0) 108
9.26 SMI# MASK REGISTER 3 – INDEX 46H (BANK 0) 108
9.27 SERIAL BUS ADDRESS REGISTER – INDEX 48H (BANK 0) 109
9.28 SMI/OVT CONTROL REGISTER1 – INDEX 4CH (BANK 0) 109
9.29 FAN IN/OUT CONTROL REGISTER – INDEX 4DH (BANK 0) 110
9.30 BANK SELECT REGISTER – INDEX 4EH (BANK 0) 111
9.31 NUVOTON VENDOR ID REGISTER – INDEX 4FH (BANK 0) 111
9.32 FAN IN/OUT CONTROL REGISTER – INDEX 50H (BANK 0) 112
9.33 CHIP ID – INDEX 58H (BANK 0) 112
9.34 VBAT MONITOR CONTROL REGISTER – INDEX 5DH (BANK 0) 113
9.35 CURRENT MODE ENABLE REGISTER – INDEX 5EH (BANK 0) 113
9.36 PORT 80 DATA INPUT REGISTER – INDEX 60 (BANK 0) 114
9.37 MONITOR TEMPERATURE 1 REGISTER (INTEGER VALUE)- INDEX 73H (BANK 0) 115
9.38 MONITOR TEMPERATURE 1 REGISTER (FRACTIONAL VALUE)- INDEX 74H (BANK 0) 115
9.39 MONITOR TEMPERATURE 2 REGISTER (INTEGER VALUE)- INDEX 75H (BANK 0) 115
9.40 MONITOR TEMPERATURE 2 REGISTER (FRACTIONAL VALUE)- INDEX 76H (BANK 0) 116
9.41 MONITOR TEMPERATURE 3 REGISTER (INTEGER VALUE)- INDEX 77H (BANK 0) 116
9.42 MONITOR TEMPERATURE 3 REGISTER (FRACTIONAL VALUE)- INDEX 78H (BANK 0) 116
9.43 MONITOR TEMPERATURE 4 REGISTER (INTEGER VALUE)- INDEX 79H (BANK 0) 117
9.44 MONITOR TEMPERATURE 4 REGISTER (FRACTIONAL VALUE)- INDEX 7AH (BANK 0) 117
9.45 MONITOR TEMPERATURE 5 REGISTER (INTEGER VALUE)- INDEX 7BH (BANK 0) 117
9.46 MONITOR TEMPERATURE 5 REGISTER (FRACTIONAL VALUE)- INDEX 7CH (BANK 0) 118
9.47 MONITOR TEMPERATURE 6 REGISTER (INTEGER VALUE)- INDEX 7DH (BANK 0) 118
9.48 MONITOR TEMPERATURE 6 REGISTER (FRACTIONAL VALUE)- INDEX 7EH (BANK 0) 118
9.49 PECI TEMPERATURE READING ENABLE FOR SMIOVT AND SMART FAN CONTROL REGISTER – INDEX AEH (BANK 0) 119
9.50 BEEP CONTROL REGISTER 1 – INDEX B2H (BANK0) 119

9.51 BEEP CONTROL REGISTER 2 – INDEX B3H (BANK0) 120
9.52 BEEP CONTROL REGISTER 3 – INDEX B4H (BANK0) 121
9.53 BEEP CONTROL REGISTER 4 – INDEX B5H (BANK0) 121
9.54 BEEP CONTROL REGISTER 5 – INDEX BFH (BANK0) 122
9.55 SYSFAN VIRTUAL1 TEMPERATURE REGISTER – INDEX EAH (BANK 0) 123
9.56 CPUFAN VIRTUAL1 TEMPERATURE REGISTER – INDEX EBH (BANK 0) 123
9.57 AUXFAN0 VIRTUAL1 TEMPERATURE REGISTER – INDEX ECH (BANK 0) 123
9.58 AUXFAN1 VIRTUAL1 TEMPERATURE REGISTER – INDEX EDH (BANK 0) 124
9.59 AUXFAN2 VIRTUAL1 TEMPERATURE REGISTER – INDEX EEH (BANK 0) 124
9.60 AUXFAN3 VIRTUAL1 TEMPERATURE REGISTER – INDEX EFH (BANK 0) 124
9.61 SYSFAN MONITOR TEMPERATURE SOURCE SELECT REGISTER/ STOPDUTY ENABLE REGISTER – INDEX 00H (BANK 1) 124
9.62 SYSFAN TARGET TEMPERATURE REGISTER / SYSFANIN TARGET SPEED_L REGISTER – INDEX 01H (BANK 1) 126
9.63 SYSFAN MODE REGISTER / SYSFAN TOLERRANCE REGISTER – INDEX 02H (BANK 1) 126
9.64 SYSFANOUT STEP UP TIME REGISTER – INDEX 03H (BANK 1) 126
9.65 SYSFANOUT STEP DOWN TIME REGISTER – INDEX 04H (BANK 1) 127
9.66 SYSFANOUT STOP VALUE REGISTER – INDEX 05H (BANK 1) 127
9.67 SYSFANOUT START-UP VALUE REGISTER – INDEX 06H (BANK 1) 127
9.68 SYSFANOUT STOP TIME REGISTER – INDEX 07H (BANK 1) 128
9.69 SYSFANOUT OUTPUT VALUE SELECT REGISTER – INDEX 09H (BANK 1) 128
9.70 SYSFANIN TOLERANCE_H / TARGET SPEED_H REGISTER – INDEX 0CH (BANK 1) 128
9.71 SYSFAN (SMART FAN™ IV) TEMPERATURE 1 REGISTER(T1) – INDEX 21H (BANK 1) 129
9.72 SYSFAN (SMART FAN™ IV) TEMPERATURE 2 REGISTER(T2) – INDEX 22H (BANK 1) 129
9.73 SYSFAN (SMART FAN™ IV) TEMPERATURE 3 REGISTER(T3) – INDEX 23H (BANK 1) 129
9.74 SYSFAN (SMART FAN™ IV) TEMPERATURE 4 REGISTER(T4) – INDEX 24H (BANK 1) 130
9.75 SYSFAN (SMART FAN™ IV) DC/PWM 1 REGISTER – INDEX 27H (BANK 1) 130
9.76 SYSFAN (SMART FAN™ IV) DC/PWM 2 REGISTER – INDEX 28H (BANK 1) 130
9.77 SYSFAN (SMART FAN™ IV) DC/PWM 3 REGISTER – INDEX 29H (BANK 1) 130
9.78 SYSFAN (SMART FAN™ IV) DC/PWM 4 REGISTER – INDEX 2AH (BANK 1) 131
9.79 SYSFAN 3-WIRE ENABLE REGISTER – INDEX 31H (BANK 1) 131
9.80 SYSFAN (SMART FAN™ IV) CRITICAL TEMPERATURE REGISTER – INDEX 35H (BANK 1) 131
9.81 SYSFAN ENABLE CRITICAL DUTY – INDEX 36H (BANK 1) 132
9.82 SYSFAN CRITICAL DUTY REGISTER – INDEX 37H (BANK 1) 132
9.83 SYSFANOUT CRITICAL TEMPERATURE TOLERANCE REGISTER – INDEX 38H (BANK 1) 132
9.84 SYSFAN PECIERR DUTY ENABLE REGISTER – INDEX 3FH (BANK 1) 133
9.85 SYSFANOUT PRE-CONFIGURED REGISTER FOR PECI ERROR – INDEX 41H (BANK 1) 133
9.86 SMIOVT2 TEMPERATURE SOURCE (HIGH BYTE) REGISTER – INDEX 50H (BANK 1) 133
9.87 SMIOVT2 TEMPERATURE SOURCE (LOW BYTE) REGISTER – INDEX 51H (BANK 1) 133
9.88 SMIOVT2 TEMPERATURE SOURCE CONFIGURATION REGISTER – INDEX 52H (BANK 1) 134
9.89 SMIOVT2 TEMPERATURE SOURCE HYSTERESIS (HIGH BYTE) REGISTER – INDEX 53H (BANK 1) 134
9.90 SMIOVT2 TEMPERATURE SOURCE HYSTERESIS (LOW BYTE) REGISTER – INDEX 54H (BANK 1) 134
9.91 SMIOVT2 TEMPERATURE SOURCE OVER-TEMPERATURE (HIGH BYTE) REGISTER – INDEX 55H (BANK1) 135
9.92 SMIOVT2 TEMPERATURE SOURCE OVER-TEMPERATURE (LOW BYTE) REGISTER – INDEX 56H (BANK 1) 135
9.93 DUTY PER STEP REGISTER – INDEX 66H (BANK 1) 135
9.94 T1 DELAY TIME REGISTER – INDEX 67H (BANK 1) 136
9.95 SYSFAN MAX DUTY COMPARE SOURCE SELECT REGISTER – INDEX 68H (BANK 1) 136
9.96 SYSFAN MAX DUTY OUTPUT REGISTER – INDEX 69H (BANK 1) 136
9.97 CPUFAN MONITOR TEMPERATURE SOURCE SELECT REGISTER/ STOPDUTY ENABLE REGISTER – INDEX 00H (BANK 2) 137
9.98 CPUFAN TARGET TEMPERATURE REGISTER / CPUFANIN TARGET SPEED_L REGISTER – INDEX 01H (BANK 2) 138
9.99 CPUFAN MODE REGISTER / CPUFAN TOLERRANCE REGISTER – INDEX 02H (BANK 2) 138
9.100 CPUFANOUT STEP UP TIME REGISTER – INDEX 03H (BANK 2) 139

9.101 CPUFANOUT STEP DOWN TIME REGISTER – INDEX 04H (BANK 2) 139
9.102 CPUFANOUT STOP VALUE REGISTER – INDEX 05H (BANK 2) 139
9.103 CPUFANOUT START-UP VALUE REGISTER – INDEX 06H (BANK 2) 140
9.104 CPUFANOUT STOP TIME REGISTER – INDEX 07H (BANK 2) 140
9.105 CPUFANOUT OUTPUT VALUE SELECT REGISTER – INDEX 09H (BANK 2) 140
9.106 CPUFANIN TOLERANCE_H / TARGET SPEED_H REGISTER – INDEX 0CH (BANK 2) 140
9.107 CPUFAN MODE REGISTER / THERMAL MARGIN REGISTER – INDEX 0DH (BANK 2) 141
9.108 CPUFAN MODE REGISTER / T CONTROL REGISTER – INDEX 0FH (BANK 2) 141
9.109 CPUFAN (SMART FAN™ IV) TEMPERATURE 1 REGISTER(T1) – INDEX 21H (BANK 2) 142
9.110 CPUFAN (SMART FAN™ IV) TEMPERATURE 2 REGISTER(T2) – INDEX 22H (BANK 2) 142
9.111 CPUFAN (SMART FAN™ IV) TEMPERATURE 3 REGISTER(T3) – INDEX 23H (BANK 2) 142
9.112 CPUFAN (SMART FAN™ IV) TEMPERATURE 4 REGISTER(T4) – INDEX 24H (BANK 2) 142
9.113 CPUFAN (SMART FAN™ IV) PWM1 REGISTER – INDEX 27H (BANK 2) 143
9.114 CPUFAN (SMART FAN™ IV) PWM2 REGISTER – INDEX 28H (BANK 2) 143
9.115 CPUFAN (SMART FAN™ IV) PWM3 REGISTER – INDEX 29H (BANK 2) 143
9.116 CPUFAN (SMART FAN™ IV) PWM4 REGISTER – INDEX 2AH (BANK 2) 143
9.117 CPUFAN 3-WIRE FAN ENABLE REGISTER – INDEX 31H (BANK 2) 144
9.118 CPUFAN (SMART FAN™ IV) CRITICAL TEMPERATURE REGISTER – INDEX 35H (BANK 2) 144
9.119 CPUFAN ENABLE CRITICAL DUTY – INDEX 36H (BANK 2) 144
9.120 CPUFAN CRITICAL DUTY REGISTER – INDEX 37H (BANK 2) 145
9.121 CPUFANOUT CRITICAL TEMPERATURE TOLERANCE REGISTER – INDEX 38H (BANK 2) 145
9.122 WEIGHT VALUE CONFIGURATION REGISTER – INDEX 39H (BANK 2) 145
9.123 CPUFANOUT TEMPERATURE STEP REGISTER – INDEX 3AH (BANK 2) 146
9.124 CPUFANOUT TEMPERATURE STEP TOLERANCE REGISTER – INDEX 3BH (BANK 2) 147
9.125 CPUFANOUT WEIGHT STEP REGISTER – INDEX 3CH (BANK 2) 147
9.126 CPUFANOUT TEMPERATURE BASE REGISTER – INDEX 3DH (BANK 2) 147
9.127 CPUFANOUT TEMPERATURE FAN DUTY BASE REGISTER – INDEX 3EH (BANK 2) 147
9.128 CPUFAN PECIERR DUTY ENABLE REGISTER – INDEX 3FH (BANK 2) 148
9.129 CPUFANOUT PRE-CONFIGURED REGISTER FOR PECI ERROR – INDEX 41H (BANK 2) 148
9.130 DUTY PER STEP REGISTER – INDEX 66H (BANK 2) 148
9.131 T1 DELAY TIME REGISTER – INDEX 67H (BANK 2) 149
9.132 CPUFAN MAX DUTY COMPARE SOURCE SELECT REGISTER – INDEX 68H (BANK 2) 149
9.133 CPUFAN MAX DUTY OUTPUT REGISTER – INDEX 69H (BANK 2) 149
9.134 AUXFAN0 MONITOR TEMPERATURE SOURCE SELECT REGISTER/ STOPDUTY ENABLE REGISTER – INDEX 00H (BANK 3) 150
9.135 AUXFAN0 TARGET TEMPERATURE REGISTER / AUXFANIN0 TARGET SPEED_L REGISTER – INDEX 01H (BANK 3) 151
9.136 AUXFAN0 MODE REGISTER / AUXFAN0 TOLERRANCE REGISTER – INDEX 02H (BANK 3) 151
9.137 AUXFANOUT0 STEP UP TIME REGISTER – INDEX 03H (BANK 3) 152
9.138 AUXFANOUT0 STEP DOWN TIME REGISTER – INDEX 04H (BANK 3) 152
9.139 AUXFANOUT0 STOP VALUE REGISTER – INDEX 05H (BANK 3) 152
9.140 AUXFANOUT0 START-UP VALUE REGISTER – INDEX 06H (BANK 3) 152
9.141 AUXFANOUT0 STOP TIME REGISTER – INDEX 07H (BANK 3) 153
9.142 AUXFANOUT0 OUTPUT VALUE SELECT REGISTER – INDEX 09H (BANK 3) 153
9.143 AUXFANIN0 TOLERANCE_H / TARGET SPEED_H REGISTER – INDEX 0CH (BANK 3) 153
9.144 AUXFAN0 MODE REGISTER / THERMAL MARGIN REGISTER – INDEX 0DH (BANK 3) 154
9.145 AUXFAN0 MODE REGISTER / T CONTROL REGISTER – INDEX 0FH (BANK 3) 154
9.146 AUXFAN0 (SMART FAN™ IV) TEMPERATURE 1 REGISTER(T1) – INDEX 21H (BANK 3) 154
9.147 AUXFAN0 (SMART FAN™ IV) TEMPERATURE 2 REGISTER(T2) – INDEX 22H (BANK 3) 155
9.148 AUXFAN0 (SMART FAN™ IV) TEMPERATURE 3 REGISTER(T3) – INDEX 23H (BANK 3) 155
9.149 AUXFAN0 (SMART FAN™ IV) TEMPERATURE 4 REGISTER(T4) – INDEX 24H (BANK 3) 155
9.150 AUXFAN0 (SMART FAN™ IV) PWM 1 REGISTER – INDEX 27H (BANK 3) 156
9.151 AUXFAN0 (SMART FAN™ IV) PWM 2 REGISTER – INDEX 28H (BANK 3) 156
9.152 AUXFAN0 (SMART FAN™ IV) PWM 3 REGISTER – INDEX 29H (BANK 3) 156
9.153 AUXFAN0 (SMART FAN™ IV) PWM 4 REGISTER – INDEX 2AH (BANK 3) 156
9.154 AUXFAN0 3-WIRE ENABLE REGISTER – INDEX 31H (BANK 3) 157

9.155 AUXFAN0 (SMART FAN™ IV) CRITICAL TEMPERATURE REGISTER – INDEX 35H (BANK 3) 157
9.156 AUXFAN0 ENABLE CRITICAL DUTY – INDEX 36H (BANK 3) 157
9.157 AUXFAN0 CRITICAL DUTY REGISTER – INDEX 37H (BANK 3) 158
9.158 AUXFANOUT0 CRITICAL TEMPERATURE TOLERANCE REGISTER – INDEX 38H (BANK 3) 158
9.159 AUXFAN0 PECIERR DUTY ENABLE REGISTER – INDEX 3FH (BANK 3) 158
9.160 AUXFANOUT0 PRE-CONFIGURED REGISTER FOR PECI ERROR – INDEX 41H (BANK 3) 159
9.161 DUTY PER STEP REGISTER – INDEX 66H (BANK 3) 159
9.162 T1 DELAY TIME REGISTER – INDEX 67H (BANK 3) 159
9.163 AUXFAN0 MAX DUTY COMPARE SOURCE SELECT REGISTER – INDEX 68H (BANK 3) 159
9.164 AUXFAN0 MAX DUTY OUTPUT REGISTER – INDEX 69H (BANK 3) 160
9.165 PCH_CHIP_CPU_MAX_TEMP REGISTER – INDEX 00H (BANK 4) 160
9.166 PCH_CHIP_TEMP REGISTER – INDEX 01H (BANK 4) 161
9.167 PCH_CPU_TEMP_H REGISTER – INDEX 02H (BANK 4) 161
9.168 PCH_CPU_TEMP_L REGISTER – INDEX 03H (BANK 4) 161
9.169 PCH_MCH_TEMP REGISTER – INDEX 04H (BANK 4) 161
9.170 AGENT0 DIMM0 REGISTER – INDEX 05H (BANK 4) 162
9.171 AGENT0 DIMM1 REGISTER – INDEX 06H (BANK 4) 162
9.172 AGENT1 DIMM0 REGISTER – INDEX 07H (BANK 4) 162
9.173 AGENT1 DIMM1 REGISTER – INDEX 08H (BANK 4) 163
9.174 PCH_TSI0_TEMP_H REGISTER – INDEX 09H (BANK 4) 163
9.175 PCH_TSI0_TEMP_L REGISTER – INDEX 0AH (BANK 4) 163
9.176 PCH_TSI1_TEMP_H REGISTER – INDEX 0BH (BANK 4) 163
9.177 PCH_TSI1_TEMP_L REGISTER – INDEX 0CH (BANK 4) 164
9.178 BYTETEMP0 REGISTER – INDEX 19H (BANK 4) 164
9.179 BYTETEMP1 REGISTER – INDEX 1AH (BANK 4) 164
9.180 VIN1 HIGH LIMIT COMPARED VOLTAGE REGISTER – INDEX 23H (BANK 4) 165
9.181 VIN1 LOW LIMIT COMPARED VOLTAGE REGISTER – INDEX 24H (BANK 4) 165
9.182 VIN0 HIGH LIMIT COMPARED VOLTAGE REGISTER – INDEX 25H (BANK 4) 165
9.183 VIN0 LOW LIMIT COMPARED VOLTAGE REGISTER – INDEX 26H (BANK 4) 165
9.184 AVSB HIGH LIMIT COMPARED VOLTAGE REGISTER – INDEX 27H (BANK 4) 166
9.185 AVSB LOW LIMIT COMPARED VOLTAGE REGISTER – INDEX 28H (BANK 4) 166
9.186 VOLTAGE COMPARATION INTERRUPT STATUS REGISTER - INDEX 42H (BANK 4) 166
9.187 AUXTIN1 TEMPERATURE SENSOR OFFSET REGISTER – INDEX 4AH (BANK 4) 167
9.188 AUXTIN2 TEMPERATURE SENSOR OFFSET REGISTER – INDEX 4BH (BANK 4) 167
9.189 AUXTIN3 TEMPERATURE SENSOR OFFSET REGISTER – INDEX 4CH (BANK 4) 167
9.190 AUXTIN4 TEMPERATURE SENSOR OFFSET REGISTER – INDEX 4DH (BANK 4) 168
9.191 INTERRUPT STATUS REGISTER 3 – INDEX 50H (BANK 4) 168
9.192 SMI# MASK REGISTER 4 – INDEX 51H (BANK 4) 168
9.193 SYSTIN TEMPERATURE SENSOR OFFSET REGISTER – INDEX 54H (BANK 4) 169
9.194 CPUTIN TEMPERATURE SENSOR OFFSET REGISTER – INDEX 55H (BANK 4) 169
9.195 AUXTIN0 TEMPERATURE SENSOR OFFSET REGISTER – INDEX 56H (BANK 4) 169
9.196 REAL TIME HARDWARE STATUS REGISTER I – INDEX 59H (BANK 4) 170
9.197 REAL TIME HARDWARE STATUS REGISTER II – INDEX 5AH (BANK 4) 171
9.198 REAL TIME HARDWARE STATUS REGISTER III – INDEX 5BH (BANK 4) 171
9.199 REAL TIME HARDWARE STATUS REGISTER III – INDEX 5DH (BANK 4) 172
9.200 IS<8:1> CURRENT REGISTER – INDEX 60H (BANK 4) 173
9.201 IS<0> CURRENT REGISTER – INDEX 61H (BANK 4) 173
9.202 POWER <9:2> REGISTER – INDEX 62H (BANK 4) 173
9.203 POWER<1:0> REGISTER – INDEX 63H (BANK 4) 174
9.204 VIN REGISTER – INDEX 64H (BANK 4) 174
9.205 RREG SETTING REGISTER – INDEX 65H (BANK 4) 174
9.206 REG_RATIO_K AND POWER_VOLTAGE ENABLE REGISTER – INDEX 66H (BANK 4) 174
9.207 POWER_V REGISTER – INDEX 67H (BANK 4) 175
9.208 VALUE RAM — INDEX 80H ~ 96H (BANK 4) 175
9.209 (SYSFANIN) FANIN1 COUNT HIGH-BYTE REGISTER – INDEX B0H (BANK 4) 176
9.210 (SYSFANIN) FANIN1 COUNT LOW-BYTE REGISTER – INDEX B1H (BANK 4) 176

9.211 (CPUFANIN) FANIN2 COUNT HIGH-BYTE REGISTER – INDEX B2H (BANK 4) 177
9.212 (CPUFANIN) FANIN2 COUNT LOW-BYTE REGISTER – INDEX B3H (BANK 4) 177
9.213 (AUXFANIN0) FANIN3 COUNT HIGH-BYTE REGISTER – INDEX B4H (BANK 4) 177
9.214 (AUXFANIN0) FANIN3 COUNT LOW-BYTE REGISTER – INDEX B5H (BANK 4) 177
9.215 (AUXFANIN1) FANIN4 COUNT HIGH-BYTE REGISTER – INDEX B6H (BANK 4) 178
9.216 (AUXFANIN1) FANIN4 COUNT LOW-BYTE REGISTER – INDEX B7H (BANK 4) 178
9.217 (AUXFANIN2) FANIN5 COUNT HIGH-BYTE REGISTER – INDEX B8H (BANK 4) 178
9.218 (AUXFANIN2) FANIN5 COUNT LOW-BYTE REGISTER – INDEX B9H (BANK 4) 179
9.219 (AUXFANIN3) FANIN6 COUNT HIGH-BYTE REGISTER – INDEX BAH (BANK 4) 179
9.220 (AUXFANIN3) FANIN6 COUNT LOW-BYTE REGISTER – INDEX BBH (BANK 4) 179
9.221 SYSFANIN SPEED HIGH-BYTE VALUE (RPM) - INDEX C0H (BANK 4) 179
9.222 SYSFANIN SPEED LOW-BYTE VALUE (RPM) - INDEX C1H (BANK 4) 180
9.223 CPUFANIN SPEED HIGH-BYTE VALUE (RPM) – INDEX C2H (BANK 4) 180
9.224 CPUFANIN SPEED LOW-BYTE VALUE (RPM) – INDEX C3H (BANK 4) 180
9.225 AUXFANIN0 SPEED HIGH-BYTE VALUE (RPM) – INDEX C4H (BANK 4) 181
9.226 AUXFANIN0 SPEED LOW-BYTE VALUE (RPM) – INDEX C5H (BANK 4) 181
9.227 AUXFANIN1 SPEED HIGH-BYTE VALUE (RPM) – INDEX C6H (BANK 4) 181
9.228 AUXFANIN1 SPEED LOW-BYTE VALUE (RPM) – INDEX C7H (BANK 4) 181
9.229 AUXFANIN2 SPEED HIGH-BYTE VALUE (RPM) – INDEX C8H (BANK 4) 182
9.230 AUXFANIN2 SPEED LOW-BYTE VALUE (RPM) – INDEX C9H (BANK 4) 182
9.231 AUXFANIN3 SPEED HIGH-BYTE VALUE (RPM) – INDEX CAH (BANK 4) 182
9.232 AUXFANIN3 SPEED LOW-BYTE VALUE (RPM) – INDEX CBH (BANK 4) 183
9.233 PECI AGENT0 CALIBRATION TEMP – INDEX F4H (BANK 4) 183
9.234 PECI AGENT1 CALIBRATION TEMP – INDEX F5H (BANK 4) 183
9.235 PECI AGENT0 CALIBRATION CONTROL REGISTER – INDEX F8H (BANK 4) 183
9.236 PECI AGENT1 CALIBRATION CONTROL REGISTER – INDEX F9H (BANK 4) 184
9.237 PECI AGENT0 CALIBRATION CONTROL REGISTER – INDEX FAH (BANK 4) 184
9.238 PECI AGENT1 CALIBRATION CONTROL REGISTER – INDEX FBH (BANK 4) 184
9.239 VALUE RAM 2 — INDEX 50H-63H (BANK 5) 185
9.240 SMI# MASK REGISTER 1 – INDEX 66H (BANK 5) 185
9.241 INTERRUPT STATUS REGISTER – INDEX 67H (BANK 5) 186
9.242 REAL TIME HARDWARE STATUS REGISTER – INDEX 68H (BANK 5) 186
9.243 CLOSE-LOOP FAN CONTROL RPM MODE REGISTER – INDEX 00 (BANK 6) 187
9.244 SYSFAN RPM MODE TOLERANCE REGISTER – INDEX 01 (BANK 6) 188
9.245 CPUFAN RPM MODE TOLERANCE REGISTER – INDEX 02 (BANK 6) 188
9.246 AUXFAN0 RPM MODE TOLERANCE REGISTER – INDEX 03 (BANK 6) 188
9.247 AUXFAN1 RPM MODE TOLERANCE REGISTER – INDEX 04 (BANK 6) 189
9.248 AUXFAN2 RPM MODE TOLERANCE REGISTER – INDEX 05 (BANK 6) 189
9.249 ENABLE RPM HIGH MODE REGISTER – INDEX 06 (BANK 6) 189
9.250 SMIOVT1 TEMPERATURE SOURCE SELECT REGISTER – INDEX 21 (BANK 6) 190
9.251 SMIOVT2 TEMPERATURE SOURCE SELECT REGISTER – INDEX 22 (BANK 6) 191
9.252 AUXFAN3 RPM MODE TOLERANCE REGISTER – INDEX 23 (BANK 6) 192
9.253 AUXFAN4 RPM MODE TOLERANCE REGISTER – INDEX 24 (BANK 6) 192
9.254 (SYSFANIN) FAN COUNT LIMIT HIGH-BYTE REGISTER – INDEX 3AH (BANK 6) 193
9.255 (SYSFANIN) FAN COUNT LIMIT LOW-BYTE REGISTER – INDEX 3BH (BANK 6) 193
9.256 (CPUFANIN) FAN COUNT LIMIT HIGH-BYTE REGISTER – INDEX 3CH (BANK 6) 193
9.257 (CPUFANIN) FAN COUNT LIMIT LOW-BYTE REGISTER – INDEX 3DH (BANK 6) 194
9.258 (AUXFANIN0) FAN COUNT LIMIT HIGH-BYTE REGISTER – INDEX 3EH (BANK 6) 194
9.259 (AUXFANIN0) FAN COUNT LIMIT LOW-BYTE REGISTER – INDEX 3FH (BANK 6) 194
9.260 (AUXFANIN1) FAN COUNT LIMIT HIGH-BYTE REGISTER – INDEX 40H (BANK 6) 195
9.261 (AUXFANIN1) FAN COUNT LIMIT LOW-BYTE REGISTER – INDEX 41H (BANK 6) 195
9.262 (AUXFANIN2) FAN COUNT LIMIT HIGH-BYTE REGISTER – INDEX 42H (BANK 6) 195
9.263 (AUXFANIN2) FAN COUNT LIMIT LOW-BYTE REGISTER – INDEX 43H (BANK 6) 195
9.264 SYSFANIN REVOLUTION PULSES SELECTION REGISTER – INDEX 44H (BANK 6) 196
9.265 CPUFANIN REVOLUTION PULSES SELECTION REGISTER – INDEX 45H (BANK 6) 196
9.266 AUXFANIN0 REVOLUTION PULSES SELECTION REGISTER – INDEX 46H (BANK 6) 197

9.267 AUXFANIN1 REVOLUTION PULSES SELECTION REGISTER – INDEX 47H (BANK 6) 197
9.268 AUXFANIN2 REVOLUTION PULSES SELECTION REGISTER – INDEX 48H (BANK 6) 197
9.269 AUXFANIN3 REVOLUTION PULSES SELECTION REGISTER – INDEX 49H (BANK 6) 198
9.270 (AUXFANIN3) FAN COUNT LIMIT HIGH-BYTE REGISTER – INDEX 4AH (BANK 6) 198
9.271 (AUXFANIN3) FAN COUNT LIMIT LOW-BYTE REGISTER – INDEX 4BH (BANK 6) 198
9.272 (AUXFANIN4) FAN COUNT LIMIT HIGH-BYTE REGISTER – INDEX 4CH (BANK 6) 199
9.273 (AUXFANIN4) FAN COUNT LIMIT LOW-BYTE REGISTER – INDEX 4DH (BANK 6) 199
9.274 AUXFANIN3 SPEED HIGH-BYTE VALUE (RPM) - INDEX 54H (BANK 6) 199
9.275 AUXFANIN3 SPEED LOW-BYTE VALUE (RPM) - INDEX 55H (BANK 6) 200
9.276 SYSFANIN SPEED HIGH-BYTE VALUE (RPM) - INDEX 56H (BANK 6) 200
9.277 SYSFANIN SPEED LOW-BYTE VALUE (RPM) - INDEX 57H (BANK 6) 200
9.278 CPUFANIN SPEED HIGH-BYTE VALUE (RPM) - INDEX 58H (BANK 6) 200
9.279 CPUFANIN SPEED LOW-BYTE VALUE (RPM) - INDEX 59H (BANK 6) 201
9.280 AUXFANIN0 SPEED HIGH-BYTE VALUE (RPM) - INDEX 5AH (BANK 6) 201
9.281 AUXFANIN0 SPEED LOW-BYTE VALUE (RPM) - INDEX 5BH (BANK 6) 201
9.282 AUXFANIN1 SPEED HIGH-BYTE VALUE (RPM) - INDEX 5CH (BANK 6) 201
9.283 AUXFANIN1 SPEED LOW-BYTE VALUE (RPM) - INDEX 5DH (BANK 6) 202
9.284 AUXFANIN2 SPEED HIGH-BYTE VALUE (RPM) - INDEX 5EH (BANK 6) 202
9.285 AUXFANIN2 SPEED LOW-BYTE VALUE (RPM) - INDEX 5FH (BANK 6) 202
9.286 AUXFANIN4 SPEED HIGH-BYTE VALUE (RPM) - INDEX 60H (BANK 6) 203
9.287 AUXFANIN4 SPEED LOW-BYTE VALUE (RPM) - INDEX 61H (BANK 6) 203
9.288 PECI ENABLE FUNCTION REGISTER – INDEX 01H (BANK 7) 203
9.289 PECI TIMING CONFIG REGISTER – INDEX 02H (BANK 7) 204
9.290 PECI AGENT CONFIG REGISTER – INDEX 03H (BANK 7) 204
9.291 PECI TEMPERATURE CONFIG REGISTER – INDEX 04H (BANK 7) 205
9.292 PECI COMMAND ADDRESS REGISTER – INDEX 05H (BANK 7) 205
9.293 PECI COMMAND WRITE LENGTH REGISTER – INDEX 06H (BANK 7) 206
9.294 PECI COMMAND READ LENGTH REGISTER – INDEX 07H (BANK 7) 206
9.295 PECI COMMAND CODE REGISTER – INDEX 08H (BANK 7) 206
9.296 PECI COMMAND TBASE0 REGISTER – INDEX 09H (BANK 7) 207
9.297 PECI COMMAND TBASE1 REGISTER – INDEX 0AH (BANK 7) 207
9.298 PECI COMMAND WRITE DATA 1 REGISTER – INDEX 0BH (BANK 7) 207
9.299 PECI COMMAND WRITE DATA 2 REGISTER – INDEX 0CH (BANK 7) 207
9.300 PECI COMMAND WRITE DATA 3 REGISTER – INDEX 0DH (BANK 7) 208
9.301 PECI COMMAND WRITE DATA 4 REGISTER – INDEX 0EH (BANK 7) 208
9.302 PECI COMMAND WRITE DATA 5 REGISTER – INDEX 0FH (BANK 7) 208
9.303 PECI COMMAND WRITE DATA 6 REGISTER – INDEX 10H (BANK 7) 209
9.304 PECI COMMAND WRITE DATA 7 REGISTER – INDEX 11H (BANK 7) 209
9.305 PECI COMMAND WRITE DATA 8 REGISTER – INDEX 12H (BANK 7) 209
9.306 PECI COMMAND WRITE DATA 9 REGISTER – INDEX 13H (BANK 7) 210
9.307 PECI COMMAND WRITE DATA 10 REGISTER – INDEX 14H (BANK 7) 210
9.308 PECI COMMAND WRITE DATA 11 REGISTER – INDEX 15H (BANK 7) 210
9.309 PECI COMMAND WRITE DATA 12 REGISTER – INDEX 16H (BANK 7) 210
9.310 PECI AGENT RELATIVE TEMPERATURE REGISTER (ARTR) – INDEX 17H-1EH (BANK 7) 211
9.311 PECI ALIVE AGENT REGISTER – INDEX 1FH (BANK 7) 212
9.312 PECI TEMPERATURE READING REGISTER (INTEGER) – INDEX 20H (BANK 7) 212
9.313 PECI TEMPERATURE READING REGISTER (FRACTION) – INDEX 21H (BANK 7) 213
9.314 PECI COMMAND TN COUNT VALUE REGISTER – INDEX 22H (BANK 7) 213
9.315 PECI COMMAND TN COUNT VALUE REGISTER – INDEX 23H (BANK 7) 213
9.316 PECI COMMAND WARNING FLAG REGISTER – INDEX 24H (BANK 7) 214
9.317 PECI COMMAND FCS DATA REGISTER – INDEX 25H (BANK 7) 214
9.318 PECI COMMAND WFCS DATA REGISTER – INDEX 26H (BANK 7) 214
9.319 PECI RFCS DATA REGISTER – INDEX 27H (BANK 7) 215
9.320 PECI AWFCS DATA REGISTER – INDEX 28H (BANK 7) 215
9.321 PECI CRC OUT WFCS DATA REGISTER – INDEX 29H (BANK 7) 215
9.322 PECI COMMAND READ DATA 1 REGISTER – INDEX 2AH (BANK 7) 216

9.323 PECI COMMAND READ DATA 2 REGISTER – INDEX 2BH (BANK 7) 216
9.324 PECI COMMAND READ DATA 3 REGISTER – INDEX 2CH (BANK 7) 216
9.325 PECI COMMAND READ DATA 4 REGISTER – INDEX 2DH (BANK 7) 217
9.326 PECI COMMAND READ DATA 5 REGISTER – INDEX 2EH (BANK 7) 217
9.327 PECI COMMAND READ DATA 6 REGISTER – INDEX 2FH (BANK 7) 217
9.328 PECI COMMAND READ DATA 7 REGISTER – INDEX 30H (BANK 7) 218
9.329 PECI COMMAND READ DATA 8 REGISTER – INDEX 31H (BANK 7) 218
9.330 PECI COMMAND READ DATA 9 REGISTER – INDEX 32H (BANK 7) 218
9.331 PECI READ DIMM DATA 1 REGISTER – INDEX 33H (BANK 7) 219
9.332 PECI READ DIMM DATA 2 REGISTER – INDEX 34H (BANK 7) 219
9.333 PECI READ DIMM DATA 3 REGISTER – INDEX 35H (BANK 7) 219
9.334 PECI READ DIMM DATA 4 REGISTER – INDEX 36H (BANK 7) 220
9.335 PECI READ MARGIN DATA 1 REGISTER – INDEX 37H (BANK 7) 220
9.336 PECI READ MARGIN DATA 2 REGISTER – INDEX 38H (BANK 7) 220
9.337 PECI READ MARGIN DATA 3 REGISTER – INDEX 39H (BANK 7) 220
9.338 PECI READ MARGIN DATA 4 REGISTER – INDEX 3AH (BANK 7) 221
9.339 PECI READ DIMM INDEX DATA REGISTER – INDEX 3BH (BANK 7) 221
9.340 PECI EAD DIMM INDEX DATA REGISTER – INDEX 3CH (BANK 7) 221
9.341 AUXFAN1 MONITOR TEMPERATURE SOURCE SELECT REGISTER/ STOPDUTY ENABLE REGISTER – INDEX 00H (BANK 8) 223
9.342 AUXFAN1 TARGET TEMPERATURE REGISTER / AUXFANIN1 TARGET SPEED_L REGISTER – INDEX 01H (BANK 8) 225
9.343 AUXFAN1 MODE REGISTER / AUXFAN1 TOLERRANCE REGISTER – INDEX 02H (BANK 8) 225
9.344 AUXFANOUT1 STEP UP TIME REGISTER – INDEX 03H (BANK 8) 225
9.345 AUXFANOUT1 STEP DOWN TIME REGISTER – INDEX 04H (BANK 8) 226
9.346 AUXFANOUT1 STOP VALUE REGISTER – INDEX 05H (BANK 8) 226
9.347 AUXFANOUT1 START-UP VALUE REGISTER – INDEX 06H (BANK 8) 226
9.348 AUXFANOUT1 STOP TIME REGISTER – INDEX 07H (BANK 8) 226
9.349 AUXFANOUT1 OUTPUT VALUE SELECT REGISTER – INDEX 09H (BANK 8) 227
9.350 AUXFANIN1 TOLERANCE_H / TARGET SPEED_H REGISTER – INDEX 0CH (BANK 8) 227
9.351 AUXFAN1 (SMART FAN™ IV) TEMPERATURE 1 REGISTER(T1) – INDEX 21H (BANK 8) 227
9.352 AUXFAN1 (SMART FAN™ IV) TEMPERATURE 2 REGISTER(T2) – INDEX 22H (BANK 8) 228
9.353 AUXFAN1 (SMART FAN™ IV) TEMPERATURE 3 REGISTER(T3) – INDEX 23H (BANK 8) 228
9.354 AUXFAN1 (SMART FAN™ IV) TEMPERATURE 4 REGISTER(T4) – INDEX 24H (BANK 8) 228
9.355 AUXFAN1 (SMART FAN™ IV) PWM 1 REGISTER – INDEX 27H (BANK 8) 229
9.356 AUXFAN1 (SMART FAN™ IV) PWM 2 REGISTER – INDEX 28H (BANK 8) 229
9.357 AUXFAN1 (SMART FAN™ IV) PWM 3 REGISTER – INDEX 29H (BANK 8) 229
9.358 AUXFAN1 (SMART FAN™ IV) PWM 4 REGISTER – INDEX 2AH (BANK 8) 229
9.359 AUXFAN1 3-WIRE ENABLE REGISTER – INDEX 31H (BANK 8) 230
9.360 AUXFAN1 (SMART FAN™ IV) CRITICAL TEMPERATURE REGISTER – INDEX 35H (BANK 8) 230
9.361 AUXFAN1 ENABLE CRITICAL DUTY – INDEX 36H (BANK 8) 230
9.362 AUXFAN1 CRITICAL DUTY REGISTER – INDEX 37H (BANK 8) 231
9.363 AUXFANOUT1 CRITICAL TEMPERATURE TOLERANCE REGISTER – INDEX 38H (BANK 8) 231
9.364 AUXFAN1 PECIERR DUTY ENABLE REGISTER – INDEX 3FH (BANK 8) 231
9.365 AUXFANOUT1 PRE-CONFIGURED REGISTER FOR PECI ERROR – INDEX 41H (BANK 8) 232
9.366 DUTY PER STEP REGISTER – INDEX 66H (BANK 8) 232
9.367 T1 DELAY TIME REGISTER – INDEX 67H (BANK 8) 232
9.368 AUXFAN1 MAX DUTY COMPARE SOURCE SELECT REGISTER – INDEX 68H (BANK 8) 232
9.369 AUXFAN1 MAX DUTY OUTPUT REGISTER – INDEX 69H (BANK 8) 233
9.370 AUXFAN2 MONITOR TEMPERATURE SOURCE SELECT REGISTER/ STOPDUTY ENABLE REGISTER – INDEX 00H (BANK 9) 233
9.371 AUXFAN2 TARGET TEMPERATURE REGISTER / AUXFANIN2 TARGET SPEED_L REGISTER – INDEX 01H (BANK 9) 234
9.372 AUXFAN2 MODE REGISTER / AUXFAN2 TOLERRANCE REGISTER – INDEX 02H (BANK 9) 235
9.373 AUXFANOUT2 STEP UP TIME REGISTER – INDEX 03H (BANK 9) 235
9.374 AUXFANOUT2 STEP DOWN TIME REGISTER – INDEX 04H (BANK 9) 235

9.375 AUXFANOUT2 STOP VALUE REGISTER – INDEX 05H (BANK 9) 236
9.376 AUXFANOUT2 START-UP VALUE REGISTER – INDEX 06H (BANK 9) 236
9.377 AUXFANOUT2 STOP TIME REGISTER – INDEX 07H (BANK 9) 236
9.378 AUXFANOUT2 OUTPUT VALUE SELECT REGISTER – INDEX 09H (BANK 9) 237
9.379 AUXFANIN2 TOLERANCE_H / TARGET SPEED_H REGISTER – INDEX 0CH (BANK 9) 237
9.380 AUXFAN2 (SMART FAN™ IV) TEMPERATURE 1 REGISTER(T1) – INDEX 21H (BANK 9) 237
9.381 AUXFAN2 (SMART FAN™ IV) TEMPERATURE 2 REGISTER(T2) – INDEX 22H (BANK 9) 238
9.382 AUXFAN2 (SMART FAN™ IV) TEMPERATURE 3 REGISTER(T3) – INDEX 23H (BANK 9) 238
9.383 AUXFAN2 (SMART FAN™ IV) TEMPERATURE 4 REGISTER(T4) – INDEX 24H (BANK 9) 238
9.384 AUXFAN2 (SMART FAN™ IV) PWM 1 REGISTER – INDEX 27H (BANK 9) 238
9.385 AUXFAN2 (SMART FAN™ IV) PWM 2 REGISTER – INDEX 28H (BANK 9) 239
9.386 AUXFAN2 (SMART FAN™ IV) PWM 3 REGISTER – INDEX 29H (BANK 9) 239
9.387 AUXFAN2 (SMART FAN™ IV) PWM 4 REGISTER – INDEX 2AH (BANK 9) 239
9.388 AUXFAN2 3-WIRE ENABLE REGISTER – INDEX 31H (BANK 9) 240
9.389 AUXFAN2 (SMART FAN™ IV) CRITICAL TEMPERATURE REGISTER – INDEX 35H (BANK 9) 240
9.390 AUXFAN2 ENABLE CRITICAL DUTY – INDEX 36H (BANK 9) 240
9.391 AUXFAN2 CRITICAL DUTY REGISTER – INDEX 37H (BANK 9) 241
9.392 AUXFANOUT2 CRITICAL TEMPERATURE TOLERANCE REGISTER – INDEX 38H (BANK 9) 241
9.393 AUXFAN2 PECIERR DUTY ENABLE REGISTER – INDEX 3FH (BANK 9) 241
9.394 AUXFANOUT2 PRE-CONFIGURED REGISTER FOR PECI ERROR – INDEX 41H (BANK 9) 241
9.395 DUTY PER STEP REGISTER – INDEX 66H (BANK 9) 242
9.396 T1 DELAY TIME REGISTER – INDEX 67H (BANK 9) 242
9.397 AUXFAN3 MONITOR TEMPERATURE SOURCE SELECT REGISTER/ STOPDUTY ENABLE REGISTER – INDEX 00H (BANK A) 242
9.398 AUXFAN3 TARGET TEMPERATURE REGISTER / AUXFANIN3 TARGET SPEED_L REGISTER – INDEX 01H (BANK A) 243
9.399 AUXFAN3 MODE REGISTER / AUXFAN2 TOLERRANCE REGISTER – INDEX 02H (BANK A) ... 244
9.400 AUXFANOUT3 STEP UP TIME REGISTER – INDEX 03H (BANK A) 244
9.401 AUXFANOUT3 STEP DOWN TIME REGISTER – INDEX 04H (BANK A) 244
9.402 AUXFANOUT3 STOP VALUE REGISTER – INDEX 05H (BANK A) 245
9.403 AUXFANOUT3 START-UP VALUE REGISTER – INDEX 06H (BANK A) 245
9.404 AUXFANOUT3 STOP TIME REGISTER – INDEX 07H (BANK A) 245
9.405 AUXFANOUT3 OUTPUT VALUE SELECT REGISTER – INDEX 09H (BANK A) 246
9.406 AUXFANIN3 TOLERANCE_H / TARGET SPEED_H REGISTER – INDEX 0CH (BANK A) 246
9.407 AUXFAN3 (SMART FAN™ IV) TEMPERATURE 1 REGISTER(T1) – INDEX 21H (BANK A) 246
9.408 AUXFAN3 (SMART FAN™ IV) TEMPERATURE 2 REGISTER(T2) – INDEX 22H (BANK A) 247
9.409 AUXFAN3 (SMART FAN™ IV) TEMPERATURE 3 REGISTER(T3) – INDEX 23H (BANK A) 247
9.410 AUXFAN3 (SMART FAN™ IV) TEMPERATURE 4 REGISTER(T4) – INDEX 24H (BANK A) 247
9.411 AUXFAN3 (SMART FAN™ IV) PWM 1 REGISTER – INDEX 27H (BANK A) 248
9.412 AUXFAN3 (SMART FAN™ IV) PWM 2 REGISTER – INDEX 28H (BANK A) 248
9.413 AUXFAN3 (SMART FAN™ IV) PWM 3 REGISTER – INDEX 29H (BANK A) 248
9.414 AUXFAN3 (SMART FAN™ IV) PWM 4 REGISTER – INDEX 2AH (BANK A) 248
9.415 AUXFAN3 3-WIRE ENABLE REGISTER – INDEX 31H (BANK A) 249
9.416 AUXFAN3 (SMART FAN™ IV) CRITICAL TEMPERATURE REGISTER – INDEX 35H (BANK A) 249
9.417 AUXFAN3 ENABLE CRITICAL DUTY – INDEX 36H (BANK A) 249
9.418 AUXFAN3 CRITICAL DUTY REGISTER – INDEX 37H (BANK A) 250
9.419 AUXFANOUT3 CRITICAL TEMPERATURE TOLERANCE REGISTER – INDEX 38H (BANK A) 250
9.420 AUXFAN3 PECIERR DUTY ENABLE REGISTER – INDEX 3FH (BANK A) 250
9.421 AUXFANOUT3 PRE-CONFIGURED REGISTER FOR PECI ERROR – INDEX 41H (BANK A) 251
9.422 DUTY PER STEP REGISTER – INDEX 66H (BANK A) 251
9.423 T1 DELAY TIME REGISTER – INDEX 67H (BANK A) 251
9.424 AUXFAN4 MONITOR TEMPERATURE SOURCE SELECT REGISTER/ STOPDUTY ENABLE REGISTER – INDEX 00H (BANK B) 251
9.425 AUXFAN4 TARGET TEMPERATURE REGISTER / AUXFANIN3 TARGET SPEED_L REGISTER – INDEX 01H (BANK B) 253
9.426 AUXFAN4 MODE REGISTER / AUXFAN2 TOLERRANCE REGISTER – INDEX 02H (BANK B) ... 253

9.427 AUXFANOUT4 STEP UP TIME REGISTER – INDEX 03H (BANK B) 253
9.428 AUXFANOUT4 STEP DOWN TIME REGISTER – INDEX 04H (BANK B) 254
9.429 AUXFANOUT4 STOP VALUE REGISTER – INDEX 05H (BANK B) 254
9.430 AUXFANOUT4 START-UP VALUE REGISTER – INDEX 06H (BANK B) 254
9.431 AUXFANOUT4 STOP TIME REGISTER – INDEX 07H (BANK B) 254
9.432 AUXFANOUT4 OUTPUT VALUE SELECT REGISTER – INDEX 09H (BANK B) 255
9.433 AUXFANIN3 TOLERANCE_H / TARGET SPEED_H REGISTER – INDEX 0CH (BANK B) 255
9.434 AUXFAN4 (SMART FAN™ IV) TEMPERATURE 1 REGISTER(T1) – INDEX 21H (BANK B) 255
9.435 AUXFAN4 (SMART FAN™ IV) TEMPERATURE 2 REGISTER(T2) – INDEX 22H (BANK B) 256
9.436 AUXFAN4 (SMART FAN™ IV) TEMPERATURE 3 REGISTER(T3) – INDEX 23H (BANK B) 256
9.437 AUXFAN4 (SMART FAN™ IV) TEMPERATURE 4 REGISTER(T4) – INDEX 24H (BANK B) 256
9.438 AUXFAN4 (SMART FAN™ IV) PWM 1 REGISTER – INDEX 27H (BANK B)..... 257
9.439 AUXFAN4 (SMART FAN™ IV) PWM 2 REGISTER – INDEX 28H (BANK B)..... 257
9.440 AUXFAN4 (SMART FAN™ IV) PWM 3 REGISTER – INDEX 29H (BANK B)..... 257
9.441 AUXFAN4 (SMART FAN™ IV) PWM 4 REGISTER – INDEX 2AH (BANK B)..... 257
9.442 AUXFAN4 3-WIRE ENABLE REGISTER – INDEX 31H (BANK B)..... 258
9.443 AUXFAN4 (SMART FAN™ IV) CRITICAL TEMPERATURE REGISTER – INDEX 35H (BANK B) 258
9.444 AUXFAN4 ENABLE CRITICAL DUTY – INDEX 36H (BANK B) 258
9.445 AUXFAN4 CRITICAL DUTY REGISTER – INDEX 37H (BANK B) 259
9.446 AUXFANOUT4 CRITICAL TEMPERATURE TOLERANCE REGISTER – INDEX 38H (BANK B)..... 259
9.447 AUXFAN4 PECIERR DUTY ENABLE REGISTER – INDEX 3FH (BANK B) 259
9.448 AUXFANOUT4 PRE-CONFIGURED REGISTER FOR PECI ERROR – INDEX 41H (BANK B) 260
9.449 DUTY PER STEP REGISTER – INDEX 66H (BANK B)..... 260
9.450 T1 DELAY TIME REGISTER – INDEX 67H (BANK B) 260
9.451 REAL TIME HARDWARE STATUS REGISTER I – INDEX 01H (BANK C)..... 260
9.452 INTERRUPT STATUS REGISTER – INDEX 02H (BANK C) 261
9.453 INTERRUPT STATUS REGISTER – INDEX 03H (BANK C) 262
9.454 SMI3-8# MASK REGISTER 1 – INDEX 04H (BANK C) 262
9.455 SMI3-8# MASK REGISTER 3 – INDEX 05H (BANK C) 263
9.456 SMI/OVT3-8 CONTROL REGISTER – INDEX 06H (BANK C)..... 263
9.457 SMIOVT3-8 TEMPERATURE SOURCE CONFIGURATION REGISTER – INDEX 07H (BANK C)..... 264
9.458 SMIOVT3-8 TEMPERATURE SOURCE CONFIGURATION REGISTER – INDEX 08H (BANK C)..... 265
9.459 CONFIGURATION REGISTER – INDEX 09H (BANK C) 265
9.460 CONFIGURATION REGISTER – INDEX 0AH (BANK C) 266
9.461 SMIOVT3-8 TEMPERATURE SOURCE CONFIGURATION REGISTER – INDEX 0CH (BANK C) 267
9.462 SMIOVT3-8 TEMPERATURE SOURCE CONFIGURATION REGISTER – INDEX 0DH (BANK C) 267
9.463 SMIOVT3 TEMPERATURE SOURCE OVER-TEMPERATURE (HIGH BYTE) REGISTER – INDEX 1AH (BANKC) 268
9.464 SMIOVT4 TEMPERATURE SOURCE OVER-TEMPERATURE (HIGH BYTE) REGISTER – INDEX 1BH (BANKC) 268
9.465 SMIOVT5 TEMPERATURE SOURCE OVER-TEMPERATURE (HIGH BYTE) REGISTER – INDEX 1CH (BANKC) 269
9.466 SMIOVT6 TEMPERATURE SOURCE OVER-TEMPERATURE (HIGH BYTE) REGISTER – INDEX 1DH (BANKC) 269
9.467 SMIOVT7 TEMPERATURE SOURCE OVER-TEMPERATURE (HIGH BYTE) REGISTER – INDEX 1EH (BANKC) 269
9.468 SMIOVT8 TEMPERATURE SOURCE OVER-TEMPERATURE (HIGH BYTE) REGISTER – INDEX 1FH (BANKC) 270
9.469 SMIOVT3 TEMPERATURE SOURCE HYSTERESIS (HIGH BYTE) REGISTER – INDEX 20H (BANK C).. 270
9.470 SMIOVT4 TEMPERATURE SOURCE HYSTERESIS (HIGH BYTE) REGISTER – INDEX 21H (BANK C).. 270
9.471 SMIOVT5 TEMPERATURE SOURCE HYSTERESIS (HIGH BYTE) REGISTER – INDEX 22H (BANK C).. 270
9.472 SMIOVT6 TEMPERATURE SOURCE HYSTERESIS (HIGH BYTE) REGISTER – INDEX 23H (BANK C).. 271
9.473 SMIOVT7 TEMPERATURE SOURCE HYSTERESIS (HIGH BYTE) REGISTER – INDEX 24H (BANK C).. 271
9.474 SMIOVT8 TEMPERATURE SOURCE HYSTERESIS (HIGH BYTE) REGISTER – INDEX 25H (BANK C).. 271
9.475 SMIOVT3 TEMPERATURE SOURCE SELECT REGISTER – INDEX 26 (BANK C)..... 272
9.476 SMIOVT4 TEMPERATURE SOURCE SELECT REGISTER – INDEX 27 (BANK C)..... 273

9.477 SMIOVT5 Temperature Source Select Register – Index 28 (Bank C) 274
9.478 SMIOVT6 Temperature Source Select Register – Index 29 (Bank C) 274
9.479 SMIOVT7 Temperature Source Select Register – Index 2A (Bank C) 275
9.480 SMIOVT8 Temperature Source Select Register – Index 2B (Bank C) 276
9.481 HM Read Only Register 277

10. UART PORT 282

10.1 UART Control Register (UCR) (Read/Write) 282
10.2 UART Status Register (USR) (Read/Write) 284
10.3 Handshake Control Register (HCR) (Read/Write) 284
10.4 Handshake Status Register (HSR) (Read/Write) 285
10.5 UART FIFO Control Register (UFR) (Write only) 286
10.6 Interrupt Status Register (ISR) (Read only) 286
10.7 Interrupt Control Register (ICR) (Read/Write) 287
10.8 Programmable Baud Generator (BLL/BHL) (Read/Write) 288
10.9 User-defined Register (UDR) (Read/Write) 289
10.10 UART RS485 Auto Flow Control 289

11. PARALLEL PORT 290

11.1 Printer Interface Logic 290
11.2 Enhanced Parallel Port (EPP) 291
11.2.1 Data Port (Data Swapper) 291
11.2.2 Printer Status Buffer 291
11.2.3 Printer Control Latch and Printer Control Swapper 292
11.2.4 EPP Address Port 292
11.2.5 EPP Data Port 0-3 293
11.2.6 EPP Pin Descriptions 293
11.2.7 EPP Operation 293
11.2.8 EPP Version 1.9 Operation 294
11.2.9 EPP Version 1.7 Operation 294
11.3 Extended Capabilities Parallel (ECP) Port 294
11.3.1 ECP Register and Bit Map 295
11.3.2 Data and ecpAFifo Port 295
11.3.3 Device Status Register (DSR) 296
11.3.4 Device Control Register (DCR) 296
11.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010 297
11.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011 297
11.3.7 TFIFO (Test FIFO Mode) Mode = 110 297
11.3.8 CNFGA (Configuration Register A) Mode = 111 297
11.3.9 CNFGB (Configuration Register B) Mode = 111 297
11.3.10 ECR (Extended Control Register) Mode = all 298
11.3.11 ECP Pin Descriptions 299
11.3.12 ECP Operation 300
11.3.13 FIFO Operation 300
11.3.14 DMA Transfers 301
11.3.15 Programmed I/O (NON-DMA) Mode 301

12. KEYBOARD CONTROLLER 303

12.1 Output Buffer 303
12.2 Input Buffer 303
12.3 Status Register 304
12.4 Commands 305
12.5 Hardware GATEA20/Keyboard Reset Control Logic 307
12.5.1 KB Control Register (Logic Device 5, CR[F0]) 307
12.5.2 Port 92 Control Register (Default Value = 0x00) 308

13. CONSUMER INFRARED REMOTE (CIR) 309

13.1 CIR REGISTER TABLE 309
13.1.1 IR Configuration Register – Base Address + 0 310
13.1.2 IR Status Register – Base Address + 1 310
13.1.3 IR Interrupt Configuration Register – Base Address + 2 311
13.1.4 RX FIFO Count– Base Address + 3 311
13.1.5 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6 312
13.1.6 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7 312
13.1.7 IR FIFO Configuration Register (FIFOCON) – Base Address + 8 312
13.1.8 IR Sample RX FIFO Status Register – Base Address + 9 313
13.1.9 IR Sample RX FIFO Register – Base Address + A 314
13.1.10 IR FSM Status Register (IRFSM) – Base Address + F 314
13.1.11 IR Minimum Length Register – Base Address + F 315

14. CONSUMER INFRARED REMOTE (CIR) WAKE-UP 316

14.1 CIR WAKE-UP REGISTER TABLE 316
14.1.1 IR Configuration Register – Base Address + 0 316
14.1.2 IR Status Register – Base Address + 1 317
14.1.3 IR Interrupt Configuration Register – Base Address + 2 318
14.1.4 IR TX Configuration Register – Base Address + 3 318
14.1.5 IR FIFO Compare Tolerance Configuration Register – Base Address + 4 319
14.1.6 RX FIFO Count– Base Address + 5 319
14.1.7 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6 319
14.1.8 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7 320
14.1.9 IR FIFO Configuration Register (FIFOCON) – Base Address + 8 320
14.1.10 IR Sample RX FIFO Status Register – Base Address + 9 320
14.1.11 IR Sample RX FIFO Register – Base Address + A 321
14.1.12 Write FIFO – Base Address + B 321
14.1.13 Read FIFO Only – Base Address + C 322
14.1.14 Read FIFO Index – Base Address + D 322
14.1.15 Reserved – Base Address + E 322
14.1.16 IR FSM Status Register (IRFSM) – Base Address + F 322
14.1.17 IR Minimum Length Register – Base Address + F 323

15. POWER MANAGEMENT EVENT 324

15.1 POWER CONTROL LOGIC 324
15.1.1 PSON# Logic 325
15.1.2 AC Power Failure Resume 325
15.1.3 PSOUT Blocking Time 327
15.2 WAKE UP THE SYSTEM BY KEYBOARD AND MOUSE 327
15.2.1 Waken up by Keyboard events 327
15.2.2 Waken up by Mouse events 328
15.3 RESUME RESET LOGIC 329

16. SERIALIZED IRQ 330

16.1 START FRAME 330
16.2 IRQ/DATA FRAME 331
16.3 STOP FRAME 332

17. WATCHDOG TIMER 333

18. GENERAL PURPOSE I/O 336

18.1 GPIO ARCHITECTURE 336
18.2 ACCESS CHANNELS 337

19. SMBUS MASTER INTERFACE 338

19.1 GENERAL DESCRIPTION 338

19.2 INTRODUCTION TO THE SMBUS MASTER 338
19.2.1 Data Transfer Format 338
19.2.2 Arbitration 338
19.2.3 Clock Synchronization 339
19.3 SB-TSI 340
19.3.1 SB-TSI Address 340
19.4 PCH 340
19.4.1 Command Summary 340
19.5 SMBUS MASTER 341
19.5.1 Block Diagram 341
19.5.2 Programming Flow 342
19.5.3 TSI Routine 343
19.5.4 PCH Routine 343
19.5.5 BYTE Ruttine 344
19.5.6 Manual Mode interface 344
19.6 REGISTER TYPE ABBREVIATIONS 345
19.6.1 Enter the Extended Function Mode 345
19.6.2 Configure the Configuration Registers 345
19.7 SMBUS MASTER REGISTER SET 346
19.7.1 SMBus Register Map 346
19.7.2 SMBus Data (SMDATA) – Bank 0 347
19.7.3 SMBus Write Data Size (SMWRSIZE) – Bank 0 347
19.7.4 SMBus Command (SMCMD) – Bank 0 347
19.7.5 SMBus INDEX (SMIDX) – Bank 0 348
19.7.6 SMBus Control (SMCTL) – Bank 0 348
19.7.7 SMBus Address (SMADDR) – Bank 0 349
19.7.8 SCL FREQ (SCLFREQ) – Bank 0 350
19.7.9 PCH Address (PCHADDR) – Bank 0 350
19.7.10 SMBus Error Status (Error_status) – Bank 0 351
19.7.11 PCH Command (PCHCMD) – Bank 0 351
19.7.12 TSI Agent Enable Register (TSI_AGENT) – Bank 352
19.7.13 SMBus Control 3 Register (SMCTL3) – Bank 0 352
19.7.14 SMBus Control 2 Register (SMCTL2) – Bank 0 353
19.7.15 BYTE ADDRESS0 (BYTE ADDR) – Bank 0 353
19.7.16 BYTE ADDRESS1 (BYTE ADDR) – Bank 0 354
19.7.17 BYTE INDEX0 (BYTE_IDX0) – Bank 0 354
19.7.18 BYTE INDEX1 (BYTE_IDX1) – Bank 0 354
19.7.19 TSI AGENT0 ADDRESS (TSI_AGENT0 ADDR) – Bank 0 355
19.7.20 SI AGENT1 ADDRESS (TSI_AGENT1 ADDR) – Bank 0 355

20. OVP & UVP DETECT 357

21. PORT80 TO UART 359

22. FADING LED 360

23. OSCILLATOR FREE 361

24. CONFIGURATION REGISTER 362

24.1 CHIP (GLOBAL) CONTROL REGISTER 362
24.2 LOGICAL DEVICE 1 385
24.3 LOGICAL DEVICE 2 387
24.4 LOGICAL DEVICE 3 389
24.5 LOGICAL DEVICE 5 392
24.6 LOGICAL DEVICE 6 394
24.7 LOGICAL DEVICE 7 395
24.8 LOGICAL DEVICE 8 401
24.9 LOGICAL DEVICE 9 409

24.10 LOGICAL DEVICE A 417
24.11 LOGICAL DEVICE B 431
24.12 LOGICAL DEVICE D 441
24.13 LOGICAL DEVICE E 446
24.14 LOGICAL DEVICE F 450
24.15 LOGICAL DEVICE 11 453
24.16 LOGICAL DEVICE 12 455
24.17 LOGICAL DEVICE 14 463
24.18 LOGICAL DEVICE 15 465
24.19 LOGICAL DEVICE 16 469

25. SPECIFICATIONS 473

25.1 ABSOLUTE MAXIMUM RATINGS 473
25.2 DC CHARACTERISTICS 473

26. AC CHARACTERISTICS 477

26.1 POWER ON / OFF TIMING 477
26.2 AC POWER FAILURE RESUME TIMING 478
26.3 CLOCK INPUT TIMING 480
26.4 PCICLK_OUT DELAY 481
26.5 PECI TIMING 481
26.6 SMBUS TIMING 483
26.7 UART/PARALLEL PORT 484
26.8 MODEM CONTROL TIMING 485
26.9 PARALLEL PORT MODE PARAMETERS 485
26.9.1 Parallel Port Timing 486
26.9.2 EPP Data or Address Read Cycle Timing Parameters 487
26.9.3 EPP Data or Address Read Cycle (EPP Version 1.9) 488
26.9.4 EPP Data or Address Read Cycle (EPP Version 1.7) 489
26.9.5 EPP Data or Address Write Cycle Timing Parameters 490
26.9.6 EPP Data or Address Write Cycle (EPP Version 1.9) 491
26.9.7 EPP Data or Address Write Cycle (EPP Version 1.7) 492
26.9.8 Parallel Port FIFO Timing Parameters 492
26.9.9 Parallel FIFO Timing 493
26.9.10 ECP Parallel Port Forward Timing Parameters 493
26.9.11 ECP Parallel Port Forward Timing 494
26.9.12 ECP Parallel Port Reverse Timing Parameters 494
26.9.13 ECP Parallel Port Reverse Timing 495
26.9.14 KBC Timing Parameters 495
26.9.15 Writing Cycle Timing 496
26.9.16 Read Cycle Timing 497
26.9.17 Send Data to K/B 497
26.9.18 Receive Data from K/B 497
26.9.19 Input Clock 498
26.9.20 Send Data to Mouse 498
26.9.21 Receive Data from Mouse 498
26.10 GPIO TIMING PARAMETERS 499
26.10.1 GPIO Write Timing 499

27. TOP MARKING SPECIFICATIONS 500

28. ORDERING INFORMATION 501

29. PACKAGE SPECIFICATION 502

30. REVISION HISTORY 503

1. GENERAL DESCRIPTION

The NCT6796D is a member of Nuvoton's Super I/O product line. The NCT6796D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures. In terms of temperature monitoring, the NCT6796D adopts the Current Mode (dual current source) and thermistor sensor approach. The NCT6796D also supports the Smart Fan control system, including "SMART FAN™ I and SMART FAN™ IV, which makes the system more stable and user-friendly.

The NCT6796D provides two high-speed serial communication port (UART), which includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem-control capability, and a processor interrupt system. The UART supports legacy speeds up to 115.2K bps as well as even higher baud rates of 230K, 460K, or 921K bps to support higher speed modems.

The NCT6796D supports the PC-compatible printer port (SPP), the bi-directional printer port (BPP), the enhanced parallel port (EPP) and the extended capabilities port (ECP). The NCT6796D supports keyboard and mouse interface which is 8042-based keyboard controller.

The NCT6796D provides flexible I/O control functions through a set of general purpose I/O (GPIO) ports. These GPIO ports may serve as simple I/O ports or may be individually configured to provide alternative functions.

The NCT6796D supports the Intel® PECI (Platform Environment Control Interface) and AMD® SB-TSI interface. The NCT6796D supports AMD® CPU power on sequence, and it also supports Intel® Deep Sleep Well glue logic to help customers to reduce the external circuits needed while using Deep Sleep Well function.

The NCT6796D supports to decode port 80 diagnostic messages on the LPC bus. This could help on system power on debugging. It also supports two-color LED control to indicate system power states. The NCT6796D supports Consumer IR function for remote control purpose. It also supports Advanced Power Saving function to further reduce the power consumption while the system is at S5 state.

The configuration registers inside the NCT6796D support mode selection, function enable and disable, and power-down selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature in Windows, making the allocation of the system resources more efficient than ever.

2. FEATURES

General

Meet LPC Specification 1.1
Meet eSPI Specification
Support LDRQ# (LPC DMA), SERIRQ (Serialized IRQ)
Integrated hardware monitor functions
Support DPM (Device Power Management), ACPI (Advanced Configuration and Power Interface)
Programmable configuration settings
Support selective pins of 5 V tolerance

UART

Two high-speed, 16550-compatible UART with 16-byte send / receive FIFO
Support RS485
--- Supports auto flow control
Fully programmable serial-interface characteristics:
--- 5, 6, 7 or 8-bit characters
--- Even, odd or no parity bit generation / detection
--- 1, 1.5 or 2 stop-bit generation
Internal diagnostic capabilities:
--- Loop-back controls for communications link fault isolation
--- Break, parity, overrun, framing error simulation
Programmable baud rate generator allows division of clock source by any value from 1 to (2^{16}-1)
Maximum baud rate for clock source 14.769 MHz is up to 921K bps. The baud rate at 24 MHz is 1.5 M bps.

Parallel Port

Compatible with IBM® parallel port
Support PS/2-compatible bi-directional parallel port
Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
Enhanced printer port back-drive current protection

Keyboard Controller

8042-based keyboard controller
Asynchronous access to two data registers and one status register
Software-compatible with 8042
Support PS/2 mouse
Support Port 92
Support both interrupt and polling modes
Fast Gate A20 and Hardware Keyboard Reset
12MHz operating frequency

Hardware Monitor Functions

Smart Fan control system
Programmable threshold temperature to speed fan fully while current temperature exceeds this threshold in the Thermal Cruise™ mode
Support Current Mode (dual current source) temperature sensing method
Fourteen voltage inputs (CPUVCORE, VIN0~9, 3VCC, AVSB, 3VSB, VTT and VBAT)
Six fan-speed monitoring inputs
Six fan-speed controls
Dual mode for fan control (PWM and DC) for SYSFANOUT
Built-in case-open and CPU socket occupied detection circuit
Programmable hysteresis and setting points for all monitored items
Issue SMI#, OVT# (Over-temperature) to activate system protection
Nuvoton Health Manager support
Provide I^2C master / slave interface to read / write registers

CIR and IR (Infrared)

Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
Support Consumer IR, including CIRRX

General Purpose I/O Ports

GPIO0 ~ GPIO8 programmable general purpose I/O ports
Two access channels, indirect (via 2E/2F or 4E/4F) and direct (Base Address) access.

ACPI Configuration

Support Glue Logic functions
Support general purpose Watch Dog Timer functions

OnNow Functions

Keyboard Wake-Up by programmable keys
Mouse Wake-Up by programmable buttons
OnNow Wake-Up from all of the ACPI sleeping states (S1-S5)

PECI Interface

Support PECI 1.1, 2.0 and 3.0 specification
Support 2 CPU addresses and 2 domains per CPU address

AMD SB-TSI Interface

Support AMD® SB-TSI specification

SMBus Interface

Support SMBus Slave interface to report Hardware Monitor device data
Support SMBus Master interface to get thermal data from PCH
Support SMBus Master interface to get thermal data from MXM module

Power Measurement

Support Power Consumption measurement
Fading LED driver control for power status and diagnostic indications

Intel Deep Sleep Well (DSW) Glue Logic

Support Deep Sleep Well (DSW) Glue Logic

Advanced Power Saving

Advanced Sleep State Control to save motherboard Stand-by power consumption

Operation voltage

3.3 voltage

Package

128-pin LQFP
Green

3. BLOCK DIAGRAM

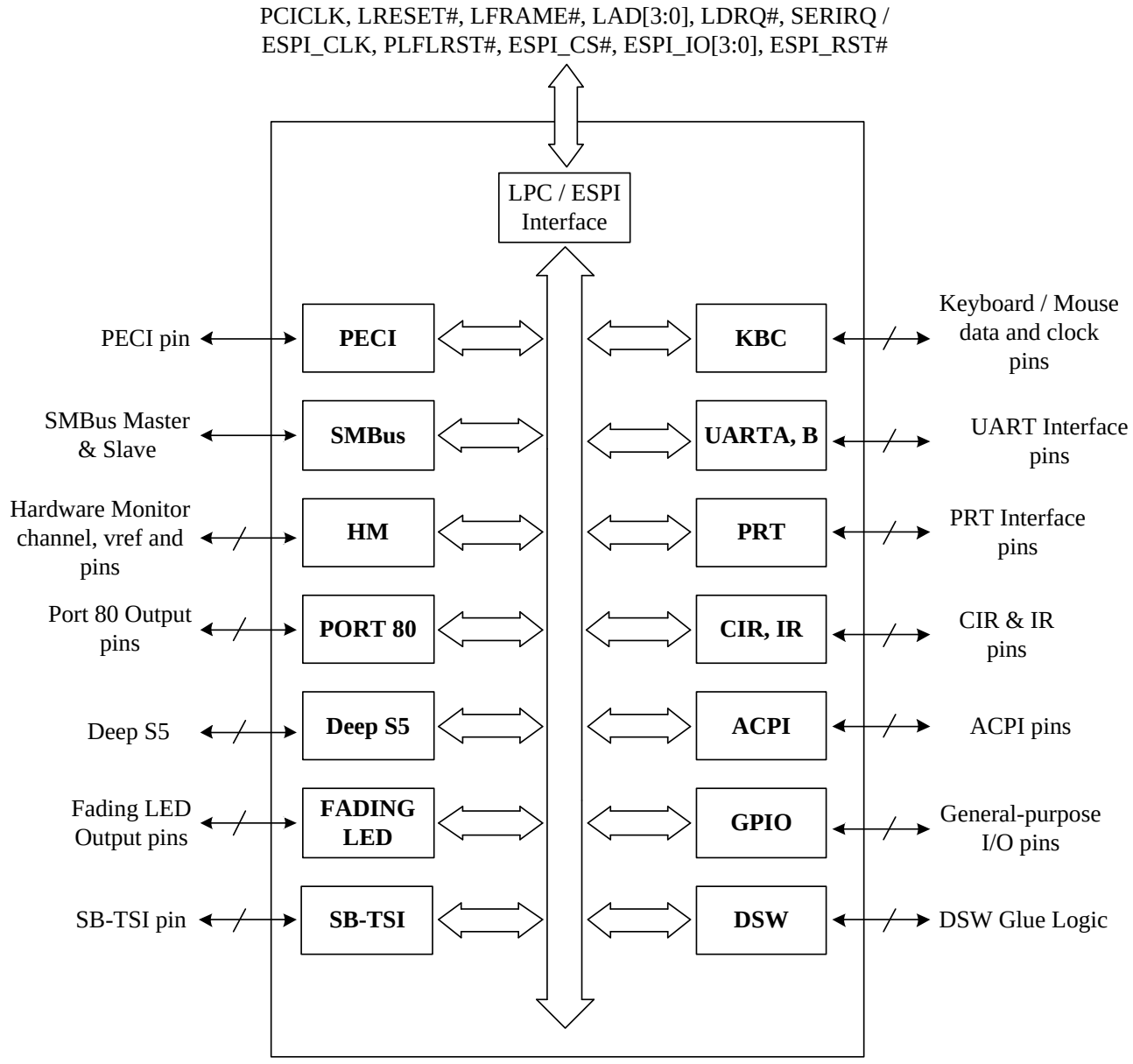


Figure 3-1 NCT6796D Block Diagram

4. PIN LAYOUT

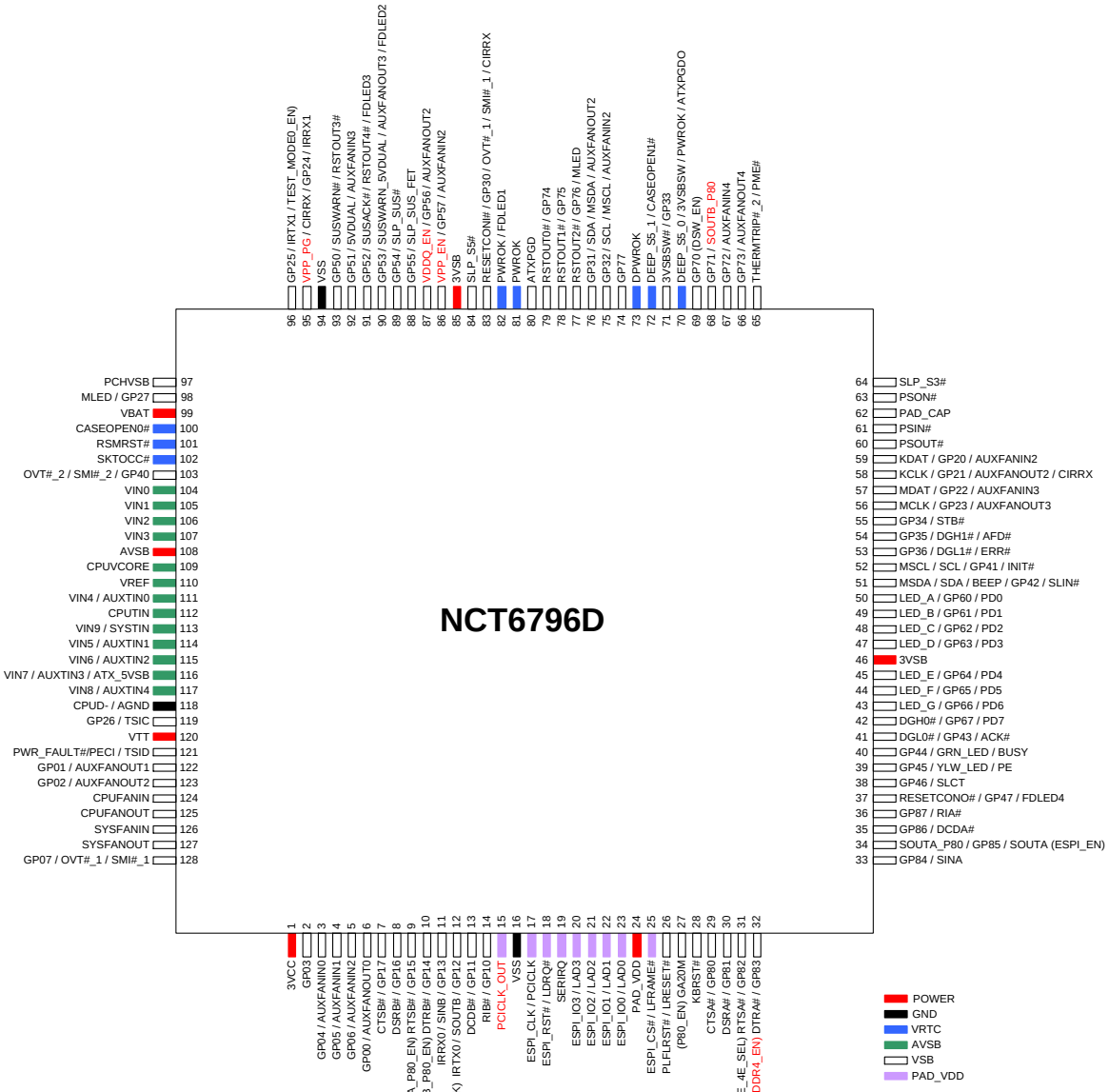


Figure 4-1 NCT6796D Pin Layout

5. PIN DESCRIPTION

Note: Please refer to 25.2 DC CHARACTERISTICS for details.

AOUT - Analog output pin
AIN - Analog input pin
IN_{tp318} - 3.3V/1.8V TTL-level input pin
IN_{sp318} - 3.3V/1.8V TTL-level, Schmitt-trigger input pin
IN_{tp3} - 3.3V TTL-level input pin
IN_{sp3} - 3.3V TTL-level, Schmitt-trigger input pin
IN_{gp3} - 3.3V GTL-level input pin
IN_{tp5} - 5V TTL-level input pin
IN_{tcup5} - 5V TTL-level, input buffer with controllable pull-up
IN_{tscup5} - 5V TTL-level, Schmitt-trigger, input buffer with controllable pull-up
IN_{tsp5} - 5V TTL-level, Schmitt-trigger input pin
IN_{tdp5} - 5V TTL-level input pin with internal pull-down resistor
O_8 - output pin with 8-mA source-sink capability
OD_8 - open-drain output pin with 8-mA sink capability
O_{12} - output pin with 12-mA source-sink capability
OD_{12} - open-drain output pin with 12-mA sink capability
O_{16} - output pin with 16-mA source-sink capability
OD_{16} - open-drain output pin with 16-mA sink capability
O_{24} - output pin with 24-mA source-sink capability
OD_{24} - open-drain output pin with 24-mA sink capability
O_{48} - output pin with 48-mA source-sink capability
OD_{48} - open-drain output pin with 48-mA sink capability
I/O_{v3} - Bi-direction pin with source capability of 6 mA and sink capability of 1 mA
I/O_{v4} - Bi-direction pin with source capability of 6 mA
O_{12cu} - output pin 12-mA source-sink capability with controllable pull-up
OD_{12cu} - open-drain 12-mA sink capability output pin with controllable pull-up
OX_8 - output pin with 8-mA source-sink capability and output voltage high level depend PAD_VDD
ODX_8 - open-drain output pin with 8-mA sink capability and output voltage high level depend PAD_VDD

5.1 LPC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
65	PME#	O	OD_{12}	VSB	Generated PME event.
17	PCICLK	I	IN_{tp318}	PAD_VDD	PCI clock input.
15	PCICLK_OUT	AOUT		PAD_VDD	PCI-clock output from pin 17 directly.
18	LDRQ#	O	OX_8	PAD_VDD	Encoded DMA Request signal.
17	SERIRQ	I/O	IN_{tp318} O_8 OD_8	PAD_VDD	Serialized IRQ input / output.
20-23	LAD[3:0]	I/O	IN_{tp318} ODX_8	PAD_VDD	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
25	LFRAME#	I	IN_{sp318}	PAD_VDD	Indicates the start of a new cycle or the termination of a broken cycle.
26	LRESET#	I	IN_{sp318}	VSB	Reset signal. It can be connected to the PCIRST# signal on the host.

5.2 ESPI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
17	ESPI_CLK	I	IN_{tp318}	PAD_VDD	The eSPI_CLK provides the reference timing for all the serial input and output operations.
18	ESPI_RST#	I	IN_{tp318}	PAD_VDD	Reset the eSPI interface for both master and slaves.
20-23	ESPI_IO[3:0]	I/O	IN_{tp318} ODX_8	PAD_VDD	These are bi-directional input/output pins used to transfer data between master and slaves.
25	ESPI_CS#	I	IN_{sp318}	PAD_VDD	Drving Chip Select# low selects a particular eSPI slave for the transaction.
26	PLTRST#	I	IN_{sp318}	VSB	Platform reset can be used to communicate through the PLATFORM reset# vw command.

5.3 Multi-Mode Parallel Port

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
38	SLCT	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer is selected. See the description of the parallel port for the definition of this pin in ECP and EPP modes.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
39	PE	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input on this pin indicates that the printer has detected the end of the paper. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
40	BUSY	I	IN_{tsp5}	VSB	PRINTER MODE: An active-high input indicates that the printer is not ready to receive data. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
41	ACK#	I	IN_{tsp5}	VSB	PRINTER MODE: ACK# An active-low input on this pin indicates that the printer has received data and is ready to accept more data. See the descriptions of the parallel port for the definition of this pin in ECP and EPP modes.
53	ERR#	I	IN_{tsp5}	VSB	PRINTER MODE: ERR# An active-low input on this pin indicates that the printer has encountered an error condition. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
51	SLIN#	O	O_{12}	VSB	PRINTER MODE: SLIN# Output line for detection of printer selection. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
52	INIT#	O	O_{12}	VSB	PRINTER MODE: INIT# Output line for the printer initialization. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
54	AFD#	O	O_{24}	VSB	PRINTER MODE: AFD# An active-low output from this pin causes the printer to auto feed a line after a line is printed. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
55	STB#	O	O_{12}	VSB	PRINTER MODE: STB# An active-low output is used to latch the parallel data into the printer. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
50	PD0	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD0 Parallel port data bus bit 0. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
49	PD1	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD1 Parallel port data bus bit 1. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
48	PD2	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD2 Parallel port data bus bit 2. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
47	PD3	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD3 Parallel port data bus bit 3. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
45	PD4	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD4 Parallel port data bus bit 4. See the description of the parallel port for the definition of this pin in ECP and EPP modes.
44	PD5	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD5 Parallel port data bus bit 5. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
43	PD6	I/O	IN_{tsp5} O_{12}	VSB	PRINTER MODE: PD6 Parallel port data bus bit 6. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.
42	PD7	I/O	IN_{tsp5} O_{24}	VSB	PRINTER MODE: PD7 Parallel port data bus bit 7. See the description of the parallel port for the definitions of this pin in ECP and EPP modes.

5.4 Serial Port Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
36	RIA#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
35	DCDA#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
34	SOUTA	O	O_{12}	VSB	UART A Serial Output. This pin is used to transmit serial data out to the communication link.
33	SINA	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
32	DTRA#	O	O_{12}	VSB	UART A Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
31	RTSA#	O	O_{12}	VSB	UART A Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
30	DSRA#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
29	CTSA#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
14	RIB#	I	IN_{tp5}	VSB	Ring Indicator. An active-low signal indicates that a ring signal is being received from the modem or the data set.
13	DCDB#	I	IN_{tp5}	VSB	Data Carrier Detection. An active-low signal indicates the modem or data set has detected a data carrier.
12	SOUTB	O	O_{12}	VSB	UART B Serial Output. This pin is used to transmit serial data out to the communication link.
11	SINB	I	IN_{tp5}	VSB	Serial Input. This pin is used to receive serial data through the communication link.
10	DTRB#	O	O_{12}	VSB	UART B Data Terminal Ready. An active-low signal informs the modem or data set that the controller is ready to communicate.
9	RTSB#	O	O_{12}	VSB	UART B Request To Send. An active-low signal informs the modem or data set that the controller is ready to send data.
8	DSRB#	I	IN_{tp5}	VSB	Data Set Ready. An active-low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
7	CTSB#	I	IN_{tp5}	VSB	Clear To Send. This is the modem-control input. The function of these pins can be tested by reading bit 4 of the handshake status register.

5.5 KBC Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
27	GA20M	O	O_{12} OD_{12}	VSB	Gate A20 output. This pin is high after system reset. (KBC P21)
28	KBRST#	O	O_{12} OD_{12}	VSB	Keyboard reset. This pin is high after system reset. (KBC P20)
58	KCLK	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Clock. Pull up is recommended if useless.
59	KDAT	I/O	IN_{tsp5} OD_{12}	VSB	Keyboard Data. Pull up is recommended if useless.
56	MCLK	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Clock. Pull up is recommended if useless.
57	MDAT	I/O	IN_{tsp5} OD_{12}	VSB	PS2 Mouse Data. Pull up is recommended if useless.

5.6 CIR Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
56	CIRRX	I	IN_{tsp5}	VSB	CIR input for long length
83	CIRRX	I	IN_{tp5}	VSB	CIR input for long length
95	CIRRX	I	IN_{tsp5}	VSB	CIR input for long length

5.7 Hardware Monitor Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
102	SKTOCC#	I	IN_{tp5}	VRTC	CPU socket occupied detection
100	CASEOPEN0#	I	IN_{tp5}	VRTC	CASE OPEN 0 detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the system is in G3 state. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
72	CASEOPEN1#	I	IN_{tp5}	VRTC	CASE OPEN 1 detection. An active-low input from an external device when the case is open. This signal can be latched if pin VBAT is connected to the battery, even if the system is in G3 state. Pulling up a 2-MΩ resistor to VBAT is recommended if not in use.
116	ATX_5VSB	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
113	VIN9	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
117	VIN8	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
116	VIN7	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
115	VIN6	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
114	VIN5	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
111	VIN4	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
107	VIN3	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
106	VIN2	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
105	VIN1	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
104	VIN0	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
109	CPUVCORE	I	AIN	AVSB	Analog input for voltage measurement (Range: 0 to 2.048 V)
110	VREF	O	AOUT	AVSB	Reference Voltage (around 2.048 V).
117	AUXTIN4	I	AIN	AVSB	The input of temperature sensor 7.
116	AUXTIN3	I	AIN	AVSB	The input of temperature sensor 6.
115	AUXTIN2	I	AIN	AVSB	The input of temperature sensor 5. It is used for AUX2 temperature sensing.
114	AUXTIN1	I	AIN	AVSB	The input of temperature sensor 4. It is used for AUX1 temperature sensing.
111	AUXTIN0	I	AIN	AVSB	The input of temperature sensor 3. It is used for AUX0 temperature sensing.
112	CPUTIN	I	AIN	AVSB	The input of temperature sensor 2. It is used for CPU temperature sensing.
113	SYSTIN	I	AIN	AVSB	The input of temperature sensor 1. It is used for system temperature sensing.
128	OVT#_1	O	OD_{12}	VSB	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
	SMI#_1	O	OD_{12}	VSB	System Management Interrupt channel output.
83	OVT#_1	O	OD_{12}	VSB	The output of over temperature Shutdown. This pin indicates the temperature is over the temperature limit. (Default after LRESET#)
	SMI#_1	O	OD_{12}	VSB	System Management Interrupt channel output.
3	AUXFANIN0	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
4	AUXFANIN1	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
5	AUXFANIN2	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
86	AUXFANIN2	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
59	AUXFANIN2	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
75	AUXFANIN2	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
92	AUXFANIN3	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
57	AUXFANIN3	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
67	AUXFANIN4	I	IN_{tp5}	VSB	0 to +5 V amplitude fan tachometer input.
6	AUXFANOUT0	O	O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
122	AUXFANOUT1	O	O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
123	AUXFANOUT2	O	O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
87	AUXFANOUT2	O	O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
58	AUXFANOUT2	O	O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
76	AUXFANOUT2	O	O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
90	AUXFANOUT3	O	O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
56	AUXFANOUT3	O	O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
66	AUXFANOUT4	O	O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
124	CPUFANIN	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
125	CPUFANOUT	O	O_{12} OD_{12}	VSB	PWM duty-cycle signal for fan speed control.
126	SYSFANIN	I	IN_{tsp5}	VSB	0 to +5 V amplitude fan tachometer input.
127	SYSFANOUT	O	O_{12} OD_{12} AOUT	VSB	PWM duty-cycle signal for fan speed control. DC voltage output for fan speed control.
51	BEEP	O	OD_{12}	VSB	Beep function for hardware monitor.

5.8 Intel® PECI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
121	PECI	I/O	I/O_{V3}	VTT	INTEL® CPU PECI interface. Connect to CPU.

5.9 Advanced Configuration & Power Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
61	PSIN#	I	IN_{tp5}	VSB	Panel Switch Input. This pin is active-low with an internal pulled-up resistor.
60	PSOUT#	O	OD_{12}	VSB	Panel Switch Output. This signal is used to wake-up the system from S3/S5 state.
101	RSMRST#	O	OD_{8}	VRTC	Resume reset signal output.
73	DPWROK	O	OD_{8}	VRTC	V3A signal output
64	SLP_S3#	I	IN_{tp318}	VSB	SLP_S3# input.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
84	SLP_S5#	I	IN_{tp318}	VSB	SLP_S5# input.
80	ATXPGD	I	IN_{tp5}	VSB	ATX power good signal.
70	ATXPGDO	O	OD_{24}	VRTC	ATX power good signal output.
63	PSON#	O	OD_{12}	VSB	Power supply on-off output.
82	PWROK	O	O_8 OD_8	VRTC	3VCC PWROK signal.
81	PWROK	O	O_8 OD_8	VRTC	3VCC PWROK signal.
70	PWROK	O	OD_{24}	VRTC	3VCC PWROK signal.
66	PWROK	O	OD_{12}	VSB	3VCC PWROK signal.
88	PWROK#	O	OD_{12}	VSB	3VCC PWROK# signal.
83	RESETCONI#	I	IN_{tp5}	VSB	Connect to the reset button. This pin has internal de-bounce circuit whose de-bounce time is at least 16 mS.
37	RESETCONO#	O	OD_{12}	VSB	RESETCONO# output.
70	3VSBSW	O	OD_{24}	VRTC	Switch 3VSB power to memory when in S3 state.
71	3VSBSW#	O	OD_{24}	VSB	Switch 3VSB power to memory when in S3 state.
66	3VSBSW#	O	OD_{12}	VSB	Switch 3VSB power to memory when in S3 state.
79	RSTOUT0#	O	O_{16} OD_{16}	VSB	PCI Reset Buffer 0. (from pin LRESET#) This pin default is push-pull output and could be programmed to open-drain output by register Logic Device D, CRE7 bit4.
78	RSTOUT1#	O	O_{16} OD_{16}	VSB	PCI Reset Buffer 1. (from pin LRESET#) This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit6.
77	RSTOUT2#	O	O_{16} OD_{16}	VSB	PCI Reset Buffer 2. (from pin LRESET#) This pin default is push-pull output and could be programmed to open-drain output by register Logic Device A, CRF7 bit7.
93	RSTOUT3#	O	O_{12}	VSB	PCI Reset Buffer 3. (from pin LRESET#) This pin is push-pull output.
91	RSTOUT4#	O	O_{12}	VSB	PCI Reset Buffer 4. (from pin LRESET#) This pin is push-pull output.

5.10 Advanced Sleep State Control Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
70	DEEP_S5_0	O	OD_{24}	VRTC	This pin is to control system power for entering “more power saving mode”.
72	DEEP_S5_1	O	OD_{12}	VRTC	This pin is to control system power for entering “more power saving mode”.

5.11 Port 80 Message Display & LED Control

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
42	DGH0#	O	O_{24}	VSB	Common cathode output of high nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
41	DGL0#	O	O_{24}	VSB	Common cathode output of low nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
54	DGH1#	O	O_{24}	VSB	Common cathode output of high nibble display on decoded Port 0x80h message. Switching frequency is about 4 KHz.
53	DGL1#	O	O_{24}	VSB	Common cathode output of low nibble display on decoded Port 0x81h message. Switching frequency is about 4 KHz.
50 49 48 47 45 44 43	LED_A LED_B LED_C LED_D LED_E LED_F LED_G	O	O_{12}	VSB	Anode outputs for 7-Segment LED.
34	SOUTA_P80	O	O_{12}	VSB	Serial PORT80 output.
68	SOUTB_P80	O	O_{12}	VSB	Serial PORT80 output.
39	YLW_LED	O	OD_{12}	VSB	Yellow LED output control. This pin could indicate the power status.
40	GRN_LED	O	OD_{12}	VSB	Green LED output control. This pin could indicate the power status.
98	MLED	O	OD_{12}	VSB	Power LED output.

5.12 SMBus Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
75	SCL	I/O	IN_{sp318} OD_{12}	VSB	SMBus slave clock.
76	SDA	I/O	IN_{sp318} OD_{12}	VSB	SMBus slave bi-directional Data.

52	SCL	I/O	IN_{sp318} OD_{12}	VSB	SMBus slave clock.
51	SDA	I/O	IN_{sp318} OD_{12}	VSB	SMBus slave bi-directional Data.
75	MSCL	I/O	IN_{sp318} OD_{12}	VSB	SMBus master clock.
76	MSDA	I/O	IN_{sp318} OD_{12}	VSB	SMBus master bi-directional Data.
52	MSCL	I/O	IN_{sp318} OD_{12}	VSB	SMBus master clock.
51	MSDA	I/O	IN_{sp318} OD_{12}	VSB	SMBus master bi-directional Data.

5.13 Power Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
46, 85	3VSB	I			+3.3 V stand-by power supply for the digital circuits.
99	VBAT	I			+3 V on-board battery for the digital circuits.
1	3VCC	I			+3.3 V power supply for driving 3 V on host interface.
24	PAD_VDD	I			+3.3 V / +1.8 V power supply for the LPC interface.
108	AVSB	I			Analog +3.3 V power input. Internally supply power to all analog circuits.
118	CPUD- / AGND	I			Analog ground. The ground reference for all analog input. Internally connected to all analog circuits. This pin should be connected to ground.
16, 94	VSS	I			Ground.
120	VTT	I			INTEL® CPU VTT power.
62	PAD_CAP	O			External Filter Capacitor 1 ~ 4.7uF (for internal VSB 1.8V)

5.14 AMD SB-TSI Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
119	TSIC	O	OD_{12}	VSB	AMD SB-TSI clock output.
121	TSID	I/O	IN_{sp3} OD_{12}	VSB	AMD SB-TSI data input / output.

5.15 DSW

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
89	SLP_SUS#	I	IN_{tp5}	VSB	This pin connects to SLP_SUS# in CPT PCH
90	SUS_WARN_5VDUAL	O	OD_{12}	VSB	This pin links to external 5VDUAL control circuits
91	SUSACK#	O	OD_{12}	VSB	This pin connects to SUSACK# in CPT PCH
92	5VDUAL	I	AIN	VSB	Analog input to monitor 5VDUAL voltage
93	SUSWARN#	I	IN_{tp5}	VSB	This pin connects to SUSWARN# in CPT PCH
88	SLP_SUS_FET	O	OD_{12}	VSB	This pin connects to VSB power switch
97	PCHVSB	I	AIN	VSB	PCHVSB function

5.16 IR

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
11	IRRX0	I	IN_{tp5}	VSB	IR Receiver input.
12	IRTX0	O	O_{12}	VSB	IR Transmitter output.
95	IRRX1	I	IN_{tsp5}	VSB	IR Receiver input.
96	IRTX1	O	O_{12}	VSB	IR Transmitter output.

5.17 Memory OK

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
77	GP77	I	IN_{tp5}	VSB	Memory OK input.

5.18 Intel Power Fault

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
119	PWR_FAULT#	O	OD_{12}	VSB	Intel Power Fault output.

5.19 DDR4 Power Sequence

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
95	VPP_PG	I	IN_{tp5}	VSB	DDR4 VPP power on sequence ok signal
86	VPP_EN	O	OD_{12}	VSB	VPP Power Enable
87	VDDQ_EN	O	OD_{12}	VSB	VDDQ Power Enable

5.20 General Purpose I/O Port

5.20.1 GPIO-0 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
6	GP00	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 0.
122	GP01	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 1.
123	GP02	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 2.
2	GP03	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 3.
3	GP04	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 4.
4	GP05	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 5.
5	GP06	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 6.
6	GP07	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 0 bit 7.

5.20.2 GPIO-1 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
14	GP10	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 0.
13	GP11	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 1.
12	GP12	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 2.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
11	GP13	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 3.
10	GP14	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 4.
9	GP15	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 5.
8	GP16	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 6.
7	GP17	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 1 bit 7.

5.20.3 GPIO-2 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
59	GP20	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 0.
58	GP21	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 1.
57	GP22	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 2.
56	GP23	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 3.
95	GP24	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 4.
96	GP25	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 5.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
119	GP26	I/O	IN_{tp3} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 6.
98	GP27	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 2 bit 7.

5.20.4 GPIO-3 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
83	GP30	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 0.
76	GP31	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 1.
75	GP32	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 2.
71	GP33	I/O	IN_{tp5} O_{24} OD_{24}	VSB	General-purpose I/O port 3 bit 3.
55	GP34	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 3 bit 4.
54	GP35	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 3 bit 5.
53	GP36	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 3 bit 6.

5.20.5 GPIO-4 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
103	GP40	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 0.
52	GP41	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 1.
51	GP42	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 2.
41	GP43	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 4 bit 3.
40	GP44	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 4.
39	GP45	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 5.
38	GP46	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 6.
37	GP47	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 4 bit 7.

5.20.6 GPIO-5 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
93	GP50	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 0.
92	GP51	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 1.
91	GP52	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 2.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
90	GP53	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 3.
89	GP54	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 4.
88	GP55	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 5.
87	GP56	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 6.
86	GP57	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 5 bit 7.

5.20.7 GPIO-6 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
50	GP60	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 0.
49	GP61	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 1.
48	GP62	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 2.
47	GP63	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 3.
45	GP64	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 4.
44	GP65	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 5.

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
43	GP66	I/O	IN_{tsp5} O_{12} OD_{12}	VSB	General-purpose I/O port 6 bit 6.
42	GP67	I/O	IN_{tsp5} O_{24} OD_{24}	VSB	General-purpose I/O port 6 bit 7.

5.20.8 GPIO-7 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
69	GP70	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 0.
68	GP71	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 1.
67	GP72	I/O	IN_{tp3} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 2.
66	GP73	I/O	IN_{tp3} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 3.
79	GP74	I/O	IN_{tp5} O_{16} OD_{16}	VSB	General-purpose I/O port 7 bit 4.
78	GP75	I/O	IN_{tp5} O_{16} OD_{16}	VSB	General-purpose I/O port 7 bit 5.
77	GP76	I/O	IN_{tp5} O_{16} OD_{16}	VSB	General-purpose I/O port 7 bit 6.
74	GP77	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 7 bit 7.

5.20.9 GPIO-8 Interface

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
29	GP80	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 0.
30	GP81	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 1.
31	GP82	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 2.
32	GP83	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 3.
33	GP84	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 4.
34	GP85	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 5.
35	GP86	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 6.
36	GP87	I/O	IN_{tp5} O_{12} OD_{12}	VSB	General-purpose I/O port 8 bit 7.

5.21 Strapping Pins

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
31	2E_4E_SEL	I	IN_{tdp5}	VSB	SIO I/O address selection. (Strapped by LRESET#) Strapped to high: SIO I/O address is 4Eh/4Fh. Strapped to low: SIO I/O address is 2Eh/2Fh.
32	DDR4_EN	I	IN_{tdp5}	VSB	Enable DDR4PWR function. (Strapped by **VSB** power: internal RSMRST# signal.) Strapped to high: Enable DDR4PWR functiion Strapped to low: Disable DDR4PWR function

PIN	SYMBOL	I/O	BUFFER TYPE	POWER WELL	DESCRIPTION
34	ESPI_EN	I	IN_{tdp5}	VSB	Host interface function selection. (Strapped by **VSB** power: internal RSMRST# signal.) Strapped to high: eSPI interface Strapped to low: LPC interface
9	UARTA_P80_EN	I	IN_{tdp5}	VSB	Serial PORT80(SOUTA_P80) function selection. (Strapped by LRESET#) See configuration register
10	UARTB_P80_EN	I	IN_{tdp5}	VSB	Serial PORT80(SOUTB_P80) function selection. (Strapped by LRESET#) See configuration register
12	Entry_Key_SEL	I	IN_{tp5}	VSB	Input clock rate selection (Strapped by VCC [internal Power OK signal without any delay]) Strapped to high: The Entry Key is 88. Strapped to low: The Entry Key is 87.
69	DSW_EN	I	IN_{tp5}	VSB	DSW position selection. (Strapped by **VSB** power: internal RSMRST# signal]) Strapped to high: DSW function Strapped to low: GPIO function
96	TEST_MODE0_EN	I	IN_{tdp5}	VSB	Test mode0 function selection. (Strapped by **VSB** power: internal RSMRST# signal]) Recommand pull-down
27	P80_EN	I	IN_{tdp5}	VSB	Port80 function selection. (Strapped by **VCC**: internal Power OK signal without any delay.) Strapped to high: Port80 function. Strapped to low: non-Port80 function

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

1) VSB Strapping result can be programming by LPC, and reset by RSMRST#.
2) VCC Strapping result can be programming by LPC, and reset by PWROK.
3) LRESET# strapping (2E_4E_SEL) can be programming by LPC, and reset by LRESET#.

5.22 Internal pull-up, pull-down pins

Signal	Pin(s)	Power well	Type	Resistor	Note
Strapping Pins					

Signal	Pin(s)	Power well	Type	Resistor	Note
2E_4E_SEL	31	3VSB	Pull-down	47.4K	1
P80_EN	27	3VSB	Pull-down	47.4K	1
UARTA_P80_EN	9	3VSB	Pull-down	47.4K	1
UARTB_P80_EN	10	3VSB	Pull-down	47.4K	1
Entry_Key_SEL	12	3VSB	Pull-down	47.4K	1
TEST_MODE0_EN	96	3VSB	Pull-down	47.4K	2
DDR4_EN	32	3VSB	Pull-down	47.4K	2
ESPI_EN	34	3VSB	Pull-down	47.4K	2
Advanced Configuration & Power Interface					
PSIN#	61	3VSB	Pull-up	47.03K	

Note1. Active only during VCC Power-up reset
Note2. Active only during VSB Power-up reset

5.23 Strapping and multi function pin control

DSW_EN

Pin88 function selection

DSW_EN	LD12 CRED [Bit0]	LDB CRE6 [Bit3]	Pin88
1	0	x	SLP_SUS_FET
1	1	0	GP55
0	0	0	GP55
0	1	1	GP55

Pin89 function selection

DSW_EN	LD12 CRED [Bit1]	Pin89
0	x	GP54
1	0	SLP_SUS#
1	1	GP54

Pin90 function selection

DSW_EN	LD12 CRED [Bit2]	CR2A [Bit3]	Pin90
1	0	0	SUSWARN_5VDUAL
1	0	1	FDLED2
1	1	0	GP53
1	1	1	AUXFANOUT3
0	0	x	FDLED2
0	1	0	GP53
0	1	1	AUXFANOUT3

Pin91 function selection

DSW_EN	LD12 CRED [Bit3]	LDB CRE6 [Bit1]	Pin91
1	0	0	SUSACK#
1	0	1	FDLED3
1	1	0	GP52
1	1	1	RSTOUT4
0	0	x	FDLED3
0	1	0	GP52
0	1	1	RSTOUT4#

Pin92 function selection

DSW_EN	LD12 CRED [Bit4]	CR2A [Bit4]	Pin92
1	0	x	5VDUAL
1	1	0	GP51
1	1	1	AUXFANIN3
0	x	0	GP51
0	x	1	AUXFANIN3

Pin93 function selection

LDE CRFA [Bit1]	DSW_EN	LD12 CRED [Bit5]	LDD CRE1 [Bit0]	LDB CRE6 [Bit2]	Pin93
1	x	x	x	x	VW_SUSWARN#
0	1	0	x	x	SUSWARN#
0	1	1	x	0	GP50
0	1	1	x	1	RSTOUT3#
0	0	x	1	x	RESERVE
0	0	x	0	0	GP50
0	0	x	0	1	RSTOUT3#

6. GLUE LOGIC

6.1 ACPI Glue Logic

Table 6-1 Pin Description

SYMBOL	PIN	DESCRIPTION
SLP_S5#	84	SLP_S5# input.
RESETCONI#	83	RESETCONI# input signal. This pin has internal de-bounce circuit whose de-bounce time is at least 16 mS.
RESETCONO#	37	RESETCONO# output signal.
PWROK	82	This pin generates the PWROK signals while 3VCC is present.
DPWROK	73	This pin generates the DPWROK signals while 3VSB is present.
ATXPGD	80	ATX power good input signal. It is connected to the PWROK signal from the power supply for PWROK/PWRGD generation. The default is enabled.
RSMRST#	101	The RSMRST# signal is a reset output and is used as the VSB power on reset signal for the South Bridge. When the NCT6796D detects the 3VSB voltage rises to "V1", it then starts a delay – "t1" before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below "V2", the RSMRST# de-asserts immediately.

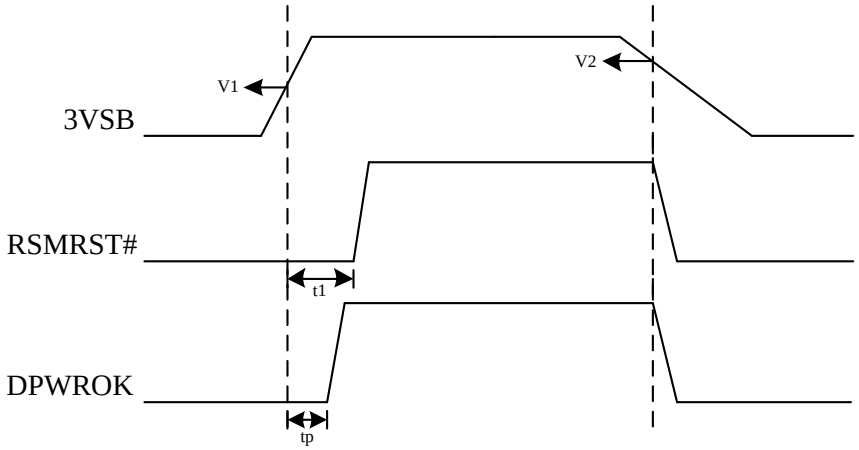


Figure 6-1 RSMRST# and DPWROK

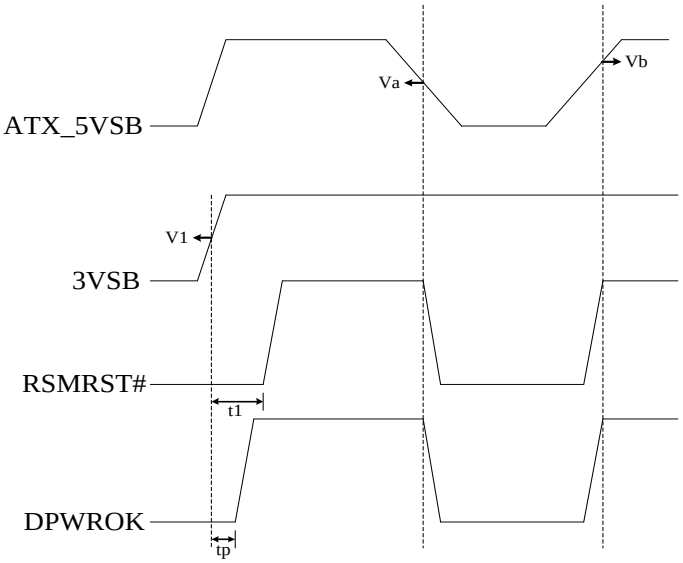


Figure 6-2 RSMRST# and DPWROK (Enable ATX_5VSB detect)

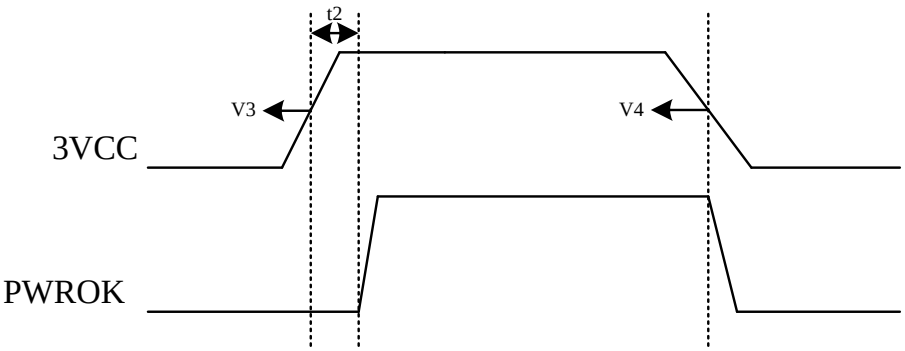


Figure 6-3 PWROK

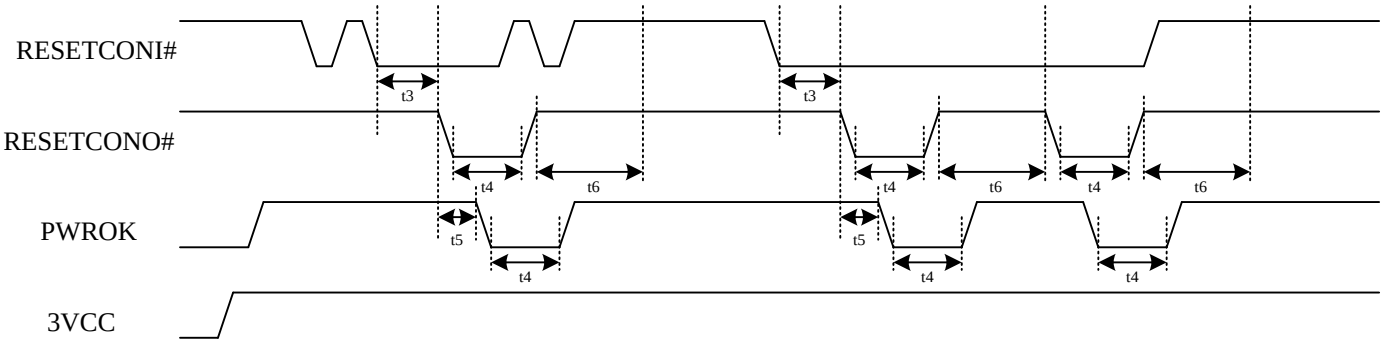


Figure 6-4 RESETCONI# and PWROK

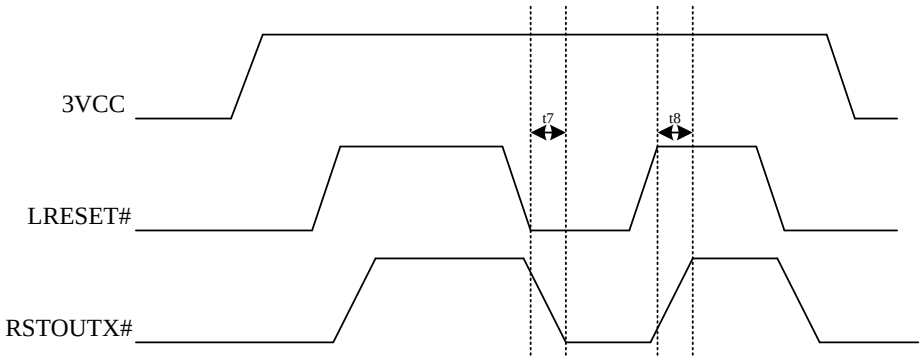


Figure 6-5 RSTOUTX# and LRESET#

TIMING	PARAMETER	MIN	MAX	UNIT
t1	Valid 3VSB to RSMRST# inactive	200	300	mS
tp	Valid 3VSB to DPWROK inactive	10	30	mS
t2	Valid 3VCC to PWROK active	50	500	mS
t3	RESETCONI# de-bounce	1	5	nS
t4	RESETCONO# and PWROK active	See LDB CRFA		
t5	RESETCONO# active to PWROK active	0	80	nS
t6	RESETCONO# inactive to RESETCONI# detect	3	4	S
t7	LRESET# active to RSTOUTX# active	0	80	nS
t8	LRESET# inactive to RSTOUTX# inactive	0	80	nS

DC	PARAMETER	MIN	MAX	UNIT
V1	3VSB Valid Voltage		3.1	Volt
V2	3VSB Ineffective Voltage	2.92		Volt
V3	3VCC Valid Voltage	-	2.83	Volt
V4	3VCC Ineffective Voltage	2.68	-	Volt
Va	ATX_5VSB Ineffective Voltage	1.25	1.3	Volt
Vb	ATX_5VSB Valid Voltage	1.37	1.41	Volt

Note： 1. The values above are the worst-case results of R&D simulation.

6.2 3VSBSW#

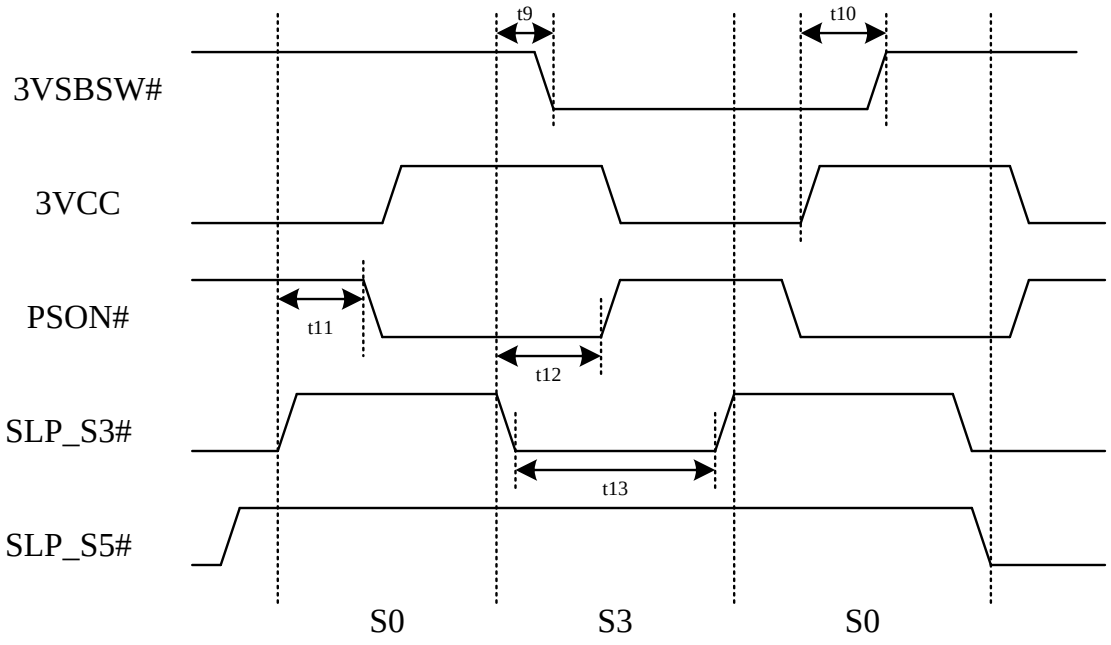


Figure 6-7 3VSBSW#

TIMING	PARAMETER	MIN	MAX	UNIT
t9	SLP_S3# active to 3VSBSW# active	0	10	mS
t10	3VCC active to 3VSBSW# inactive	120	190	mS
t11	SLP_S3# inactive to PSON# active	0	200	nS
t12	SLP_S3# active to PSON# inactive	15	45	mS
t13	SLP_S3# minimal Low Time	40	-	mS

6.3 PSON# Block Diagram

The PSON# function controls the main power on/off. The main power is turned on when PSON# is low. Please refer to the figure below.

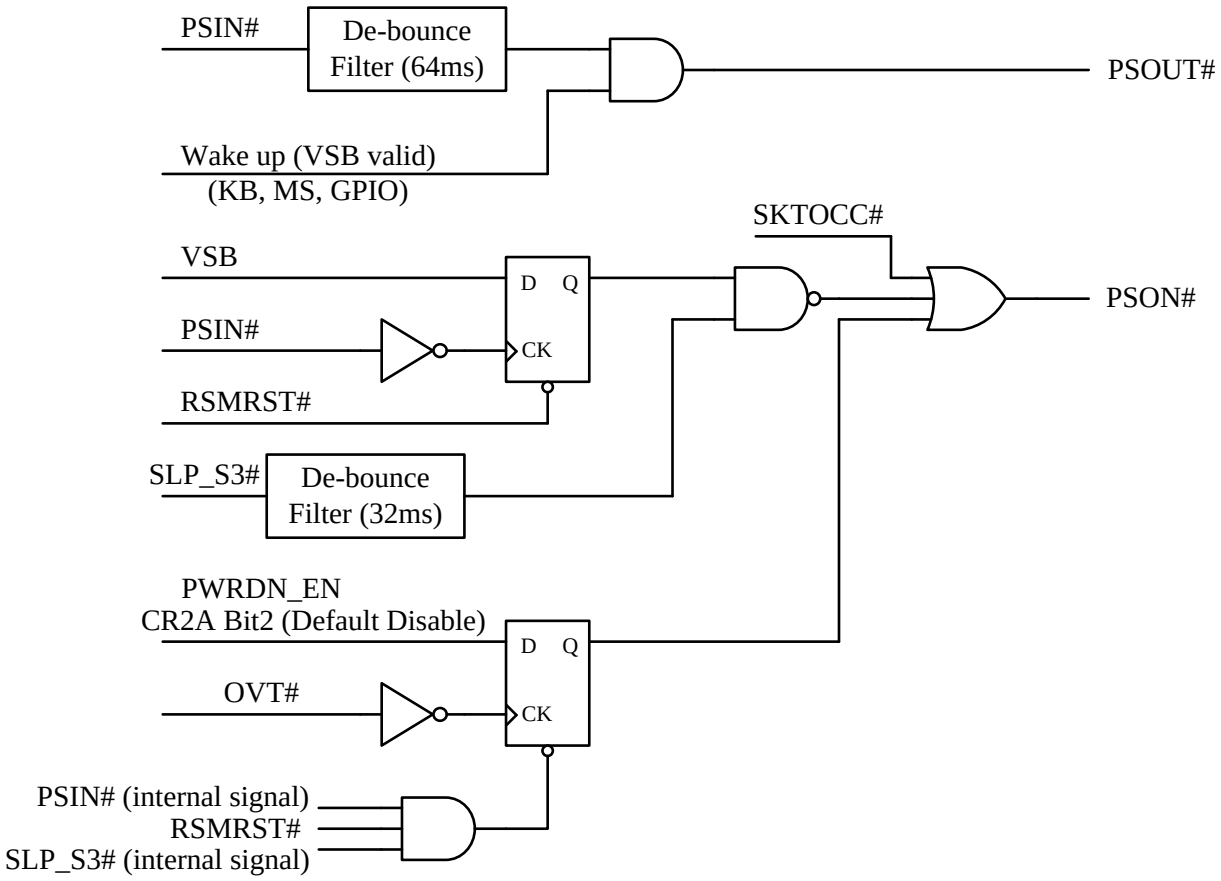


Figure 6-8 PSON# Block Diagram

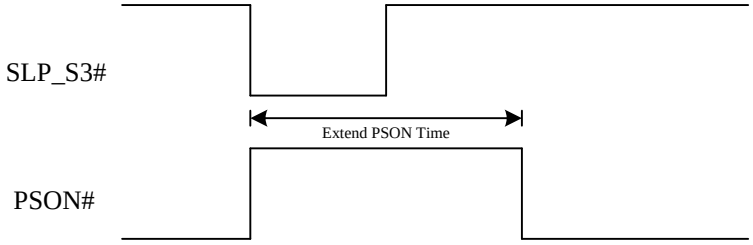
6.4 Extend PSON# after power off

When system goes form S0 state to S3/S5 state (ie. SLPS3# from high to low), PSON# is de-asserted (ie. From low to high). Then if SLPS3# goes back to high immediately, less than a certain period of time (LD12, CREA bit[1:0]), the PSON# signal should be kept high for above-mentioned duration.

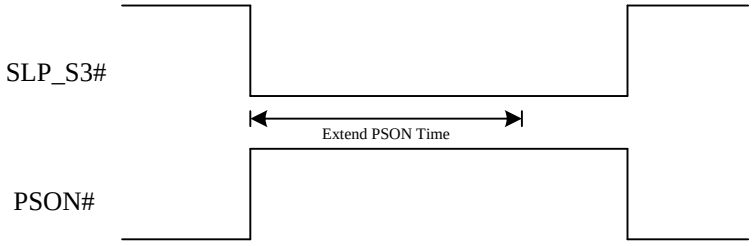
If SLPS3# stays at high longer than the certain period of time, PSON# follows state of SLPS3# again after said duration.

This certain period of time could be set to Disable 2/3/4 seconds. (Disable = 0 seonds).

Condition1 :

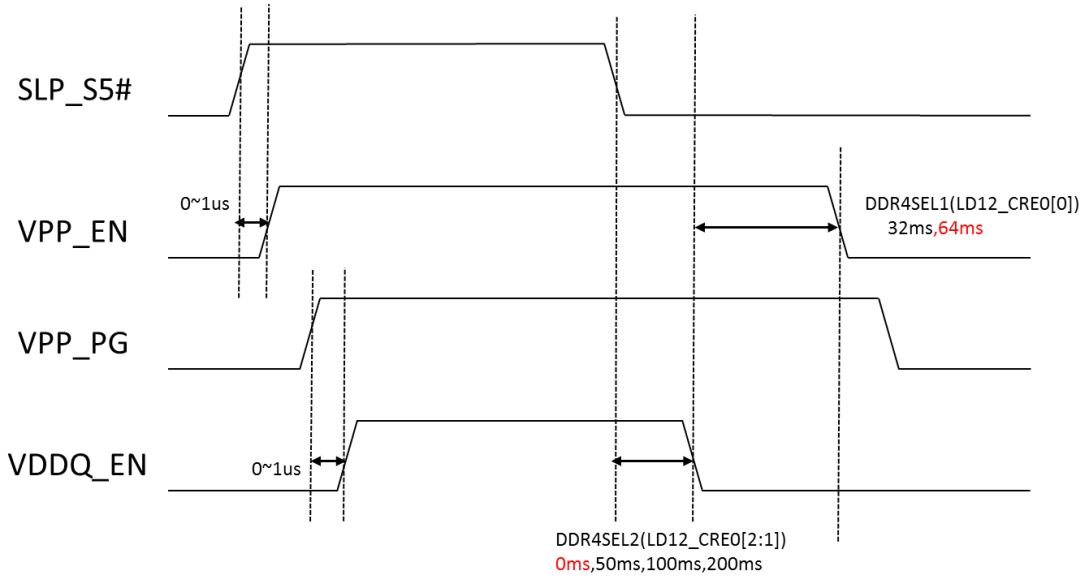


Condition2 :



6.5 DDR4PWR

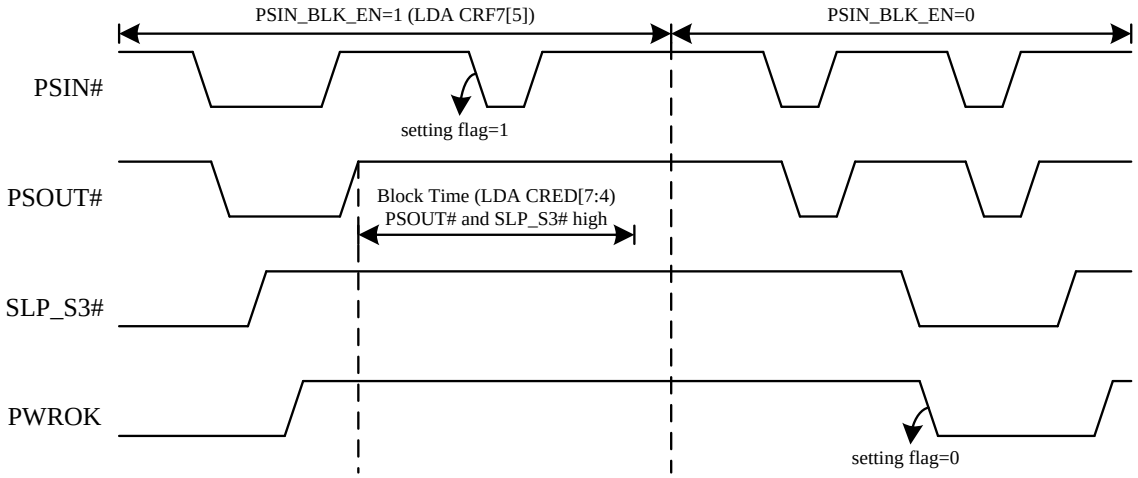
DDR4PWR is the power sequence control of DDR4 SDRAM. It is a high speed and low power platform. There are two timer register can be select in the sequence (DDR4SEL1: LD12 CRE0 bit[0], DDR4SEL2: LD12 CRE0 bit [2:1]).



6.6 PSIN#

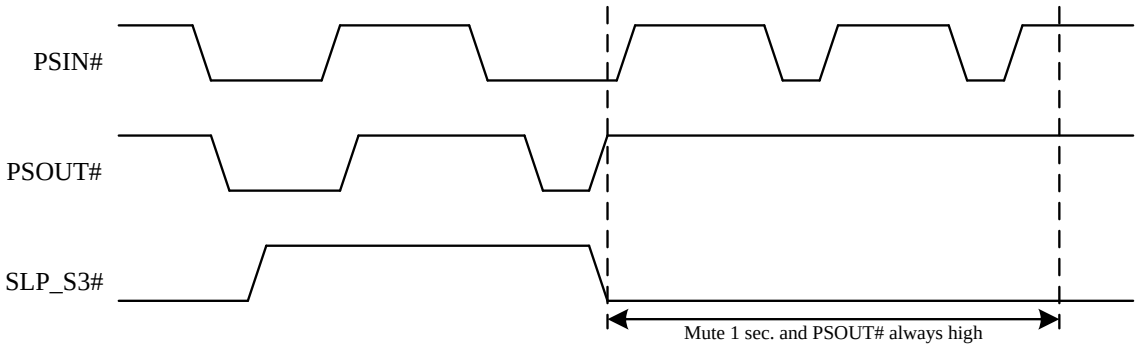
6.6.1 PSIN# Block Diagram (S5 -> S0)

When system is at S5 to S0 state, we add block time to avoid system enter S5 again by PSIN# glitch. The block time can be set by LDA CRED bit[7:4] and the default is 0.5sec. If the glitch happen in the block time, the flag (LDA CREC bit[2]) will set high and can be observe when user enter S0 state. The function need to set enable bit (LDA CRF7 bit[5]: PSIN_BLK_EN).



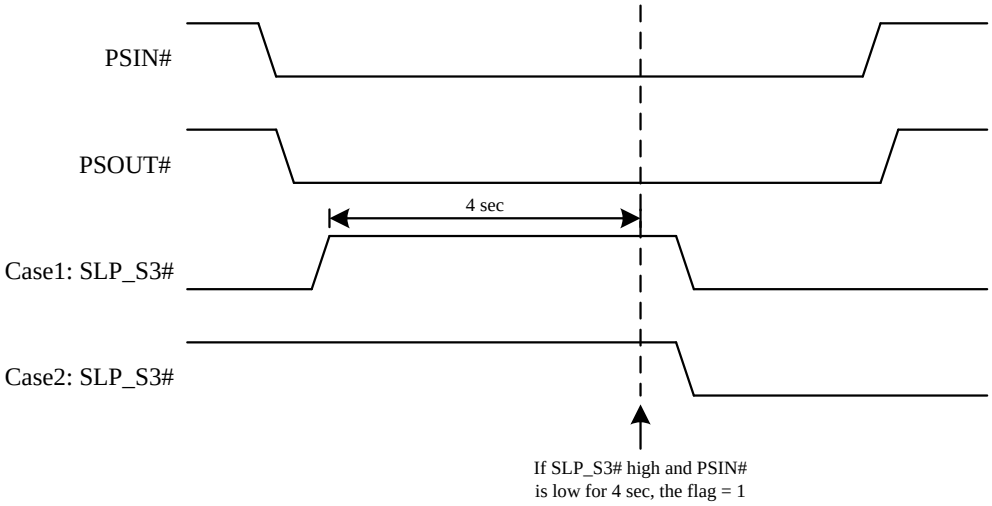
6.6.2 PSIN# Block 1sec Diagram (S0 -> S5)

When system is at S0 to S5 state, we add block 1 sec to avoid system enter S0 again by PSIN# glitch. The block time is fix and can't be set. The function need to set enable bit (LDA CRF7 bit[5]: PSIN_BLK_EN).

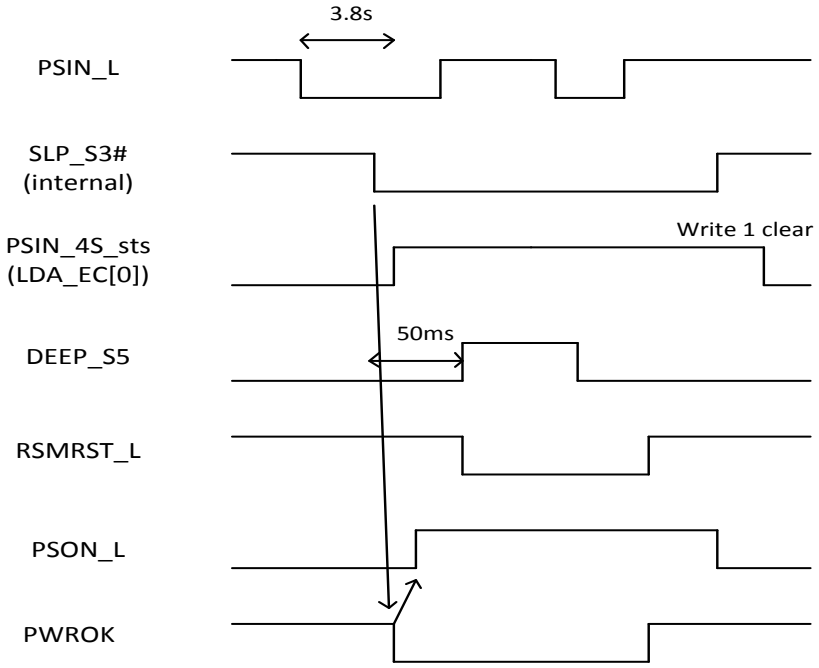


6.6.3 PSIN# 4sec Status Diagram

When user push PSIN button sustainably more than 4 sec and LD11_CRE0[2] =0, the system will enter S5 state and we have a flag to monitor (LDA CREC bit[0]).

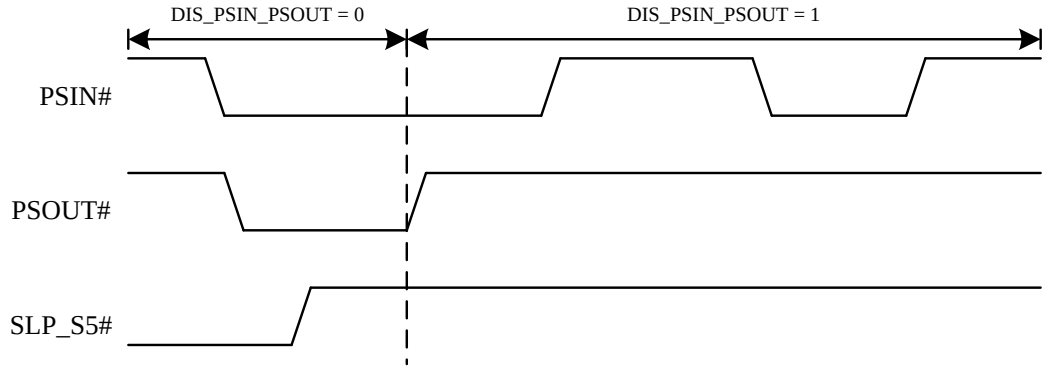


When user push PSIN button sustainably more than 3.8 sec and LD11_CRE0[2] =1, the system will enter DeepS5 state and we have a flag to monitor (LDA CREC bit[0]).



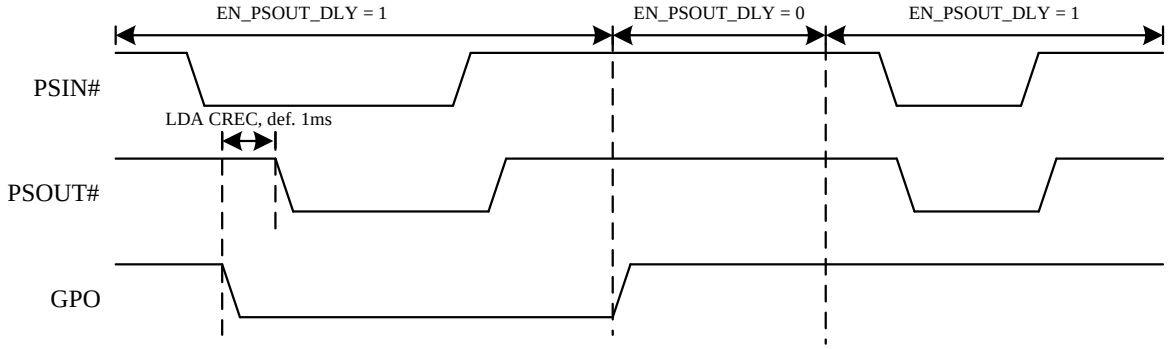
6.6.4 Disable PSIN# to PSOUT# Diagram

When system enter S0 from S5, user can monitor PSIN status by register (LDA CREC bit[7]) for several application. For example, user can set DIS_PSIN_PSOUT (LDA CREC bit[1]) to disconnect PSIN and PSOUT. If DIS_PSIN_PSOUT = 1, PSOUT will not follow PSIN. To avoid BIOS not clear this bit abnormally, it can be cleared automatically by PSIN rising signal to set LDA CREC bit[3] = 1.



6.6.5 Enable PSOUT# Delay Diagram

Normally, PSOUT follows PSIN. For particular case, we can add PSOUT delay from PSIN when system enters S0 state. The delay time can be set by LDA CREC bit[6:5], and need to enable by LDA CREC bit [4] (EN_PSOUT_DLY). As system enter S0 state, the enable bit need to clear to release GP73 bus, otherwise, GP73 will keep low. When system enter S5 state from S0, the function will not work even we set the enable bit.



6.7 PWROK

PWROK Signal indicates the main power (VCC Power) is valid. Besides, valid PWROK signal also requires the following conditions, as shown in the figure below.

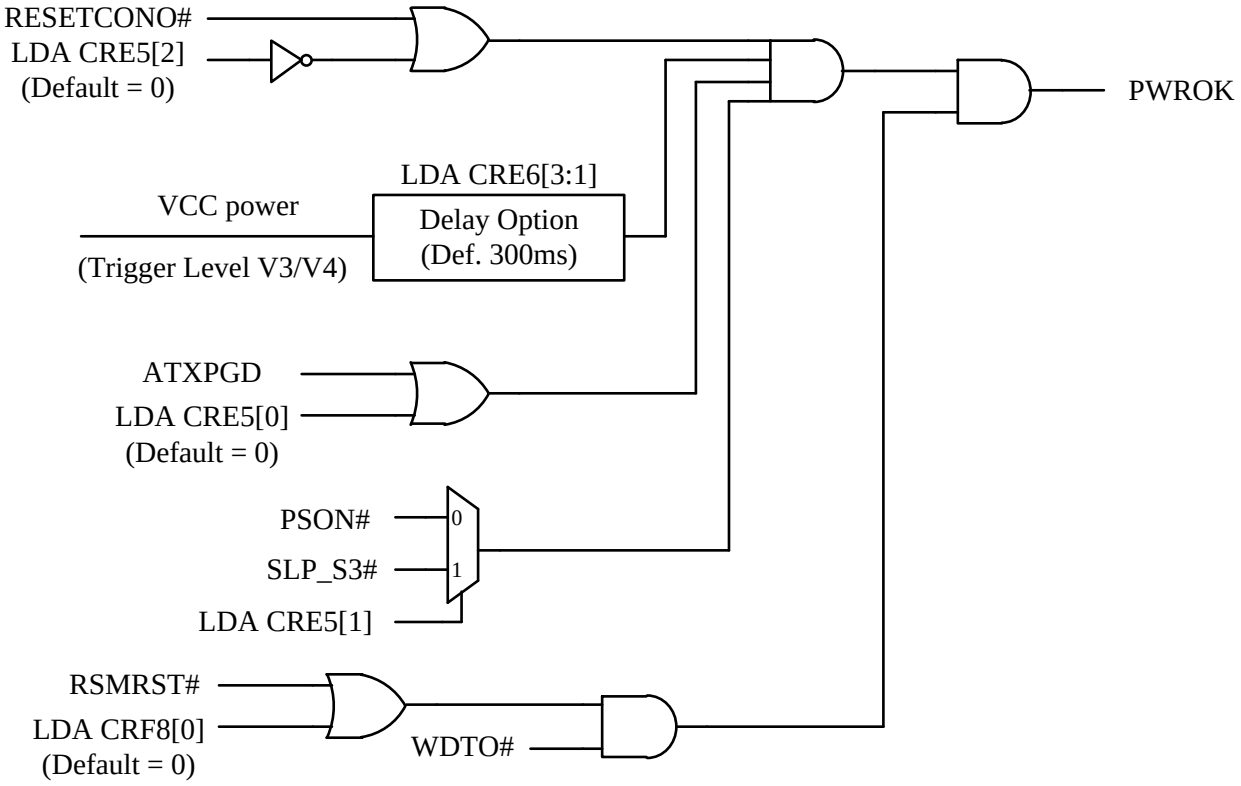


Figure 6-9 PWROK Block Diagram

6.8 Front Panel LEDs

NCT6796D supports two LED control pins – GRN_LED and YLW_LED.

For dual-color LED application:

(1)GRN_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the green LED and the anode of the yellow LED.

(2)YLW_LED pin is connected to a 470ohm resistor to 5VSB, and the cathode of the yellow LED and the anode of the green LED.

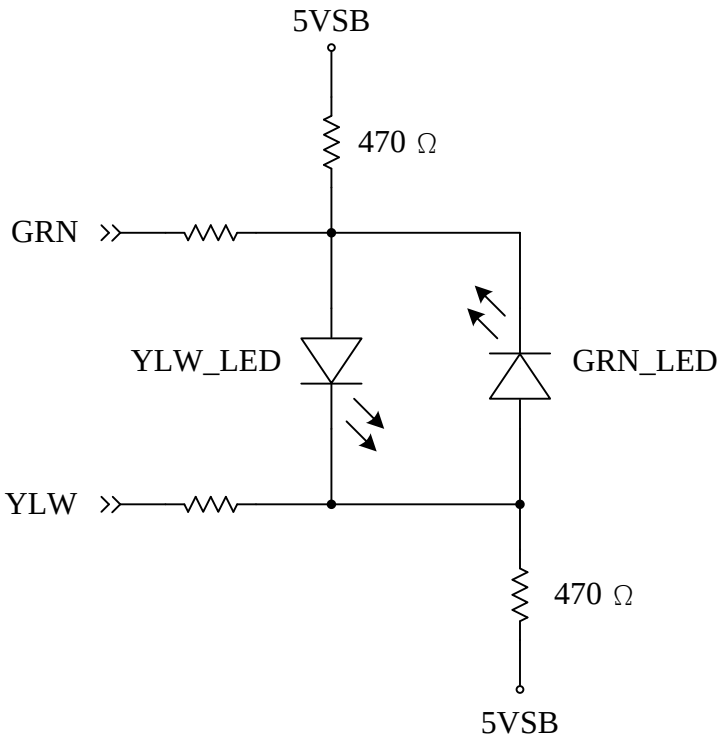


Figure 6-10 Illustration of Dual Color LED application

GRN_LED and YLW_LED pins are designed to show currently power states. There are Manual Mode and Automatic Mode:

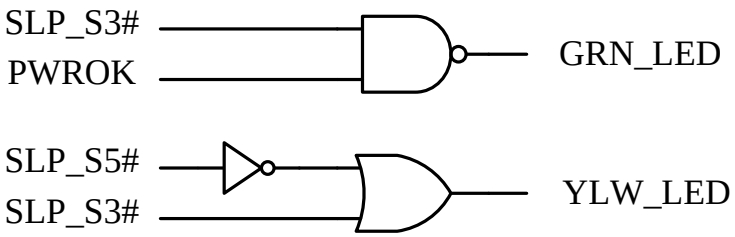
6.8.1 Automatic Mode

Power state is S0 or S1: GRN_LED will be asserted by default.

Power state is S3: YLW_LED will be asserted by default.

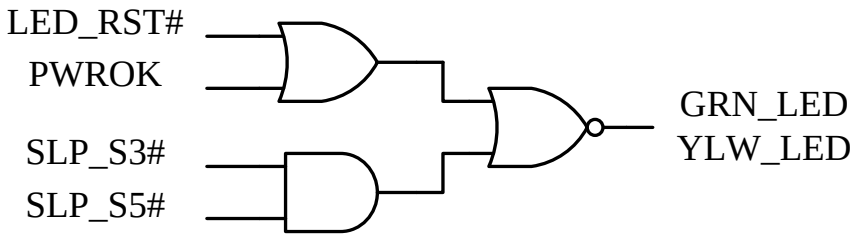
Power state is S4 or S5: Both GRN_LED and YLW_LED will be de-asserted by default.

AUTO_EN	GRN_LED_RST (YLW_LED_RST)	Pwr State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
1	X	S0,S1	1	1	GRN_BLK_FREQ	HIGH-Z
1	X	S3	0	1	HIGH-Z	YLW_BLK_FREQ
1	X	S4,S5	X	0	HIGH-Z	HIGH-Z



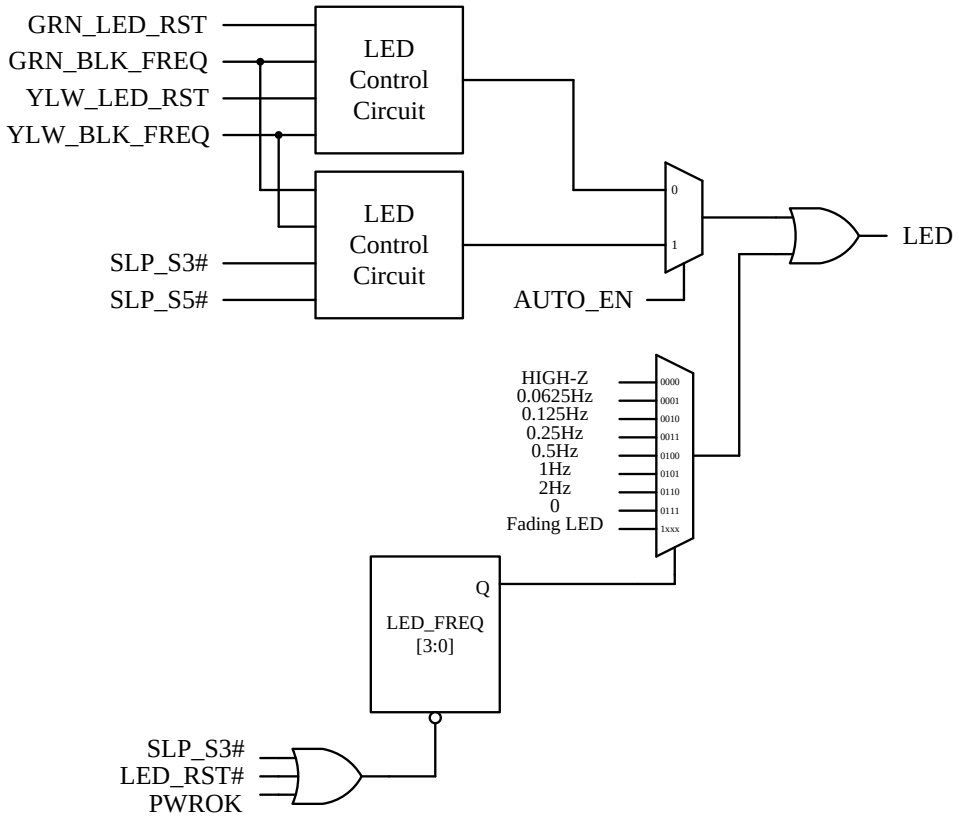
6.8.2 Manual Mode

AUTO_EN	GRN_LED_RST# (YLW_LED_RST)	Pwr State	SLP_S3#	SLP_S5#	GRN_LED	YLW_LED
0	0	S0,S1	1	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	0	S3	0	1	HIGH-Z	HIGH-Z
0	0	S4,S5	X	0	HIGH-Z	HIGH-Z
0	1	S0,S1	1	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	1	S3	0	1	GRN_BLK_FREQ	YLW_BLK_FREQ
0	1	S4,S5	X	0	GRN_BLK_FREQ	YLW_BLK_FREQ



Register Neme	Register Location
AUTO_EN	Logic Device B, CRF7h, bit7
GRN_BLK_FREQ	Logic Device B, CRF7h, bit3~0
YLW_BLK_FREQ	Logic Device B, CRF8h, bit3~0
GRN_LED_RST#	Logic Device B, CRF7h, bit6
YLW_LED_RST#	Logic Device B, CRF8h, bit6

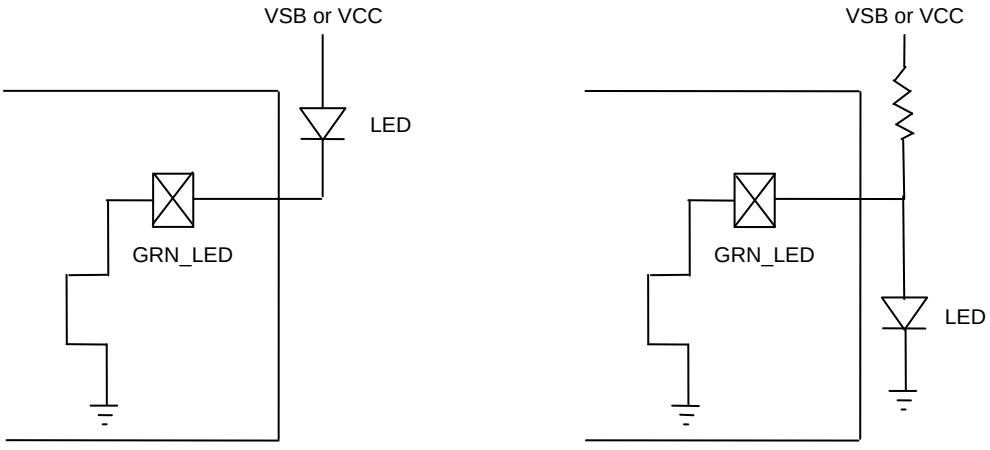
6.8.3 S0~S5 LED Blink Block Diagram



6.8.4 LED Pole (LED_POL)

Set to 0b, GRN_LED output is active low, as the following Figure(a)

Set to 1b, GRN_LED output is active high, as the following Figure(b)



(a) Active Low

(b) Active High

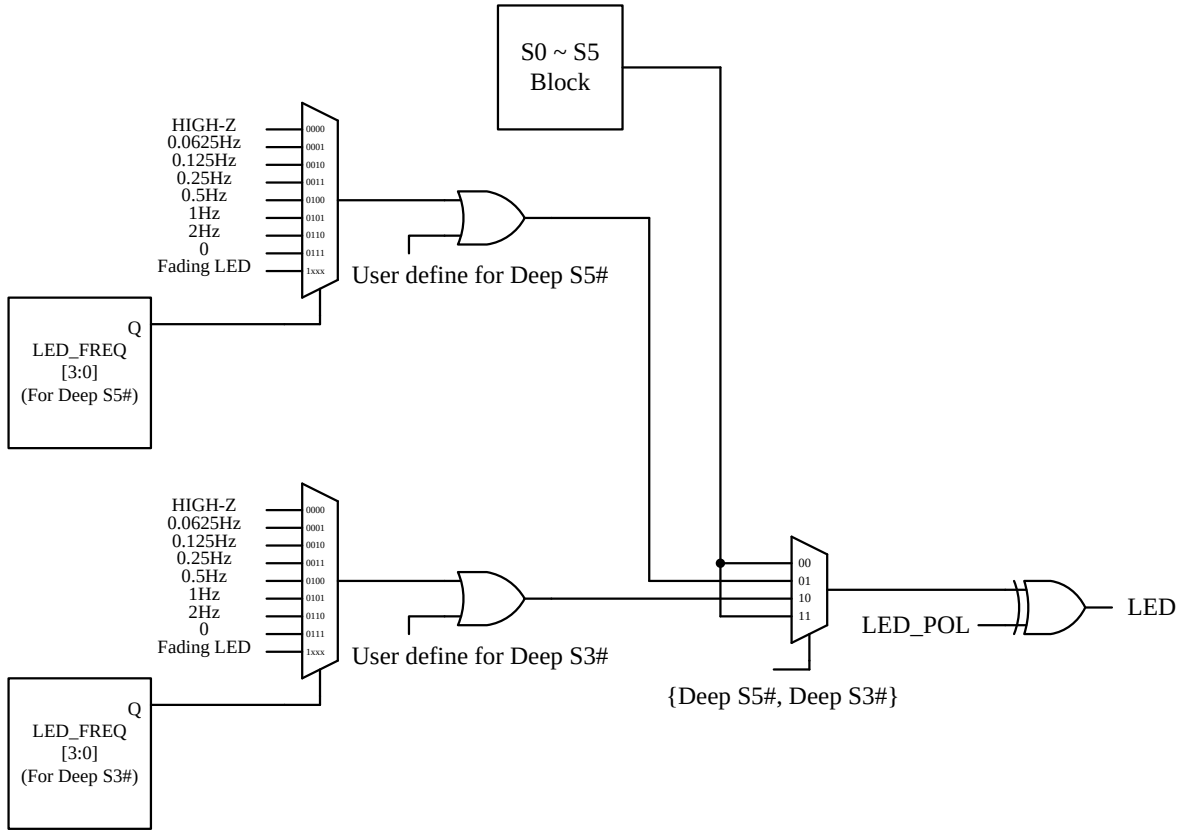
Figure 6-11 Illustration of LED polarity

6.8.5 Deeper Sleeping State Detect Function

These two LED pins could also be used to indicate if the system is in Deeper Sleeping State. For more detail, please refer to the section of Advanced Sleep State Control Function.

Enable_DEEP_S5	GRN_DEEPS#_Disable (YLW_DEEPS#_Disable)	Pwr State	GRN_LED	YLW_LED
1	0	DEEP_S5	DeepS5_GRN_BLK_FREQ	DeepS5_YLW_BLK_FREQ
1	1	DEEP_S5	HIGH-Z	HIGH-Z
0	X	S0~S5	S0~S5 behavior	S0~S5 behavior

Enable_DEEP_S3	GRN_DEEPS#_Disable (YLW_DEEPS#_Disable)	Pwr State	GRN_LED	YLW_LED
1	0	DEEP_S3	DeepS3_GRN_BLK_FREQ	DeepS3_YLW_BLK_FREQ
1	1	DEEP_S3	HIGH-Z	HIGH-Z
0	X	S0~S5	S0~S5 behavior	S0~S5 behavior



6.9 Advanced Sleep State Control (ASSC) Function

Advanced Sleep State Control (ASSC) Function is used to control the system power at S3 or S5 state. The purpose of this function is to provide a method to reduce power consumption at S3 or S5 state. This function is disabled by default. When VCC power is first supplied, BIOS can program the register to enable ASSC Function. The register is powered by 3VSB_IO and some is powered by VBAT. The related registers are located at Logic Device 16 CRE0h ~ CRE3h.

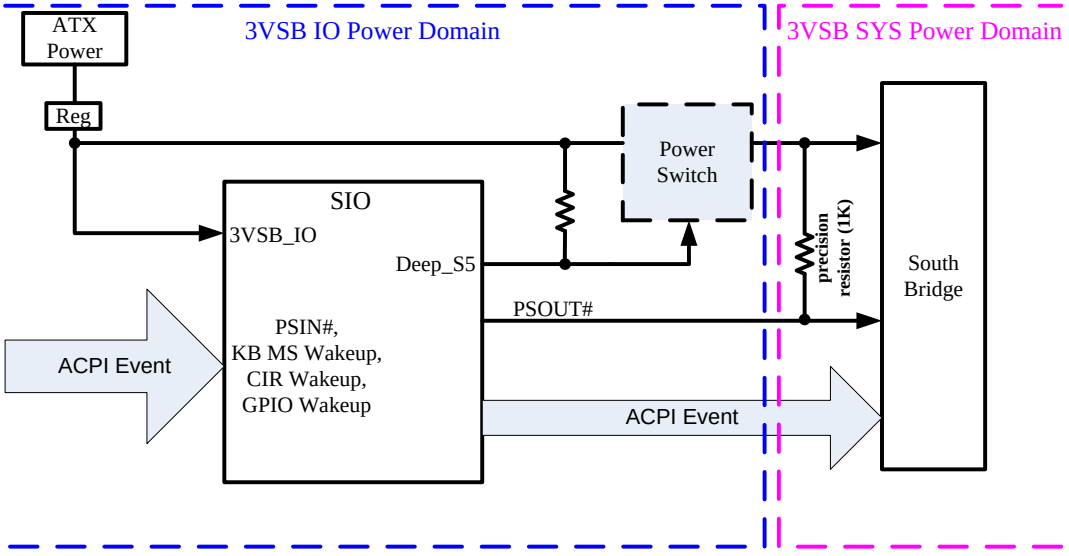
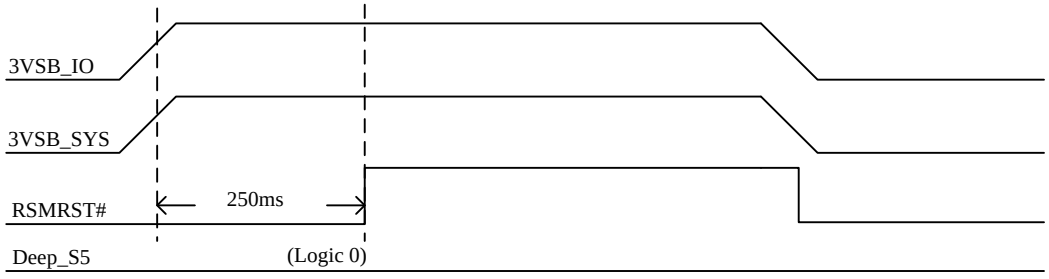


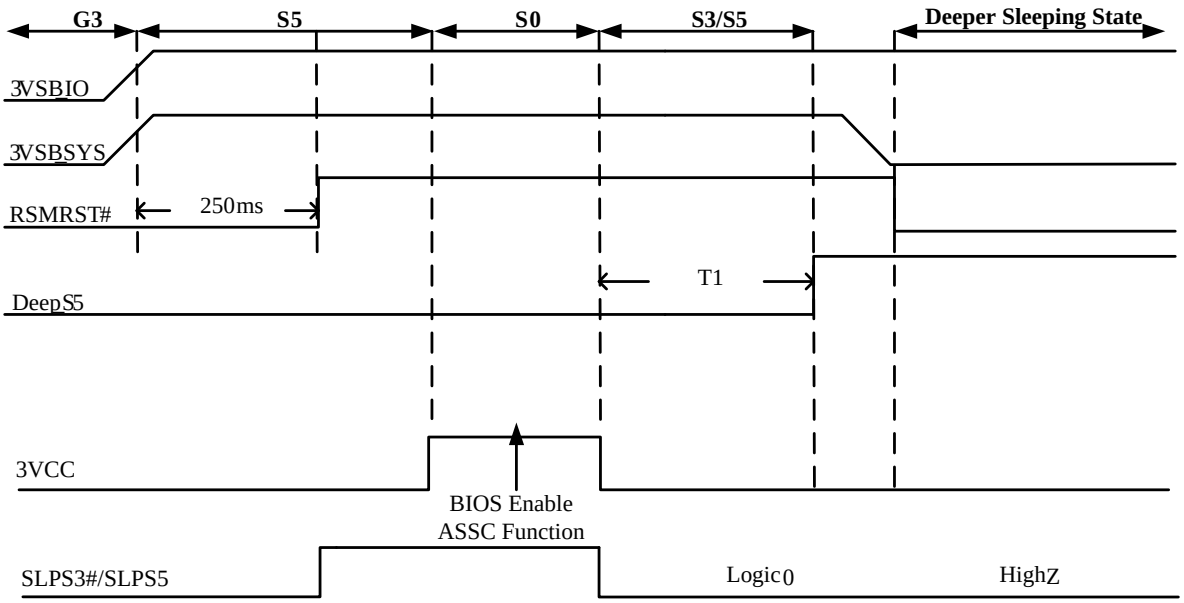
Figure 6-12 ASSC Application Diagram

6.9.1 When ASSC is disabled



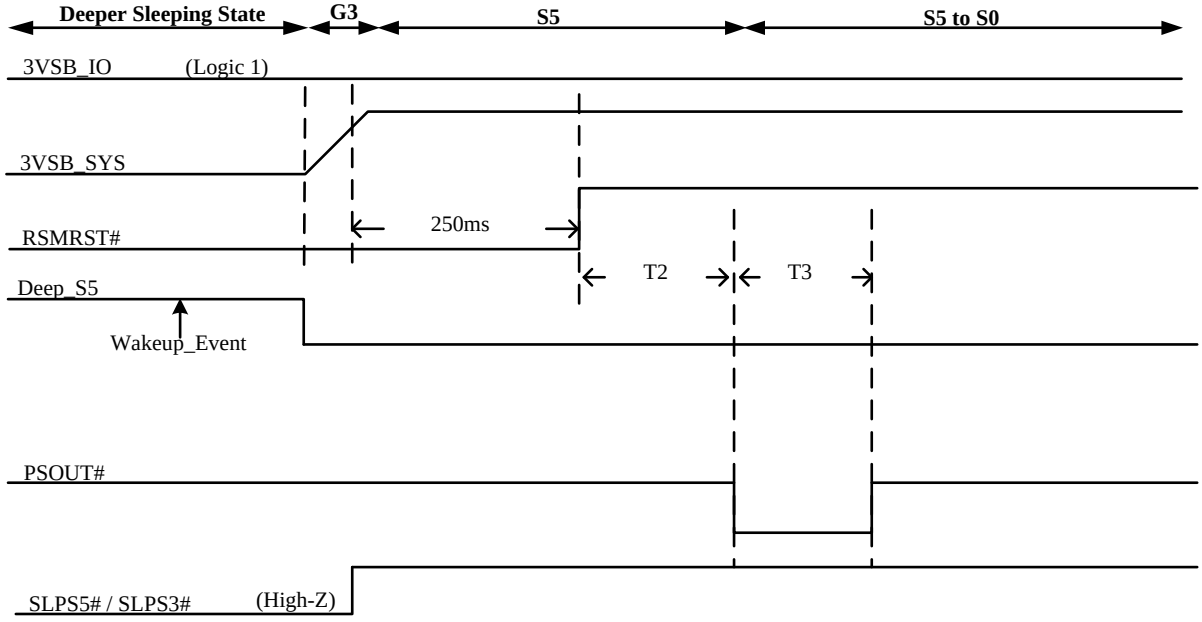
When ASSC is disabled, ACPI function is as same as the normal ACPI behavior.

6.9.2 When ASSC is enabled (Enter into Deeper Sleeping State)



When the first time AC plug in and enter into S0 State, BIOS can enable ASSC Function (DeepS3 or DeepS5), when the system enters S3/S5 state, the pin DEEP_S5 will be asserted after pre configuration delay time (power_off_dly_time, LD16 CRE2) to make the system entering the “Deeper Sleeping State (DSS)” where system’s VSB power is cut off. When pin DEEP_S5 asserts, the pin RSMRST# will de-assert by detecting PSOUT# signal (monitor 3VSB SYS Power).

6.9.3 When ASSC is enabled (Exit Deeper Sleeping State)

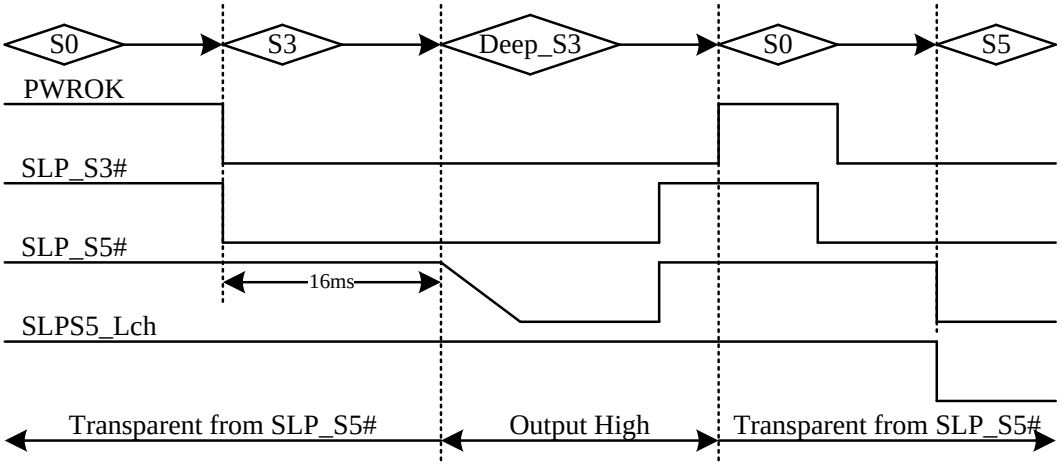


When any Wakeup Event (PSIN#, KB MS Wakeup, CIR wakeup, GPIO Wakeup) happened, pin DEEP_S5 will be de-asserted to turn on the VSB power to the system. The pin RSMRST# will de-assert when 3VSB_SYS power reach valid voltage. And then the pin PSOUT# will issue a low pulse (T3) turn on the system after T2 time

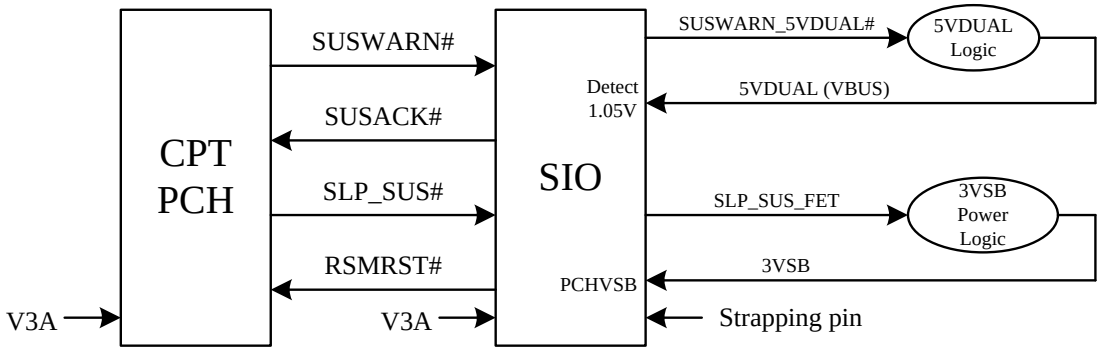
(wakeup delay time, LD16 CRE0). The PSOUT# low pulse is also programmable (LD16 CRE1). The T4 time is the delay from Deep_S5 ds-assert to Deeo_S5#_DELAY de-assert.

6.9.4 SLP_S5#_LATCH Control Function

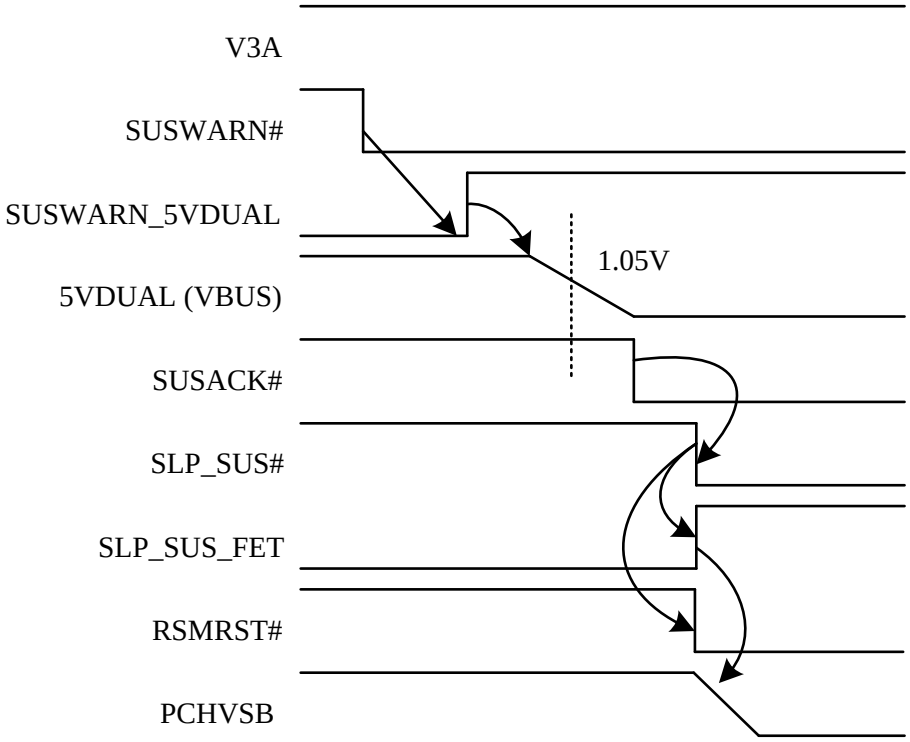
SLP_S5#_LATCH control signal is similar to SLPS5# signal. When System is at S0 ~ S5 state, SLP_S5#_LATCH follows the SLPS5# signal. When system is at DeepS5 State, SLP_S5#_LATCH will keep low state till system returns to S0 state. When system is at DeepS3 State, SLP_S5#_LATCH will keep high till system returns to S0 state. Please see the following timing diagram:



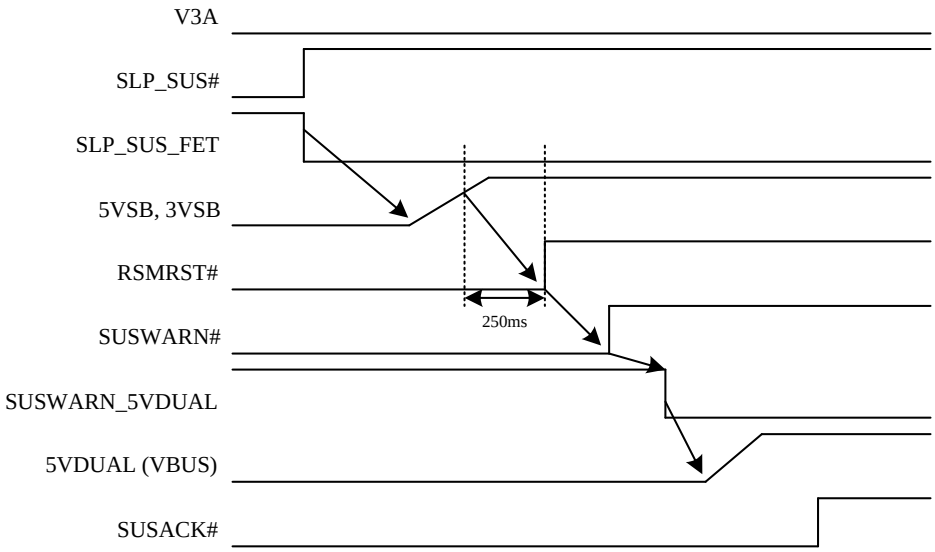
6.10 Intel DSW Function



6.10.1 Enter DSW State timing diagram

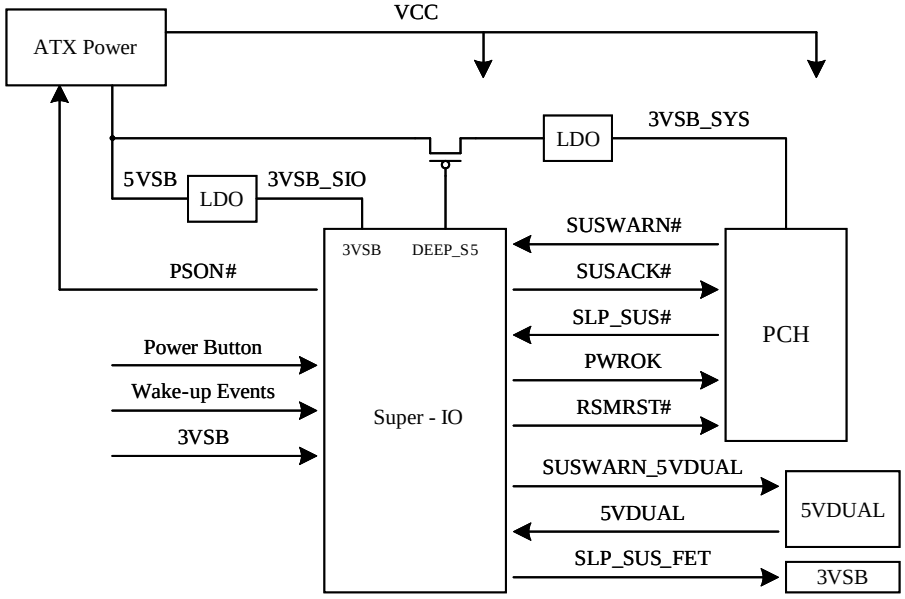


6.10.2 Exit DSW State timing diagram



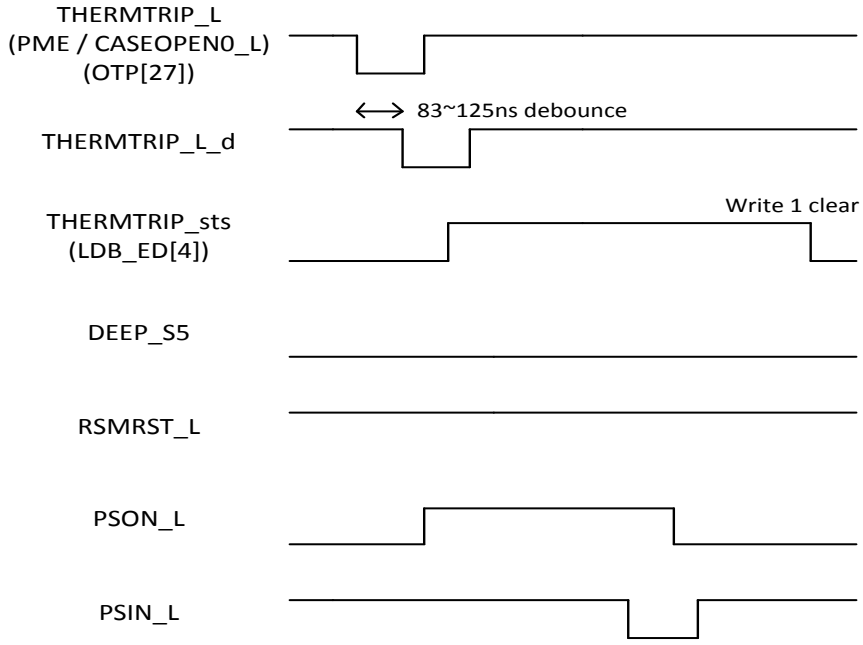
6.10.3 Application Circuit

The NCT6796D can not only provide SIO Deep S5/S3 function, but Intel DSW function. The application circuit should follow the guide below:

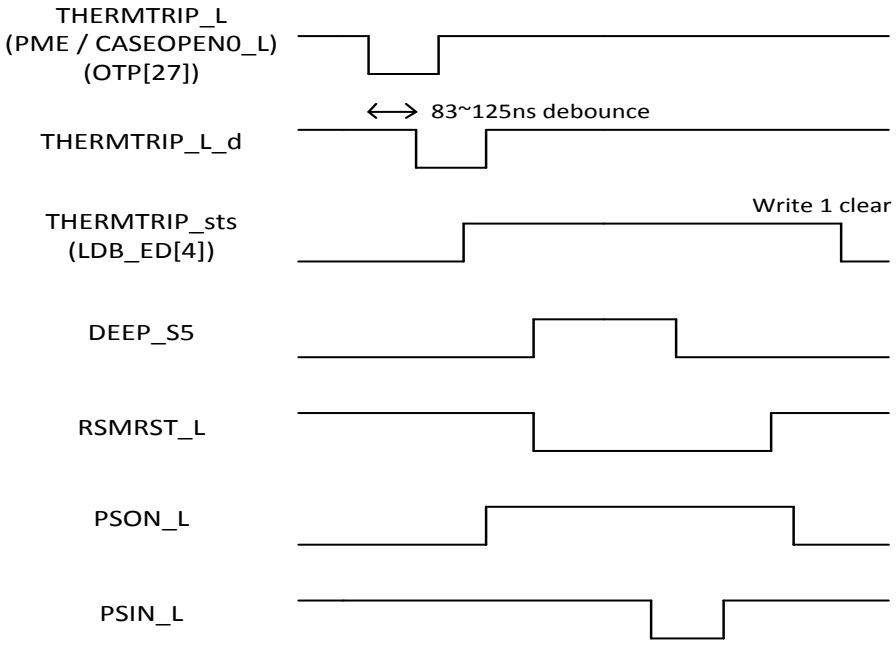


6.11 Thermtrip function

When user push Thermtrip button in S0 state and LDB_CRED[3] =0, the system will enter S5 state and we have a flag to monitor (LDB CRED bit[4]).



When user push Thermtrip button in S0 state and LDB_CRED[3] =1, the system will enter DeepS5 state and we have a flag to monitor (LDB CRED bit[4]).



7. CONFIGURATION REGISTER ACCESS PROTOCOL

The NCT6796D uses a special protocol to access configuration registers to set up different types of configurations. The NCT6796D has a total of 16 Logical Devices (from Logical Device 1 to Logical Device 16).

It would require a large address space to access all of the logical device configuration registers if they were mapped into the normal PC address space. The NCT6796D, then, maps all the configuration registers through two I/O addresses (2Eh/2Fh or 4Eh/4Fh) set at power on by the strap pin 2E_4E_SEL. The two I/O addresses act as an index/data pair to read or write data to the Super I/O. One must write an index to the first I/O address which points to the register and read or write to the second address which acts as a data register.

An extra level of security is added by only allowing data updates when the Super I/O is in a special mode, called the Extended Function Mode. This mode is entered by two successive writes of 87h data to the first I/O address. This special mode ensures no false data can corrupt the Super I/O configuration during a program runaway.

There are a set of global registers located at index 0h – 2Fh, containing information and configuration for the entire chip.

The method to access the control registers of the individual logical devices is straightforward. Simply write the desired logical device number into the global register 07h. Subsequent accesses with indexes of 30h or higher are directly to the logical device registers.

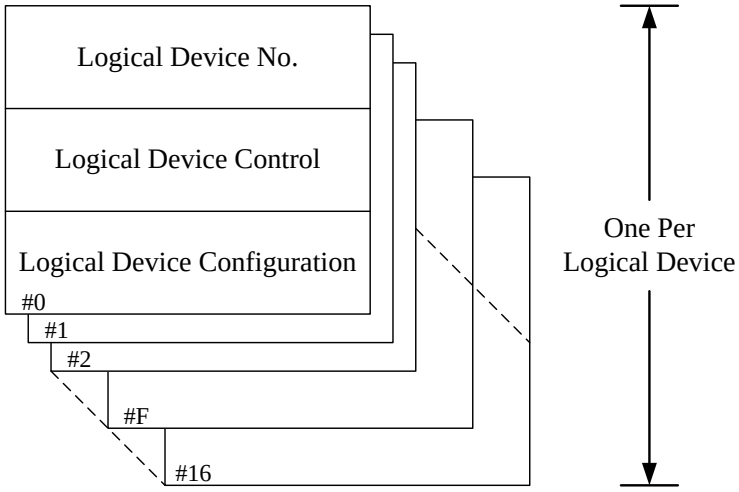


Figure 7-1 Structure of the Configuration Register

7.1 Configuration Sequence

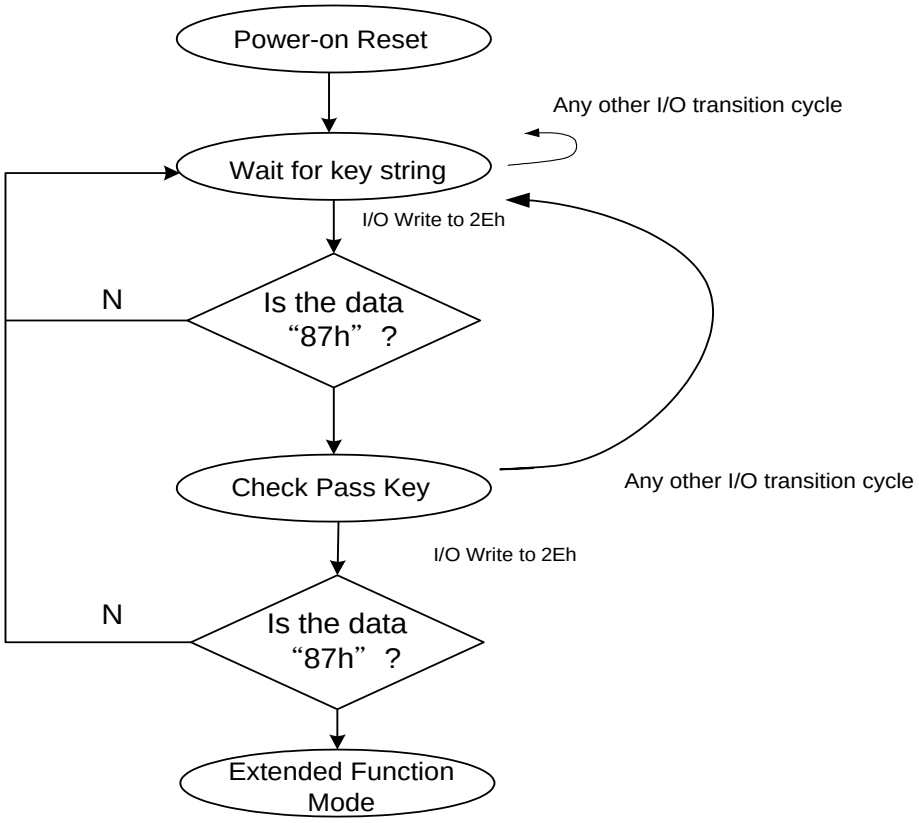


Figure 7-2 Configuration Register

To program the NCT6796D configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

(3). Exit the Extended Function Mode.

7.1.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

7.1.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

7.1.3 Exit the Extended Function Mode

To exit the Extended Function Mode, writing 0xAA to the EFER is required. Once the chip exits the Extended Function Mode, it is in the normal running mode and is ready to enter the configuration mode.

7.1.4 Software Programming Example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so the EFIR is located at 2Eh and the EFDR is located at 2Fh. If the HEFRAS (CR[26h] bit 6 showing the value of the strap pin at power on) is set, 2Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

This example programs the configuration register F0h (clock source) of logical device 1 (UART A) to the value of 3Ch (24MHz). First, one must enter the Extended Function Mode, then setting the Logical Device Number (Index 07h) to 01h. Then program index F0h to 3Ch. Finally, exit the Extended Function Mode.

```
;-----------------------------------------------------
; Enter the Extended Function Mode
;-----------------------------------------------------
MOV    DX, 2EH
MOV    AL, 87H
OUT    DX, AL
OUT    DX, AL
;--------------------------------------------------------------------------
; Configure Logical Device 1, Configuration Register CRF0
;--------------------------------------------------------------------------
MOV    DX, 2EH
MOV    AL, 07H
OUT    DX, AL          ; point to Logical Device Number Reg.
MOV    DX, 2FH
MOV    AL, 01H
OUT    DX, AL          ; select Logical Device 1
;
MOV    DX, 2EH
MOV    AL, F0H
OUT    DX, AL          ; select CRF0
MOV    DX, 2FH
MOV    AL, 3CH
OUT    DX, AL          ; update CRF0 with value 3CH
;-----------------------------------------------
; Exit the Extended Function Mode
;-----------------------------------------------
MOV    DX, 2EH
MOV    AL, AAH
OUT    DX, AL
```

8. HARDWARE MONITOR

8.1 General Description

The NCT6796D monitors several critical parameters in PC hardware, including power supply voltages, fan speeds, and temperatures, all of which are very important for a high-end computer system to work stably and properly. In addition, proprietary hardware reduces the amount of programming and processor intervention to control cooling fan speeds, minimizing ambient noise and maximizing system temperature and reliability.

The NCT6796D can simultaneously monitor all of the following inputs:

- Fifteen analog voltage inputs (Six internal voltages CPUVCORE, VBAT, VTT, 3VSB, 3VCC and AVSB; Nine external voltage inputs)
- Seven fan tachometer inputs
- Seven remote temperatures, using either a thermistor or from the CPU thermal diode (voltage or Current Mode measurement method)
- One case-open detection signal.

These inputs are converted to digital values using the integrated, eight-bit analog-to-digital converter (ADC).

In response to these inputs, the NCT6796D can generate the following outputs:

- Seven PWM (pulse width modulation) and one DC fan outputs for the fan speed control
- SMI#
- OVT# signals for system protection events

The NCT6796D provides hardware access to all monitored parameters through the LPC or I^2C interface and software access through application software, such as Nuvoton's Hardware Doctor™, or BIOS.

The rest of this section introduces the various features of the NCT6796D hardware-monitor capability. These features are divided into the following sections:

- Access Interfaces
- Analog Inputs
- Fan Speed Measurement and Control
- Smart Fan Control
- SMI# interrupt mode
- OVT# interrupt mode
- Registers and Value RAM

8.2 Access Interfaces

The NCT6796D provides two interfaces, LPC and I^2C, for the microprocessor to read or write the internal registers of the hardware monitor.

8.3 LPC Interface

The internal registers of the hardware monitor block are accessible through two separate methods on the LPC bus. The first set of registers, which primarily enable the block and set its address in the CPU I/O address space are accessed by the Super I/O protocol described in Chapter 7 at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed form an index/data pair of CPU I/O addresses. The

standard locations are usually 295h/296h and are set by CR[60h]&CR[61h] accessed using the Super I/O protocol as described in Chapter 7.

Due to the number of internal register, it is necessary to separate the register sets into “banks” specified by register 4Eh. The structure of the internal registers is shown in the following figure.

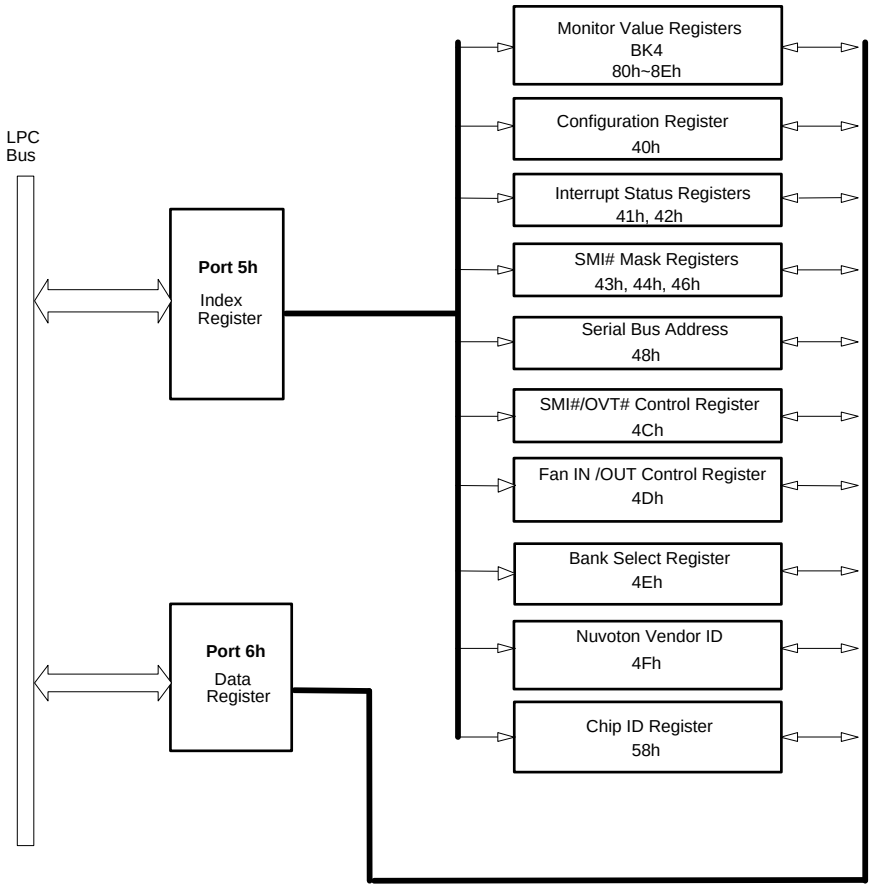


Figure 8-1 LPC Bus’ Reads from / Write to Internal Registers

8.4 ESPI interface

The Enhanced Serial Peripheral Interface (ESPI) operates in master/slave mode of operation where the eSPI master dictates the flow of command and data between itself and the eSPI slave by controlling the Chip Select# pins for each of the eSPI slaves. At any one time, the eSPI must ensure that only one of the Chip Select# pins is assered based on source code, thus allowing transactions to flow between the eSPI master and the corresponding eSPI slave associated with the Chip Select# pin. The eSPI master is the only component that is allowed to drive Chip Select# when eSPI Reset# is de-asserted.

For an eSPI bus, there is only the eSPI master and one or more eSPI slaves. In single Master-Single Slave configuration, a single eSPI master will be connected to a single eSPI slave.

The eSPI provided an alternative for connecting an SIO to the platform (besides the LPC interface). Note the LPC and eSPI co-exist on the platform but only one interface can be enabled at a time via a hardware strap.

The first set of registers, which primarily enable the block and set its address in the CPU I/O address space are accessed by the Super I/O protocol at address 2Eh/2Fh or 4Eh/4Fh. The bulk of the functionality and internal registers of this block are accessed form an index/data pair of CPU I/O addresses. The NCT6796's eSPI is only support IO Read and Write, Get PCH temperature by OOB, and virtual wire.

The basic protocol is shown as below. For the detail eSPI specification, please refer to ***Enhanced Serial Peripheral Interface Base Specification (for Client and Server Platform) Rev 0.75***

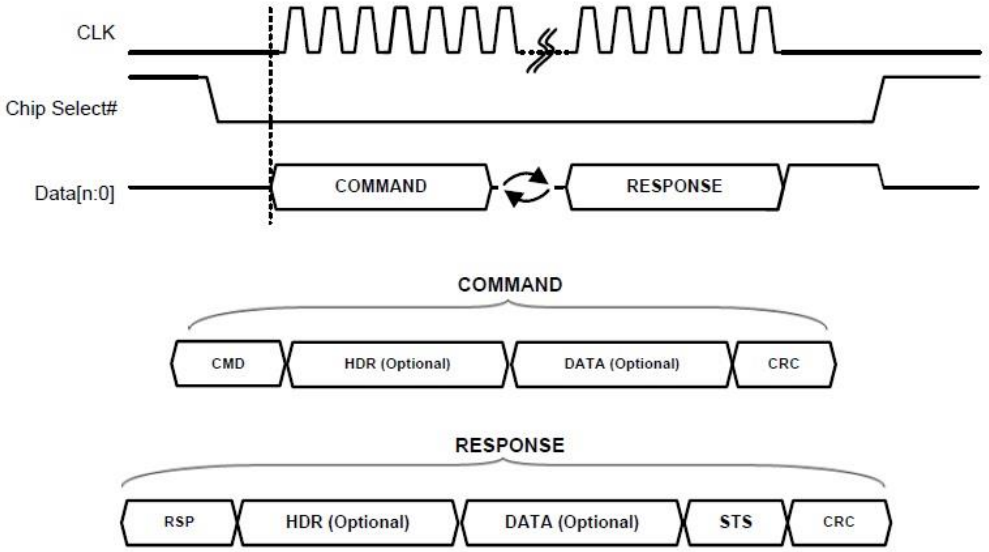


Table 8.4.1 eSPI Protocol Transcation

8.5 I²C interface

The I²C interface is a second, serial port into the internal registers of the hardware monitor function block. The interface is totally compatible with the industry-standard I²C specification, allowing external components that are also compatible to read the internal registers of the NCT6796D hardware monitor and control fan speeds. The address of the I²C peripheral is set by the register located at index 48h (which is accessed by the index/data pair at I/O address typically at 295h/296h)

The two timing diagrams below illustrate how to use the I²C interface to write to an internal register and how to read the value in an internal register, respectively.

(a) Serial bus write to internal address register followed by the data byte

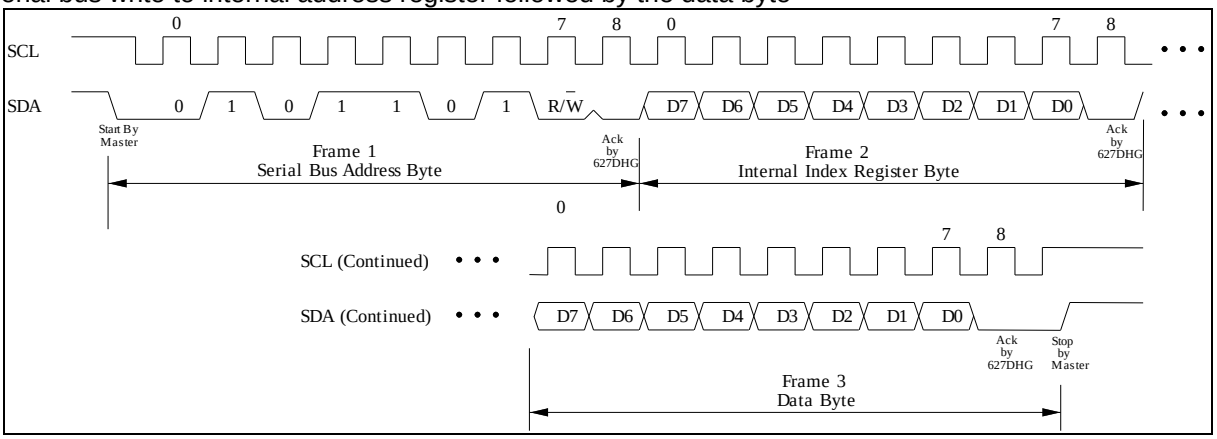


Figure 8-2 Serial Bus Write to Internal Address Register Followed by the Data Byte

(b) Serial bus read from a register

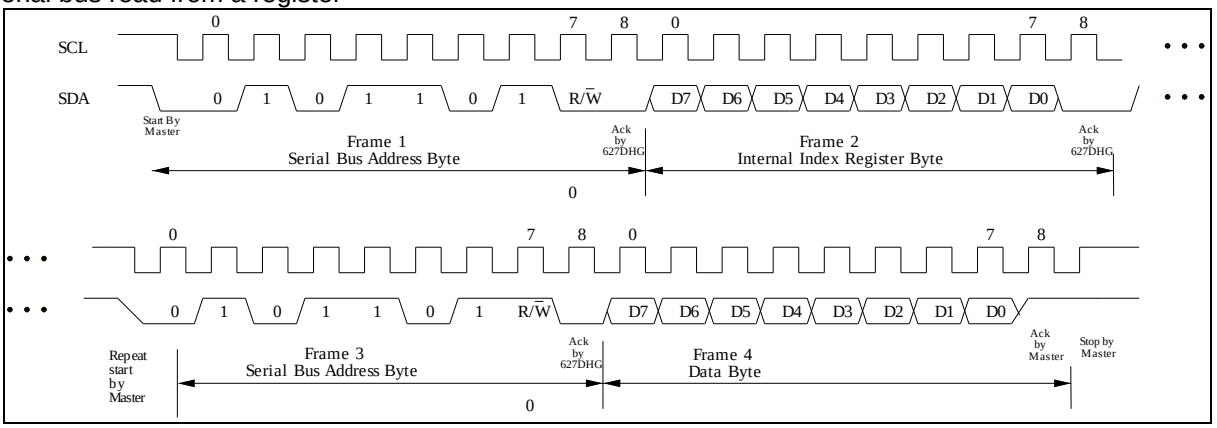


Figure 8-3 Serial Bus Read from Internal Address Register

8.6 Analog Inputs

The Nine analog inputs of the hardware monitor block connect to an 8-bit Analog to Digital Converter (ADC) and consist of 9 general-purpose inputs connected to external device pins (VIN0 – VIN9) and Six internal signals connected to the power supplies (CPUVCORE, AVSB, VBAT, VTT, 3VSB and 3VCC). All inputs are limited to a maximum voltage of 2.048V due to an internal setting of 8mV LSB (256 steps x 8mV = 2.048V). All inputs to the ADC must limit the maximum voltage by using a voltage divider. The power supplies have internal resistors, while the external pins require outside limiting resistors as described below.

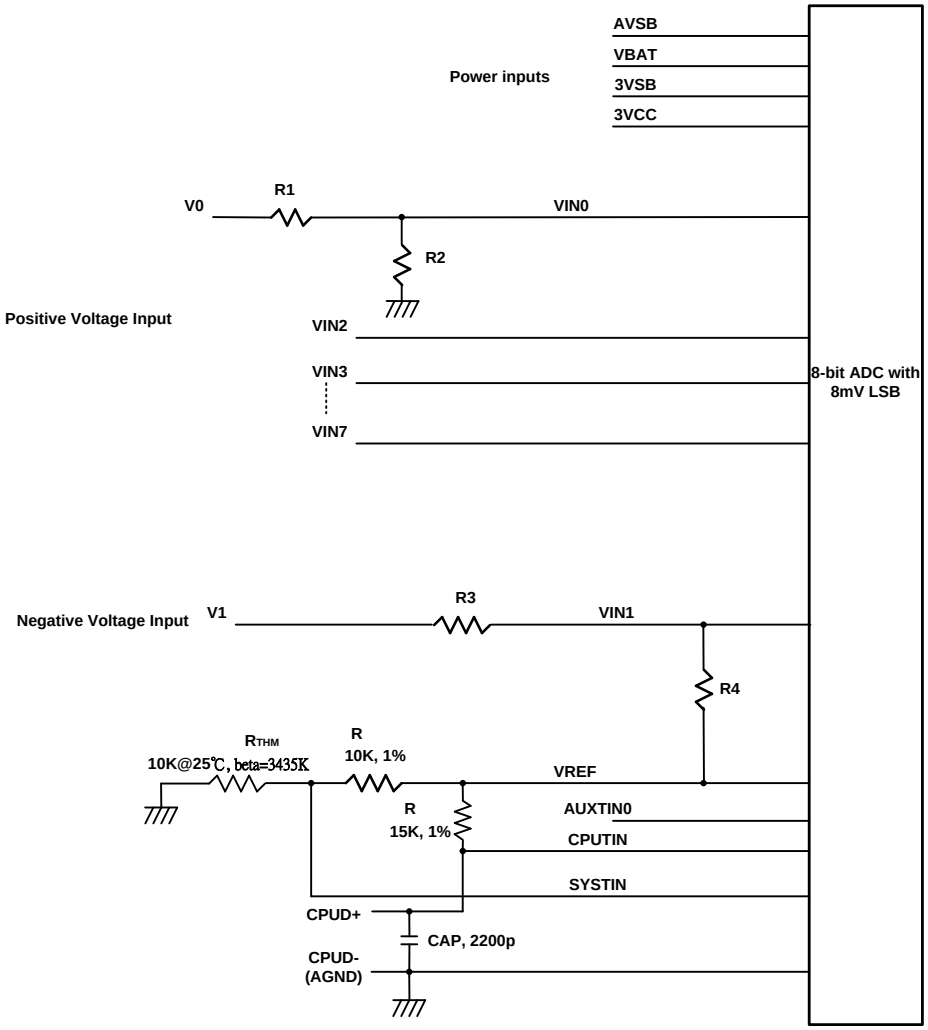


Figure 8-4 Analog Inputs and Application Circuit of the NCT6796D

As illustrated in the figure above, other connections may require some external circuits. The rest of this section provides more information about voltages outside the range of the 8-bit ADC, CPU Vcore voltage detection, and temperature sensing.

8.6.1 Voltages Over 2.048 V or Less Than 0 V

Input voltages greater than 2.048 V should be reduced by an external resistor divider to keep the input voltages in the proper range. For example, input voltage V_0 (+12 V) should be reduced before it is connected to VIN0 according to the following equation:

$$VIN0 = V_0 \times \frac{R_2}{R_1 + R_2}$$

R1 and R2 can be set to 56 KΩ and 10 KΩ, respectively, to reduce V_0 from +12 V to less than 2.048 V.

All the internal inputs of the ADC, AVSB, VBAT, 3VSB and 3VCC utilize an integrated voltage divider with both resistors equal to 34KΩ, yielding a voltage one half of the power supply. Since one would expect a worst-case 10% variation or a 3.63V maximum voltage, the input to the ADC will be 1.815V, well within the maximum range.

$$V_{in} = VCC \times \frac{34K\Omega}{34K\Omega + 34K\Omega} \cong 1.65V$$, where VCC is set to 3.3V

The CPUVCORE pin feeds directly into the ADC with no voltage divider since the nominal voltage on this pin is only 1.2V.

Negative voltages are handled similarly, though the equation looks a little more complicated. For example, negative voltage V1 (-12V) can be reduced according to the following equation:

$$VIN1 = (V_1 - 2.048) \times \frac{R_4}{R_3 + R_4} + 2.048, where V_1 = -12$$

R3 and R4 can be set to 232 KΩ and 10 KΩ, respectively, to reduce negative input voltage V_1 from –12 V to less than 2.048 V. Note that R4 is referenced to VREF, or 2.048V instead of 0V to allow for more dynamic range. This is simply good analog practice to yield the most precise measurements.

Both of these solutions are illustrated in the figure above.

8.6.2 Voltage Data Format

The data format for voltage detection is an eight-bit value, and each unit represents an interval of 8 mV.

Detected Voltage = Reading * 0.008 V

If the source voltage was reduced by a voltage divider, the detected voltage value must be scaled accordingly.

8.6.2.1. Voltage Reading

NCT6796D has 16 voltage reading:

	CPUVCORE	VIN1	AVSB	3VCC	VIN0
Voltage reading	Bank4, Index80	Bank4, Index81	Bank4, Index82	Bank4, Index83	Bank4, Index84
	VIN8	VIN4	3VSB	VBAT	VTT
Voltage reading	Bank4, Index85	Bank4, Index86	Bank4, Index87	Bank4, Index88	Bank4, Index89
	VIN5	VIN6	VIN2	VIN3	VIN7
Voltage reading	Bank4, Index8A	Bank4, Index8B	Bank4, Index8C	Bank4, Index8D	Bank4, Index8E

	VIN9				
Voltage reading	Bank4, Index8F				

Note: Bank0 CR BD bit 7:6 are lowest bit1:0 for ADC. These two bits accrancy is not guarantee.

8.6.3 Temperature Data Format

The data format for sensors SYSTIN, CPUTIN, AUXTIN0, AUXTIN1, AUXTIN2, AUXTIN3 and AUXTIN4 is 9-bit, two's-complement. This is illustrated in the table below. There are two sources of temperature data: external thermistors or thermal diodes.

Table 8-1 Temperature Data Format

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1Ceh
-55°C	1100,1001	C9h	1,1001,0010	192h

8.6.3.1. Monitor Temperature from Thermistor

External thermistors should have a β value of 3435K and a resistance of 10 KΩ at 25°C. As illustrated in the schematic above, the thermistor is connected in series with a 10-KΩ resistor and then connects to VREF. The configuration registers to select a thermistor temperature sensor and the measurement method are found at Bank 0, index 59h, 5Dh, and 5Eh.

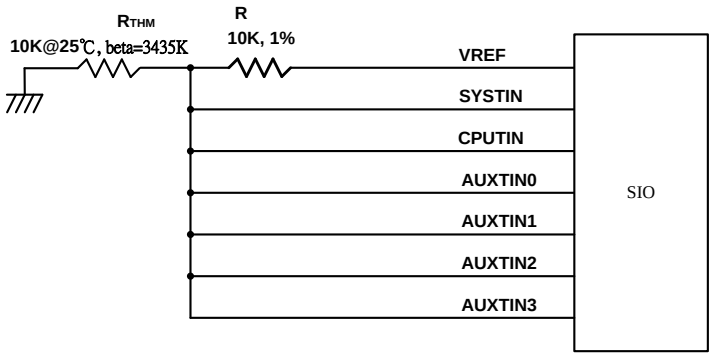


Figure 8-5 Monitoring Temperature from Thermistor

8.6.3.2. Monitor Temperature from Thermal Diode (Voltage Mode)

The thermal diode D- pin is connected to AGND, and the D+ pin is connected to the temperature sensor pin in the NCT6796D. A 15-KΩ resistor is connected to VREF to supply the bias current for the diode, and the 2200-pF, bypass capacitor is added to filter high-frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh, and 5Eh.

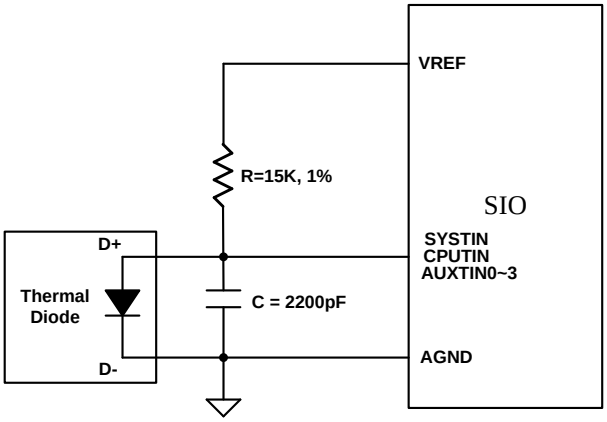


Figure 8-6 Monitoring Temperature from Thermal Diode (Voltage Mode)

8.6.3.3. Monitor Temperature from Thermal Diode (Current Mode)

The NCT6796D can also sense the diode temperature through Current Mode and the circuit is shown in the following figure.

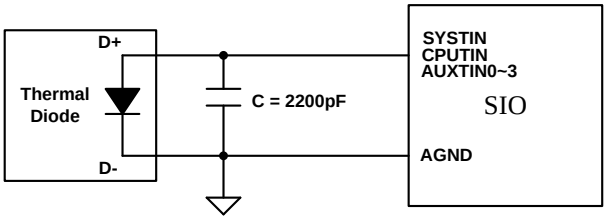


Figure 8-7 Monitoring Temperature from Thermal Diode (Current Mode)

The pin of processor D- is connected to CPUD- and the pin D+ is connected to temperature sensor pin in the NCT6796D. A bypass capacitor C=2200pF should be added to filter the high frequency noise. The configuration registers to select a thermal diode temperature sensor and the measurement method are found at Bank 0, index 5Dh and 5Eh.

8.6.3.4. Temperature Reading

NCT6796D has 6 temperature reading can monitor different temperature sources (ex. SYSTIN, CPUTIN, AUXTIN0, PECI…etc).

	SMIOVT1	SMIOVT2	SMIOVT3	SMIOVT4
Temperature source select	Bank6,index21 bit[4:0] default: SYSTIN	Bank6, index22 bit[4:0] default:CPUTIN	BankC,index26 bit[4:0] default: AUXTIN0	BankC,index27 bit[4:0] default: AUXTIN1

Temperature reading	Bank0, index27	Bank1, index50	Bank6, index70	Bank6, index72

	SMIOVT5	**SMIOVT6**	**SMIOVT7**	**SMIOVT8**
Temperature source select	BankC,index28 bit[4:0] default: AUXTIN2	BankC,index29 bit[4:0] default: AUXTIN3	BankC,index2A bit[4:0] default: AUXTIN4	BankC,index2B bit[4:0] default: CPUTIN
Temperature reading	Bank6, index74	Bank6, index76	Bank6, index78	Bank6, index7A

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

8.6.4 ADC Conversion Time and Cycle Time

The ADC conversion time of each channel is about 2ms and the period of Cycle time formula is conversion time multipleis total channel number and average time. For example, the NCT6796 support 15 voltage channels and 7 temperature channels, and average time is 8 times, so the period of update time is 2ms x (15 + 7) x 8 = 352ms.

8.7 PECI

PECI (Platform Environment Control Interface) is a new digital interface to read the CPU temperature of Intel® CPUs. With a bandwidth ranging from 2 Kbps to 2 Mbps, PECI uses a single wire for self-clocking and data transfer. By interfacing to the Digital Thermal Sensor (DTS) in the Intel® CPU, PECI reports a negative temperature (in counts) relative to the processor's temperature at which the thermal control circuit (TCC) is activated. At the TCC Activation temperature, the Intel CPU will operate at reduced performance to prevent the device from thermal damage.

PECI is one of the temperature sensing methods that the NCT6796D supports. The NCT6796D contains a PECI master and reads the CPU PECI temperature. The CPU is a PECI client.

The PECI temperature values returning from the CPU are in "counts" which are approximately linear in relation to changes in temperature in degrees centigrade. However, this linearity is approximate and cannot be guaranteed over the entire range of PECI temperatures. For further information, refer to the PECI specification. All references to "temperature" in this section are in "counts" instead of "°C".

Figure 8-8 PECI Temperature shows a typical fan speed (PWM duty cycle) and PECI temperature relationship.

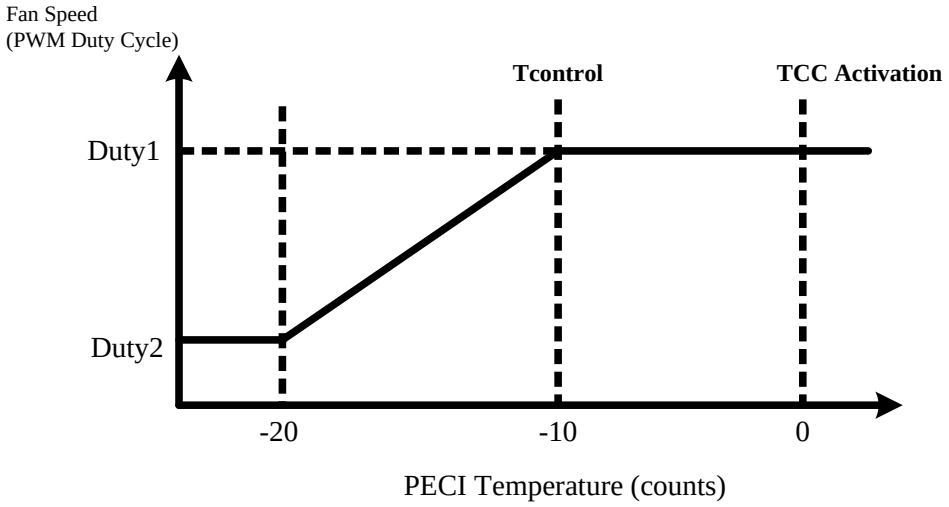


Figure 8-8 PECI Temperature

In this illustration, when PECI temperature is -20, the PWM duty cycle for fan control is at Duty2. When CPU is getting hotter and the PECI temperature is -10, the PWM duty cycle is at Duty1.

At Tcontrol PECI temperature, the recommendation from Intel is to operate the CPU fan at full speed. Therefore Duty1 is 100% if this recommendation is followed. The value of Tcontrol can be obtained by reading the related Machine Specific Register (MSR) in the Intel CPU. The Tcontrol MSR address is usually in the BIOS Writer's guide for the CPU family in question. Refer to the relevant CPU documentation from Intel for more information. In this example, Tcontrol is -10.

When the PECI temperature is below -20, the duty cycle is fixed at Duty2 to maintain a minimum (and constant) RPM for the CPU fan.

The device also provides an offset register to 'shift' the negative PECI readings to positive values. The offset registers are called "Tbase", which are located at Bank7 Index 09h for Agent0 and Bank7 Index 0Ah for Agent1. All default values of these Tbase registers are 8'h00. The unit of the Tbase register contents is "count" to match that of PECI values. The resultant value (Tbase + PECI) should not be interpreted as the "temperature" (whether in count or °C) of the PECI client (CPU).

The Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsets, shows the temperature and fan-speed relationship after Tbase offset is applied (based on Figure 8-8 PECI Temperature). This view is from the perspective of the NCT6796D fan control circuit.

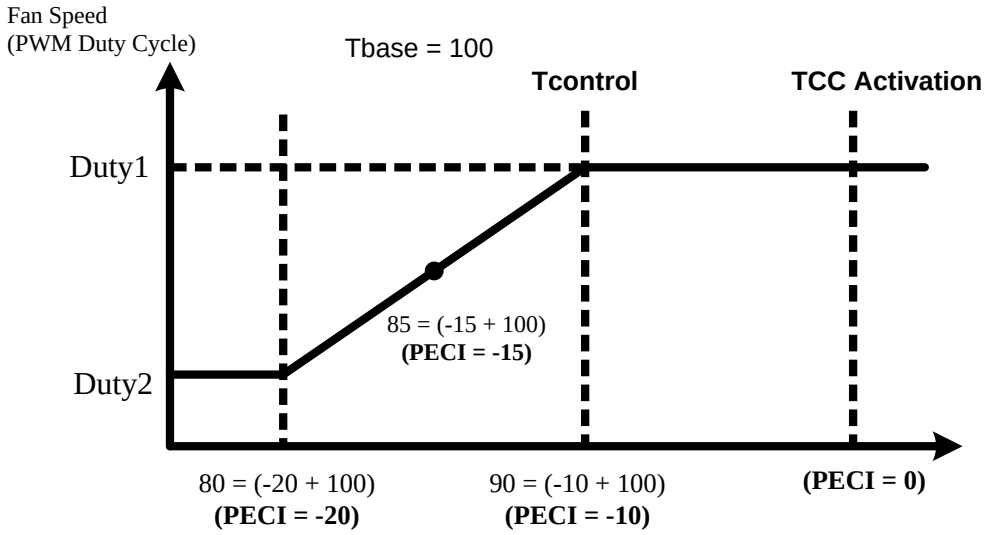


Figure 8-9 Temperature and Fan Speed Relation after Tbase Offsets

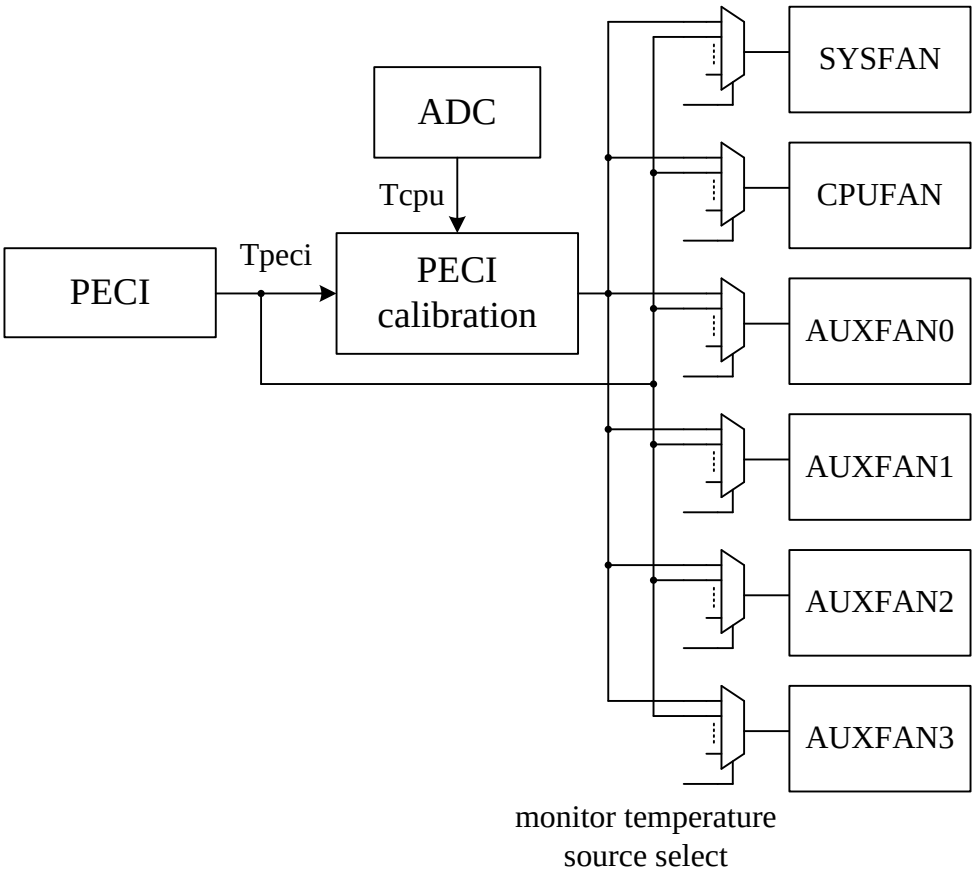
Assuming Tbase is set to 100 and the PECI temperature is -15 , the real-time temperature value to the fan control circuit will be 85 (-15 + 100). The value of 55 (hex) will appear in the relevant real-time temperature register.

While using Smart Fan control function of NCT6796D, BIOS/software can include Tbase in determining the thresholds (limits). In this example, assuming Tcontrol is -10 and Tbase is set to 100 (1), the threshold temperature value corresponding to the “100% fan duty-cycle” event is 90 (-10+100). The value of 5A (hex) should be written to the relevant threshold register.

Tcontrol is typically -10 to -20 for PECI-enabled CPUs. Base on that, a value of 85 ~100 for Tbase could be set for proper operation of the fan control circuit. This recommendation is applicable for most designs. In general, the concept presented in this section could be used to determine the optimum value of Tcontrol to match the specific application.

8.7.1 PECI Calibration

NCT6796D support PECI calibration to adjust the temperature read from CPU to thermistor because the source of thermistor is more accurate than PECI. We have several register for user to set. Bank4 Index FAh, FBh [0] is the enable bit for two agents. If user disable the function, the output will be the original source of PECI. Index FAh, FBh [7:4] is interval time for each calibrate, for example, every 0.1 sec (default) will calibrate again. Index F8h, F9h [7:3] is the max number of update times, number = 0 means only update 1 times. Index F8h, F9h [2:0] is the unit step, unit = 0 means 1 degree. Index F4h, F5h is the result of calibration. We have the overflow and underflow mechanism to protect the system.


ADC
Tcpu
PECI
Tpeci
PECI calibration
SYSFAN
CPUFAN
AUXFAN0
AUXFAN1
AUXFAN2
AUXFAN3
monitor temperature source select

8.8 Fan Speed Measurement and Control

This section is divided into two parts, one to measure the speed and one to control the speed.

8.8.1 Fan Speed Reading

The fan speed reading at:

	FAN COUNT READING 13-bit		FAN RPM READING 16-bit	
	[12:5]	[4:0]	[15:8]	[7:0]
SYSFANIN	Bank4, indexB0	Bank4, indexB1	Bank4, indexC0	Bank4, indexC1
CPUFANIN	Bank4, indexB2	Bank4, indexB3	Bank4, indexC2	Bank4, indexC3
AUXFANIN0	Bank4, indexB4	Bank4, indexB5	Bank4, indexC4	Bank4, indexC5
AUXFANIN1	Bank4, indexB6	Bank4, indexB7	Bank4, indexC6	Bank4, indexC7
AUXFANIN2	Bank4, indexB8	Bank4, indexB9	Bank4, indexC8	Bank4, indexC9
AUXFANIN3	Bank4, indexBA	Bank4, indexBB	Bank4, indexCA	Bank4, indexCB
AUXFANIN4	Bank4, indexCC	Bank4, indexCD	Bank4, indexCE	Bank4, indexCF

8.8.2 Fan Speed Calculation by Fan Count Reading

In 13-bit fan count reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count}$$

8.8.3 Fan Speed Calculation by Fan RPM Reading

In 16-bit fan RPM reading, please read high byte first then low byte.

Fan speed RPM can be evaluated by translating 16-bit RPM reading from hexadecimal to decimal.

Register reading 0x09C4h = 2500 RPM

8.8.4 Fan Speed Control

The NCT6796D has seven output pins for fan control, Only SYSFANOUT offers PWM duty cycle and DC voltage to control the fan speed.

	SYSFANOUT	CPUFANOUT	AUXFANOUT0
Output Type Select	Bank0, index04 bit0 **0: PWM output** **1: DC output (default)**	**Only PWM output**	**Only PWM output**
Output Type Select	CR24 bit4	CR24 bit3	CR24 bit5

(in PWM output)		0: open-drain (default) 1: push-pull	0: open-drain (default) 1: push-pull	0: open-drain (default) 1: push-pull
PWM Output Freqency		Bank0, Index00	Bank0, Index02	Bank0, Index10
Fan Control Mode Select		Bank1, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank2, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank3, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV
Output Value (write)	**PWM output (Duty)**	Bank1, index09 bit[7:0]	Bank2, index09 bit[7:0]	Bank3, index09 bit[7:0]
	DC output (Voltage)	Bank1, index09 bit[7:2]		
Current Output Value (read only)		Bank0, index01	Bank0, index03	Bank0, index11

		AUXFANOUT1	**AUXFANOUT2**	**AUXFANOUT3**	**AUXFANOUT4**
Output Type Select		**Only PWM output**	**Only PWM output**	**Only PWM output**	**Only PWM output**
Output Type Select (in PWM output)		CR24 bit6 0: open-drain (default) 1: push-pull	CR24 bit7 0: open-drain (default) 1: push-pull	CR24 bit1 0: open-drain (default) 1: push-pull	CR25 bit0 0: open-drain (default) 1: push-pull
PWM Output Freqency		Bank0, Index12	Bank0, Index14	Bank0, Index16	Bank0, Index28
Fan Control Mode Select		Bank8, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank9, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	BankA, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	BankB, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV
Output Value (write)	**PWM output (Duty)**	Bank8, index09 bit[7:0]	Bank9, index09 bit[7:0]	BankA, index09 bit[7:0]	BankB, index09 bit[7:0]
	DC output (Voltage)				
Current Output Value (read only)		Bank0, Index13	Bank0, Index15	Bank0, Index17	Bank0, Index29

For PWM, the duty cycle is programmed by eight-bit registers at Bank1 Index 09h for SYSFANOUT, Bank2 Index 09h for CPUFANOUT, Bank3 Index 09h for AUXFANOUT0, Bank8 Index 09h for AUXFANOUT1, Bank9 Index 09h for AUXFANOUT2, BankA Index 09h for AUXFANOUT3 and BankB Index 09h for AUXFANOUT4. The duty cycle can be calculated using the following equation:

$$\text{Duty cycle}(\%) = \frac{\text{Programmed 8-bit Register Value}}{255} \times 100\%$$

The default duty cycle is 7Fh, or 50% for SYSFANOUT, CPUFANOUT, AUXFANOUT0, AUXFANOUT1, AUXFANOUT2, AUXFANOUT3 and AUXFANOUT4.

Note.The default speed of fan output is specified in registers CR[E0h] ~ CR[E4h] and CR[E7h] of Logical Device B, and the AUXFANOUT4 default speed of fan output is specified in register CR[E3h] of Logical Device D.

The PWM clock frequency is programmed at Bank0 Index 00h, Index 02h, Index 10h, Index 12h, Index 14h, Index 16h and Index 28h.

For DC, the NCT6796D has a six bit digital-to-analog converter (DAC) that produces 0 to 2.048 Volts DC. The analog output is programmed at Bank1 Index 09h bit[7:2] for SYSFANOUT. The analog output can be calculated using the following equation:

$$\text{OUTPUT Voltage (V)} = Vref \times \frac{\text{Programmed 6-bit Register Value}}{64}$$

The default value is 111111YY, or nearly 2.048 V, and Y is a reserved bit.

8.8.5 SMART FAN™ Control

The NCT6796D supports various different fan control features:

- SMART FAN™ I (Thermal Cruise & Speed Cruise)
- SMART FAN™ IV
- SMART FAN™ IV Close-Loop Fan Control RPM mode

	SYSFANOUT	CPUFANOUT	AUXFANOUT0
Fan Control Mode Select	Bank1, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank2, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank3, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV

	AUXFANOUT1	AUXFANOUT2	AUXFANOUT3
Fan Control Mode Select	Bank8, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	Bank9, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV	BankA, index02, bit[7:4] 0h: Manual mode(def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV

	AUXFANOUT4
Fan Control Mode Select	BankB, index02, bit[7:4] 0h: Manual mode (def.) 1h: Thermal Cruise 2h: Speed Cruise 4h: SMART FAN IV

8.8.6 Temperature Source & Reading for Fan Control

Select temperature source for each fan control output:

	SYSFANOUT	CPUFANOUT	AUXFANOUT0
Fan Control Temperature Source Select	Bank1, index00 bit[4:0] Default: SYSTIN	Bank2, index00 bit[4:0] Default: CPUTIN	Bank3, index00 bit[4:0] Default: AUXTIN0
Fan Control Temperature Reading	Bank0, index73 & Bank0, index74 bit7	Bank0, index75 & Bank0, index76 bit7	Bank0, index77 & Bank0, index78 bit7

	AUXFANOUT1	AUXFANOUT2	AUXFANOUT3
Fan Control Temperature Source Select	Bank8, index00 bit[4:0] Default: AUXTIN0	Bank9, index00 bit[4:0] Default: AUXTIN0	BankA, index00 bit[4:0] Default: AUXTIN0
Fan Control Temperature Reading	Bank0, index79 & Bank0, index7A bit7	Bank0, index7B & Bank0, index7C bit7	Bank0, index7D & Bank0, index7E bit7

	AUXFANOUT4
Fan Control Temperature Source Select	BankB, index00 bit[4:0] Default: AUXTIN0
Fan Control Temperature Reading	Bank4, indexA0 & Bank4, index9E bit6

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

8.9 SMART FAN™ I

8.9.1 Thermal Cruise Mode

Thermal Cruise mode controls the fan speed to keep the temperature in a specified range. First, this range is defined in BIOS by a temperature and the interval (e.g., 55 °C ± 3 °C). As long as the current temperature remains below the low end of this range (i.e., 52 °C), the fan is off. Once the temperature exceeds the low end, the fan turns on at a speed defined in BIOS (e.g., 20% output). Thermal Cruise mode then controls the fan output according to the current temperature. Three conditions may occur:

(1) If the temperature still exceeds the high end, fan output increases slowly. If the fan is operating at full speed but the temperature still exceeds the high end, a warning message is issued to protect the system.

(2) If the temperature falls below the high end (e.g., 58°C) but remains above the low end (e.g., 52 °C), fan output remains the same.
(3) If the temperature falls below the low end (e.g., 52 °C), fan output decreases slowly to zero or to a specified “stop value”.

This “stop value” is enabled by the Bank1, Index00h, Bit7 for SYSFANOUT; Bank2, Index00h, Bit7 for CPUFANOUT; Bank3, Index00h, Bit7 for AUXFANOUT0; Bank8, Index00h, Bit7 for AUXFANOUT1; Bank9, Index00h, Bit7 for AUXFANOUT2; BankA, Index00h, Bit7 for AUXFANOUT3; BankB, Index00h, Bit7 for AUXFANOUT4.
The “stop value” itself is separately specified in Bank1 Index05h, Bank2 Index05h, Bank3 Index05h, Bank8 Index05h, Bank9 Index05h, BankA Index05h and BankB Index05h.

The “stop time” means fan remains at the stop value for the period of time also separately defined in Bank1 Index07h, Bank2 Index07h, Bank3 Index07h, Bank8 Index07h, Bank9 Index07h, BankA Index07h and BankB Index07h.

Note. The function only support for Thermal Cruise Mode.

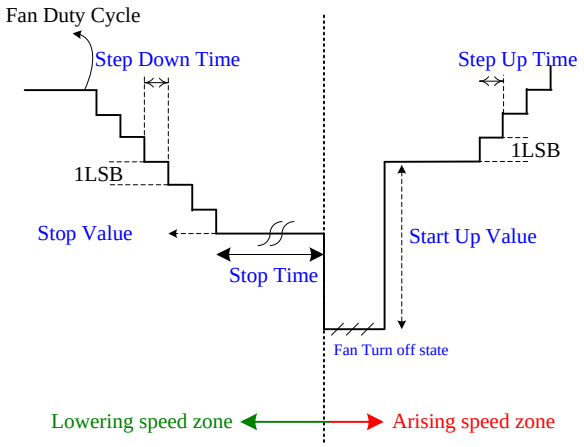


Figure 8-11 Thermal Cruise™ Mode Parameters Figure

In general, Thermal Cruise mode means

- If the current temperature is higher than the high end, increase the fan speed.
- If the current temperature is lower than the low end, decrease the fan speed.
- Otherwise, keep the fan speed the same.

The following figures illustrate two examples of Thermal Cruise mode.

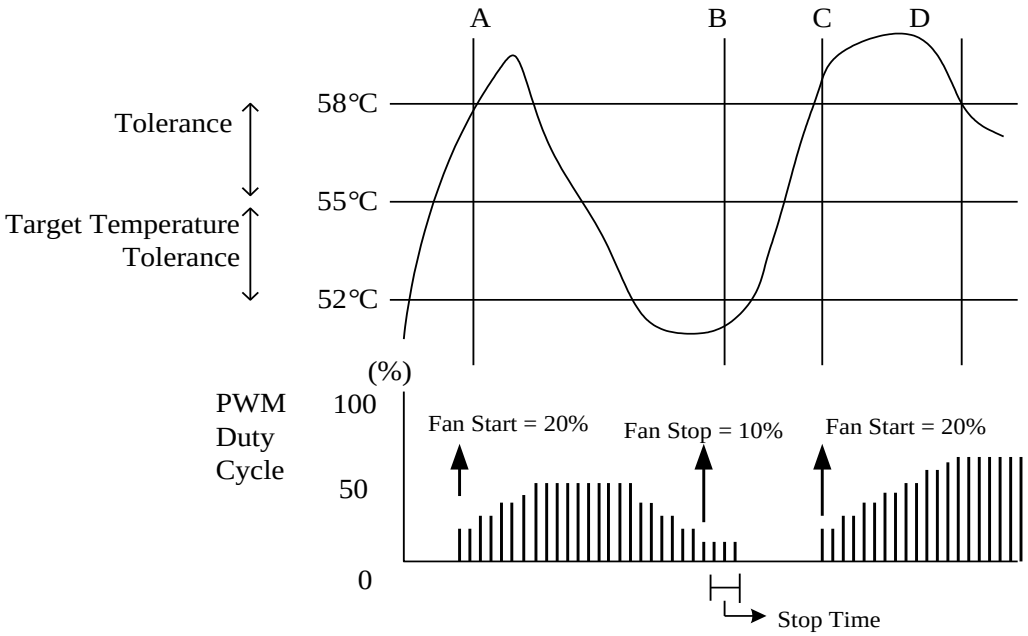


Figure 8-12 Mechanism of Thermal Cruise™ Mode (PWN Duty Cycle)

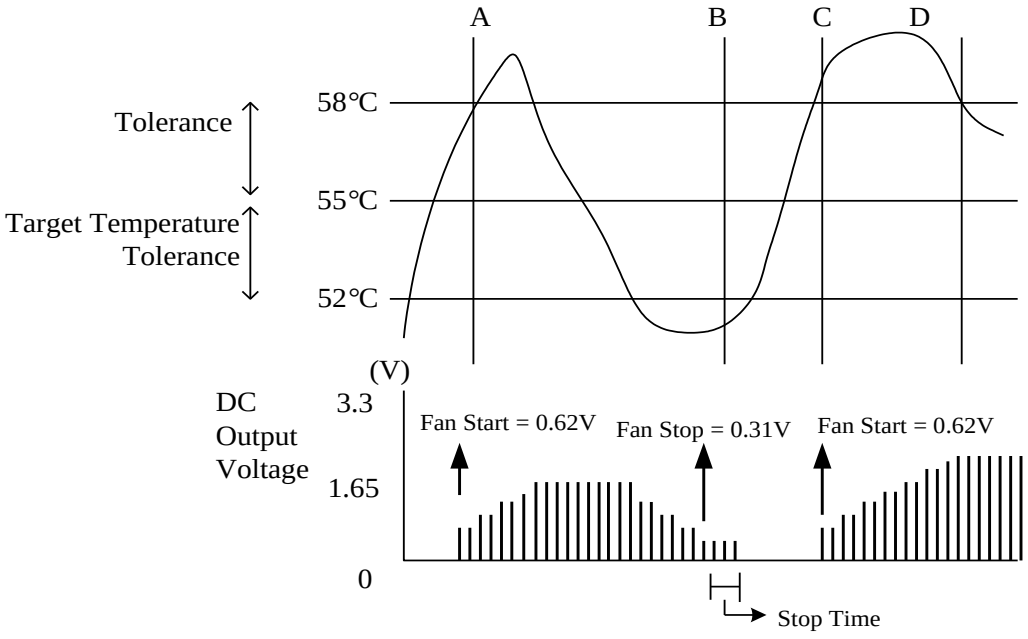


Figure 8-13 Mechanism of Thermal Cruise™ Mode (DC Output Voltage)

8.9.2 Speed Cruise Mode

Speed Cruise mode keeps the fan speed in a specified range. First, this range is defined in BIOS by a fan speed count (the amount of time between clock input signals, not the number of clock input signals in a period of time) and an interval (e.g., 160 ± 10). As long as the fan speed count is in the specified range, fan output remains the same. If the fan speed count is higher than the high end (e.g., 170), fan output increases to make the count lower. If the fan speed count is lower than the low end (e.g., 150), fan output decreases to make the count higher. One example is illustrated in this figure.

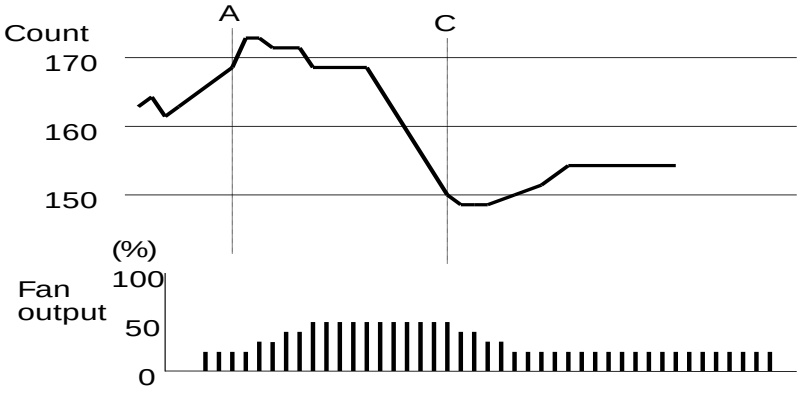


Figure 8-14 Mechanism of Fan Speed Cruise™ Mode

The following tables show current temperatures, fan output values and the relative control registers at Thermal Cruise and Fan Speed mode.

Table 8-2 Relative Registers – at Thermal CruiseTM Mode

THERMAL CRUISE MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP- UP TIME	STEP-DOWN TIME
SYSFANOUT	Bank 1, index 01h bit[7:0]	Bank 1, index 02h Bit[2:0]	Bank 1, index 06h	Bank 1, index 05h	Bank 1, Index 00h, bit7	Bank 1, index 07h	Bank 1, index 03h	Bank 1, index 04h
CPUFANOUT	Bank 2, index 01h bit[7:0]	Bank 2, index 02h Bit[2:0]	Bank 2, index 06h	Bank 2, index 05h	Bank 2, Index 00h, bit7	Bank 2, index 07h	Bank 2, index 03h	Bank 2, index 04h
AUXFANOUT0	Bank 3, index 01h bit[7:0]	Bank 3, index 02h Bit[2:0]	Bank 3, index 06h	Bank 3, index 05h	Bank 3, Index 00h, bit7	Bank 3, index 07h	Bank 3, index 03h	Bank 3, index 04h
AUXFANOUT1	Bank 8, index 01h bit[7:0]	Bank 8, index 02h Bit[2:0]	Bank 8, index 06h	Bank 8, index 05h	Bank 8, Index 00h, bit7	Bank 8, index 07h	Bank 8, index 03h	Bank 8, index 04h
AUXFANOUT2	Bank 9, index 01h bit[7:0]	Bank 9, index 02h Bit[2:0]	Bank 9, index 06h	Bank 9, index 05h	Bank 9, Index 00h, bit7	Bank 9, index 07h	Bank 9, index 03h	Bank 9, index 04h
AUXFANOUT3	Bank A, index 01h bit[7:0]	Bank A, index 02h Bit[2:0]	Bank A, index 06h	Bank A, index 05h	Bank A, Index 00h, bit7	Bank A, index 07h	Bank A, index 03h	Bank A, index 04h
AUXFANOUT4	Bank B, index 01h bit[7:0]	Bank B, index 02h Bit[2:0]	Bank B, index 06h	Bank B, index 05h	Bank B, Index 00h, bit7	Bank B, index 07h	Bank B, index 03h	Bank B, index 04h

THERMAL CRUISE MODE	TARGET TEMPERATURE	TOLERANCE	START-UP VALUE	STOP VALUE	KEEP MIN. FAN OUTPUT VALUE	STOP TIME	STEP- UP TIME	STEP-DOWN TIME

THERMAL CRUISE MODE	CRITICAL TEMPERATURE	ENABLE THERMAL CRUISE MODE
SYSFANOUT	Bank 1, index 35h	Bank 1, Index 02h, bit[7:4] = 01h
CPUFANOUT	Bank 2, Index 35h	Bank 2, Index 02h, bit[7:4] = 01h
AUXFANOUT0	Bank 3, Index 35h	Bank 3, Index 02h, bit[7:4] = 01h
AUXFANOUT1	Bank 8, Index 35h	Bank 8, Index 02h, bit[7:4] = 01h
AUXFANOUT2	Bank 9, Index 35h	Bank 9, Index 02h, bit[7:4] = 01h
AUXFANOUT3	Bank A, Index 35h	Bank A, Index 02h, bit[7:4] = 01h
AUXFANOUT4	Bank B, Index 35h	Bank B, Index 02h, bit[7:4] = 01h

Table 8-3 Relative Registers – at Speed CruiseTM Mode

SPEED CRUISE MODE	TARGET-SPEED COUNT_L	TARGET-SPEED COUNT_H	TOLERANCE_L	TOLERANCE2_H	STEP-UP TIME	STEP-DOWN TIME	STEP-UP VALUE	STEP-DOWN VALUE	ENABLE SPEED CRUISE MODE
SYSFANOUT	Bank 1, Index 01h	Bank 1, Index 0C bit[3:0]	Bank 1, Index 02 bit[2:0]	Bank 1, Index 0C bit[6:4]	Bank 1, Index 03h	Bank 1, Index 04h	Bank1, Index66 Bit[7:4]	Bank1, Index66 Bit[3:0]	Bank 1, Index 02h bit[7:4] = 02h
CPUFANOUT	Bank 2, Index 01h	Bank 2, Index 0C bit[3:0]	Bank 2, Index 02 bit[2:0]	Bank 2, Index 0C bit[6:4]	Bank 2, Index 03h	Bank 2, Index 04h	Bank2, Index66 Bit[7:4]	Bank2, Index66 Bit[3:0]	Bank 2, Index 02h bit[7:4] = 02h

SPEED CRUISE MODE	TARGET-SPEED COUNT_L	TARGET-SPEED COUNT_H	TOLERANCE_L	TOLERANCE2_H	STEP-UP TIME	STEP-DOWN TIME	STEP-UP VALUE	STEP-DOWN VALUE	ENABLE SPEED CRUISE MODE
AUXFANOUT0	Bank 3, Index 01h	Bank 3, Index 0C bit[3:0]	Bank 3, Index 02 bit[2:0]	Bank 3, Index 0C bit[6:4]	Bank 3, Index 03h	Bank 3, Index 04h	Bank3, Index66 Bit[7:4]	Bank3, Index66 Bit[3:0]	Bank 3, Index 02h bit[7:4] = 02h
AUXFANOUT1	Bank 8, Index 01h	Bank 8, Index 0C bit[3:0]	Bank 8, Index 02 bit[2:0]	Bank 8, Index 0C bit[6:4]	Bank 8, Index 03h	Bank 8, Index 04h	Bank8, Index66 Bit[7:4]	Bank8, Index66 Bit[3:0]	Bank 8, Index 02h bit[7:4] = 02h
AUXFANOUT2	Bank 9, Index 01h	Bank 9, Index 0C bit[3:0]	Bank 9, Index 02 bit[2:0]	Bank 9, Index 0C bit[6:4]	Bank 9, Index 03h	Bank 9, Index 04h	Bank9, Index66 Bit[7:4]	Bank9, Index66 Bit[3:0]	Bank 9, Index 02h bit[7:4] = 02h
AUXFANOUT3	Bank A, Index 01h	Bank A, Index 0C bit[3:0]	Bank A, Index 02 bit[2:0]	Bank A, Index 0C bit[6:4]	Bank A, Index 03h	Bank A, Index 04h	BankA, Index66 Bit[7:4]	BankA, Index66 Bit[3:0]	Bank A, Index 02h bit[7:4] = 02h
AUXFANOUT4	Bank B, Index 01h	Bank B, Index 0C bit[3:0]	Bank B, Index 02 bit[2:0]	Bank B, Index 0C bit[6:4]	Bank B, Index 03h	Bank B, Index 04h	BankB, Index66 Bit[7:4]	BankB, Index66 Bit[3:0]	Bank B, Index 02h bit[7:4] = 02h

8.10 SMART FAN™ IV & Close Loop Fan Control Mode

SMART FAN™ IV and Close Loop Fan Control Mode offer 3 slopes to control the fan speed.

Set **Critical Temperature, Bank1 Index 35_{HEX} , Bank2 Index 35_{HEX} , Bank3 Index 35_{HEX} , Bank8 Index 35_{HEX}, Bank9 Index 35_{HEX}, BankA Index 35_{HEX}.**

- Set the **Relative Register-at SMART FAN™ IV Control Mode Table**
  If fan control mode is set as Close Loop Fan Control, the unit step is 50RPM. So the maximum controllable RPM is 50*255=12,750RPM.
  If Enable RPM High Mode (Bank6 index6 Bit0), unit is 100RPM.
- Set Tolerance **of Target Temperature, Bank1 Index 02_{HEX} bit[2:0], Bank2 Index 02_{HEX} bit[2:0], Bank3 Index 02_{HEX} bit[2:0], Bank8 Index 02_{HEX} bit[2:0], Bank9 Index 02_{HEX} bit[2:0], BankA Index 02_{HEX} bit[2:0].**

The 3 slopes can be obtained by setting FanDuty1/RPM1~FanDuty4/RPM4 and T1~T4 through the registers. When the temperature rises, FAN Output will calculate the target FanDuty/RPM based on the current slope. For example, assuming Tx is the current temperature and Ty is the target, then

The slope:

$$X3 = \frac{(FanDuty4/RPM4) - (FanDuty3/RPM3)}{(T4 - T3)}$$

Fan Output:

$$Target\ FanDuty\ or\ RPM = (FanDuty3\ or\ RPM3) + (Tx - T3) \cdot X3$$

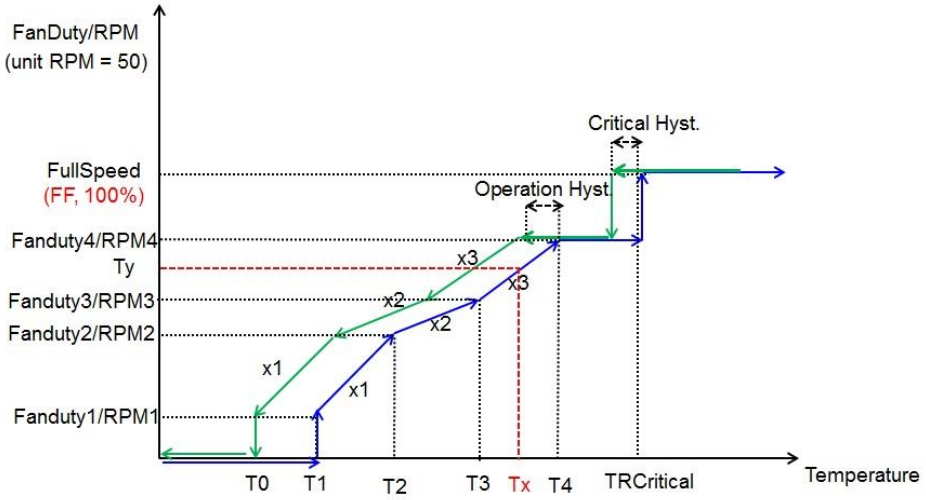


Figure 8-15 SMART FAN™ IV & Close Loop Fan Control Mechanism

Table 8-4 Relative Register-at SMART FAN™ IV Control Mode

DESCRIPTION	T1	T2	T3	T4
SYSFANOUT	Bank 1, Index 21h	Bank 1, Index 22h	Bank 1, Index 23h	Bank 1, Index 24h
CPUFANOUT	Bank 2, Index 21h	Bank 2, Index 22h	Bank 2, Index 23h	Bank 2, Index 24h
AUXFANOUT0	Bank 3, Index 21h	Bank 3, Index 22h	Bank 3, Index 23h	Bank 3, Index 24h
AUXFANOUT1	Bank 8, Index 21h	Bank 8, Index 22h	Bank 8, Index 23h	Bank 8, Index 24h
AUXFANOUT2	Bank 9, Index 21h	Bank 9, Index 22h	Bank 9, Index 23h	Bank 9, Index 24h

DESCRIPTION	T1	T2	T3	T4
AUXFANOUT3	Bank A, Index 21h	Bank A, Index 22h	Bank A, Index 23h	Bank A, Index 24h
AUXFANOUT4	Bank B, Index 21h	Bank B, Index 22h	Bank B, Index 23h	Bank B, Index 24h
DESCRIPTION	**FD1/PWM1**	**FD2/PWM2**	**FD3/PWM3**	**FD4/PWM4**
SYSFANOUT	Bank 1, Index 27h	Bank 1, Index 28h	Bank 1, Index 29h	Bank 1, Index 2Ah
CPUFANOUT	Bank 2, Index 27h	Bank 2, Index 28h	Bank 2, Index 29h	Bank 2, Index 2Ah
AUXFANOUT0	Bank 3, Index 27h	Bank 3, Index 28h	Bank 3, Index 29h	Bank 3, Index 2Ah
AUXFANOUT1	Bank 8, Index 27h	Bank 8, Index 28h	Bank 8, Index 29h	Bank 8, Index 2Ah
AUXFANOUT2	Bank 9, Index 27h	Bank 9, Index 28h	Bank 9, Index 29h	Bank 9, Index 2Ah
AUXFANOUT3	Bank A, Index 27h	Bank A, Index 28h	Bank A, Index 29h	Bank A, Index 2Ah
AUXFANOUT4	Bank B, Index 27h	Bank B, Index 28h	Bank B, Index 29h	Bank B, Index 2Ah

DESCRIPTION	CRITICAL TEMPERATURE (TR Critical)	CRITICAL TOLERANCE (Critical Hyst)	TEMPERATURE TOLERANCE (Operation Hyst)	ENABLE RPM MODE	RPM TOLERANCE	ENABLE RPM HIGH MODE
SYSFANOUT	Bank 1, Index 35h	Bank 1, Index 38h, bit[2:0]	Bank 1, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit0	Bank 6, index 01h Bit[3:0]	Bank 6, Index 06h, Bit0
CPUFANOUT	Bank 2, Index 35h	Bank 2, Index 38h, bit[2:0]	Bank 2, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit1	Bank 6, index 02h Bit[3:0]	Bank 6, Index 06h, Bit1
AUXFANOUT0	Bank 3, Index 35h	Bank 3, Index 38h, bit[2:0]	Bank 3, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit2	Bank 6, index 03h Bit[3:0]	Bank 6, Index 06h, Bit2
AUXFANOUT1	Bank 8, Index 35h	Bank 8, Index 38h, bit[2:0]	Bank 8, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit3	Bank 6, index 04h Bit[3:0]	Bank 6, Index 06h, Bit3
AUXFANOUT2	Bank 9, Index 35h	Bank 9, Index 38h, bit[2:0]	Bank 9, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit4	Bank 6, index 05h Bit[3:0]	Bank 6, Index 06h, Bit4

AUXFANOUT3	Bank A, Index 35h	Bank A, Index 38h, bit[2:0]	Bank A, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit5	Bank 6, index 23h Bit[3:0]	Bank 6, Index 06h, Bit5
AUXFANOUT4	Bank B, Index 35h	Bank B, Index 38h, bit[2:0]	Bank B, Index 02h, bit[2:0]	Bank 6, Index 00h, Bit6	Bank 6, index 24h Bit[3:0]	Bank 6, Index 06h, Bit6

DESCRIPTION	STEP-UP TIME	STEP-DOWN TIME	STEP UP VALUE	STEP DOWN VALUE	Enable SMART FAN IV	ENABLE CRITICAL DUTY	CRITICAL DUTY
SYSFANOUT	Bank 1, index 03h	Bank 1, index 04h	Bank1, index66 Bit[7:4]	Bank1, index66 Bit[3:0]	Bank 1,Index 02h bit[7:4] = 04h	Bank 1, Index 36h, Bit0	Bank 1, index 37h
CPUFANOUT	Bank 2, index 03h	Bank 2, index 04h	Bank2, index66 Bit[7:4]	Bank2, index66 Bit[3:0]	Bank 2,Index 02h bit[7:4] = 04h	Bank 2, Index 36h, Bit0	Bank 2, index 37h
AUXFANOUT0	Bank 3, index 03h	Bank 3, index 04h	Bank3 index66 Bit[7:4]	Bank3, index66 Bit[3:0]	Bank 3,Index 02h bit[7:4] = 04h	Bank 3, Index 36h, Bit0	Bank 3, index 37h
AUXFANOUT1	Bank 8, Index 03h	Bank 8, Index 04h	Bank8, index66 Bit[7:4]	Bank8, index66 Bit[3:0]	Bank 8,Index 02h bit[7:4] = 04h	Bank 8, Index 36h, Bit0	Bank 8, index 37h
AUXFANOUT2	Bank 9, Index 03h	Bank 9, Index 04h	Bank9, index66 Bit[7:4]	Bank9, index66 Bit[3:0]	Bank 9,Index 02h bit[7:4] = 04h	Bank 9, Index 36h, Bit0	Bank 9, index 37h
AUXFANOUT3	Bank A, Index 03h	Bank A, Index 04h	BankA, index66 Bit[7:4]	BankA, index66 Bit[3:0]	Bank A,Index 02h bit[7:4] = 04h	Bank A, Index 36h, Bit0	Bank A, index 37h
AUXFANOUT4	Bank B, Index 03h	Bank B, Index 04h	BankB, index66 Bit[7:4]	BankB, index66 Bit[3:0]	Bank B,Index 02h bit[7:4] = 04h	Bank B, Index 36h, Bit0	Bank B, index 37h

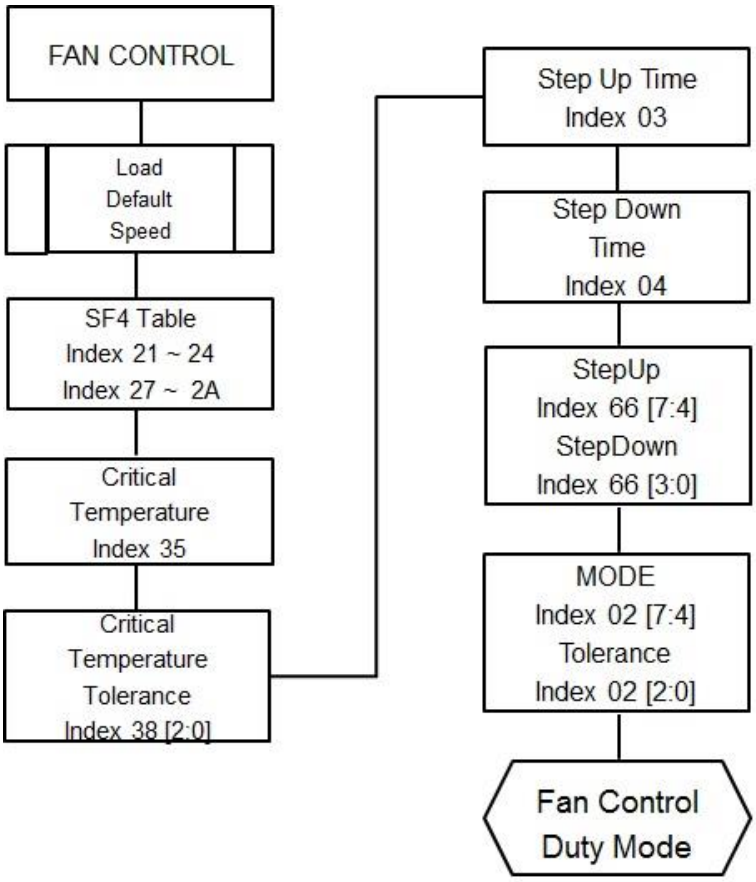


Figure 8-16 Fan Control Duty Mode Programming Flow

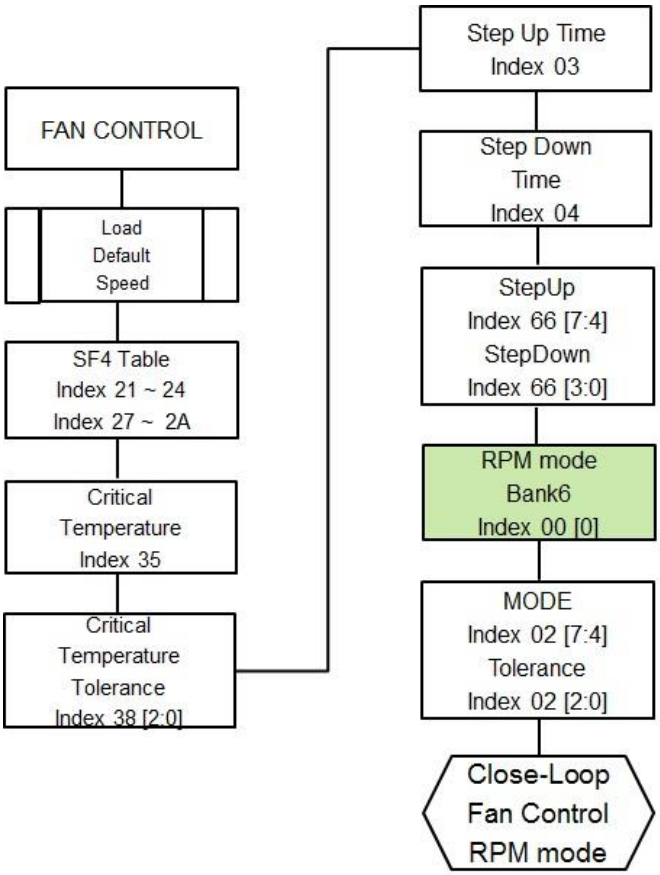


Figure 8-17 Close-Loop Fan Control RPM mode Programming Flow

8.10.1 Step Up Time / Step Down Time

SMART FAN™ IV is designed for the smooth operation of the fan. The Up Time / Down Time register defines the time interval between successive duty increases or decreases. If this value is set too small, the fan will not have enough time to speed up after tuning the duty and sometimes may result in unstable fan speed. On the other hand, if Up Time / Down Time is set too large, the fan may not work fast enough to dissipate the heat.

8.10.2 Fan Output Step

The “Fanout Step” itself is separately specified in Bank1 Index20h bit0 for SYSFANOUT, Bank2 Index20h bit0 for CPUFANOUT, Bank3 Index20h bit0 for AUXFANOUT0, Bank8 Index20h bit0 for AUXFANOUT1, Bank9 Index20h bit0 for AUXFANOUT2, BankA Index20h bit0 for AUXFANOUT3 and BankB Index20h bit0 for AUXFANOUT4.

This example for Fanout Step exposition:

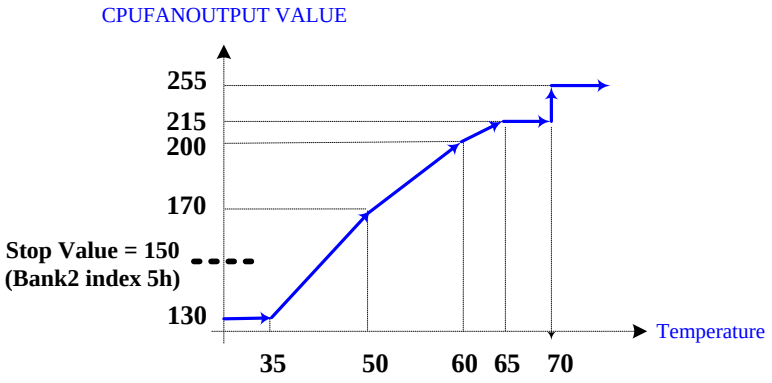


Figure 8-18 CPUFAN SMART FAN™ IV Table Parameters Figure

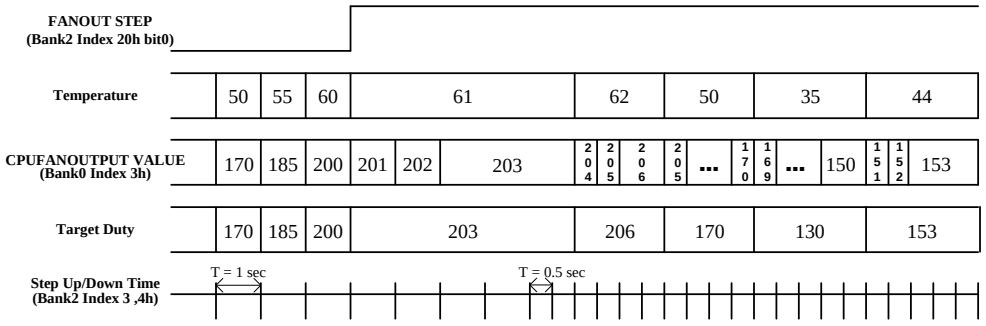


Figure 8-19 Fanout Step Relation of CPUFANOUT

8.10.3 Revolution Pulse Selection

The NCT6796D supports four RPM output of the pulses selection function for different type of FAN which has the character of different pulses per revolution.The others could be set by HM register at Bank6, Index44, Bit1-0 for SYSFANIN; Index45, Bit1-0 for CPUFANIN; Index46, Bit1-0 for AUXFANIN0; Index47, Bit1-0 for AUXFANIN1; Index48, Bit1-0 for AUXFANIN2; Index49, Bit1-0 for AUXFANIN3; Index4F, Bit1-0 for AUXFANIN4. All default value of pulse selection registers are 2 pulses of one revolution.

Setting description for “Pulse Selections Bits”:

00: 4 pulses per revolution
01: 1 pulse per revolution
10: 2 pulses per revolution (default)
11: 3 pulses per revolution

8.10.4 Weight Value Control

The NCT6796D supports weight value control for fan duty output. By register configuration, the results of weight value circuit can be added to the fan duty of SMART FAN™ I or IV and output to the fan. Take CPUFANOUT for example, if SMART FAN™ IV is selected, CPUTIN is the temperature source, and weight value control is enabled, SMART FAN™ IV will calculate the output duty, and weight value circuit will calculate the corresponding weight value based on SYSTIN. As the SYSTIN temperature rises, its corresponding weight value increases. Then, the two values will be summed up and output to CPU fan. In other words, the CPU fan duty is affected not only by the CPUTIN but also the SYSTIN temperature.

Figure 8-20 CPU TEMP and Weight Value Relations shows the relation between the SYSTIN temperature and the weight value. Tolerance setup is offered on each change point to avoid weight value fluctuation resulted from SYSTIN temperature change. The weight value will increase by one weight value step only when the SYSTIN temperature is higher than the point value plus tolerance. Likewise, the weight value decreases by one weight value step only when the SYSTIN temperature is lower than the point value minus tolerance.

Nots：This relative register should not be zero and not support negative temperature.

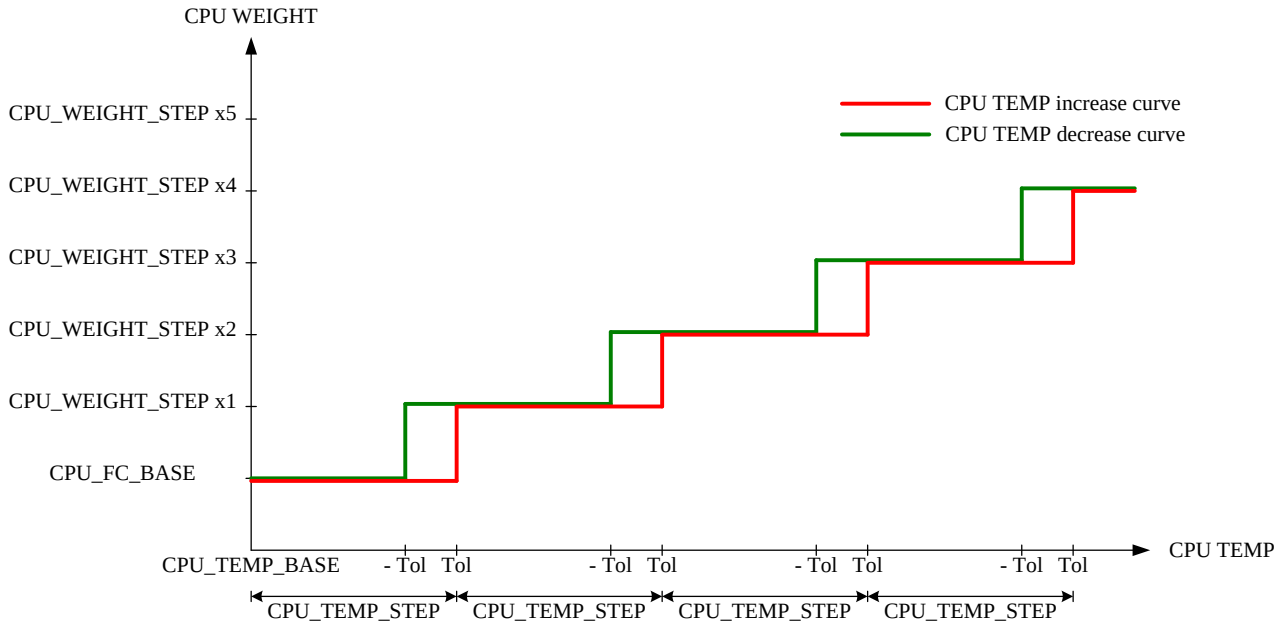


Figure 8-20 CPU TEMP and Weight Value Relations

Table 8-5 Relative Register-at Weight Value Control

DESCRIPTION	ENABLE WEIGHT MODE	WEIGHT TEMPERATURE SOURCE SELECT
CPUFANOUT	Bank 2, Index 39h, bit7	Bank 2, Index 39h, bit[4:0]

DESCRIPTION	TEMP BASE	DUTY BASE	TEMP STEP	TEMP STEP TOLERANCE	WEIGHT STEP
CPUFANOUT	Bank 2, Index 3Dh	Bank 2, Index 3Eh	Bank 2, Index 3Ah	Bank 2, Index 3Bh	Bank 2, Index 3Ch

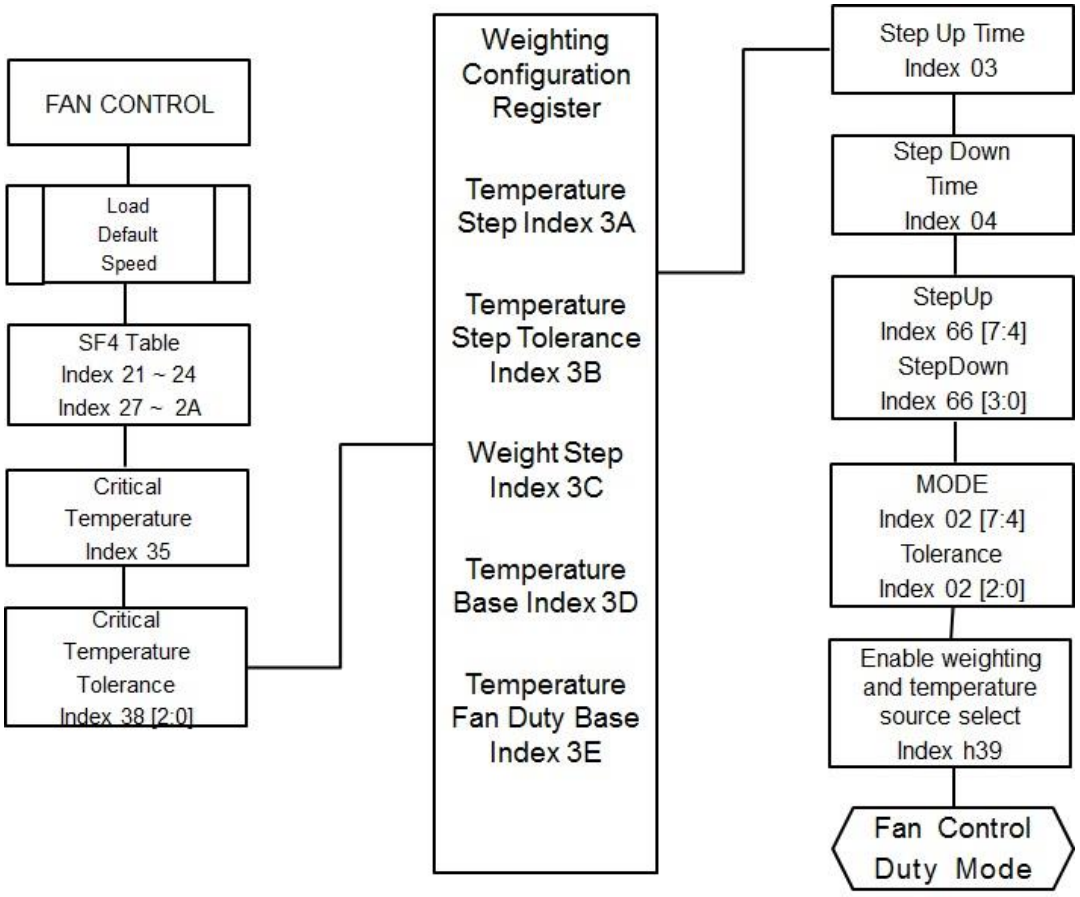


Figure 8-21 Fan Control Weighting Duty Mode Programming Flow

8.10.5 DTS2.0

When current temperature ≥ Tcontrol, it will change from SMART FAN™ IV to DTS2.0, and when current temperature < Tcontrol, it will change from DTS2.0 to SMART FAN™ IV. In DTS2.0, it compares the thermal margin (from PECI) and target thermal margin, when thermal margin > target thermal margin, mean it's over-cooling and duty (RPM) will decrease, when thermal margin < target thermal margin, mean it's poor-cooling and duty (RPM) increase.

Enable thermal margin and T ≥ Tcontrol, thermal margin correspond to duty (RPM) as follow figures

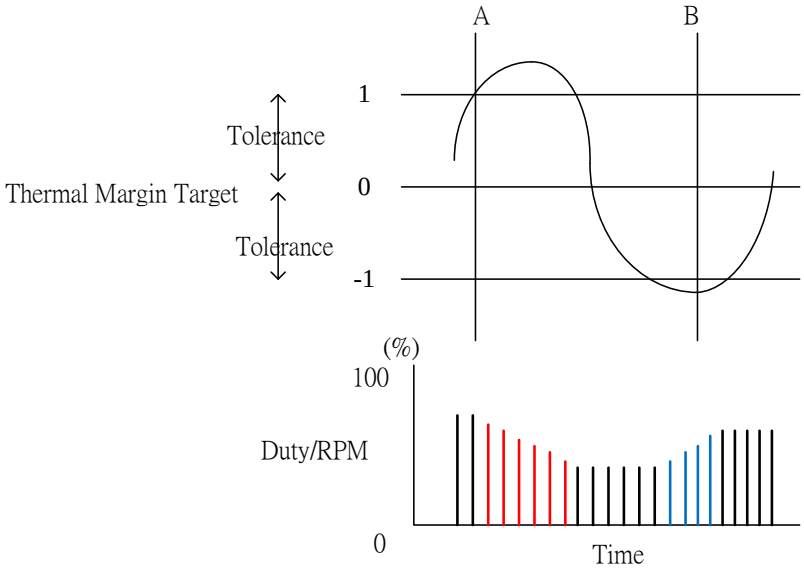


Figure 8-22 (a) Mechanism of thermal Margin

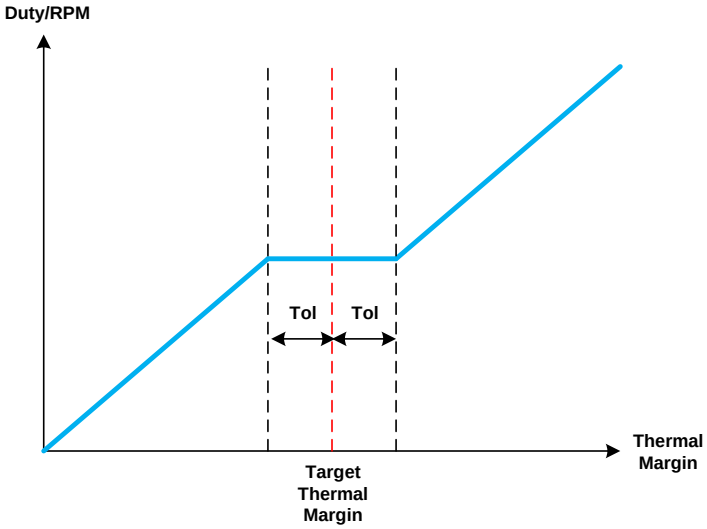


Figure 8-23 (b) Mechanism of thermal Margin

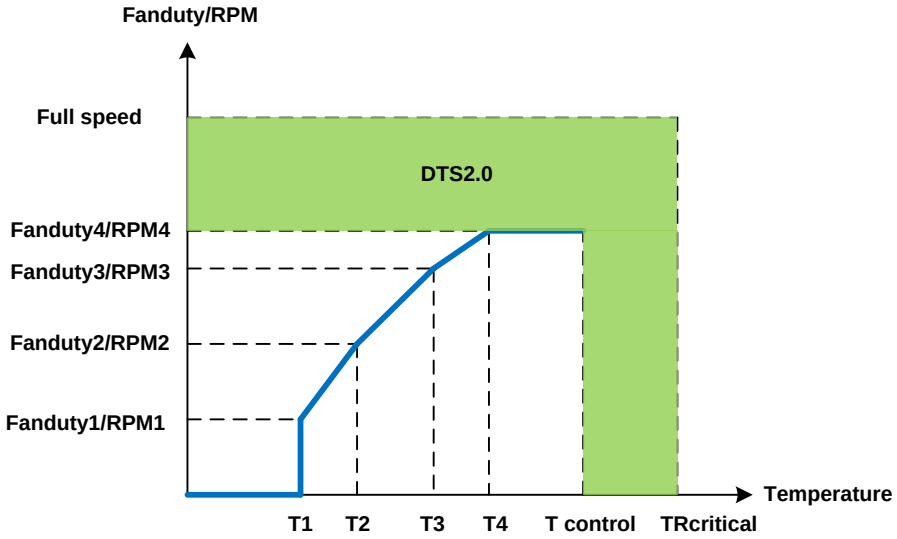


Figure 8-24 DTS2.0 region of SMART FAN™ IV

Table 8-6 Relative Registers – at DTS2.0

DESCRIPTION	THERMAL MARGIN ENABLE	T CONTROL	TARGET THERMAL MARGIN	THERMAL MARGIN TOLERANCE
CPUFANOUT	Bank 2, index 0Dh Bit[0]	Bank 2, index 0Fh	Bank2, index01	Bank2, index0D Bit[4:2]
AUXFANOUT0	Bank 3, index 0Dh Bit[0]	Bank 3, index 0Fh	Bank3, index01	Bank3, index0D Bit[4:2]

8.11 Alert and Interrupt

NCT6796D supports 6 Temperature Sensors for interrupt detection depending on selective monitor temperature source.

	SMIOVT1	SMIOVT2	SMIOVT3	SMIOVT4
Temperature source select	Bank6, index21 bit[4:0] default: SYSTIN	Bank6, index22 bit[4:0] default: CPUTIN	BankC, index26 bit[4:0] default: AUXTIN0	BankC, index27 bit[4:0] default: AUXTIN1
Temperature reading (2's complement)	Bank0, index27	Bank1, index50 & index51 bit7	Bank6, index70	Bank6, index72
Temperature High Limit (TOL)	Bank0, index39	Bank1, index55 & index56 bit7	BankC, index1A	BankC, index1B

Temperature Low Limit (THTST)	Bank0, index3A	Bank1, index53 & index54 bit7	BankC, index20	BankC, index21

	SMIOVT5	**SMIOVT6**	**SMIOVT7**	**SMIOVT8**
Temperature source select	BankC, index28 bit[4:0] default: AUXTIN2	BankC, index29 bit[4:0] default: AUXTIN3	BankC, index2A bit[4:0] default: AUXTIN4	BankC, index2B bit[4:0] default: CPUTIN
Temperature reading (2's complement)	Bank6, index74	Bank6, index76	Bank6, index78	Bank6, index7A
Temperature High Limit (TOL)	BankC, index1C	BankC, index1D	BankC, index1E	BankC, index1F
Temperature Low Limit (THTST)	BankC, index22	BankC, index23	BankC, index24	BankC, index25

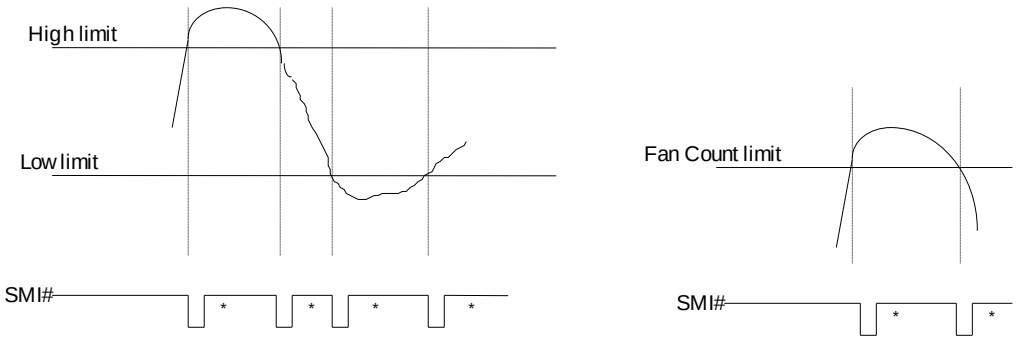
SMIOVT Relative Temperature Registers

8.11.1 SMI# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in HM_SMI# mode or in OVT# mode by setting Configuration Register CR24h, bit 2. In HM_SMI# mode, it can monitor voltages, fan counts, or temperatures.

8.11.2 Voltage SMI# Mode

The SMI# pin can create an interrupt if a voltage rises above a specified high limit or falls below a specified low limit. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

Figure 8-25 SMI Mode of Voltage and Fan Inputs

8.11.3 Fan SMI# Mode

The SMI# pin can create an interrupt if a fan count crosses a specified fan limit (rises above it or falls below it). This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This mode is illustrated in the figure above.

8.11.4 Temperature SMI# Mode

The SMI# pin can create interrupts that depend on the temperatures measured by SYSTIN, CPUTIN, and AUXTIN0.

8.11.4.1. Temperature Sensor 1 SMI# Interrupt (Default: SYSTIN)

8.11.4.2. Temperature Sensor 3 SMI# Interrupt (Default: AUXTIN0)

8.11.4.3. Temperature Sensor 4 SMI# Interrupt (Default: AUXTIN1)

8.11.4.4. Temperature Sensor 5 SMI# Interrupt (Default: AUXTIN2)

8.11.4.5. Temperature Sensor 6 SMI# Interrupt (Default: AUXTIN3)

8.11.4.6. Temperature Sensor 7 SMI# Interrupt (Default: AUXTIN4)

8.11.4.7. Temperature Sensor 8 SMI# Interrupt (Default: CPUTIN)

The SMI# pin has four interrupt modes with Temperature Sensor 1, Sensor 3, Sensor 4, Sensor 5, Sensor 6, Sensor 7, and Sensor 8.

(1) Shut-down Interrupt Mode

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

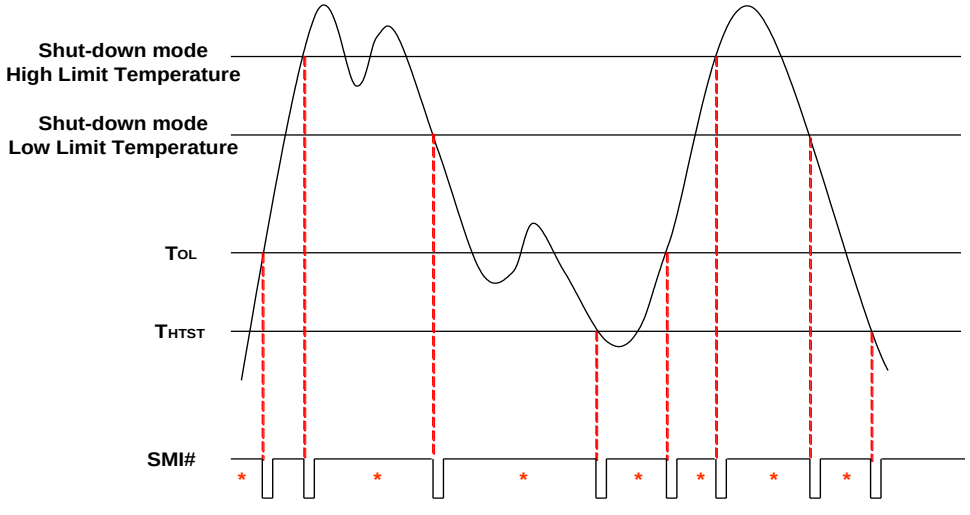
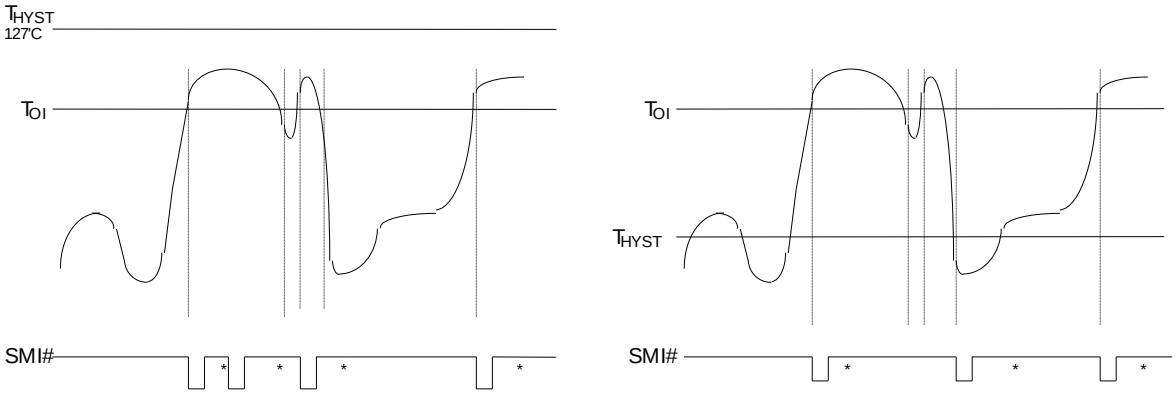


Figure 8-26 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting T_{HYST} (Temperature Hysteresis) to 127°C.

In this mode, the SMI# pin can create an interrupt as long as the current temperature rises above T_O (Over Temperature). This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. If the interrupt is reset, the SMI# pin continues to create interrupts until the temperature goes below T_O. This is illustrated in the figure below.



*Interrupt Reset when Interrupt Status Registers are read

Comparator Interrupt Mode Two-Times Interrupt Mode

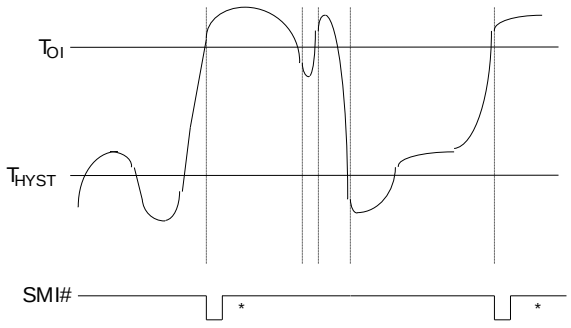
Figure 8-27 SMI Mode of Sensor1 I

(3) Two-Times Interrupt Mode

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

(4) One-Times Interrupt Mode

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the following figure.



*Interrupt Reset when Interrupt Status Registers are read

One-Time Interrupt Mode

Figure 8-28 SMI Mode of Sensor1 II

8.11.4.8. SMI# Interrupt of Temperature Sensor 2

The SMI# pin has 3 interrupt modes with Temperature Sensor 2.

(1) Shut-down Interrupt Mode

This mode is enabled by Bank0 Index 40h, bit5 to one for Temperature Sensor 2.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_{OL} or Shut-down mode high limit temperature, and when the current temperature falls below T_{HYST} or Shut-down mode low limit temperature. Once the temperature rises above T_{OL}, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_{OL}, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts, except the first time current temperature rises above Shut-down mode high limit temperature. This is illustrated in the following figure.

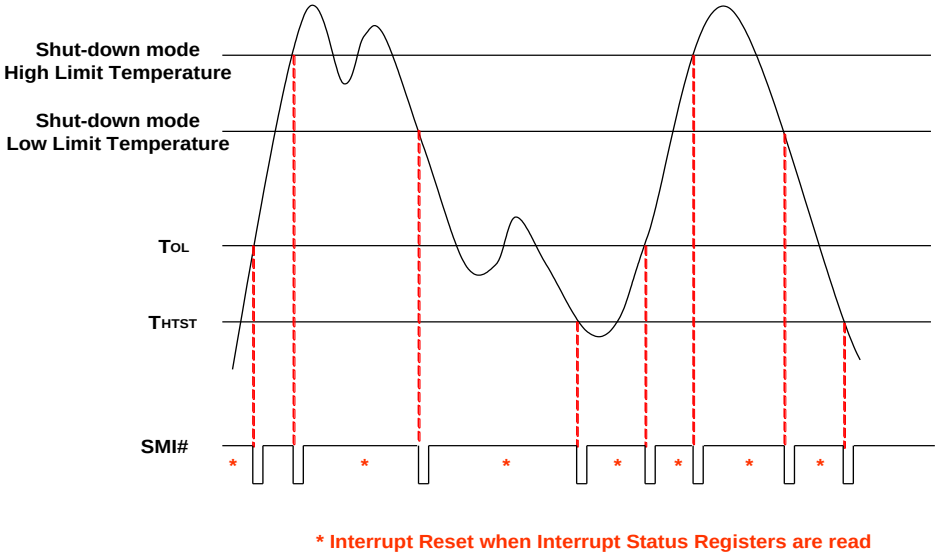
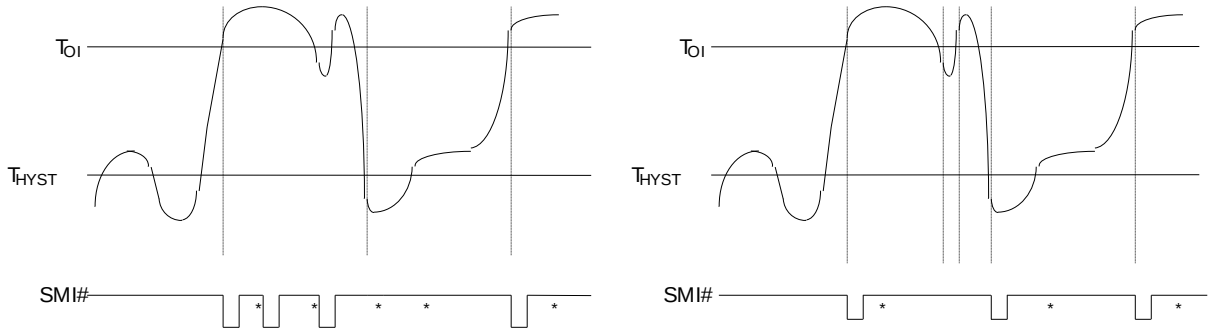


Figure 8-29 Shut-down Interrupt Mode

(2) Comparator Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to one.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O (Over Temperature) and continues to create interrupts until the temperature falls below T_{HYST}. This interrupt can be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure below.



*Interrupt Reset when Interrupt Status Registers are read

Comparator Interrupt Mode Two-Times Interrupt Mode

Figure 8-30 SMI Mode of Sensor2

(3) Two-Times Interrupt Mode

This mode is enabled by setting Bank0 Index 4Ch, bit 6, to zero.

In this mode, the SMI# pin can create an interrupt when the current temperature rises above T_O or when the current temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers, or subsequent events do not generate interrupts. This is illustrated in the figure above.

Table 8-7 Relative Register of SMI functions

	SHUTDOWN MODE	COMPARATOR MODE	TWO-TIME INTERRUPT MODE	ONE-TIME INTERRUPT MODE
SMIOVT1	Bank0,Index40_Bit4 (EN_WS=1) Bank0,Index43 _Bit4(TIN=0) Bank0,Index46 _Bit3 (Shut = 0)	Bank0,Index43_Bit4 (TIN=0) Bank0,Index3A (Thyst = 8'h7F)	Bank0,Index43_Bit4 (TIN=0) Bank0,Index4C_Bit5 (EN_T1_One = 0)	Bank0,Index43_ Bit4 Bank0,Index4C_ Bit5
SMIOVT2	Bank0,Index40_Bit5 (EN_WS=1) Bank0,Index43_ Bit5(TIN=0) Bank0,Index46_ Bit 4 (Shut = 0)	Bank0,Index43_Bit5 (TIN=0) Bank0,Index4C_ Bit6 (T2T3_INT=1)	Bank0,Index43_ Bit5(TIN=0) Bank0,Index4C_ Bit6 (T2T3_INT=0)	
SMIOVT3	BankC,Index09_Bit 0(EN_WS=1) BankC,Index04_ Bit0(TIN=0) BankC,Index05_ Bit0(Shut = 0)	BankC,Index04_ Bit0(TIN=0) BankC,Index20 (Thyst = 8'h7F)	BankC,Index04_ Bit0(TIN=0) BankC,Index0A_Bit 2 (EN_T3_One = 0)	BankC,Index04_ Bit0(TIN=0) BankC,Index0A_ Bit2 (EN_T3_One = 1)
SMIOVT4	BankC,Index09_Bit 1(EN_WS=1) BankC,Index04_ Bit1(TIN=0)	BankC,Index04_ Bit1(TIN=0) BankC,Index21	BankC,Index04_ Bit1(TIN=0) BankC,Index0A_Bit	BankC,Index04_ Bit1(TIN=0) BankC,Index0A_ Bit3

	BankC,Index05_ Bit1(Shut = 0)	(Thyst = 8'h7F)	3 (EN_T4_One = 0)	(EN_T4_One = 1)
SMIOVT5	BankC,Index09_Bit 2(EN_WS=1) BankC,Index04_ Bit2(TIN=0) BankC,Index05_ Bit2(Shut = 0)	BankC,Index04_ Bit2(TIN=0) BankC,Index22 (Thyst = 8'h7F)	BankC,Index04_ Bit2(TIN=0) BankC,Index0A_Bit 4 (EN_T5_One = 0)	BankC,Index04_ Bit2(TIN=0) BankC,Index0A_ Bit4 (EN_T5_One = 1)
SMIOVT6	BankC,Index09_Bit 3(EN_WS=1) BankC,Index04_ Bit3(TIN=0) BankC,Index05_ Bit3(Shut = 0)	BankC,Index04_ Bit3(TIN=0) BankC,Index23 (Thyst = 8'h7F)	BankC,Index04_ Bit3(TIN=0) BankC,Index0A_Bit 5 (EN_T6_One = 0)	BankC,Index04_ Bit3(TIN=0) BankC,Index0A_ Bit5 (EN_T6_One = 1)
SMIOVT7	BankC,Index09_Bit 4(EN_WS=1) BankC,Index04_ Bit4(TIN=0) BankC,Index05_ Bit4(Shut = 0)	BankC,Index04_ Bit4(TIN=0) BankC,Index24 (Thyst = 8'h7F)	BankC,Index04_ Bit4(TIN=0) BankC,Index0A_Bit 6 (EN_T7_One = 0)	BankC,Index04_ Bit4(TIN=0) BankC,Index0A_ Bit6 (EN_T7_One = 1)
SMIOVT8	BankC,Index09_Bit 5(EN_WS=1) BankC,Index04_ Bit5(TIN=0) BankC,Index05_ Bit5(Shut = 0)	BankC,Index04_ Bit5(TIN=0) BankC,Index25 (Thyst = 8'h7F)	BankC,Index04_ Bit5(TIN=0) BankC,Index0A_Bit 7 (EN_T8_One = 0)	BankC,Index04_ Bit5(TIN=0) BankC,Index0A_ Bit7 (EN_T8_One = 1)

Table 8-8 Relative Register of OVT functions

SMIOVT1	SMIOVT2	SMIOVT3	SMIOVT4
Bank0,Index18_Bit6=0 **0:** Disable SMIOVT1 temperature sensor over temperature output **1:** Enable SMIOVT1 temperature sensor over temperature output **Bank0,Index18_Bit4** **0:** Comparator Mode (def.) **1:** Interrupt Mode **Bank0, Index18_Bit0** **0:** Start to monitor the source of SMIOVT1 temperature.	**Bank 0, Index4C_Bit 3** **0:** Disable SMIOVT2 temperature sensor over temperature output **1:** Enable SMIOVT2 temperature sensor over temperature output **Bank 1, Index52_Bit 1** **0:** Comparator Mode (def.) **1:** Interrupt Mode **Bank1, Index52_Bit0** **0:** Start to monitor the source of SMIOVT2 temperature.	**Bank C, Index06_Bit 0** **0:** Disable SMIOVT3 temperature sensor over temperature output **1:** Enable SMIOVT3 temperature sensor over temperature output **Bank C, Index07_Bit 0** **0:** Comparator Mode (def.) **1:** Interrupt Mode **Bank C, Index08_Bit0** **0:** Start to monitor the source of SMIOVT3 temperature.	**Bank C, Index06_Bit 1** **0:** Disable SMIOVT4 temperature sensor over temperature output **1:** Enable SMIOVT4 temperature sensor over temperature output **Bank C, Index07_Bit 1** **0:** Comparator Mode (def.) **1:** Interrupt Mode **Bank C, Index08_Bit1** **0:** Start to monitor the source of SMIOVT4 temperature.

1: Stop monitoring the source of SMIOVT1 temperature. **Bank 0, IndexBE_Bit 4~5** Number of faults to detect before setting OVT# output.	**1:** Stop monitoring the source of SMIOVT2 temperature. **Bank 1, Index52_Bit 3~4** Number of faults to detect before setting OVT# output.	**1:** Stop monitoring the source of SMIOVT3 temperature. **Bank C, Index0C_Bit 0~1** Number of faults to detect before setting OVT# output.	**1:** Stop monitoring the source of SMIOVT4 temperature. **Bank C, Index0C_Bit 2~3** Number of faults to detect before setting OVT# output.

SMIOVT5	SMIOVT6	SMIOVT7	SMIOVT8
Bank C, Index06_Bit 2 **0:** Disable SMIOVT5 temperature sensor over temperature output **1:** Enable SMIOVT5 temperature sensor over temperature output **Bank C, Index07_Bit 2** **0:** Comparator Mode (def.) **1:** Interrupt Mode **Bank C, Index08_Bit2** **0:** Start to monitor the source of SMIOVT5 temperature. **1:** Stop monitoring the source of SMIOVT5 temperature. **Bank C, Index0C_Bit 4~5** Number of faults to detect before setting OVT# output.	**Bank C, Index06_Bit 3** **0:** Disable SMIOVT6 temperature sensor over temperature output **1:** Enable SMIOVT6 temperature sensor over temperature output **Bank C, Index07_Bit 3** **0:** Comparator Mode (def.) **1:** Interrupt Mode **Bank C, Index08_Bit3** **0:** Start to monitor the source of SMIOVT6 temperature. **1:** Stop monitoring the source of SMIOVT6 temperature. **Bank C, Index0C_Bit 6~7** Number of faults to detect before setting OVT# output.	**Bank C, Index06_Bit 4** **0:** Disable SMIOVT7 temperature sensor over temperature output **1:** Enable SMIOVT7 temperature sensor over temperature output **Bank C, Index07_Bit 4** **0:** Comparator Mode (def.) **1:** Interrupt Mode **Bank C, Index08_Bit4** **0:** Start to monitor the source of SMIOVT7 temperature. **1:** Stop monitoring the source of SMIOVT7 temperature. **Bank C, Index0D_Bit 0~1** Number of faults to detect before setting OVT# output.	**Bank C, Index06_Bit 5** **0:** Disable SMIOVT8 temperature sensor over temperature output **1:** Enable SMIOVT8 temperature sensor over temperature output **Bank C, Index07_Bit 5** **0:** Comparator Mode (def.) **1:** Interrupt Mode **Bank C, Index08_Bit5** **0:** Start to monitor the source of SMIOVT8 temperature. **1:** Stop monitoring the source of SMIOVT8 temperature. **Bank C, Index0D_Bit 2~3** Number of faults to detect before setting OVT# output.

8.11.5 OVT# Interrupt Mode

The SMI#/OVT# pin is a multi-function pin. It can be in SMI# mode or in OVT# mode by setting Configuration Register CR[24h], bit 2 to one or zero, respectively. In OVT# mode, it can monitor temperatures, and OVT pin could be enabled to OVT output by Bank0 Index 18h, bit 6 for Temperature Sensor 1(default: SYSTIN); Bank1 Index 52h, bit 1 for Temperature Sensor 2(default: CPUTIN) ; BankC Index 06h, bit 0 for Temperature Sensor 3(default: AUXTIN0) ; BankC Index 06h, bit 1 for Temperature Sensor 4(default: AUXTIN1) ; BankC Index 06h, bit 2 for Temperature Sensor 5(default: AUXTIN2) ; BankC Index 06h, bit 3 for Temperature Sensor 6(default: AUXTIN3) ; BankC Index 06h, bit 4 for Temperature Sensor 7(default: AUXTIN4).

The OVT# pin has two interrupt modes, comparator and interrupt. The modes are illustrated in this figure.

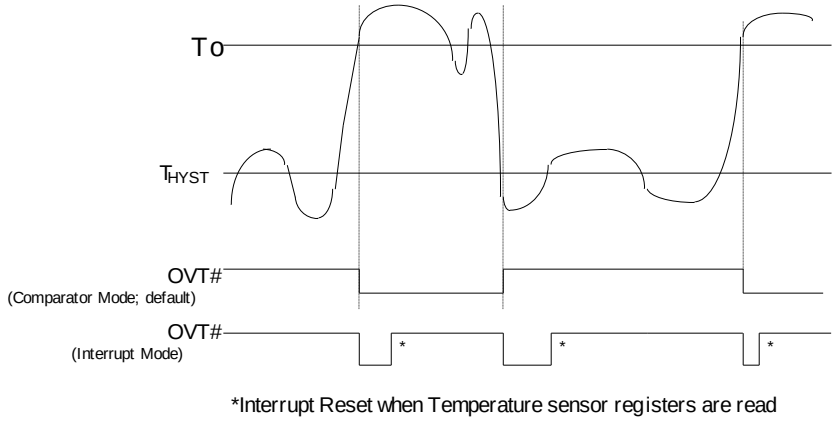


Figure 8-31 OVT# Modes of Temperature Inputs

In comparator mode, the OVT# pin can create an interrupt once the current temperature rises above T_O and continues to create interrupts until the temperature falls below T_{HYST}. The OVT# pin is asserted once the temperature has rised above T_O and has not yet fallen below T_{HYST}.

In interrupt mode, the OVT# pin can create an interrupt once the current temperature rises above T_O or when the temperature falls below T_{HYST}. Once the temperature rises above T_O, however, and generates an interrupt, this mode does not generate additional interrupts, even if the temperature remains above T_O, until the temperature falls below T_{HYST}. This interrupt must be reset by reading all the interrupt status registers. The OVT# pin is asserted when an interrupt is generated and remains asserted until the interrupt is reset.

8.11.6 Caseopen Detection

The purpose of Caseopen function is used to detect whether the computer case has been opened and possible tampered with. This feature must function even when there is no 3VSB power. Consequently, the power source for the circuit is from either VBAT or 3VSB. 3VSB is the default power source. If there is no 3VSB power, the power source is VBAT. This is designed to save power consumption of the battery.

When the case is closed, CASEOPEN0# or CASEOPEN1# must be pulled high by an externally pulled-up 2MΩ resistor that is connected to VBAT. When the case is opened, CASEOPEN0# or CASEOPEN1# will be switched from high to low. Meanwhile, the detection circuit inside the IC latches the signal. As a result, the interrupt status and the real-time status can be read at the registers next time when the computer is powered. The CASEOPEN0# status will not be cleared unless CR[46h], bit 7, or CR[E6h] bit 5 at Logical Device A is set to “1” first and then to “0”. The CASEOPEN1# status will not be cleared unless CR[46h], bit 6, or CR[Eeh] bit 0 at Logical Device A is set to “1” first and then to “0”.

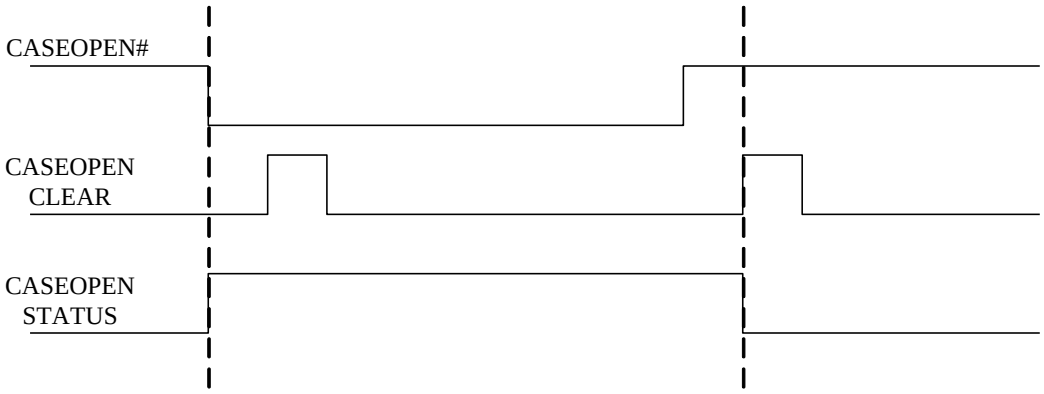


Figure 8-32 Caseopen Mechanism

9. HARDWARE MONITOR REGISTER SET

The base address of the Address Port and Data Port is specified in registers CR[60h] and CR[61h] of Logical Device B, the hardware monitor device. CR[60h] is the high byte, and CR[61h] is the low byte. The Address Port and Data Port are located at the base address, plus 5h and 6h, respectively. For example, if CR[60h] is 02h and CR[61h] is 90h, the Address Port is at 0x295h, and the Data Port is at 0x296h.

NCT6796D added 91byte read-only registers for Hardware Monitor. The base address is specified in registers CR[64h] and CR[65h] of Logical Device B, the hardware monitor device. CR[64h] is the high byte, and CR[65h] is the low byte. The least byte of the base address recommend to be zero. For example, {CR[64h], CR[65h]} = {XX00h}.

Remember that this access is from the host CPU I/O address range. To conserve space in the crowded CPU I/O addresses, many of the hardware monitor registers are “banked” with the bank number located at Bank0, index 04Eh.

9.1 Address Port (Port x5h)

Attribute: Bit 6:0 Read/Write , Bit 7: Reserved
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RESERVED**
6-0	**READ/WRITE.**

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	Address Pointer (Power On default 00h)						
(Power On default 0)	A6	A5	A4	A3	A2	A1	A0

9.2 Data Port (Port x6h)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	DATA							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Data to be read from or to be written to Value RAM and Register.

9.3 SYSFANOUT PWM Output Frequency Configuration Register – Index 00h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL1	PWM_SCALE1						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when SYSFANOUT is progarmmed for PWM output (i.e., Bank0, Index 04h, bit 0 is 0).

BIT	DESCRIPTION
7	**PWM_CLK_SEL1. SYSFANOUT PWM Input Clock Source Select.** This bit selects the clock source for PWM output frequency. Refer the Divisor table.
6-0	**PWM_SCALE1. SYSFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.4 SYSFANOUT Output Value Select Register – Index 01h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index 04h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index 04h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation. **OUTPUT Voltage =** $Vref * \frac{FANOUT}{64}$ Note. VREF is approx 2.048V.						Reserved	
This register could be programmed by Bank1, Index 09									

9.5 CPUFANOUT PWM Output Frequency Configuration Register – Index 02h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL2	PWM_SCALE2						
DEFAULT	0	0	0	0	0	1	0	0

The register is meaningful only when CPUFANOUT is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL2. CPUFANOUT PWM Input Clock Source Select.** This bit selects the clock source for the PWM output. Refer the Divisor table.
6-0	**PWM_SCALE2. CPUFANOUT PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz			
0000001	2	46.95KHz			

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000010	3	31.3KHz	…….		
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.6 CPUFANOUT Output Value Select Register – Index 03h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	CPUFANOUT PWM Duty. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and creates a duty cycle of 0%.							
This register could be programmed by Bank2, Index 09									

9.7 SYSFANOUT Configuration Register I – Index 04h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED							SYSFANOUT_SEL
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	Reserved
0	**SYSFANOUT Output Mode Selection.** 0: SYSFANOUT pin produces a PWM duty cycle output. **(Default)** 1: SYSFANOUT pin produces DC output.

9.8 AUXFANOUT0 PWM Output Frequency Configuration Register – Index 10h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL3	PWM_SCALE3						
DEFAULT	0	0	0	0	0	1	0	0

This register is only meaningful when AUXFANOUT0 is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL3. AUXFANOUT0 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE3. AUXFANOUT0 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.9 AUXFANOUT0 Output Value Select Register – Index 11h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	AUXFANOUT0 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
This register could be programmed by Bank3, Index 09									

9.10 AUXFANOUT1 PWM Output Frequency Configuration Register – Index 12h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL4	PWM_SCALE4						
DEFAULT	0	0	0	0	0	1	0	0

This register is only meaningful when AUXFANOUT1 is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL4. AUXFANOUT1 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE4. AUXFANOUT1 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz			
0000001	2	46.95KHz			

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000010	3	31.3KHz	…….		
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.11 AUXFANOUT1 Output Value Select Register – Index 13h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	AUXFANOUT1 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
This register could be programmed by Bank8, Index 09									

9.12 AUXFANOUT2 PWM Output Frequency Configuration Register – Index 14h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL5	PWM_SCALE5						
DEFAULT	0	0	0	0	0	1	0	0

This register is only meaningful when AUXFANOUT2 is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL5. AUXFANOUT2 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE5. AUXFANOUT2 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.13 AUXFANOUT2 Output Value Select Register – Index 15h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0

PWM Output	**DESCRIPTION**	AUXFANOUT2 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.
This register could be programmed by Bank9, Index 09		

9.14 AUXFANOUT3 PWM Output Frequency Configuration Register – Index 16h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL6	PWM_SCALE6						
DEFAULT	0	0	0	0	0	1	0	0

This register is only meaningful when AUXFANOUT3 is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL6. AUXFANOUT3 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE6. AUXFANOUT3 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.15 AUXFANOUT3 Output Value Select Register – Index 17h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	AUXFANOUT3 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
This register could be programmed by BankA, Index 09									

9.16 AUXFANOUT4 PWM Output Frequency Configuration Register – Index 28h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PWM_CLK_SEL7	PWM_SCALE7						
DEFAULT	0	0	0	0	0	1	0	0

This register is only meaningful when AUXFANOUT4 is programmed for PWM output.

BIT	DESCRIPTION
7	**PWM_CLK_SEL7. AUXFANOUT4 PWM Input Clock Source Select.** This bit selects the clock source of PWM output frequency. Refer the Divisor table.
6-0	**PWM_CLK_SCALE7. AUXFANOUT4 PWM Pre-Scale divider.** The clock source for PWM output is divided by this seven-bit value to calculate the actual PWM output frequency. Refer the Divisor table.

The clock source selected by CKSEL will be divided by the divisor and used as a fan PWM output frequency.
If CKSEL equals **0**, then the output clock is simply equal to **93.9/ (Divisor[6:0]+1) KHz**
MappedDivisor depends on **Divisor[6:0]** and is described in the table below.

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000000	1	93.9KHz	.....		
0000001	2	46.95KHz			
0000010	3	31.3KHz			

Divisor[6:0]	Mapped Divisor	Output Frequency	Divisor[6:0]	Mapped Divisor	Output Frequency
0000011	4	23.47KHz			
0000100	5	18.78KHz	0001111	16	5.86KHz
0000101	6	15.65KHz	0011111	32	2.93KHz
0000110	7	13.41KHz	0111111	64	1.46KHz
0000111	8	11.73KHz	1111111	128	734Hz

If CKSEL equals **1**, then the output clock is simply equal to **1008/ Mapped Divisor Hz**
MappedDivisor depends on **Divisor[3:0]** and is described in the table below.

Divisor[3:0]	Mapped Divisor	Output Frequency	Divisor[3:0]	Mapped Divisor	Output Frequency
0000	1	1008Hz	1000	12	84Hz
0001	2	504Hz	1001	16	63Hz
0010	3	336Hz	1010	32	31.5Hz
0011	4	252Hz	1011	64	15.75Hz
0100	5	201Hz	1100	128	7.875Hz
0101	6	168Hz	1101	256	3.94Hz
0110	7	144Hz	1110	512	1.97Hz
0111	8	126Hz	1111	1024	0.98Hz

9.17 AUXFANOUT4 Output Value Select Register – Index 29h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT4 Value							
DEFAULT	7Fh							

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	AUXFANOUT4 PWM Duty Cycle. The PWM duty cycle is equal to this 8-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
This register could be programmed by BankB, Index 09									

9.18 OVT# Configuration Register – Index 18h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
BIT	RESERVED	DIS_OVT1	RESERVED	OVT1_Mode	RESERVED			STOP
DEFAULT	0	1	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7	**Reserved**
6	**DIS_OVT1.** 0: Enable SMIOVT1 OVT# output. (Default) 1: Disable temperature sensor SMIOVT1 over-temperature (OVT#) output.
5	**Reserved**
4	**OVT1_Mode. SMIOVT1 Mode Select.** 0 : Compare Mode. (Default) 1 : Interrupt Mode.
3-1	**Reserved**
0	**STOP.** **0: Monitor SMIOVT1 temperature source.** **1: Stop monitoring SMIOVT1 temperature source.**

9.19 Value RAM — Index 27h ~ 3Fh (Bank 0)

ADDRESS A6-A0	DESCRIPTION
27h	SMIOVT1 temperature source reading.
2Bh	CPUVCORE High Limit
2Ch	CPUVCORE Low Limit
2Dh	VIN1 High Limit
2Eh	VIN1 Low Limit
2Fh	AVSB High Limit
30h	AVSB Low Limit
31h	3VCC High Limit
32h	3VCC Low Limit
33h	VIN0 High Limit
34h	VIN0 Low Limit
35h	VIN8 High Limit
36h	VIN8 Low Limit
37h	VIN4 High Limit
38h	VIN4 Low Limit
39h	SMIOVT1 temperature sensor High Limit
3Ah	SMIOVT1 temperature sensor Hysteresis Limit

9.20 Configuration Register – Index 40h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	INITIALIZATION	RESERVED	EN_WS1	EN_WS	INT_CLEAR	RESERVED	SMI#ENABLE	START

DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Initialization.** A one restores the power-on default values to some registers. This bit clears itself since the power-on default of this bit is zero.
6	**RESERVED**
5	**Output type of SMIOVT2:** 1: SMI# output type of SMIOVT Source2 temperature (Default: CPUTIN) is Shut-down Interrupt Mode. 0: Depond on the value of Bank0, Index 4C, bit6.
4	**Output type of SMIOVT1** 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is Shut-down Interrupt Mode. 0: Depond on the value of Bank0, Index 4C, bit5.
3	**INT_Clear.** A one disables the SMI# output without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
2	**Reserved**
1	**SMI# Enable.** A one enables the SMI# Interrupt output. 1: Enable SMI# function (Deafult) 0: Disable SMI# function
0	**Start.** A one enables startup of monitoring operations. A zero puts the part in standby mode. **Note:** Unlike the "INT_Clear" bit, the outputs of interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred.

9.21 Interrupt Status Register 1 – Index 41h (Bank 0)

Attribute: Read Clear
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN	SYSFANIN	SOURCE2 _ SMI	SOURCE1 _ SMI	3VCC	AVSB	VIN1	CPUVCORE
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN.** A one indicates the fan count limit of CPUFANIN has been exceeded.
6	**SYSFANIN.** A one indicates the fan count limit of SYSFANIN has been exceeded.
5	**SMIOVT2.** A one indicates the high limit of SMIOVT2 temperature has been exceeded. (CPUTIN is default temperature)
4	**SMIOVT1.** A one indicates the high limit of SMIOVT1 temperature has been exceeded. (SYSTIN is default temperature)
3	**3VCC.** A one indicates the high or low limit of 3VCC has been exceeded.
2	**AVSB.** A one indicates the high or low limit of AVSB has been exceeded.
1	**VIN1.** A one indicates the high or low limit of VIN1 has been exceeded.
0	**CPUVCORE.** A one indicates the high or low limit of CPUVCORE has been exceeded.

9.22 Interrupt Status Register 2 – Index 42h (Bank 0)

Attribute: Read Clear
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	CASEOPEN1	Reserved	CASEOPEN0	AUXFANIN0	Reserved	VIN4	VIN0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved**
6	**CASEOPEN1.** A one indicates the case has been opened.
5	**Reserved**
4	**CASEOPEN0.** A one indicates the case has been opened.
3	**AUXFANIN0.** A one indicates the fan count limit of AUXFANIN0 has been exceeded.
2	**Reserved**
1	**VIN4.** A one indicates the high or low limit of VIN4 has been exceeded.
0	**VIN0.** A one indicates the high or low limit of VIN0 has been exceeded.

9.23 SMI# Mask Register 1 – Index 43h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN	SYSFANIN	SMIOVT2	SMIOVT1	3VCC	AVSB	VIN1	CPUVCORE
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**CPUFANIN.**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 1 – Index 41h (Bank0))
6	**SYSFANIN.**	
5	**SMIOVT2.**	
4	**SMIOVT1.**	
3	**3VCC.**	
2	**AVSB.**	
1	**VIN1.**	
0	**CPUVCORE.**	

9.24 SMI# Mask Register 2 – Index 44h (Bank 0)

Attribute: Read/Write
Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TAR2	TAR1	Reserved	CASEOPEN0	AUXFANIN0	VIN4	Reserved	VIN0
DEFAULT	1	1	0	1	1	1	1	1

BIT	DESCRIPTION	
7	**TAR2.**	A one disables the corresponding interrupt status bit for the interrupt. (See Interrupt Status Register 2 – Index 42h (*Bank 0*))
6	**TAR1.**	
5	**Reserved**	
4	**CASEOPEN0.**	
3	**AUXFANIN0.**	
2	**VIN4.**	
1	**Reserved**	
0	**VIN0.**	

9.25 Interrupt Status Register 4 – Index 45h (Bank 0)

Attribute: Read Clear
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUX FANOUT4	AUX FANOUT0	CPU FANOUT	SYS FANOUT	Reserved	Shut_ SOURCE2_SMI	Shut_ SOURCE1_SMI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved**
6	**AUXFANOUT4.** "1" indicates that AUXFANOUT4 works for three minutes at the full fan speed.
5	**AUXFANOUT0.** "1" indicates that AUXFANOUT0 works for three minutes at the full fan speed.
4	**CPUFANOUT.** "1" indicates that CPUFANOUT works for three minutes at the full fan speed.
3	**SYSFANOUT.** "1" indicates that SYSFANOUT works for three minutes at the full fan speed.
2	**Reserved**
1	**Shut_SOURCE2_SMI.** "1" indicates the high limit of SMIOVT _SOURCE2 temperature of SMI# Shut-down mode has been exceeded. (CPUTIN is default temperature)
0	**Shut_SOURCE1_SMI.** "1" indicates the high limit of SMIOVT _SOURCE1 temperature of SMI# Shut-down mode has been exceeded. (SYSTIN is default temperature)

9.26 SMI# Mask Register 3 – Index 46h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0

NAME	Reserved	AUXFANIN4	AUXFANIN3	Shut_CPU	Shut_SYS	AUXFANIN2	AUXFANIN1	CASEOPEN1
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**CASEOPEN0 Clear Control.** Writing 1 to this bit will clear CASEOPEN0 status. This bit will be cleared itself. The function is the same as LDA, CR[E6h], bit 5.	
6	**AUXFANIN4**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt.
5	**AUXFANIN3**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt.
4	**Shut_SOURCE2_SMI**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt. (See Interrupt Status Register 4 – Index 45h (Bank 0)).
3	**Shut_SOURCE1_SMI**	
2	**AUXFANIN2**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt.
1	**AUXFANIN1**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt
0	**CASEOPEN1**	"1" disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt.

9.27 Serial Bus Address Register – Index 48h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	SERIAL BUS ADDRESS						
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7	**Reserved**
6-0	**Serial Bus Address <7:1>**

9.28 SMI/OVT Control Register1 – Index 4Ch (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	T2ToT6_INT MODE	EN_T1 _ONE	RESERVED	DIS_ OVT2	OVTPOL	RESERVED	

DEFAULT	0	0	0	0	1	0	0	0

BIT	DESCRIPTION
7	**Reserved**
6	**T2ToT6_INTMode.** 1: SMI# output type of Temperature SMIOVT2, SMIOVT3, SMIOVT4, SMIOVT5 and SMIOVT6 temperature source is in Comparator Interrupt mode. 0: SMI# output type of Temperature SMIOVT2, SMIOVT3, SMIOVT4, SMIOVT5 and SMIOVT6 temperature source is in Two-Times Interrupt mode. (Default)
5	**EN_T1_ONE.** 1: SMI# output type of SMIOVT Source1 temperature (Default: SYSTIN) is One-Time Interrupt Mode. 0: SMI# output type is in Two-Times Interrupt Mode. (Default)
4	**Reserved**
3	**DIS_OVT2.** 1: Disable SMIOVT Source2 temperature sensor (Default: CPUTIN) over-temperature (OVT) output. 0: Enable SMIOVT Source2 temperature OVT output through pin OVT#. (Default)
2	**OVTPOL (Over-temperature polarity).** 1: OVT# is active high. 0: OVT# is active low (Default).
1-0	**Reserved**

9.29 FAN IN/OUT Control Register – Index 4Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANOPV4	FANINC4	FANOPV3	FANINC3	FANOPV2	FANINC2	FANOPV1	FANINC1
DEFAULT	0	1	0	1	0	1	0	1

BIT	DESCRIPTION
7	**FANOPV4. AUXFANIN1 output value**, only if bit 2 is set to zero. 1: AUXFANIN1 generates a logic-high signal. 0: AUXFANIN1 generates a logic-low signal. (Default)
6	**FANINC4. AUXFANIN1 Input Control.** 1: AUXFANIN1 acts as a fan tachometer input. (Default) 0: AUXFANIN1 acts as a fan control signal, and the output value is set by bit 1.
5	**FANOPV3. AUXFANIN0 output value**, only if bit 2 is set to zero. 1: AUXFANIN0 generates a logic-high signal. 0: AUXFANIN0 generates a logic-low signal. (Default)
4	**FANINC3. AUXFANIN0 Input Control.** 1: AUXFANIN0 acts as a fan tachometer input. (Default) 0: AUXFANIN0 acts as a fan control signal, and the output value is set by bit 1.
3	**FANOPV2. CPUFANIN output value**, only if bit 2 is set to zero. 1: CPUFANIN generates a logic-high signal.

BIT	DESCRIPTION
	0: CPUFANIN generates a logic-low signal. (Default)
2	**FANINC2. CPUFANIN Input Control.** 1: CPUFANIN acts as a fan tachometer input. (Default) 0: CPUFANIN acts as a fan control signal, and the output value is set by bit 3.
1	**FANOPV1. SYSFANIN output value**, only if bit 0 is set to zero. 1: SYSFANIN generates a logic-high signal. 0: SYSFANIN generates a logic-low signal. (Default)
0	**FANINC1. SYSFANIN Input Control.** 1: SYSFANIN acts as a fan tachometer input. (Default) 0: SYSFANIN acts as a fan control signal, and the output value is set by bit 1.

9.30 Bank Select Register – Index 4Eh (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	HBACS	Reserved			BANK SEL3	BANK SEL2	BANK SEL1	BANK SEL0
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**HBACS. HBACS – High Byte Access.** 1: Access Index 4Fh high-byte register. (Default) 0: Access Index 4Fh low-byte register.	
6	**Reserved**	
5	**Reserved**	
4	**Reserved**	
3	**BANKSEL3.**	Bank Select for Bank0 to Bank7. The Three -bit binary value corresponds to the bank number. For example, "0010" selects bank2.
2	**BANKSEL2.**	
1	**BANKSEL1.**	
0	**BANKSEL0.**	

9.31 Nuvoton Vendor ID Register – Index 4Fh (Bank 0)

Attribute: Read Only
Size: 16 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	15	14	13	12	11	10	9	8
NAME	VIDH							
DEFAULT	0	1	0	1	1	1	0	0

BIT	7	6	5	4	3	2	1	0
NAME	VIDL							
DEFAULT	1	0	1	0	0	0	1	1

BIT	DESCRIPTION
15-8	**Vendor ID High-Byte**, if Index 4Eh, bit 7 is 1. Default 5Ch.
7-0	**Vendor ID Low-Byte**, if Index 4Eh, bit 7 is 0. Default A3h.

9.32 FAN IN/OUT Control Register – Index 50h (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		FANOPV7	FANINC7	FANOPV6	FANINC6	FANOPV5	FANINC5
DEFAULT	0	0	0	1	0	1	0	1

BIT	DESCRIPTION
7-6	**Reserved**
5	**FANOPV7. AUXFANIN4 output value**, only if bit 0 is set to zero. 1: AUXFANIN4 generates a logic-high signal. 0: AUXFANIN4 generates a logic-low signal. (Default)
4	**FANOPV7. AUXFANIN4 output value**, only if bit 0 is set to zero. 1: AUXFANIN4 generates a logic-high signal. 0: AUXFANIN4 generates a logic-low signal. (Default)
3	**FANOPV6. AUXFANIN3 output value**, only if bit 0 is set to zero. 1: AUXFANIN3 generates a logic-high signal. 0: AUXFANIN3 generates a logic-low signal. (Default)
2	**FANINC6. AUXFANIN3 Input Control.** 1: AUXFANIN3 acts as a fan tachometer input. (Default) 0: AUXFANIN3 acts as a fan control signal, and the output value is set by bit 1.
1	**FANOPV5. AUXFANIN2 output value**, only if bit 0 is set to zero. 1: AUXFANIN2 generates a logic-high signal. 0: AUXFANIN2 generates a logic-low signal. (Default)
0	**FANINC5. AUXFANIN2 Input Control.** 1: AUXFANIN2 acts as a fan tachometer input. (Default) 0: AUXFANIN2 acts as a fan control signal, and the output value is set by bit 1.

9.33 Chip ID – Index 58h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0

NAME	CHIPID							
DEFAULT	1	1	0	0	0	0	0	1

BIT	DESCRIPTION
7-0	Nuvoton Chip ID number. Default C1h.

9.34 VBAT Monitor Control Register – Index 5Dh (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	DIODES7	DIODES6	DIODES5	DIODES4	DIODES3	DIODES2	DIODES1	EN_VBAT_MNT
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**DIODES 7. Sensor type selection for AUXTIN4.** 1: Diode sensor. 0: Thermistor sensor. (default)
6	**DIODES 6. Sensor type selection for AUXTIN3.** 1: Diode sensor. 0: Thermistor sensor. (default)
5	**DIODES 5. Sensor type selection for AUXTIN2.** 1: Diode sensor. 0: Thermistor sensor. (default)
4	**DIODES 4. Sensor type selection for AUXTIN1.** 1: Diode sensor. 0: Thermistor sensor. (default)
3	**DIODES 3. Sensor type selection for AUXTIN0.** 1: Diode sensor. 0: Thermistor sensor. (default)
2	**DIODES 2. Sensor type selection for CPUTIN.** 1: Diode sensor. (default) 0: Thermistor sensor.
1	**DIODES 1. Sensor type selection for SYSTIN.** 1: Diode sensor. 0: Thermistor sensor. (default)
0	**EN_VBAT_MNT.** 1: Enable battery voltage monitor. When this bit changes from zero to one, it takes one monitor cycle time to update the VBAT reading value register. 0: Disable battery voltage monitor.

9.35 Current Mode Enable Register – Index 5Eh (Bank 0)

Attribute: Read/Write

Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	EN_ AUXTIN4 CURRENT MODE	EN_ AUXTIN3 CURRENT MODE	EN_ AUXTIN2 CURRENT MODE	EN_ AUXTIN1 CURRENT MODE	EN_ AUXTIN0 CURRENT MODE	EN_ CPUTIN CURRENT MODE	EN_ SYSTIN CURRENT MODE	Reserved
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7	**Enable AUXTIN4 Current Mode**. With AUXTIN4 is selected to Diode sensor (Bank0, Index 5Dh, Bit 7 = 1). 1: Temperature sensing of AUXTIN4 by Current Mode. 0: Temperature sensing of AUXTIN4 depends on the setting of Index 5Dh. **(Default)**
6	**Enable AUXTIN3 Current Mode**. With AUXTIN3 is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN3 by Current Mode. 0: Temperature sensing of AUXTIN3 depends on the setting of Index 5Dh. **(Default)**
5	**Enable AUXTIN2 Current Mode**. With AUXTIN2 is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN2 by Current Mode. 0: Temperature sensing of AUXTIN2 depends on the setting of Index 5Dh. **(Default)**
4	**Enable AUXTIN1 Current Mode**. With AUXTIN1 is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN1 by Current Mode. 0: Temperature sensing of AUXTIN1 depends on the setting of Index 5Dh. **(Default)**
3	**Enable AUXTIN0 Current Mode**. With AUXTIN0 is selected to Diode sensor (Bank0, Index 5Dh, Bit 3 = 1). 1: Temperature sensing of AUXTIN0 by Current Mode. 0: Temperature sensing of AUXTIN0 depends on the setting of Index 5Dh. **(Default)**
2	**Enable CPUTIN Current Mode.** With CPUTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 2 = 1). 1: Temperature sensing of CPUTIN by Current mode. **(Default)** 0: Temperature sensing of CPUTIN depends on the setting of Index 5Dh.
1	**Enable SYSTIN Current Mode.** With SYSTIN is selected to Diode sensor (Bank0, Index 5Dh, Bit 1 = 1). 1: Temperature sensing of SYSTIN by Current Mode. 0: Temperature sensing of SYSTIN depends on the setting of Index 5Dh. **(Default)**
0	**Reserved**

9.36 PORT 80 DATA INPUT Register – Index 60 (Bank 0)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	P80_IN							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PORT 80 DATA INPUT**

9.37 MONITOR TEMPERATURE 1 Register (Integer Value)- Index 73h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 1 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 1 [8:1]** SYSFANOUT fan control temperature reading. (Source is selected by Bank1, Index00 bit[4:0])

9.38 MONITOR TEMPERATURE 1 Register (Fractional Value)- Index 74h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 1 [0]	Reserved						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**MONITOR TEMPERATURE 1 [0]** SYSFANOUT fan control temperature reading. (Source is selected by Bank1, Index00 bit[4:0])
6-0	**Reserved**

9.39 MONITOR TEMPERATURE 2 Register (Integer Value)- Index 75h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 2 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 2 [8:1]** CPUFANOUT fan control temperature reading. (Source is selected by Bank2, Index00 bit[4:0])

9.40 MONITOR TEMPERATURE 2 Register (Fractional Value)- Index 76h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	**MONITOR TEMPERATURE 2 [0]**	**Reserved**						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**MONITOR TEMPERATURE 2 [0]** CPUFANOUT fan control temperature reading. (Source is selected by Bank2, Index00 bit[4:0])
6-0	**Reserved**

9.41 MONITOR TEMPERATURE 3 Register (Integer Value)- Index 77h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	**MONITOR TEMPERATURE 3 [8:1]**							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 3 [8:1]** AUXFANOUT0 fan control temperature reading. (Source is selected by Bank3, Index00 bit[4:0])

9.42 MONITOR TEMPERATURE 3 Register (Fractional Value)- Index 78h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	**MONITOR TEMPERATURE 3 [0]**	**Reserved**						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 3 [0]** AUXFANOUT0 fan control temperature reading. (Source is selected by Bank3, Index00 bit[4:0])
6-0	**Reserved**

9.43 MONITOR TEMPERATURE 4 Register (Integer Value)- Index 79h (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 4 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 4 [8:1]** AUXFANOUT1 fan control temperature reading. (Source is selected by Bank8, Index00 bit[4:0])

9.44 MONITOR TEMPERATURE 4 Register (Fractional Value)- Index 7Ah (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 4 [0]	Reserved						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 4 [0]** AUXFANOUT1 fan control temperature reading. (Source is selected by Bank8, Index00 bit[4:0])
6-0	**Reserved**

9.45 MONITOR TEMPERATURE 5 Register (Integer Value)- Index 7Bh (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	MONITOR TEMPERATURE 5 [8:1]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 5 [8:1]** AUXFANOUT2 fan control temperature reading. (Source is selected by Bank9, Index00 bit[4:0])

9.46 MONITOR TEMPERATURE 5 Register (Fractional Value)- Index 7Ch (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	**MONITOR TEMPERATURE 5 [0]**	**Reserved**						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 5 [0]** AUXFANOUT2 fan control temperature reading. (Source is selected by Bank9, Index00 bit[4:0])
6-0	**Reserved**

9.47 MONITOR TEMPERATURE 6 Register (Integer Value)- Index 7Dh (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	**MONITOR TEMPERATURE 6 [8:1]**							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 6 [8:1]** AUXFANOUT3 fan control temperature reading. (Source is selected by BankA, Index00 bit[4:0])

9.48 MONITOR TEMPERATURE 6 Register (Fractional Value)- Index 7Eh (Bank 0)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	**MONITOR TEMPERATURE 6 [0]**	**Reserved**						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**MONITOR TEMPERATURE 6 [0]** AUXFANOUT3 fan control temperature reading. (Source is selected by BankA, Index00 bit[4:0])
6-0	**Reserved**

9.49 PECI Temperature Reading Enable for SMIOVT and SMART FAN Control Register – Index AEh (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_PECI1	EN_PECI0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**Reserved**
1	**Enable PECI Agent1**
0	**Enable PECI Agent0**

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.50 BEEP Control Register 1 – Index B2h (Bank0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	En3VSB_BP	EnVIN4_BP	Reserved	EnVIN0_BP	En3VCC_BP	EnAVSB_BP	EnVIN1_BP	EnCPUVCORE_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En3VSB_BP** **1 : Enable 3VSB Beep function** **0 : Disable 3VSB Beep function**
6	**EnVIN4_BP** **1 : Enable VIN4 Beep function** **0 : Disable VIN4 Beep function**
5	**Reserved**
4	**EnVIN0_BP** **1 : Enable VIN0 Beep function** **0 : Disable VIN0 Beep function**
3	**En3VCC_BP**

BIT	DESCRIPTION
	1 : Enable 3VCC Beep function **0 : Disable 3VCC Beep function**
2	**EnAVSB_BP** **1 : Enable AVSB Beep function** **0 : Disable AVSB Beep function**
1	**EnVIN1_BP** **1 : Enable VIN1 Beep function** **0 : Disable VIN1 Beep function**
0	**EnCPUVCORE_BP** **1 : Enable CPUVCORE Beep function** **0 : Disable CPUVCORE Beep function**

9.51 BEEP Control Register 2 – Index B3h (Bank0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	EnVIN9_BP	EnVIN7_BP	EnVIN3_BP	EnVIN2_BP	EnVIN6_BP	EnVIN5_BP	EnVTT_BP	EnVBAT_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**EnVIN9_BP** **1 : Enable VIN9 Beep function** **0 : Disable VIN9 Beep function**
6	**EnVIN7_BP** **1 : Enable VIN7 Beep function** **0 : Disable VIN7 Beep function**
5	**EnVIN3_BP** **1 : Enable VIN3 Beep function** **0 : Disable VIN3 Beep function**
4	**EnVIN2_BP** **1 : Enable VIN2 Beep function** **0 : Disable VIN2 Beep function**
3	**EnVIN6_BP** **1 : Enable VIN6 Beep function** **0 : Disable VIN6 Beep function**
2	**EnVIN5_BP** **1 : Enable VIN5 Beep function** **0 : Disable VIN5 Beep function**
1	**EnVTT_BP** **1 : Enable VTT Beep function** **0 : Disable VTT Beep function**
0	**EnVBAT_BP**

BIT	DESCRIPTION
	1 : Enable VBAT Beep function **0 : Disable VBAT Beep function**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.52 BEEP Control Register 3 – Index B4h (Bank0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	EnT8_BP	EnT7_BP	EnT6_BP	EnT5_BP	EnT4_BP	EnT3_BP	EnT2_BP	EnT1_BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**EnT8_BP** **1 : Enable SMIOVT8 Beep function** **0 : Disable SMIOVT8 Beep function**
6	**EnT7_BP** **1 : Enable SMIOVT7 Beep function** **0 : Disable SMIOVT7 Beep function**
5	**EnT6_BP** **1 : Enable SMIOVT6 Beep function** **0 : Disable SMIOVT6 Beep function**
4	**EnT5_BP** **1 : Enable SMIOVT5 Beep function** **0 : Disable SMIOVT5 Beep function**
3	**EnT4_BP** **1 : Enable SMIOVT4 Beep function** **0 : Disable SMIOVT4 Beep function**
2	**EnT3_BP** **1 : Enable SMIOVT3 Beep function** **0 : Disable SMIOVT3 Beep function**
1	**EnT2_BP** **1 : Enable SMIOVT2 Beep function** **0 : Disable SMIOVT2 Beep function**
0	**EnT1_BP** **1 : Enable SMIOVT1 Beep function** **0 : Disable SMIOVT1 Beep function**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.53 BEEP Control Register 4 – Index B5h (Bank0)

Attribute: Read/Write
Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	En Caseopen1_BP	En Caseopen0_BP	En AUXFANIN2 _BP	En AUXFANIN1 _BP	En AUXFANIN0 _BP	En CPUFANIN _BP	En SYSFANIN _BP	En_Beep
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En Caseopen1_BP** **1 : Enable Caseopen1 Beep function** **0 : Disable Caseopen1 Beep function**
6	**En Caseopen0_BP** **1 : Enable Caseopen0_bp Beep function** **0 : Disable Caseopen0_bp Beep function**
5	**En AUXFANIN2_BP** **1 : Enable AUXFANIN2 Beep function** **0 : Disable AUXFANIN2 Beep function**
4	**En AUXFANIN1_BP** **1 : Enable AUXFANIN1 Beep function** **0 : Disable AUXFANIN1 Beep function**
3	**En AUXFANIN0_BP** **1 : Enable AUXFANIN0 Beep function** **0 : Disable AUXFANIN0 Beep function**
2	**En CPUFANIN _BP** **1 : Enable CPUFANIN Beep function** **0 : Disable CPUFANIN Beep function**
1	**En SYSFANIN _BP** **1 : Enable SYSFANIN Beep function** **0 : Disable SYSFANIN Beep function**
0	**Enable Beep Function:** **1 : Enable Beep Function** **0 : Disable Beep Function**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.54 BEEP Control Register 5 – Index BFh (Bank0)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	En AUXFANIN4 _BP	En AUXFANIN3 _BP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7-1	**Reserved**
1	**En AUXFANIN4_BP** **1 : Enable AUXFANIN4 Beep function** **0 : Disable AUXFANIN4 Beep function**
0	**En AUXFANIN3_BP** **1 : Enable AUXFANIN3 Beep function** **0 : Disable AUXFANIN3 Beep function**

Note: For each beep alarm event, please set “Bank0, Index B5, bit0” to 1.

9.55 SYSFAN Virtual1 Temperature Register – Index EAh (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Virtual1 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	SYSFAN Virtual1 TEMP

9.56 CPUFAN Virtual1 Temperature Register – Index EBh (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Virtual1 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN Virtual1 TEMP

9.57 AUXFAN0 Virtual1 Temperature Register – Index ECh (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 Virtual1 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN0 Virtual1 TEMP

9.58 AUXFAN1 Virtual1 Temperature Register – Index EDh (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 Virtual1 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN1 Virtual1 TEMP

9.59 AUXFAN2 Virtual1 Temperature Register – Index EEh (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 Virtual1 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 Virtual1 TEMP

9.60 AUXFAN3 Virtual1 Temperature Register – Index EFh (Bank 0)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 Virtual1 Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN3 Virtual1 TEMP

9.61 SYSFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 1)

Attribute: Read/Write
Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		SYSFAN SOURCE1[4:0]				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to SYSFANOUT Stop Value (Bank1, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**SYSFAN Temperature Source1 Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SYSFAN monitoring source. 0 0 0 1 0: Select **CPUTIN** as SYSFAN monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SYSFAN monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SYSFAN monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SYSFAN monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SYSFAN monitoring source. 0 0 1 1 1: Select **AUXTIN4** as SYSFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as SYSFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SYSFAN monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as SYSFAN monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SYSFAN monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SYSFAN monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SYSFAN monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SYSFAN monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SYSFAN monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as SYSFAN monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as SYSFAN monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as SYSFAN monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as SYSFAN monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as SYSFAN monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as SYSFAN monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as SYSFAN monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as SYSFAN monitoring source. 1 1 1 1 1: Select **Virtual_TEMP1** as SYSFAN monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.62 SYSFAN Target Temperature Register / SYSFANIN Target Speed_L Register – Index 01h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSTIN Target Temperature / SYSFANIN Target Speed_L / CPUFANIN Target Thermal Margin							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	SYSFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	SYSFANIN Target Speed [7:0], [11:8] associate index 0C [3:0]							
SMART FAN™ IV	DESCRIPTION	CPUFANIN Target Thermal Margin							

9.63 SYSFAN MODE Register / SYSFAN TOLERRANCE Register – Index 02h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#(Bit2-0)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN MODE				Reserved	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**SYSFANOUT Mode Select.** 0000: SYSFANOUT is in Manual Mode. **(Default)** 0001: SYSFANOUT is in Thermal Cruise Mode. 0010: SYSFANOUT is in Speed Cruise Mode. 0100: SYSFANOUT is in SMART FAN IV Mode.
3	**Reserved**
2-0	Tolerance of SYSFAN Target Temperature or SYSFANIN Target Speed_L.

9.64 SYSFANOUT Step Up Time Register – Index 03h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

9.65 SYSFANOUT Step Down Time Register – Index 04h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time SYSFANOUT takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:

The units are intervals of 0.4 second. The default time is 4 seconds.

9.66 SYSFANOUT Stop Value Register – Index 05h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the SYSFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.67 SYSFANOUT Start-up Value Register – Index 06h (Bank 1)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, SYSFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.68 SYSFANOUT Stop Time Register – Index 07h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes SYSFANOUT value to fall from the stop value to zero.

(1) For PWM output:
The units are intervals of 0.1 second. The default time is 1 second.

(2) For DC output:
The units are intervals of 0.4 second. The default time is 4 seconds.

9.69 SYSFANOUT Output Value Select Register – Index 09h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT Value							
DEFAULT	0	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E0h] is the Default Speed Configuration Register of SYSFANOUT.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output (Bank0, Index 04h, bit 0 is 0)	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							
DC Voltage Output Bank0, Index 04h, bit 0 is 1)	DESCRIPTION	SYSFANOUT voltage control. The output voltage is calculated according to this equation. **OUTPUT Voltage =** $AVSB * \frac{FANOUT}{64}$						Reserved	

9.70 SYSFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	SYSFANIN TOL_H			SYSFANIN Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	SYSFANIN Tolerance_H [5:3]
3-0	SYSFANIN Target Speed_H [11:8]

9.71 SYSFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.72 SYSFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.73 SYSFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.74 SYSFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.75 SYSFAN (SMART FAN™ IV) DC/PWM 1 Register – Index 27h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 1 Register.

9.76 SYSFAN (SMART FAN™ IV) DC/PWM 2 Register – Index 28h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 2 Register.

9.77 SYSFAN (SMART FAN™ IV) DC/PWM 3 Register – Index 29h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 3 Register.

9.78 SYSFAN (SMART FAN™ IV) DC/PWM 4 Register – Index 2Ah (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) DC/PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) DC/PWM 4 Register.

9.79 SYSFAN 3-Wire Enable Register – Index 31h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_SYS_3WFAN
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_SYS_3WFAN (SYSFAN type setting)** 0: 4-wire fan 1: 3-wire fan

9.80 SYSFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	SYSFAN (SMART FAN™ IV) Critical Temperature Register.

9.81 SYSFAN Enable Critical Duty – Index 36h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_SYS_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_SYS_CRITICAL_DUTY (set 0 in manual mode)** 0: Load default Full Speed 8'hFF for SYSFANOUT. 1: Used Index 37 CRITICAL_DUTY Value for SYSFANOUT.

9.82 SYSFAN Critical Duty Register – Index 37h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	SYSFAN Critical Duty.

9.83 SYSFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					SYSFANOUT Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	SYSFANOUT Critical Temperature Tolerance

9.84 SYSFAN PECIERR DUTY Enable Register – Index 3Fh (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_SYS_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**
1-0	**EN_SYS_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_SYSOUT** Value for SYSFANOUT. 10,11: Keep Full Speed

9.85 SYSFANOUT Pre-Configured Register For PECI Error – Index 41h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANOUT pre-configured register for PECI error (PECI_ERR_SYSOUT)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**SYSFANOUT pre-configured register for PECI error.**

9.86 SMIOVT2 Temperature Source (High Byte) Register – Index 50h (Bank 1)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<8:1>							

BIT	DESCRIPTION
7-0	**Temperature <8:1> (default: CPUTIN temperature source).** The nine-bit value is in units of 0.5℃.

9.87 SMIOVT2 Temperature Source (Low Byte) Register – Index 51h (Bank 1)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TEMP<0>	RESERVED						

BIT	DESCRIPTION
7	**Temperature <0> (default: CPUTIN temperature source).** The nine-bit value is in units of 0.5°C.
6-0	**Reserved**

9.88 SMIOVT2 Temperature Source Configuration Register – Index 52h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FAULT		RESERVED	OVTMOD	STOP
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved** This bit should be set to zero.
4-3	**Fault.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise.
2	**Reserved** This bit should be set to zero.
1	**OVTMOD. SMIOVT2 Mode Select.** 0 : Compare Mode. (Default) 1: Interrupt Mode.
0	**STOP.** 0: Monitor SMIOVT2 temperature source. 1: Stop monitoring SMIOVT2 temperature source.

9.89 SMIOVT2 Temperature Source Hysteresis (High Byte) Register – Index 53h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.90 SMIOVT2 Temperature Source Hysteresis (Low Byte) Register – Index 54h (Bank 1)

Attribute: Read/Write
Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**THYST<0>. Hysteresis temperature bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**Reserved**

9.91 SMIOVT2 Temperature Source Over-temperature (High Byte) Register – Index 55h (Bank1)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.92 SMIOVT2 Temperature Source Over-temperature (Low Byte) Register – Index 56h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<0>	RESERVED						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TOVF<0>. Over-temperature bit 0.** The nine-bit value is in units of 0.5°C.
6-0	**Reserved**

9.93 DUTY PER STEP Register – Index 66h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			

DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.94 T1 Delay Time Register – Index 67h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.95 SYSFAN Max Duty compare Source Select Register – Index 68h (Bank 1)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					SYSFAN Max Duty compare Source Select		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2	**SYSFAN Max Duty Source Select** 0: Disable AUXFAN1 Duty 1: Enable AUXFAN1 Duty
1	**SYSFAN Max Duty Source Select** 0: Disable AUXFAN0 Duty 1: Enable AUXFAN0 Duty
0	**SYSFAN Max Duty Source Select** 0: Disable CPUFAN Duty 1: Enable CPUFAN Duty

9.96 SYSFAN Max Duty Output Register – Index 69h (Bank 1)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFAN Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	**SYSFAN Max Duty Output**

9.97 CPUFAN Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		CPUFAN SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to CPUFANOUT Stop Value (Bank2, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**CPUFAN Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as CPUFAN monitoring source. 0 0 0 1 0: Select **CPUTIN** as CPUFAN monitoring source. 0 0 0 1 1: Select **AUXTIN0** as CPUFAN monitoring source. 0 0 1 0 0: Select **AUXTIN1** as CPUFAN monitoring source. 0 0 1 0 1: Select **AUXTIN2** as CPUFAN monitoring source. 0 0 1 1 0: Select **AUXTIN3** as CPUFAN monitoring source. 0 0 1 1 1: Select **AUXTIN4** as CPUFAN monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as CPUFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as CPUFAN monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as CPUFAN monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as CPUFAN monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as CPUFAN monitoring source.

BIT	DESCRIPTION
	1 0 0 1 1: Select **PCH_CHIP_TEMP** as CPUFAN monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as CPUFAN monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as CPUFAN monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as CPUFAN monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as CPUFAN monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as CPUFAN monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as CPUFAN monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as CPUFAN monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as CPUFAN monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as CPUFAN monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as CPUFAN monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as CPUFAN monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.98 CPUFAN Target Temperature Register / CPUFANIN Target Speed_L Register – Index 01h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUTIN Target Temperature / CPUFANIN Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	CPUFAN Target Temperature							
Fan Speed Cruise™	DESCRIPTION	CPUFANIN Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.99 CPUFAN MODE Register / CPUFAN TOLERRANCE Register – Index 02h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#(Bit2-0)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN MODE				Reserved	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L		
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-4	**CPUFANOUT Mode Select.** 0000: CPUFANOUT is in Manual Mode. (Default) 0001: CPUFANOUT is in Thermal Cruise Mode. 0010: CPUFANOUT is in Speed Cruise Mode. 0100: CPUFANOUT is in SMART FAN IV Mode.

3	**Reserved**
2-0	Tolerance of CPUFAN Target Temperature or CPUFANIN Target Speed_L.

9.100 CPUFANOUT Step Up Time Register – Index 03h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.101 CPUFANOUT Step Down Time Register – Index 04h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time CPUFANOUT takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.102 CPUFANOUT Stop Value Register – Index 05h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the CPUFANOUT value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.103 CPUFANOUT Start-up Value Register – Index 06h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, CPUFANOUT value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.104 CPUFANOUT Stop Time Register – Index 07h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes CPUFANOUT value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.105 CPUFANOUT Output Value Select Register – Index 09h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Value							
DEFAULT	0	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E1h] is the Default Speed Configuration Register of CPUFANOUT.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output Only	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.106 CPUFANIN Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 2)

Attribute: Read/Write

Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	CPUFANIN TOL_H			CPUFANIN Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	CPUFANIN Tolerance_H [5:3]
3-0	CPUFANIN Target Speed_H [11:8]

9.107 CPUFAN MODE Register / THERMAL MARGIN Register – Index 0Dh (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			Thermal Margin tolerance			Reserved	Thermal Margin enable
DEFAULT	0	0	0	0			0	0

BIT	DESCRIPTION
7-5	**Reserved**
4-2	**Thermal Margin tolerance**
1	**Reserved**
0	**Thermal Margin enable**

9.108 CPUFAN MODE Register / T control Register – Index 0Fh (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T control							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**T control**

9.109 CPUFAN (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 1 Register (T1).

9.110 CPUFAN (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	1	0	0	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 2 Register (T2).

9.111 CPUFAN (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 3 Register (T3).

9.112 CPUFAN (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature 4							

DEFAULT	0	1	0	0	0	1	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Temperature 4 Register (T4).

9.113 CPUFAN (SMART FAN™ IV) PWM1 Register – Index 27h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM1 Register.

9.114 CPUFAN (SMART FAN™ IV) PWM2 Register – Index 28h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM2 Register.

9.115 CPUFAN (SMART FAN™ IV) PWM3 Register – Index 29h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM3 Register.

9.116 CPUFAN (SMART FAN™ IV) PWM4 Register – Index 2Ah (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) PWM4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) PWM4 Register.

9.117 CPUFAN 3-Wire FAN Enable Register – Index 31h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_CPU_3WFAN
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_CPU_3WFAN (CPUFAN type setting)** 0: 4-wire fan 1: 3-wire fan

9.118 CPUFAN (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	CPUFAN (SMART FAN™ IV) Critical Temperature Register.

9.119 CPUFAN Enable Critical Duty – Index 36h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0

NAME	Reserved	En_CPU_CRITICAL_DUTY
DEFAULT	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_CPU_CRITICAL_DUTY (set 0 in manual mode)** 0: Load default Full Speed 8'hFF for CPUFANOUT. 1: Used Index 37 CRITICAL_DUTY Value for CPUFANOUT.

9.120 CPUFAN Critical Duty Register – Index 37h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFAN Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	CPUFAN Critical Duty.

9.121 CPUFANOUT Critical Temperature Tolerance Register – Index 38h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					CPUFANOUT Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**CPUFANOUT Critical Temperature Tolerance**

9.122 Weight value Configuration Register – Index 39h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	EN_CPUFAN_ WEIGHT	Reserved		CPU_WEIGHT_SEL				
DEFAULT	0	0		0	0	0	0	1

BIT	DESCRIPTION
7	**EN_CPUFAN_WEIGHT.** 0: Disable Weight Value Control for CPUFAN. 1: Enable Weight Value Control for CPUFAN.
6-5	**Reserved**
4-0	**CPUFAN Weighting Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as CPUFAN monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as CPUFAN monitoring source. 0 0 0 1 1: Select **AUXTIN0** as CPUFAN monitoring source. 0 0 1 0 0: Select **AUXTIN1** as CPUFAN monitoring source. 0 0 1 0 1: Select **AUXTIN2** as CPUFAN monitoring source. 0 0 1 1 0: Select **AUXTIN3** as CPUFAN monitoring source. 0 0 1 1 1: Reserved 0 1 0 0 0: Select **SMBUSMASTER 0** as CPUFAN monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as CPUFAN monitoring source. 0 1 0 1 0: Select **SMBUSMASTER 2** as CPUFAN monitoring source. 0 1 0 1 1: Select **SMBUSMASTER 3** as CPUFAN monitoring source. 0 1 1 0 0: Select **SMBUSMASTER 4** as CPUFAN monitoring source. 0 1 1 0 1: Select **SMBUSMASTER 5** as CPUFAN monitoring source. 0 1 1 1 0: Select **SMBUSMASTER 6** as CPUFAN monitoring source. 0 1 1 1 1: Select **SMBUSMASTER 7** as CPUFAN monitoring source. 1 0 0 0 0: Select **PECI Agent 0** as CPUFAN monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as CPUFAN monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as CPUFAN monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as CPUFAN monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as CPUFAN monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as CPUFAN monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as CPUFAN monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as CPUFAN monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as CPUFAN monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as CPUFAN monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as CPUFAN monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as CPUFAN monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as CPUFAN monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as CPUFAN monitoring source.

9.123 CPUFANOUT Temperature Step Register – Index 3Ah (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Temperature Step (CPU_TEMP_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Step**

9.124 CPUFANOUT Temperature Step Tolerance Register – Index 3Bh (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Temperature Step Tolerance (CPU_TEMP_STEP_TOL)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Step Tolerance**

9.125 CPUFANOUT Weight Step Register – Index 3Ch (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
BIT	CPUFANOUT Weight Step (CPU_WEIGHT_STEP)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Weight Step**

9.126 CPUFANOUT Temperature Base Register – Index 3Dh (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_TEMP_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Temperature Base**

9.127 CPUFANOUT Temperature Fan Duty Base Register – Index 3Eh (Bank 2)

Attribute: Read/Write
Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT Temperature Base (CPU_FC_BASE)							
DEFAULT	0							

BIT	DESCRIPTION
7-0	**CPUFANOUT Start point of Fan Duty increasing**

9.128 CPUFAN PECIERR DUTY Enable Register – Index 3Fh (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_CPU_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**
1-0	**EN_CPU_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_CPUOUT** Value for CPUFANOUT. 10,11: Keep Full Speed

9.129 CPUFANOUT Pre-Configured Register For PECI Error – Index 41h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANOUT pre-configured register for PECI error (PECI_ERR_CPUOUT)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**CPUFANOUT pre-configured register for PECI error.**

9.130 DUTY PER STEP Register – Index 66h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.131 T1 Delay Time Register – Index 67h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.132 CPUFAN Max Duty compare Source Select Register – Index 68h (Bank 2)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					CPUFAN Max Duty compare Source Select		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2	**CPUFAN Max Duty Source Select** 0: Disable AUXFAN1 Duty 1: Enable AUXFAN1 Duty
1	**CPUFAN Max Duty Source Select** 0: Disable AUXFAN0 Duty 1: Enable AUXFAN0 Duty
0	**CPUFAN Max Duty Source Select** 0: Disable SYSFAN Duty 1: Enable SYSFAN Duty

9.133 CPUFAN Max Duty Output Register – Index 69h (Bank 2)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0

NAME	CPUFAN Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	**CPUFAN Max Duty Output**

9.134 AUXFAN0 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN0 SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT0 Stop Value (Bank3, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**AUXFAN0 Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN0 monitoring source. 0 0 0 1 0: Select **CPUTIN** as AUXFAN0 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as AUXFAN0 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as AUXFAN0 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as AUXFAN0 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as AUXFAN0 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as AUXFAN0 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as AUXFAN0 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as AUXFAN0 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as AUXFAN0 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as AUXFAN0 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN0 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as AUXFAN0 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as AUXFAN0 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as AUXFAN0 monitoring source.

BIT	DESCRIPTION
	1 0 1 1 0: Select **Agent0 Dimm0** as AUXFAN0 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as AUXFAN0 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as AUXFAN0 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as AUXFAN0 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as AUXFAN0 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as AUXFAN0 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as AUXFAN0 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as AUXFAN0 monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as AUXFAN0 monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.135 AUXFAN0 Target Temperature Register / AUXFANIN0 Target Speed_L Register – Index 01h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN0 Target Temperature / AUXFANIN0 Target Speed_L / AUXFAN0 Target Thermal Margin							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN0 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN0 Target Speed [7:0], [11:8] associate index 0C [3:0]							
SMART FAN™ IV	DESCRIPTION	AUXFANIN0 Target Thermal Margin							

9.136 AUXFAN0 MODE Register / AUXFAN0 TOLERRANCE Register – Index 02h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#(Bit2-0)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 MODE				Reseved	Tolerance of AUXFAN0 Target Temperature or AUXFANIN0 Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**AUXFANOUT0 Mode Select.** 0000: **AUXFANOUT0** is in Manual Mode. **(Default)** 0001: **AUXFANOUT0** is in Thermal Cruise Mode. 0010: **AUXFANOUT0** is as Speed Cruise Mode. 0100: **AUXFANOUT0** is in SMART FAN IV Mode.
3	**Reseved**

2-0	Tolerance of AUXFAN0 Target Temperature or AUXFANIN0 Target Speed_L.

9.137 AUXFANOUT0 Step Up Time Register – Index 03h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT0 takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.138 AUXFANOUT0 Step Down Time Register – Index 04h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT0 takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.139 AUXFANOUT0 Stop Value Register – Index 05h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT0 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.140 AUXFANOUT0 Start-up Value Register – Index 06h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, AUXFANOUT0 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.141 AUXFANOUT0 Stop Time Register – Index 07h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes AUXFANOUT0 value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.142 AUXFANOUT0 Output Value Select Register – Index 09h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 Value							
DEFAULT	1	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E2h] is the Default Speed Configuration Register of AUXFANOUT0.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.143 AUXFANIN0 Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUXFANIN0 TOL_H			AUXFANIN0 Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	AUXFANIN0 Tolerance_H [5:3]
3-0	AUXFANIN0 Target Speed_H [11:8]

9.144 AUXFAN0 MODE Register / THERMAL MARGIN Register – Index 0Dh (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved			Thermal Margin tolerance			Reserved	Thermal Margin enable
DEFAULT	0	0	0	0			0	0

BIT	DESCRIPTION
7-5	**Reserved**
4-2	**Thermal Margin tolerance**
1	**Reserved**
0	**Thermal Margin enable**

9.145 AUXFAN0 MODE Register / T control Register – Index 0Fh (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T control							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**T control**

9.146 AUXFAN0 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 3)

Attribute: Read/Write

Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 1 Register (T1).

9.147 AUXFAN0 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 2 Register (T2).

9.148 AUXFAN0 (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 3 Register (T3).

9.149 AUXFAN0 (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Temperature 4 Register (T4).

9.150 AUXFAN0 (SMART FAN™ IV) PWM 1 Register – Index 27h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 1 Register.

9.151 AUXFAN0 (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 2 Register.

9.152 AUXFAN0 (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 3 Register.

9.153 AUXFAN0 (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) PWM 4 Register.

9.154 AUXFAN0 3-Wire Enable Register – Index 31h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_AUX0_3WFAN
DEFAULT	0		0					0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_AUX0_3WFAN (AUXFAN0 type setting)** 0: 4-wire fan 1: 3-wire fan

9.155 AUXFAN0 (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN0 (SMART FAN™ IV) Critical Temperature Register

9.156 AUXFAN0 Enable Critical Duty – Index 36h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX0_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUX0_CRITICAL_DUTY (set 0 in manual mode)** 0: Load default Full Speed 8'hFF for AUXFANOUT0. 1: Used Index 37 CRITICAL_DUTY Value for AUXFANOUT0.

9.157 AUXFAN0 Critical Duty Register – Index 37h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN0 Critical Duty.

9.158 AUXFANOUT0 Critical Temperature Tolerance Register – Index 38h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT0 Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**AUXFANOUT0 Critical Temperature Tolerance**

9.159 AUXFAN0 PECIERR DUTY Enable Register – Index 3Fh (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX0_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**

1-0	**EN_AUX0_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_AUXOUT0** Value for AUXFANOUT0. 10,11: Keep Full Speed

9.160 AUXFANOUT0 Pre-Configured Register For PECI Error – Index 41h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT0 pre-configured register for PECI error (PECI_ERR_AUXOUT0)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**AUXFANOUT0 pre-configured register for PECI error.**

9.161 DUTY PER STEP Register – Index 66h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.162 T1 Delay Time Register – Index 67h (Bank 3)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.163 AUXFAN0 Max Duty compare Source Select Register – Index 68h (Bank 3)

Attribute: Read/Write

Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					AUXFAN0 Max Duty compare Source Select		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2	**AUXFAN0 Max Duty Source Select** 0: Disable AUXFAN1 Duty 1: Enable AUXFAN1 Duty
1	**AUXFAN0 Max Duty Source Select** 0: Disable CPUFAN Duty 1: Enable CPUFAN Duty
0	**AUXFAN0 Max Duty Source Select** 0: Disable SYSFAN Duty 1: Enable SYSFAN Duty

9.164 AUXFAN0 Max Duty Output Register – Index 69h (Bank 3)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN0 Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	**AUXFAN0 Max Duty Output**

9.165 PCH_CHIP_CPU_MAX_TEMP Register – Index 00h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_CPU_MAX_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CHIP_CPU_MAX_TEMP:** The maximum temperature in absolute degree C, of the CPU and MCH.

9.166 PCH_CHIP_TEMP Register – Index 01h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CHIP_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CHIP_TEMP** The IBX_CHIP temperature in degree C.

9.167 PCH_CPU_TEMP_H Register – Index 02h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CPU_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_CPU_TEMP_H** The CPU temperature in degree C. (Integer Part)

9.168 PCH_CPU_TEMP_L Register – Index 03h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_CPU_TEMP_L						Reserved	Reading _Flag
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**PCH_CPU_TEMP_L** The CPU temperature in degree C. (Fractional Part)
1	**Reserved**
0	**Reading_Flag:** If there is an error when the IBX read the data from the CPU, then Bit0 is set to '1'.

9.169 PCH_MCH_TEMP Register – Index 04h (Bank 4)

Attribute: Read

Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_MCH_TEMP							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_MCH_TEMP** The MCH temperature in degree C.

9.170 Agent0 Dimm0 Register – Index 05h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Agent0 Dimm0							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Agent0 Dimm0** The Agent0 Dimm0 temperature.

9.171 Agent0 Dimm1 Register – Index 06h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Agent0 Dimm1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Agent0 Dimm1** The Agent0 Dimm1 temperature.

9.172 Agent1 Dimm0 Register – Index 07h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Agent1 Dimm0							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Agent1 Dimm0** The Agent1 Dimm0 temperature.

9.173 Agent1 Dimm1 Register – Index 08h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Agent1 Dimm1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Agent1 Dimm1** The Agent1 Dimm1 temperature.

9.174 PCH_TSI0_TEMP_H Register – Index 09h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI0_TEMP_H** The TSI High-Byte temperature in degree C.

9.175 PCH_TSI0_TEMP_L Register – Index 0Ah (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI0_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI0_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.176 PCH_TSI1_TEMP_H Register – Index 0Bh (Bank 4)

Attribute: Read
Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI1_TEMP_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**PCH_TSI1_TEMP_H** The TSI High-Byte temperature in degree C.

9.177 PCH_TSI1_TEMP_L Register – Index 0Ch (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PCH_TSI1_TEMP_L			Reserved				
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**PCH_TSI1_TEMP_L** The TSI Low-Byte temperature in degree C.
4-0	**Reserved**

9.178 ByteTemp0 Register – Index 19h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	ByteTemp_H							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**ByteTemp0** The Byte format Device0 Byte temperature in degree C.

9.179 ByteTemp1 Register – Index 1Ah (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	ByteTemp_L							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**ByteTemp1** The Byte format Device1 Byte temperature in degree C.

9.180 VIN1 High Limit Compared Voltage Register – Index 23h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	VIN1 High Limit Compared Voltage (VIN1_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION
7-0	**VIN1 High Limit Compared Voltage.** Default: 0x96h (1.2V)

9.181 VIN1 Low Limit Compared Voltage Register – Index 24h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	VIN1 Low Limit Compared Voltage (VIN1_LimtH)							
DEFAULT	0	1	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	**VIN1 Low Limit Compared Voltage.** Default: 0x64h (0.8V)

9.182 VIN0 High Limit Compared Voltage Register – Index 25h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	VIN0 High Limit Compared Voltage (VIN0_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION
7-0	**VIN0 High Limit Compared Voltage.** Default: 0x96h (1.2V)

9.183 VIN0 Low Limit Compared Voltage Register – Index 26h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	VIN0 Low Limit Compared Voltage (VIN0_LimtH)							
DEFAULT	0	1	1	0	0	1	0	0

BIT	DESCRIPTION
7-0	**VIN0 Low Limit Compared Voltage.** Default: 0x64h (0.8V)

9.184 AVSB High Limit Compared Voltage Register – Index 27h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AVSB High Limit Compared Voltage (AVSB _LimtH)							
DEFAULT	1	1	1	0	0	0	0	1

BIT	DESCRIPTION
7-0	**AVSB High Limit Compared Voltage.** Default: 0xE1h (1.8V *2)

9.185 AVSB Low Limit Compared Voltage Register – Index 28h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AVSB Low Limit Compared Voltage (AVSB_LimtH)							
DEFAULT	1	0	0	1	0	1	1	0

BIT	DESCRIPTION
7-0	**AVSB Low Limit Compared Voltage (AVSB_LimtH).** Default: 0x96h (1.2V *2)

9.186 Voltage Comparation Interrupt Status Register - Index 42h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					AVSB_Warn	VIN0_Warn	VIN1_Warn
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Reserved**

BIT	DESCRIPTION
2	**AVSB_Warn.** A one indicates the limit of AVSB voltage has been exceeded.
1	**VIN0_Warn.** A one indicates the limit of VIN0 voltage has been exceeded.
0	**VIN1_Warn** A one indicates the limit of VIN1 voltage has been exceeded.

9.187 AUXTIN1 Temperature Sensor Offset Register – Index 4Ah (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN1 Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.188 AUXTIN2 Temperature Sensor Offset Register – Index 4Bh (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN2 Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.189 AUXTIN3 Temperature Sensor Offset Register – Index 4Ch (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7-0	**AUXTIN3 Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.190 AUXTIN4 Temperature Sensor Offset Register – Index 4Dh (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN4 Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.191 Interrupt Status Register 3 – Index 50h (Bank 4)

Attribute: Read Clear
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2	AUXFANOUT1	AUXFANIN2	AUXFANIN1	RESERVED		VBAT	3VSB
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**AUXFANOUT2.** “1” indicates that AUXFANOUT2 works for three minutes at the full fan speed.
6	**AUXFANOUT1.** “1” indicates that AUXFANOUT1 works for three minutes at the full fan speed.
5	**AUXFANIN2. A one indicates the fan count limit of AUXFANIN2 has been exceeded.**
4	**AUXFANIN1. A one indicates the fan count limit of AUXFANIN1 has been exceeded.**
2-3	**Reserved**
1	**VBAT.** A one indicates the high or low limit of VBAT has been exceeded.
0	**3VSB.** A one indicates the high or low limit of 3VSB has been exceeded.

9.192 SMI# Mask Register 4 – Index 51h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED	TAR5	TAR4	TAR3	RESERVED		SMSKVBAT	SMSKVSB
DEFAULT	1	1	1	1	0	0	1	1

BIT	DESCRIPTION
7	**Reserved**
6	**TAR5.** A one disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
5	**TAR4.** A one disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
4	**TAR3.** A one disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt. (See Interrupt Status Register 3 – Index 45h (Bank 0))
3-2	**Reserved**
1	**SMSKVBAT.** A one disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))
0	**SMSKVSB.** A one disables the corresponding interrupt status bit for the $\overline{SMI}$ interrupt. (See Interrupt Status Register 3 – Index 50h (Bank 4))

9.193 SYSTIN Temperature Sensor Offset Register – Index 54h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSTIN Temperature Offset Value.** The value in this register is added to the monitored value so that the read value will be the sum of the monitored value and this offset value.

9.194 CPUTIN Temperature Sensor Offset Register – Index 55h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUTIN Temperature Offset Value.** The value in this register will be added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.195 AUXTIN0 Temperature Sensor Offset Register – Index 56h (Bank 4)

Attribute: Read/Write
Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	OFFSET<7:0>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXTIN0 Temperature Offset Value.** The value in this register is added to the monitored value so that the read value is the sum of the monitored value and this offset value.

9.196 Real Time Hardware Status Register I – Index 59h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN _STS	SYSFANIN _STS	CPUTIN _STS	SYSTIN _STS	3VCC _STS	AVSB _STS	VIN1 _STS	CPUVCORE _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**CPUFANIN_STS. CPUFANIN Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
6	**SYSFANIN_STS. SYSFANIN Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
5	**CPUTIN_STS. CPUTIN Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
4	**SYSTIN_STS. SYSTIN Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
3	**3VCC_STS. 3VCC Voltage Status.** 1: 3VCC voltage is over or under the allowed range. 0: 3VCC voltage is in the allowed range.
2	**AVSB_STS. AVSB Voltage Status.** 1: AVSB voltage is over or under the allowed range. 0: AVSB voltage is in the allowed range.
1	**VIN1_STS. VIN1 Voltage Status.** 1: VIN1 voltage is over or under the allowed range. 0: VIN1 voltage is in the allowed range.
0	**CPUVCORE_STS. CPUVCORE Voltage Status.** 1: CPUVCORE voltage is over or under the allowed range. 0: CPUVCORE voltage is in the allowed range.

9.197 Real Time Hardware Status Register II – Index 5Ah (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TAR2_STS	TAR1_STS	Reserved	CASEOPEN0_STS	AUXFANIN0_STS	AUXFANIN1_STS	CASEOPEN1_STS	VIN0_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**TAR2_STS. Smart Fan of CPUFANIN Warning Status.** 1: Selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: Selected temperature has not reached the warning range.
6	**TAR1_STS. Smart Fan of SYSFANIN Warning Status.** 1: SYSTIN temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: SYSTIN temperature has not reached the warning range.
5	**Reserved**
4	**CASEOPEN0_STS. CaseOpen Status.** 1: Caseopen0 is detected and latched. 0: Caseopen0 is not latched.
3	**AUXFANIN0_STS. AUXFANIN0 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
2	**AUXFANIN1_STS. AUXFANIN1 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
1	**CASEOPEN1_STS. CaseOpen Status.** 1: Caseopen1 is detected and latched. 0: Caseopen1 is not latched.
0	**VIN0_STS. VIN0 Voltage Status.** 1: VIN0 voltage is over or under the allowed range. 0: VIN0 voltage is in the allowed range.

9.198 Real Time Hardware Status Register III – Index 5Bh (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2_STS	TAR5_STS	VIN8_STS	VIN4_STS	TAR4_STS	TAR3_STS	VBAT_STS	VSB_STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**AUXFANIN2_STS. AUXFANIN2 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
6	**TAR5_STS. Smart Fan of AUXFANIN2 Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: The selected temperature has not reached the warning range.
5	**VIN8_STS. VIN8 Voltage Status.** 1: VIN8 voltage is over or under the allowed range. 0: VIN8 voltage is in the allowed range.
4	**VIN4_STS. VIN4 Voltage Status.** 1: VIN4 voltage is over or under the allowed range. 0: VIN4 voltage is in the allowed range.
3	**TAR4_STS. Smart Fan of AUXFANIN1 Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: The selected temperature has not reached the warning range.
2	**TAR3_STS. Smart Fan of AUXFANIN0 Warning Status.** 1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: The selected temperature has not reached the warning range.
1	**VBAT_STS. VBAT Voltage Status.** 1: The VBAT voltage is over or under the allowed range. 0: The VBAT voltage is in the allowed range.
0	**VSB_STS. 3VSB Voltage Status.** 1: The 3VSB voltage is over or under the allowed range. 0: The 3VSB voltage is in the allowed range.

9.199 Real Time Hardware Status Register III – Index 5Dh (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME							AUXFANIN3 _STS	TAR6 _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**RESERVED**
1	**AUXFANIN3 Status.** 1: Fan speed count is over the threshold value. 0: Fan speed count is in the allowed range.
0	**TAR6_STS. Smart Fan of AUXFANIN3 Warning Status.**

BIT	DESCRIPTION
7-2	**RESERVED**
	1: The selected temperature has been over the target temperature for three minutes at full fan speed in Thermal Cruise Mode and SMART FAN™ IV. 0: The selected temperature has not reached the warning range.

9.200 Is<8:1> Current Register – Index 60h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Is<8:1>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Is<8:1>.** Current measure by current measure IC (1LSB=31.25mA)

9.201 Is<0> Current Register – Index 61h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							Is<0>
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
0	**Is<0>.** Current measure by current measure IC (1LSB=31.25mA)

9.202 POWER <9:2> Register – Index 62h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	POWER <9:2>							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**POWER <9:2>.** Power calculate by IO (1LSB=0.25W)

9.203 POWER<1:0> Register – Index 63h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						POWER<1:0>	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-1	**Reserved**
1:0	**POWER<1:0>.** Power calculate by IO (1LSB=0.25W)

9.204 VIN Register – Index 64h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	VIN							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**VIN.** Power voltage given by customer. (1LSB=128mV)

9.205 Rreg Setting Register – Index 65h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Rreg							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Rreg.** Equivalent electric impedance in order to calculate Is. (1LSB=1m ohm)

9.206 Reg_Ratio_K and POWER_Voltage Enable Register – Index 66h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0

NAME	Reg_Ration_K				Reserved			Power_ Volt_En
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**Reg_Ration_K:** The ration in order to make power voltage input to IO is below 2.048. Reg_Ration_K=(R1+R2)/(R1)
3-1	**Reserved**
0	**Power_Volt_En** 0:Power voltage is monitored by IO 1:Power voltage is given by customer

9.207 POWER_V Register – Index 67h (Bank 4)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	POWER_V							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**POWER_V:** Power voltage (1LSB=128mV)

9.208 Value RAM — Index 80h ~ 96h (Bank 4)

ADDRESS A6-A0	DESCRIPTION
80h	CPUVCORE reading
81h	VIN1 reading
82h	AVSB reading
83h	3VCC reading
84h	VIN0 reading
85h	VIN8 reading
86h	VIN4 reading
87h	3VSB reading
88h	VBAT reading
89h	VTT reading
8Ah	VIN5 reading
8Bh	VIN6 reading
8Ch	VIN2 reading
8Dh	VIN3 reading

ADDRESS A6-A0	DESCRIPTION
80h	CPUVCORE reading
81h	VIN1 reading
82h	AVSB reading
83h	3VCC reading
84h	VIN0 reading
85h	VIN8 reading
8Eh	VIN7 reading
8Fh	Reserved
90h	SYSTIN temperature reading
91h	CPUTIN temperature reading
92h	AUXTIN0 temperature reading
93h	AUXTIN1 temperature reading
94h	AUXTIN2 temperature reading
95h	AUXTIN3 temperature reading

9.209 (SYSFANIN) FANIN1 COUNT High-byte Register – Index B0h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT1 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT1_H:** 13-bit SYSFANIN Fan Count, High Byte

9.210 (SYSFANIN) FANIN1 COUNT Low-byte Register – Index B1h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT1 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANCNT1_L:** 13-bit SYSFANIN Fan Count, Low Byte

9.211 (CPUFANIN) FANIN2 COUNT High-byte Register – Index B2h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT2 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT2_H:** 13-bit CPUFANIN Fan Count, High Byte

9.212 (CPUFANIN) FANIN2 COUNT Low-byte Register – Index B3h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT2 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANCNT2_L:** 13-bit CPUFANIN Fan Count, Low Byte

9.213 (AUXFANIN0) FANIN3 COUNT High-byte Register – Index B4h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT3 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT3_H:** 13-bit AUXFANIN0 Fan Count, High Byte

9.214 (AUXFANIN0) FANIN3 COUNT Low-byte Register – Index B5h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0

NAME	RESERVED	FANCNT3 [4:0]
DEFAULT	0	1F

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANCNT3_L:** 13-bit AUXFANIN0 Fan Count, Low Byte

9.215 (AUXFANIN1) FANIN4 COUNT High-byte Register – Index B6h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT4 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT4_H:** 13-bit AUXFANIN0 Fan Count, High Byte

9.216 (AUXFANIN1) FANIN4 COUNT Low-byte Register – Index B7h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT4 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANCNT4_L:** 13-bit AUXFANIN0 Fan Count, Low Byte

9.217 (AUXFANIN2) FANIN5 COUNT High-byte Register – Index B8h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT5 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION

7-0	**FANCNT5_H:** 13-bit AUXFANIN2 Fan Count, High Byte

9.218 (AUXFANIN2) FANIN5 COUNT Low-byte Register – Index B9h (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT5 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANCNT5_L:** 13-bit AUXFANIN2 Fan Count, Low Byte

9.219 (AUXFANIN3) FANIN6 COUNT High-byte Register – Index BAh (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANCNT6 [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANCNT6_H:** 13-bit AUXFANIN3 Fan Count, High Byte

9.220 (AUXFANIN3) FANIN6 COUNT Low-byte Register – Index BBh (Bank 4)

Attribute: Read
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANCNT6 [4:0]				
DEFAULT	0			1F				

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANCNT6_L:** 13-bit AUXFANIN3 Fan Count, Low Byte

9.221 SYSFANIN SPEED HIGH-BYTE VALUE (RPM) - Index C0h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSFANIN SPEED HIGH-BYTE VALUE.**

9.222 SYSFANIN SPEED LOW-BYTE VALUE (RPM) - Index C1h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSFANIN SPEED LOW-BYTE VALUE.**

9.223 CPUFANIN SPEED HIGH-BYTE VALUE (RPM) – Index C2h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN SPEED HIGH-BYTE VALUE.**

9.224 CPUFANIN SPEED LOW-BYTE VALUE (RPM) – Index C3h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN SPEED LOW-BYTE VALUE.**

9.225 AUXFANIN0 SPEED HIGH-BYTE VALUE (RPM) – Index C4h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN0 SPEED HIGH-BYTE VALUE.**

9.226 AUXFANIN0 SPEED LOW-BYTE VALUE (RPM) – Index C5h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN0 SPEED LOW-BYTE VALUE.**

9.227 AUXFANIN1 SPEED HIGH-BYTE VALUE (RPM) – Index C6h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED HIGH –BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIIN1 SPEED HIGH-BYTE VALUE.**

9.228 AUXFANIN1 SPEED LOW-BYTE VALUE (RPM) – Index C7h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN1 SPEED LOW-BYTE VALUE.**

9.229 AUXFANIN2 SPEED HIGH-BYTE VALUE (RPM) – Index C8h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED HIGH –BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIIN2 SPEED HIGH-BYTE VALUE.**

9.230 AUXFANIN2 SPEED LOW-BYTE VALUE (RPM) – Index C9h (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN2 SPEED LOW-BYTE VALUE.**

9.231 AUXFANIN3 SPEED HIGH-BYTE VALUE (RPM) – Index CAh (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN3 SPEED HIGH –BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIIN3 SPEED HIGH-BYTE VALUE.**

9.232 AUXFANIN3 SPEED LOW-BYTE VALUE (RPM) – Index CBh (Bank 4)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN3 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN3 SPEED LOW-BYTE VALUE.**

9.233 PECI Agent0 Calibration Temp – Index F4h (Bank 4)

Attribute: Read / Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Agent0 Calibration Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**The temperature is after PECI Agent0 Calibration**

9.234 PECI Agent1 Calibration Temp – Index F5h (Bank 4)

Attribute: Read / Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Agent1 Calibration Temperature							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**The temperature is after PECI Agent1 Calibration**

9.235 PECI Agent0 Calibration Control Register – Index F8h (Bank 4)

Attribute: Read / Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	UP or Down Times					Adjust unit		

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**UP or Down Times For PECI Agent0 Calibration**
2-0	**Adjust unit for PECI Agent0 Calibration**

9.236 PECI Agent1 Calibration Control Register – Index F9h (Bank 4)

Attribute: Read / Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	UP or Down Times					Adjust unit		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**UP or Down Times For PECI Agent1 Calibration**
2-0	**Adjust unit for PECI Agent1 Calibration**

9.237 PECI Agent0 Calibration Control Register – Index FAh (Bank 4)

Attribute: Read / Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Update Time					Reserved		Enable
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Update Times For PECI Agent0 Calibration (0.1~3.2sec)**
2-1	**Reserved**
0	**Function Enable for PECI Agent0 Calibration**

9.238 PECI Agent1 Calibration Control Register – Index FBh (Bank 4)

Attribute: Read / Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Update Time					Reserved		Enable
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Update Times For PECI Agent1 Calibration (0.1~3.2sec)**
2-1	**Reserved**
0	**Function Enable for PECI Agent1 Calibration**

9.239 Value RAM 2 — Index 50h-63h (Bank 5)

ADDRESS A6-A0	DESCRIPTION
54h	**3VSB High Limit**
55h	**3VSB Low Limit**
56h	**VBAT High Limit**
57h	**VBAT Low Limit**
58h	**VTT High Limit**
59h	**VTT Low Limit**
5Ah	**VIN5 High Limit**
5Bh	**VIN5 Low Limit**
5Ch	**VIN6 High Limit**
5Dh	**VIN6 Low Limit**
5Eh	**VIN2 High Limit**
5Fh	**VIN2 Low Limit**
60h	**VIN3 High Limit**
61h	**VIN3 Low Limit**
62h	**VIN7 High Limit**
63h	**VIN7 Low Limit**
64h	**VIN9 High Limit**
65h	**VIN9 Low Limit**

9.240 SMI# Mask Register 1 – Index 66h (Bank 5)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	VIN7	VIN3	VIN2	VIN6	VIN5	VTT
DEFAULT	0	1	1	1	1	1	1	1

BIT	DESCRIPTION	
7	**Reserved**	A one disables the corresponding interrupt status bit for the $\overline{\text{SMI}}$ interrupt. (See Interrupt Status Register 1 – Index 41h (Bank0))
6	**Reserved**	
5	**VIN7**	

BIT	DESCRIPTION	
4	**VIN3**	
3	**VIN2**	
2	**VIN6**	
1	**VIN5**	
0	**VTT**	

9.241 Interrupt Status Register – Index 67h (Bank 5)

Attribute: Read Clear
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	VIN7	VIN3	VIN2	VIN6	VIN5	VTT
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved**
6	**Reserved**
5	**VIN7.** A one indicates the high or low limit of VIN7 has been exceeded.
4	**VIN3.** A one indicates the high or low limit of VIN3 has been exceeded.
3	**VIN2.** A one indicates the high or low limit of VIN2 has been exceeded.
2	**VIN6.** A one indicates the high or low limit of VIN6 has been exceeded.
1	**VIN5.** A one indicates the high or low limit of VIN5 has been exceeded.
0	**VTT.** A one indicates the high or low limit of VTT has been exceeded.

9.242 Real Time Hardware Status Register – Index 68h (Bank 5)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	VIN9 _STS	VIN7 _STS	VIN3 _STS	VIN2 _STS	VIN6 _STS	VIN5 _STS	VTT _STS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved**
6	**VIN9_STS. VIN9 Voltage Status.** 1: VIN9 voltage is over or under the allowed range. 0: VIN9 voltage is in the allowed range.
5	**VIN7_STS. VIN7 Voltage Status.** 1: VIN7 voltage is over or under the allowed range.

BIT	DESCRIPTION
	0: VIN7 voltage is in the allowed range.
4	**VIN3_STS. VIN3 Voltage Status.** 1: VIN3 voltage is over or under the allowed range. 0: VIN3 voltage is in the allowed range.
3	**VIN2_STS. VIN2 Voltage Status.** 1: VIN2 voltage is over or under the allowed range. 0: VIN2 voltage is in the allowed range.
2	**VIN6_STS. VIN6 Voltage Status.** 1: VIN6 voltage is over or under the allowed range. 0: VIN6 voltage is in the allowed range.
1	**VIN5_STS. VIN5 Voltage Status.** 1: VIN5 voltage is over or under the allowed range. 0: VIN5 voltage is in the allowed range.
0	**VTT_STS. VTT Voltage Status.** 1: VTT voltage is over or under the allowed range. 0: VTT voltage is in the allowed range.

9.243 Close-Loop Fan Control RPM mode Register – Index 00 (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		En_AUX3_RPM	En_AUX2_RPM	En_AUX1_RPM	En_AUX0_RPM	En_CPU_RPM	En_SYS_RPM
DEFAULT	0		0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**RESERVED**
5	**En_AUX3_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.
4	**En_AUX2_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.
3	**En_AUX1_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.
2	**En_AUX0_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.
1	**En_CPU_RPM** 0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.
0	**En_SYS_RPM**

	0: Disable SMART FAN™ IV Close Loop Fan Control RPM Mode. 1: Enable SMART FAN™ IV Close Loop Fan Control RPM Mode.

9.244 SYSFAN RPM Mode Tolerance Register – Index 01 (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ SYS_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit0）, unit is 100 RPM.

9.245 CPUFAN RPM Mode Tolerance Register – Index 02 (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ CPU_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit1）, unit is 100 RPM.

9.246 AUXFAN0 RPM Mode Tolerance Register – Index 03 (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ AUX0_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**

3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit2）, unit is 100 RPM.

9.247 AUXFAN1 RPM Mode Tolerance Register – Index 04 (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ AUX1_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit3）, unit is 100 RPM.

9.248 AUXFAN2 RPM Mode Tolerance Register – Index 05 (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ AUX2_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit4）, unit is 100 RPM.

9.249 Enable RPM High Mode Register – Index 06 (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		En_AUX3_RPM_HIGH	En_AUX2_RPM_HIGH	En_AUX1_RPM_HIGH	En_AUX0_RPM_HIGH	En_CPU_RPM_HIGH	En_SYS_RPM_HIGH
DEFAULT	0		0	0	0	0	0	0

BIT	DESCRIPTION

7-6	**RESERVED**
5	**En_AUX3_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
4	**En_AUX2_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
3	**En_AUX1_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
2	**En_AUX0_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
1	**En_CPU_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable
0	**En_SYS_RPM_HIGH** For High Speed Fan Control at RPM Mode, the unit is 100 RPM. Support 100 rpm ~ 25500 rpm Fan, 0: Disable 1: Enable

9.250 SMIOVT1 Temperature Source Select Register – Index 21 (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC1				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT1 Temperature selection.** **Bits** **4 3 2 1 0**

	0 0 0 0 1: Select **SYSTIN** as SMIOVT1 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT1 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SMIOVT1 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SMIOVT1 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SMIOVT1 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SMIOVT1 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as SMIOVT1 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as SMIOVT1 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SMIOVT1 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as SMIOVT1 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SMIOVT1 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT1 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SMIOVT1 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SMIOVT1 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SMIOVT1 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as SMIOVT1 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as SMIOVT1 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as SMIOVT1 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as SMIOVT1 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as SMIOVT1 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as SMIOVT1 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as SMIOVT1 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as SMIOVT1 monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as SMIOVT1 monitoring source.

9.251 SMIOVT2 Temperature Source Select Register – Index 22 (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC2				
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT2 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT2 monitoring source. 0 0 0 1 0: Select **CPUTIN** as SMIOVT2 monitoring source. (Default)

	0 0 0 1 1: Select **AUXTIN0** as SMIOVT2 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SMIOVT2 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SMIOVT2 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SMIOVT2 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as SMIOVT2 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as SMIOVT2 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SMIOVT2 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as SMIOVT2 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SMIOVT2 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT2 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SMIOVT2 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SMIOVT2 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SMIOVT2 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as SMIOVT2 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as SMIOVT2 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as SMIOVT2 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as SMIOVT2 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as SMIOVT2 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as SMIOVT2 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as SMIOVT2 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as SMIOVT2 monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as SMIOVT2 monitoring source.

9.252 AUXFAN3 RPM Mode Tolerance Register – Index 23 (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ AUX3_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit5）, unit is 100 RPM.

9.253 AUXFAN4 RPM Mode Tolerance Register – Index 24 (Bank 6)

Attribute: Read/Write
Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED				Generic_Tol_ AUX4_RPM			
DEFAULT	0				0			

BIT	DESCRIPTION
7-4	**RESERVED**
3-0	Tolerance of RPM mode, unit 50 RPM. If Enable RPM High Mode（Bank6 index6 bit6）, unit is 100 RPM.

9.254 (SYSFANIN) Fan Count Limit High-byte Register – Index 3Ah (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANIN1_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, High Byte

9.255 (SYSFANIN) Fan Count Limit Low-byte Register – Index 3Bh (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN1_HL [4:0]				
DEFAULT	000			11111				

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANIN1_HL:** 13-bit SYSFANIN Fan Count Limit, Low Byte

9.256 (CPUFANIN) Fan Count Limit High-byte Register – Index 3Ch (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANIN2_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, High Byte

9.257 (CPUFANIN) Fan Count Limit Low-byte Register – Index 3Dh (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN2_HL [4:0]				
DEFAULT	000			11111				

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANIN2_HL:** 13-bit CPUFANIN Fan Count Limit, Low Byte

9.258 (AUXFANIN0) Fan Count Limit High-byte Register – Index 3Eh (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANIN3_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN3_HL:** 13-bit AUXFANIN0 Fan Count Limit, High Byte

9.259 (AUXFANIN0) Fan Count Limit Low-byte Register – Index 3Fh (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN3_HL [4:0]				
DEFAULT	000			11111				

BIT	DESCRIPTION

7-5	**Reserved**
4-0	**FANIN3_HL:** 13-bit AUXFANIN0 Fan Count Limit, Low Byte

9.260 (AUXFANIN1) Fan Count Limit High-byte Register – Index 40h (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANIN4_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN4_HL:** 13-bit AUXFANIN1 Fan Count Limit, High Byte

9.261 (AUXFANIN1) Fan Count Limit Low-byte Register – Index 41h (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN4_HL [4:0]				
DEFAULT	000			11111				

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANIN4_HL:** 13-bit AUXFANIN1 Fan Count Limit, Low Byte

9.262 (AUXFANIN2) Fan Count Limit High-byte Register – Index 42h (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANIN5_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN5_HL:** 13-bit AUXFANIN2 Fan Count Limit, High Byte

9.263 (AUXFANIN2) Fan Count Limit Low-byte Register – Index 43h (Bank 6)

Attribute: Read /Write
Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN5_HL [4:0]				
DEFAULT	000			11111				

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANIN5_HL:** 13-bit AUXFANIN2 Fan Count Limit, Low Byte

9.264 SYSFANIN Revolution Pulses Selection Register – Index 44h (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan1_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**SYSFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.265 CPUFANIN Revolution Pulses Selection Register – Index 45h (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan2_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**CPUFANIN Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.266 AUXFANIN0 Revolution Pulses Selection Register – Index 46h (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan3_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**AUXFANIN0 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.267 AUXFANIN1 Revolution Pulses Selection Register – Index 47h (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan4_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**AUXFANIN1 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.268 AUXFANIN2 Revolution Pulses Selection Register – Index 48h (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan5_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**AUXFANIN2 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.269 AUXFANIN3 Revolution Pulses Selection Register – Index 49h (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						HM_Rev_Pulse_Fan6_Sel	
DEFAULT	0	0	0	0	0	0	1	0

BIT	DESCRIPTION
7-2	Reserved
1-0	**AUXFANIN3 Revolution Pulses Selection** = 00, four pulses per revolution. = 01, one pulse per revolution. = 10, two pulses per revolution. (default) = 11, three pulses per revolution.

9.270 (AUXFANIN3) Fan Count Limit High-byte Register – Index 4Ah (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANIN6_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN6_HL:** 13-bit AUXFANIN3 Fan Count Limit, High Byte

9.271 (AUXFANIN3) Fan Count Limit Low-byte Register – Index 4Bh (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN6_HL [4:0]				

DEFAULT	000	11111

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANIN6_HL:** 13-bit AUXFANIN3 Fan Count Limit, Low Byte

9.272 (AUXFANIN4) Fan Count Limit High-byte Register – Index 4Ch (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	FANIN7_HL [12:5]							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**FANIN7_HL:** 13-bit AUXFANIN4 Fan Count Limit, High Byte

9.273 (AUXFANIN4) Fan Count Limit Low-byte Register – Index 4Dh (Bank 6)

Attribute: Read /Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			FANIN7_HL [4:0]				
DEFAULT	000			11111				

BIT	DESCRIPTION
7-5	**Reserved**
4-0	**FANIN7_HL:** 13-bit AUXFANIN4 Fan Count Limit, Low Byte

9.274 AUXFANIN3 SPEED HIGH-BYTE VALUE (RPM) - Index 54h (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN3 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN3 SPEED HIGH-BYTE VALUE.**

9.275 AUXFANIN3 SPEED LOW-BYTE VALUE (RPM) - Index 55h (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN3 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN3 SPEED LOW-BYTE VALUE.**

9.276 SYSFANIN SPEED HIGH-BYTE VALUE (RPM) - Index 56h (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSFANIN SPEED HIGH-BYTE VALUE.**

9.277 SYSFANIN SPEED LOW-BYTE VALUE (RPM) - Index 57h (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	SYSFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**SYSFANIN SPEED LOW-BYTE VALUE.**

9.278 CPUFANIN SPEED HIGH-BYTE VALUE (RPM) - Index 58h (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED HIGH-BYTE VALUE							

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN SPEED HIGH-BYTE VALUE.**

9.279 CPUFANIN SPEED LOW-BYTE VALUE (RPM) - Index 59h (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CPUFANIN SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**CPUFANIN SPEED LOW-BYTE VALUE.**

9.280 AUXFANIN0 SPEED HIGH-BYTE VALUE (RPM) - Index 5Ah (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN0 SPEED HIGH-BYTE VALUE.**

9.281 AUXFANIN0 SPEED LOW-BYTE VALUE (RPM) - Index 5Bh (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN0 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN0 SPEED LOW-BYTE VALUE.**

9.282 AUXFANIN1 SPEED HIGH-BYTE VALUE (RPM) - Index 5Ch (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN1 SPEED HIGH-BYTE VALUE.**

9.283 AUXFANIN1 SPEED LOW-BYTE VALUE (RPM) - Index 5Dh (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN1 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN1 SPEED LOW-BYTE VALUE.**

9.284 AUXFANIN2 SPEED HIGH-BYTE VALUE (RPM) - Index 5Eh (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN2 SPEED HIGH-BYTE VALUE.**

9.285 AUXFANIN2 SPEED LOW-BYTE VALUE (RPM) - Index 5Fh (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN2 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN2 SPEED LOW-BYTE VALUE.**

9.286 AUXFANIN4 SPEED HIGH-BYTE VALUE (RPM) - Index 60h (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN4 SPEED HIGH-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN4 SPEED HIGH-BYTE VALUE.**

9.287 AUXFANIN4 SPEED LOW-BYTE VALUE (RPM) - Index 61h (Bank 6)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANIN4 SPEED LOW-BYTE VALUE							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**AUXFANIN4 SPEED LOW-BYTE VALUE.**

9.288 PECI Enable Function Register – Index 01h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI_En	Dimm_En	Margin_En	Reserved		Is_PECI30	Manual_En	Routine_En
DEFAULT	0	0	0	1	0	1	0	0

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable PECI Function. (**PECI_En**)
6	R / W	Enable PECI Dimm Function. (**Dimm_En**)
5	R / W	Enable PECI Margin Function. (**Margin_En**)
4 ~ 3	R / W	Reserved
2	R / W	Enable PECI 3.0 Command function (**Is_PECI30**)

BIT	READ / WRITE	DESCRIPTION
1	R / W	Enable PECI 3.0 Manual Function (**Manual_En**) (**One-shot clear**)
0	R / W	Enable PECI 3.0 Routine Function (**Routine_En**)

9.289 PECI Timing Config Register – Index 02h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		TN_Extend		Adj[2:0]			PECI_DC
DEFAULT	0	0	0	0	0	0	1	0

BIT	READ / WRITE	DESCRIPTION
7 ~ 6	R / W	Reserve
5	R / W	**TN_Extend[1:0]** Adjust Transaction Rate. 00_{BIN} = 1.5 MHz (Default) 01_{BIN} = 750 KHz 10_{BIN} = 375 KHz 11_{BIN} = 187.5 KHz
4	R / W	
3	R / W	**Adj[2:0]** Compensate the effect of rising time on physical bus Default Value = 001
2	R / W	
1	R / W	
0	R / W	Adjust PECI Tbit Duty cycle selection. **(PECI_DC)** 0 = 75% Tbit high duty cycle time. (Default) 1 = 68% Tbit high duty cycle time.

9.290 PECI Agent Config Register – Index 03h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		En_Agt[1:0]		Reserved		Domain1_Agt1	Domain1_Agt0
DEFAULT	0	0	0	0	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7 ~ 6	R / W	Reserved
5	R / W	**En_Agt[1:0] Enable Agent** 00 = Disable Agent.

BIT	READ / WRITE	DESCRIPTION
4	R / W	01= Enable Agent0. 10 = Reserved 11 = Enable Agent0 and Agent1.
3 ~ 2	R / W	Reserved
1	R / W	Enable domain 1 for Agent1 0 = Agent1 without domain1 1 = Agent1 with domain 1
0	R / W	Enable domain 1 for Agent0 0 = Agent0 without domain 1 1 = Agent0 with domain 1

9.291 PECI Temperature Config Register – Index 04h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Virtual_En	Reserved		Clamp	Reserved	RtDmn_Agt[1:0]		RtHigher
DEFAULT	0	0	0	0	0	0	0	0

BIT	READ / WRITE	DESCRIPTION
7	R / W	Virtual Temp Function Enable.(**Virtual_En)** When enable this function, the temperature raw data can use LPC to write raw data to CR 17_{HEX} ~ CR $1E_{HEX}$
6 ~ 5	R / W	Reserved
4	R / W	When temperature data reading is positive or less than -128, can enable this function to clamp temperature data.(**Clamp**)
3	R / W	Reserved
2	R / W	**RtDmn_Agt[1:0]** Agent 1 – Agent 0 always return the relative domain Temperature. 0 = Agent always returns the relative temperature from domain 0. 1 = Agent always returns the relative temperature from domain 1.
1	R / W	
0	R / W	Return High Temperature of doamin0 or domain1.(**RtHigher**) 0 = The temperature of each agent is returned from domain 0 or domain 1, which is controlled by (CR 04_{HEX}) 1 = Return the highest temperature in domain 0 and domain 1 of individual Agent.

9.292 PECI Command Address Register – Index 05h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0

NAME	PECI Command Address							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.293 PECI Command Write Length Register – Index 06h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Write Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.294 PECI Command Read Length Register – Index 07h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Read Length							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.295 PECI Command Code Register – Index 08h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Command Code							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.296 PECI Command Tbase0 Register – Index 09h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 0						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.297 PECI Command Tbase1 Register – Index 0Ah (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Tbase 1						
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.298 PECI Command Write Data 1 Register – Index 0Bh (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.299 PECI Command Write Data 2 Register – Index 0Ch (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 2							

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.300 PECI Command Write Data 3 Register – Index 0Dh (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.301 PECI Command Write Data 4 Register – Index 0Eh (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.302 PECI Command Write Data 5 Register – Index 0Fh (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.303 PECI Command Write Data 6 Register – Index 10h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 6							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.304 PECI Command Write Data 7 Register – Index 11h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.305 PECI Command Write Data 8 Register – Index 12h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.306 PECI Command Write Data 9 Register – Index 13h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.307 PECI Command Write Data 10 Register – Index 14h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 10							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.308 PECI Command Write Data 11 Register – Index 15h (Bank 7)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 11							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.309 PECI Command Write Data 12 Register – Index 16h (Bank 7)

Attribute: Read/Write

Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Write Data 12							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be sent to client. **Default value is 00_{HEX}.**

9.310 PECI Agent Relative Temperature Register (ARTR) – Index 17h-1Eh (Bank 7)

These registers return the **"raw data"** retrieved from PECI GetTemp() command. These data could be the error codes (range: 8000H~81FFH) or relative temperatures to process the defined Tbase. The error code will only be update in **ARTR**; while "Temperature Reading Register", Bank7 Index 20h and 21h, will not be updated when the error code is received. If the **RtHigher** mechanism is activated, the normal temperature will always be returned first. In case both 2 domains return errors, the return priority will be Overflow Error > Underflow Error > Missing Diode > General Error. The reset value is $8001_{HEX,}$ in that PECI is defaulted to be off. In PECI, 8001_{HEX} means the diode is missing.

Attribute: Read / Write(When Virtual_En enable)

ADDRESS 17-1E	DESCRIPTION
17h[15:8],18h[7:0]	Domain0 Relative Temperature Agent0 [15:0]
19h[15:8],1Ah[7:0]	Domain1 Relative Temperature Agent0 [15:0]
1Bh[15:8],1Ch[7:0]	Domain0 Relative Temperature Agent1 [15:0]
1Dh[15:8],1Eh[7:0]	Domain1 Relative Temperature Agent1 [15:0]

GetTemp() PECI Temperature format:

BIT	DESCRIPTION
15	Sign Bit. **(Sign)** In PECI Protocol, this bit should always be 1 to represent a negative temperature.
14-6	The integer part of the relative temperature. (**Temperature[8:0]**)
5	**TEMP_2**. 0.5℃ unit.
4	**TEMP_4**. 0.25℃ unit.
3	**TEMP_8**. 0.125℃ unit.
2	**TEMP_16**. 0.0625℃ unit.
1	**TEMP_32**. 0.03125℃ unit.
0	**TEMP_64**. 0.015625℃ unit.

GetTemp() Response Definition:

RESPONSE	MEANING
General Sensor Error (GSE)	Thermal scan did not complete in time. Retry is appropriate.

0x0000	Processor is running at its maximum temperature or is currently being reset.
All other data	Valid temperature reading, reported as a negative offset from the TCC activation temperature. The valide temperature reading is referred to GetTemp() PECI Temperature format

Error Code	Description	Host operation
8000_{HEX}	General Sensor Error	No further processing.
8001_{HEX}	Sensing Device Missing	
8002_{HEX}	Operational, but the temperature is lower than the sensor operation range.	Compulsorily write 0℃ back to the temperature readouts.
8003_{HEX}	Operational, but the temperature is higher than the sensor operation range.	Compulsorily write 127 ℃ back to the temperature readouts.
8004_{HEX} ' $81FF_{HEX}$	Reserved	No further operation.

9.311 PECI Alive Agent Register – Index 1Fh (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)
Record which agentis able to respond to Ping().**Default value is 00_{HEX}.**
1: agent is able to respond to Ping() command. Agent alive
0: agent isn't able to respond to Ping() command. Agent is not alive

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Alive Agent	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~2	Reserve
1	1: agent1 is able to respond to Ping() command. Agent alive 0: agent1 isn't able to respond to Ping() command. Agent is not alive
0	1: agent0 is able to respond to Ping() command. Agent alive 0: agent0 isn't able to respond to Ping() command. Agent is not alive

9.312 PECI Temperature Reading Register (Integer) – Index 20h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0

NAME	PECI Temperature Reading---Integer [9:2]							
DEFAULT	0	0	1	0	1	0	0	0

BIT	DESCRIPTION
7~0	**Temperature value [9] (Sign bit)** **Temperature value [8:2] (Integer bits)** Temperature value [1:0] (Fraction bits)

Note. Temperature reading register is count from raw data and Tbase, for example:

Raw data	**+**	***Tbase***	**=**	***Temp Reading***
Bank7, Index [17][18]	**+**	**Bank7, Index [09]**	**=**	**Bank7, Index [20][21]**

9.313 PECI Temperature Reading Register (Fraction) – Index 21h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Temperature Vaule[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Temperature value [9] (Sign bit) Temperature value [8:2] (Integer bits) **Temperature value [1:0] (Fraction bits)**

9.314 PECI Command TN Count Value Register – Index 22h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Timing Negotiation count Value[7:0]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.315 PECI Command TN Count Value Register – Index 23h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				PECI Timing Negotiation count Value[11:8]			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.316 PECI Command Warning Flag Register – Index 24h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						Alert Value[1:0]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
1~0	**Agent Alert Bit** (Default value is 0) 0: Agent has valid FCS. 1: Agent has invalid FCS in the previous 3 transactions. **Default value is 00_{HEX}.**

9.317 PECI Command FCS Data Register – Index 25h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserve		Wraning	CC_Fail	ZeroWFCS	AbortWFCS	BadRFCS	BadWFCS
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
5~0	Retrieve PECI related data from client and host. **Default value is 00_{HEX}.**

9.318 PECI Command WFCS Data Register – Index 26h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI WFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI WFCS related data from client. **Default value is 00_{HEX}.**

9.319 PECI RFCS Data Register – Index 27h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI RFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI related data from client. **Default value is 00_{HEX}.**

9.320 PECI AWFCS Data Register – Index 28h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI AWFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PCI related data from client. **Default value is 00_{HEX}.**

9.321 PECI CRC OUT WFCS Data Register – Index 29h (Bank 7)

Attribute: Read only

Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI CRC OUT WFCS							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	Retrieve PECI related data from client. **Default value is 00_{HEX}.**

9.322 PECI Command Read Data 1 Register – Index 2Ah (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 1							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.323 PECI Command Read Data 2 Register – Index 2Bh (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 2							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.324 PECI Command Read Data 3 Register – Index 2Ch (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 3							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.325 PECI Command Read Data 4 Register – Index 2Dh (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 4							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.326 PECI Command Read Data 5 Register – Index 2Eh (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 5							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.327 PECI Command Read Data 6 Register – Index 2Fh (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 6							

DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.328 PECI Command Read Data 7 Register – Index 30h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 7							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.329 PECI Command Read Data 8 Register – Index 31h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 8							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.330 PECI Command Read Data 9 Register – Index 32h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Data 9							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data would be get from client. **Default value is 00_{HEX}.**

9.331 PECI Read Dimm Data 1 Register – Index 33h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read CPU Agent0 Dimm0 Temp							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Dimm enable. LSB bit is decimal point.

9.332 PECI Read Dimm Data 2 Register – Index 34h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read CPU Agent0 Dimm1 Temp							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Dimm enable. LSB bit is decimal point.

9.333 PECI Read Dimm Data 3 Register – Index 35h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read CPU Agent1 Dimm0 Temp							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Dimm enable. LSB bit is decimal point.

9.334 PECI Read Dimm Data 4 Register – Index 36h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read CPU Agent1 Dimm1 Temp							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Dimm enable. LSB bit is decimal point.

9.335 PECI Read Margin Data 1 Register – Index 37h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Read CPU Agent0 Margin Temp[9:8]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Margin enable. MSB bit is sign bit.

9.336 PECI Read Margin Data 2 Register – Index 38h (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read CPU Agent0 Margin Temp[7:0]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Margin enable

9.337 PECI Read Margin Data 3 Register – Index 39h (Bank 7)

Attribute: Read only

Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						PECI Read CPU Agent1 Margin Temp[9:8]	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Margin enable. MSB bit is sign bit.

9.338 PECI Read Margin Data 4 Register – Index 3Ah (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read CPU Agent1 Margin Temp[7:0]							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	The data will update when PECI Margin enable

9.339 PECI Read Dimm Index Data Register – Index 3Bh (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Dimm Index data							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	When PECI Read Dimm enable, the register will be index data

9.340 PECI ead Dimm Index Data Register – Index 3Ch (Bank 7)

Attribute: Read only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	PECI Read Margin Index data							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7~0	When PECI Read Margin enable, the register will be index data

PECI Manual Command Address Table

Command Bank 7	Address CR 05_{HEX}	WriteLength CR 06_{HEX}	Read Length CR 07_{HEX}	Command Code CR 08_{HEX}
Ping	Addr	00	00	
GetDIB		01	08	F7
GetTemp		01	02	01
PCIRd30		06	02 / 03 / 05	61
PCIWr30		08 / 09 / 0B	01	65
PCIRdLocal30		05	02 / 03 / 05	E1
PCIWrLocal30		07 / 08 / 0A	01	E5
PKGRd30		05	02 / 03 / 05	A1
PKGWr30		07 / 08 / 0A	01	A5
IAMSRRd30		05	02 / 03 / 05 / 09	B1
IAMSRWr30		07 / 08 / 0A / 0E	01	B5

PECI Manual Command Read Data Table

Command	PCI Rd30	PCI Wr30	PCIRd Local30	PCIWr Local30	PKG Rd30	PKG Wr30	IAMSR Rd30	IAMSR Wr30	GetDIB	GetTemp
Command Code	61	65	E1	E5	A1	A5	B1	B5	F7	01
RdData 1 CR $2A_{HEX}$	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	Ccode	X	X
RdData 2 CR $2B_{HEX}$	X	X	X	X	X	X	Data LSB_1	X	Device Info	X
RdData 3 CR $2C_{HEX}$	X	X	X	X	X	X	Data LSB_2	X	Revision Number	X
RdData 4 CR $2D_{HEX}$	X	X	X	X	X	X	Data LSB_3	X	Reserved 1	X
RdData 5 CR $2E_{HEX}$	X	X	x	X	X	X	Data LSB_4	X	Reserved 2	X
RdData 6	Data	X	Data	X	Data	X	Data	X	Reserved	X

CR 2F$_{HEX}$	LSB_1		LSB_1		LSB_1		LSB_5		3	
RdData 7 CR 30$_{HEX}$	Data LSB_2	X	Data LSB_2	X	Data LSB_2	X	Data LSB_6	X	Reserved 4	X
RdData 8 CR 31$_{HEX}$	Data LSB_3	X	Data LSB_3	X	Data LSB_3	X	Data LSB_7	X	Reserved 5	Temp_LB
RdData 9 CR 32$_{HEX}$	Data MSB	x	Data MSB	X	Data MSB	X	Data MSB	X	Reserved 6	Temp_HB

PECI Manual Command Write Data Table

Command	PCI Rd30	PCI Wr30	PCIRd Local30	PCIWr Local30	PKG Rd30	PKG Wr30	IAMSR Rd30	IAMSR Wr30
Command Code	**61**	**65**	**E1**	**E5**	**A1**	**A5**	**B1**	**B5**
WrData 1 CR 0B$_{HEX}$	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID	Host ID
WrData 2 CR 0C$_{HEX}$	Addr LSB_1	Addr LSB_1	Addr LSB_1	Addr LSB_1	Index	Index	Processor ID	Processor ID
WrData 3 CR 0D$_{HEX}$	Addr LSB_2	Addr LSB_2	Addr LSB_2	Addr LSB_2	Param LSB	Param LSB	Addr LSB	Addr LSB
WrData 4 CR 0E$_{HEX}$	Addr LSB_3	Addr LSB_3	Addr MSB	Addr MSB	Param MSB	Param MSB	Addr MSB	Addr MSB
WrData 5 CR 0F$_{HEX}$	Addr MSB	Addr MSB	X	Data LSB_1	X	Data LSB_1	X	Data LSB_1
WrData 6 CR 10$_{HEX}$	X	Data LSB_1	X	Data LSB_2	X	Data LSB_2	X	Data LSB_2
WrData 7 CR 11$_{HEX}$	X	Data LSB_2	X	Data LSB_3	X	Data LSB_3	X	Data LSB_3
WrData 8 CR 12$_{HEX}$	X	Data LSB_3	X	Data MSB	X	Data MSB	X	Data LSB_4
WrData 9 CR 13$_{HEX}$	X	Data MSB	X	X	X	X	X	Data LSB_5
WrData10 CR 14$_{HEX}$	X	X	X	X	X	X	X	Data LSB_6
WrData11 CR 15$_{HEX}$	X	X	X	X	X	X	X	Data LSB_7
WrData12 CR 16$_{HEX}$	X	X	X	X	X	X	X	Data MSB

9.341 AUXFAN1 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 8)

Attribute: Read/Write

Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN1 SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT1 Stop Value (Bank8, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**AUXFAN1 Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN1 monitoring source. 0 0 0 1 0: Select **CPUTIN** as AUXFAN1 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as AUXFAN1 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as AUXFAN1 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as AUXFAN1 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as AUXFAN1 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as AUXFAN1 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as AUXFAN1 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as AUXFAN1 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as AUXFAN1 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as AUXFAN1 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN1 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as AUXFAN1 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as AUXFAN1 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as AUXFAN1 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as AUXFAN1 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as AUXFAN1 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as AUXFAN1 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as AUXFAN1 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as AUXFAN1 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as AUXFAN1 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as AUXFAN1 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as AUXFAN1 monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as AUXFAN1 monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.342 AUXFAN1 Target Temperature Register / AUXFANIN1 Target Speed_L Register – Index 01h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN1 Target Temperature / AUXFANIN1 Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN1 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN1 Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.343 AUXFAN1 MODE Register / AUXFAN1 TOLERRANCE Register – Index 02h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#(Bit2-0)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 MODE				Reseved	Tolerance of AUXFAN1 Target Temperature or AUXFANIN1 Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**AUXFANOUT1 Mode Select.** 0000: **AUXFANOUT1** is in Manual Mode. **(Default)** 0001: **AUXFANOUT1** is in Thermal Cruise Mode. 0010: **AUXFANOUT1** is as Speed Cruise Mode. 0100: **AUXFANOUT1** is in SMART FAN IV Mode.
3	**Reseved**
2-0	Tolerance of AUXFAN1 Target Temperature or AUXFANIN1 Target Speed_L.

9.344 AUXFANOUT1 Step Up Time Register – Index 03h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT1 takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.345 AUXFANOUT1 Step Down Time Register – Index 04h (Bank 8)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT1 takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.346 AUXFANOUT1 Stop Value Register – Index 05h (Bank 8)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT1 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.347 AUXFANOUT1 Start-up Value Register – Index 06h (Bank 8)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, AUXFANOUT1 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.348 AUXFANOUT1 Stop Time Register – Index 07h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes AUXFANOUT1 value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.349 AUXFANOUT1 Output Value Select Register – Index 09h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 Value							
DEFAULT	1	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E3h] is the Default Speed Configuration Register of AUXFANOUT1.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.350 AUXFANIN1 Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUXFANIN1 TOL_H			AUXFANIN1 Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	AUXFANIN1 Tolerance_H [5:3]
3-0	AUXFANIN1 Target Speed_H [11:8]

9.351 AUXFAN1 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 1 Register (T1).

9.352 AUXFAN1 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 2 Register (T2).

9.353 AUXFAN1 (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1(SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 3 Register (T3).

9.354 AUXFAN1 (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Temperature 4 Register (T4).

9.355 AUXFAN1 (SMART FAN™ IV) PWM 1 Register – Index 27h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) PWM 1 Register.

9.356 AUXFAN1 (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) PWM 2 Register.

9.357 AUXFAN1 (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) PWM 3 Register.

9.358 AUXFAN1 (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) PWM 4 Register.

9.359 AUXFAN1 3-Wire Enable Register – Index 31h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_AUX1_3WFAN
DEFAULT	0		0					0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_AUX1_3WFAN (AUXFAN1 type setting)** 0: 4-wire fan 1: 3-wire fan

9.360 AUXFAN1 (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN1 (SMART FAN™ IV) Critical Temperature Register

9.361 AUXFAN1 Enable Critical Duty – Index 36h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX1_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUX1_CRITICAL_DUTY (set 0 in manual mode)** 0: Load default Full Speed 8'hFF for AUXFANOUT1. 1: Used Index 37 CRITICAL_DUTY Value for AUXFANOUT1.

9.362 AUXFAN1 Critical Duty Register – Index 37h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN1 Critical Duty.

9.363 AUXFANOUT1 Critical Temperature Tolerance Register – Index 38h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT1 Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**AUXFANOUT1 Critical Temperature Tolerance**

9.364 AUXFAN1 PECIERR DUTY Enable Register – Index 3Fh (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX1_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**

1-0	**EN_AUX1_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_AUXOUT1** Value for AUXFANOUT1. 10,11: Keep Full Speed

9.365 AUXFANOUT1 Pre-Configured Register For PECI Error – Index 41h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT1 pre-configured register for PECI error (PECI_ERR_AUXOUT1)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**AUXFANOUT1 pre-configured register for PECI error.**

9.366 DUTY PER STEP Register – Index 66h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.367 T1 Delay Time Register – Index 67h (Bank 8)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.368 AUXFAN1 Max Duty compare Source Select Register – Index 68h (Bank 8)

Attribute: Read/Write

Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED					AUXFAN1 Max Duty compare Source Select		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2	**AUXFAN1 Max Duty Source Select** 0: Disable AUXFAN0 Duty 1: Enable AUXFAN0 Duty
1	**AUXFAN1 Max Duty Source Select** 0: Disable CPUFAN Duty 1: Enable CPUFAN Duty
0	**AUXFAN1 Max Duty Source Select** 0: Disable SYSFAN Duty 1: Enable SYSFAN Duty

9.369 AUXFAN1 Max Duty Output Register – Index 69h (Bank 8)

Attribute: Read Only
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN1 Max Duty Output							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
0	**AUXFAN1 Max Duty Output**

9.370 AUXFAN2 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN2 SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary.

BIT	DESCRIPTION
	1: FANOUT will decrease to AUXFANOUT2 Stop Value (Bank9, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**AUXFAN2 Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN2 monitoring source. 0 0 0 1 0: Select **CPUTIN** as AUXFAN2 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as AUXFAN2 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as AUXFAN2 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as AUXFAN2 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as AUXFAN2 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as AUXFAN2 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as AUXFAN2 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as AUXFAN2 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as AUXFAN2 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as AUXFAN2 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN2 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as AUXFAN2 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as AUXFAN2 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as AUXFAN2 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as AUXFAN2 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as AUXFAN2 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as AUXFAN2 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as AUXFAN2 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as AUXFAN2 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as AUXFAN2 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as AUXFAN2 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as AUXFAN2 monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as AUXFAN2 monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.371 AUXFAN2 Target Temperature Register / AUXFANIN2 Target Speed_L Register – Index 01h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN2 Target Temperature / AUXFANIN2 Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN2 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN2 Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.372 AUXFAN2 MODE Register / AUXFAN2 TOLERRANCE Register – Index 02h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#(Bit2-0)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 MODE				Reseved	Tolerance of AUXFAN2 Target Temperature or AUXFANIN2 Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**AUXFANOUT2 Mode Select.** 0000: **AUXFANOUT2** is in Manual Mode. **(Default)** 0001: **AUXFANOUT2** is in Thermal Cruise Mode. 0010: **AUXFANOUT2** is as Speed Cruise Mode. 0100: **AUXFANOUT2** is in SMART FAN IV Mode.
3	**Reseved**
2-0	Tolerance of AUXFAN2 Target Temperature or AUXFANIN2 Target Speed_L.

9.373 AUXFANOUT2 Step Up Time Register – Index 03h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT2 takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.374 AUXFANOUT2 Step Down Time Register – Index 04h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT2 takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.375 AUXFANOUT2 Stop Value Register – Index 05h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT2 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.376 AUXFANOUT2 Start-up Value Register – Index 06h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, AUXFANOUT2 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.377 AUXFANOUT2 Stop Time Register – Index 07h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes AUXFANOUT2 value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.378 AUXFANOUT2 Output Value Select Register – Index 09h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 Value							
DEFAULT	1	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E4h] is the Default Speed Configuration Register of AUXFANOUT2.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.379 AUXFANIN2 Tolerance_H / Target Speed_H Register – Index 0Ch (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUXFANIN2 TOL_H			AUXFANIN2 Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	AUXFANIN2 Tolerance_H [5:3]
3-0	AUXFANIN2 Target Speed_H [11:8]

9.380 AUXFAN2 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank 9)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 1 Register (T1).

9.381 AUXFAN2 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 2 Register (T2).

9.382 AUXFAN2 (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2(SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 3 Register (T3).

9.383 AUXFAN2 (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Temperature 4 Register (T4).

9.384 AUXFAN2 (SMART FAN™ IV) PWM 1 Register – Index 27h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) PWM 1 Register.

9.385 AUXFAN2 (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) PWM 2 Register.

9.386 AUXFAN2 (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) PWM 3 Register.

9.387 AUXFAN2 (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) PWM 4 Register.

9.388 AUXFAN2 3-Wire Enable Register – Index 31h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_AUX2_3WFAN
DEFAULT	0		0					0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_AUX2_3WFAN (AUXFAN2 type setting)** 0: 4-wire fan 1: 3-wire fan

9.389 AUXFAN2 (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN2 (SMART FAN™ IV) Critical Temperature Register

9.390 AUXFAN2 Enable Critical Duty – Index 36h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX2_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUX2_CRITICAL_DUTY (set 0 in manual mode)** 0: Load default Full Speed 8'hFF for AUXFANOUT2. 1: Used Index 37 CRITICAL_DUTY Value for AUXFANOUT2.

9.391 AUXFAN2 Critical Duty Register – Index 37h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN2 Critical Duty.

9.392 AUXFANOUT2 Critical Temperature Tolerance Register – Index 38h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT2 Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**AUXFANOUT2 Critical Temperature Tolerance**

9.393 AUXFAN2 PECIERR DUTY Enable Register – Index 3Fh (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX2_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**
1-0	**EN_AUX2_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_AUXOUT2** Value for AUXFANOUT2. 10,11: Keep Full Speed

9.394 AUXFANOUT2 Pre-Configured Register For PECI Error – Index 41h (Bank 9)

Attribute: Read/Write

Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT2 pre-configured register for PECI error (PECI_ERR_AUXOUT2)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**AUXFANOUT2 pre-configured register for PECI error.**

9.395 DUTY PER STEP Register – Index 66h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.396 T1 Delay Time Register – Index 67h (Bank 9)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.397 AUXFAN3 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN3 SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT2 Stop Value (Bank9, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**AUXFAN3 Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN3 monitoring source. 0 0 0 1 0: Select **CPUTIN** as AUXFAN3 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as AUXFAN3 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as AUXFAN3 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as AUXFAN3 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as AUXFAN3 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as AUXFAN3 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as AUXFAN3 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as AUXFAN3 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as AUXFAN3 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as AUXFAN3 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN3 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as AUXFAN3 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as AUXFAN3 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as AUXFAN3 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as AUXFAN3 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as AUXFAN3 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as AUXFAN3 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as AUXFAN3 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as AUXFAN3 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as AUXFAN3 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as AUXFAN3 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as AUXFAN3 monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as AUXFAN3 monitoring source.

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.398 AUXFAN3 Target Temperature Register / AUXFANIN3 Target Speed_L Register – Index 01h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN3 Target Temperature / AUXFANIN2 Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN3 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN3 Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.399 AUXFAN3 MODE Register / AUXFAN2 TOLERRANCE Register – Index 02h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#(Bit2-0)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 MODE				Reseved	Tolerance of AUXFAN3 Target Temperature or AUXFANIN3 Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**AUXFANOUT3 Mode Select.** 0000: **AUXFANOUT3** is in Manual Mode. **(Default)** 0001: **AUXFANOUT3** is in Thermal Cruise Mode. 0010: **AUXFANOUT3** is as Speed Cruise Mode. 0100: **AUXFANOUT3** is in SMART FAN IV Mode.
3	**Reseved**
2-0	Tolerance of AUXFAN3 Target Temperature or AUXFANIN3 Target Speed_L.

9.400 AUXFANOUT3 Step Up Time Register – Index 03h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT3 takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.401 AUXFANOUT3 Step Down Time Register – Index 04h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT3 takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.402 AUXFANOUT3 Stop Value Register – Index 05h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT3 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.403 AUXFANOUT3 Start-up Value Register – Index 06h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, AUXFANOUT3 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.404 AUXFANOUT3 Stop Time Register – Index 07h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Value Stop Time							

DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes AUXFANOUT3 value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.405 AUXFANOUT3 Output Value Select Register – Index 09h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 Value							
DEFAULT	1	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E4h] is the Default Speed Configuration Register of AUXFANOUT3.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.406 AUXFANIN3 Tolerance_H / Target Speed_H Register – Index 0Ch (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUXFANIN3 TOL_H			AUXFANIN3 Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	AUXFANIN3 Tolerance_H [5:3]
3-0	AUXFANIN3 Target Speed_H [11:8]

9.407 AUXFAN3 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank A)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0

NAME	AUXFAN3 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) Temperature 1 Register (T1).

9.408 AUXFAN3 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) Temperature 2 Register (T2).

9.409 AUXFAN3 (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2(SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) Temperature 3 Register (T3).

9.410 AUXFAN3 (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) Temperature 4 Register (T4).

9.411 AUXFAN3 (SMART FAN™ IV) PWM 1 Register – Index 27h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) PWM 1 Register.

9.412 AUXFAN3 (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) PWM 2 Register.

9.413 AUXFAN3 (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) PWM 3 Register.

9.414 AUXFAN3 (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) PWM 4							

DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) PWM 4 Register.

9.415 AUXFAN3 3-Wire Enable Register – Index 31h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_AUX3_3WFAN
DEFAULT	0		0					0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_AUX3_3WFAN (AUXFAN2 type setting)** 0: 4-wire fan 1: 3-wire fan

9.416 AUXFAN3 (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN3 (SMART FAN™ IV) Critical Temperature Register

9.417 AUXFAN3 Enable Critical Duty – Index 36h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX3_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION

7-1	**Reserved**
0	**En_AUX3_CRITICAL_DUTY (set 0 in manual mode)** 0: Load default Full Speed 8'hFF for AUXFANOUT3. 1: Used Index 37 CRITICAL_DUTY Value for AUXFANOUT3.

9.418 AUXFAN3 Critical Duty Register – Index 37h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN3 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN3 Critical Duty.

9.419 AUXFANOUT3 Critical Temperature Tolerance Register – Index 38h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT3 Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**AUXFANOUT3 Critical Temperature Tolerance**

9.420 AUXFAN3 PECIERR DUTY Enable Register – Index 3Fh (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX3_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**
1-0	**EN_AUX3_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_AUXOUT3** Value for AUXFANOUT2.

	10,11: Keep Full Speed

9.421 AUXFANOUT3 Pre-Configured Register For PECI Error – Index 41h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT3 pre-configured register for PECI error (PECI_ERR_AUXOUT3)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**AUXFANOUT3 pre-configured register for PECI error.**

9.422 DUTY PER STEP Register – Index 66h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.423 T1 Delay Time Register – Index 67h (Bank A)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.424 AUXFAN4 Monitor Temperature Source Select Register/ STOPDUTY Enable Register – Index 00h (Bank B)

Attribute: Read/Write
Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Stopduty_En	Reserved		AUXFAN4 SOURCE[4:0]				
DEFAULT	0	0	0	0	0	0	1	1

BIT	DESCRIPTION
7	**Stopduty_En:** 0: FANOUT will decrease to zero value at most if necessary. 1: FANOUT will decrease to AUXFANOUT4 Stop Value (BankB, index05h) at most if necessary. (This function is for Thermal Cruise mode.)
6-5	**Reserved**
4-0	**AUXFAN4 Temperature Source Select**: **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as AUXFAN4 monitoring source. 0 0 0 1 0: Select **CPUTIN** as AUXFAN4 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as AUXFAN4 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as AUXFAN4 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as AUXFAN4 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as AUXFAN4 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as AUXFAN4 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as AUXFAN4 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as AUXFAN4 monitoring source. 0 1 0 1 0: Select **Virtual_TEMP** as AUXFAN4 monitoring source. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as AUXFAN4 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as AUXFAN4 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as AUXFAN4 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as AUXFAN4 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as AUXFAN4 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as AUXFAN4 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as AUXFAN4 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as AUXFAN4 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as AUXFAN4 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as AUXFAN4 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as AUXFAN4 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as AUXFAN4 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as AUXFAN4 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as AUXFAN4 monitoring source. 1 1 1 1 1: Reserved..

Note. If the temperature source is selecting to PECI, please set Bank0 Index AEh first for reading correct value.

9.425 AUXFAN4 Target Temperature Register / AUXFANIN3 Target Speed_L Register – Index 01h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXTIN3 Target Temperature / AUXFANIN2 Target Speed_L							
DEFAULT	0	0	0	0	0	0	0	0

FUNCTION MODE		7	6	5	4	3	2	1	0
Thermal Cruise™	DESCRIPTION	AUXFAN4 Target Temperature							
Fan Speed Cruise™	DESCRIPTION	AUXFANIN3 Target Speed [7:0], [11:8] associate index 0C [3:0]							

9.426 AUXFAN4 MODE Register / AUXFAN2 TOLERRANCE Register – Index 02h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#(Bit2-0)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN4 MODE				Reseved	Tolerance of AUXFAN4 Target Temperature or AUXFANIN3 Target Speed_L		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**AUXFANOUT4 Mode Select.** 0000: **AUXFANOUT4** is in Manual Mode. **(Default)** 0001: **AUXFANOUT4** is in Thermal Cruise Mode. 0010: **AUXFANOUT4** is as Speed Cruise Mode. 0100: **AUXFANOUT4** is in SMART FAN IV Mode.
3	**Reseved**
2-0	Tolerance of AUXFAN4 Target Temperature or AUXFANIN3 Target Speed_L.

9.427 AUXFANOUT4 Step Up Time Register – Index 03h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT4 Value Step Up Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT4 takes to increase its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.428 AUXFANOUT4 Step Down Time Register – Index 04h (Bank B)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT4 Value Step Down Time							
DEFAULT	0	0	0	0	1	0	1	0

In SMART FAN™ mode, this register determines the amount of time AUXFANOUT4 takes to decrease its value by one step.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.429 AUXFANOUT4 Stop Value Register – Index 05h (Bank B)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT4 Stop Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, the AUXFANOUT4 value decreases to this eight-bit value if the temperature stays below the lowest temperature limit. This value should not be zero.

Please note that Stop Value does not mean that the fan really stops. It means that if the temperature keeps below low temperature limit, then the fan speed keeps on decreasing until reaching a minimum value, and this is Stop Value.

9.430 AUXFANOUT4 Start-up Value Register – Index 06h (Bank B)

Attribute: Read/Write

Size: 8 bits

Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT4 Start-Up Value							
DEFAULT	0	0	0	0	0	0	0	1

In Thermal Cruise mode, AUXFANOUT4 value increases from zero to this eight-bit register value to provide a minimum value to turn on the fan. This value should not be zero.

9.431 AUXFANOUT4 Stop Time Register – Index 07h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT4 Value Stop Time							
DEFAULT	0	0	1	1	1	1	0	0

In Thermal Cruise mode, this register determines the amount of time it takes AUXFANOUT4 value to fall from the stop value to zero.

(1) For PWM output:

The units are intervals of 0.1 second. The default time is 1 second.

9.432 AUXFANOUT4 Output Value Select Register – Index 09h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT4 Value							
DEFAULT	1	1	1	1	1	1	1	1

The default speed of fan output is specified in registers CR[E0h] to CR[E4h] of Logical Device B, CR[E4h] is the Default Speed Configuration Register of AUXFANOUT4.

FUNCTION MODE		7	6	5	4	3	2	1	0
PWM Output	DESCRIPTION	The PWM duty cycle is equal to this eight-bit value, divided by 255, times 100%. FFh creates a duty cycle of 100%, and 00h creates a duty cycle of 0%.							

9.433 AUXFANIN4 Tolerance_H / Target Speed_H Register – Index 0Ch (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	AUXFANIN4 TOL_H			AUXFANIN4 Target Speed_H			
DEFAULT	0	0			0			

BIT	DESCRIPTION
7	**Reserved**
6-4	AUXFANIN4 Tolerance_H [5:3]
3-0	AUXFANIN4 Target Speed_H [11:8]

9.434 AUXFAN4 (SMART FAN™ IV) Temperature 1 Register(T1) – Index 21h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN4 (SMART FAN™ IV) Temperature 1							
DEFAULT	0	0	0	1	1	0	0	1

BIT	DESCRIPTION
7-0	AUXFAN4 (SMART FAN™ IV) Temperature 1 Register (T1).

9.435 AUXFAN4 (SMART FAN™ IV) Temperature 2 Register(T2) – Index 22h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN4 (SMART FAN™ IV) Temperature 2							
DEFAULT	0	0	1	0	0	0	1	1

BIT	DESCRIPTION
7-0	AUXFAN4 (SMART FAN™ IV) Temperature 2 Register (T2).

9.436 AUXFAN4 (SMART FAN™ IV) Temperature 3 Register(T3) – Index 23h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN2(SMART FAN™ IV) Temperature 3							
DEFAULT	0	0	1	0	1	1	0	1

BIT	DESCRIPTION
7-0	AUXFAN4 (SMART FAN™ IV) Temperature 3 Register (T3).

9.437 AUXFAN4 (SMART FAN™ IV) Temperature 4 Register(T4) – Index 24h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN4 (SMART FAN™ IV) Temperature 4							
DEFAULT	0	0	1	1	0	1	1	1

BIT	DESCRIPTION
7-0	AUXFAN4 (SMART FAN™ IV) Temperature 4 Register (T4).

9.438 AUXFAN4 (SMART FAN™ IV) PWM 1 Register – Index 27h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN4 (SMART FAN™ IV) PWM 1							
DEFAULT	1	0	0	0	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN4 (SMART FAN™ IV) PWM 1 Register.

9.439 AUXFAN4 (SMART FAN™ IV) PWM 2 Register – Index 28h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN4 (SMART FAN™ IV) PWM 2							
DEFAULT	1	0	1	0	1	0	1	0

BIT	DESCRIPTION
7-0	AUXFAN4 (SMART FAN™ IV) PWM 2 Register.

9.440 AUXFAN4 (SMART FAN™ IV) PWM 3 Register – Index 29h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN4 (SMART FAN™ IV) PWM 3							
DEFAULT	1	1	0	0	1	0	0	0

BIT	DESCRIPTION
7-0	AUXFAN4 (SMART FAN™ IV) PWM 3 Register.

9.441 AUXFAN4 (SMART FAN™ IV) PWM 4 Register – Index 2Ah (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN4 (SMART FAN™ IV) PWM 4							
DEFAULT	1	1	1	0	0	1	1	0

BIT	DESCRIPTION
7-0	AUXFAN4 (SMART FAN™ IV) PWM 4 Register.

9.442 AUXFAN4 3-Wire Enable Register – Index 31h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							EN_AUX3_3WFAN
DEFAULT	0		0					0

BIT	DESCRIPTION
7-1	**Reserved**
0	**EN_AUX3_3WFAN (AUXFAN2 type setting)** 0: 4-wire fan 1: 3-wire fan

9.443 AUXFAN4 (SMART FAN™ IV) Critical Temperature Register – Index 35h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN4 (SMART FAN™ IV) Temperature Critical							
DEFAULT	0	0	1	1	1	1	0	0

BIT	DESCRIPTION
7-0	AUXFAN4 (SMART FAN™ IV) Critical Temperature Register

9.444 AUXFAN4 Enable Critical Duty – Index 36h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved							En_AUX3_CRITICAL_DUTY
DEFAULT	0							0

BIT	DESCRIPTION
7-1	**Reserved**
0	**En_AUX3_CRITICAL_DUTY (set 0 in manual mode)** 0: Load default Full Speed 8'hFF for AUXFANOUT4. 1: Used Index 37 CRITICAL_DUTY Value for AUXFANOUT4.

9.445 AUXFAN4 Critical Duty Register – Index 37h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFAN4 Critical Duty							
DEFAULT	CC							

BIT	DESCRIPTION
7-0	AUXFAN4 Critical Duty.

9.446 AUXFANOUT4 Critical Temperature Tolerance Register – Index 38h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved					AUXFANOUT4 Critical Temperature Tolerance		
DEFAULT	0					0	0	0

BIT	DESCRIPTION
7-3	**Reserved**
2-0	**AUXFANOUT4 Critical Temperature Tolerance**

9.447 AUXFAN4 PECIERR DUTY Enable Register – Index 3Fh (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved						EN_AUX3_PECIERR_DUTY	
DEFAULT	0						0	0

BIT	DESCRIPTION
7-2	**Reserved**

1-0	**EN_AUX3_PECIERR_DUTY** 00: Disable PECIERR DUTY FANOUT (default) 01: Enable PECIERR DUTY FANOUT, Used Index 41 **PECI_ERR_AUXOUT3** Value for AUXFANOUT2. 10,11: Keep Full Speed

9.448 AUXFANOUT4 Pre-Configured Register For PECI Error – Index 41h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	AUXFANOUT4 pre-configured register for PECI error (PECI_ERR_AUXOUT3)							
DEFAULT	1	1	1	1	1	1	1	1

BIT	DESCRIPTION
7-0	**AUXFANOUT4 pre-configured register for PECI error.**

9.449 DUTY PER STEP Register – Index 66h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	UP_STEP				DOWN_STEP			
DEFAULT	0	0	0	1	0	0	0	1

BIT	DESCRIPTION
7-4	UP unit.
3-0	DOWN unit.

9.450 T1 Delay Time Register – Index 67h (Bank B)

Attribute: Read/Write
Size: 8 bits
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	T1 Delay time							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	T1 Delay time for FAN. 1 bit = 0.1 sec.

9.451 Real Time Hardware Status Register I – Index 01h (Bank C)

Attribute: Read Only

Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		CPUTIN _STS	AUXTIN4 _STS	AUXTIN3 _STS	AUXTIN2 _STS	AUXTIN1 _STS	AUXTIN0 _STS
DEFAULT	0		0	0	0	0	0	0

BIT	DESCRIPTION
7-6	Reserved.
5	**CPUTIN_STS. CPUTIN Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
4	**AUXTIN4_STS. AUXTIN4 Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
3	**AUXTIN3_STS. AUXTIN3 Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
2	**AUXTIN2_STS. AUXTIN2 Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
1	**AUXTIN1_STS. AUXTIN1 Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.
0	**AUXTIN0_STS. AUXTIN0 Temperature Sensor Status.** 1: Temperature exceeds the over-temperature value. 0: Temperature is under the hysteresis value.

9.452 Interrupt Status Register – Index 02h (Bank C)

Attribute: Read Clear
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.		SOURCE8 _ SMI	SOURCE7 _ SMI	SOURCE6 _ SMI	SOURCE5 _ SMI	SOURCE4 _ SMI	SOURCE3 _ SMI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Reserved.**
5	**SMIOVT8.** A one indicates the high limit of SMIOVT8 temperature has been exceeded.
4	**SMIOVT7.** A one indicates the high limit of SMIOVT7 temperature has been exceeded.
3	**SMIOVT6.**

BIT	DESCRIPTION
	A one indicates the high limit of SMIOVT6 temperature has been exceeded.
2	**SMIOVT5.** A one indicates the high limit of SMIOVT5 temperature has been exceeded.
1	**SMIOVT4.** A one indicates the high limit of SMIOVT4 temperature has been exceeded.
0	**SMIOVT3.** A one indicates the high limit of SMIOVT3 temperature has been exceeded.

9.453 Interrupt Status Register – Index 03h (Bank C)

Attribute: Read Clear
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Shut_ SOURCE8_SMI	Shut_ SOURCE7_SMI	Shut_ SOURCE6_SMI	Shut_ SOURCE5_SMI	Shut_ SOURCE4_SMI	Shut_ SOURCE3_SMI
DEFAULT	0		0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Reserved**
5	**Shut_SOURCE8_SMI.** "1" indicates the high limit of SMIOVT _SOURCE4 temperature of SMI# Shut-down mode has been exceeded.
4	**Shut_SOURCE7_SMI.** "1" indicates the high limit of SMIOVT _SOURCE4 temperature of SMI# Shut-down mode has been exceeded.
3	**Shut_SOURCE6_SMI.** "1" indicates the high limit of SMIOVT _SOURCE4 temperature of SMI# Shut-down mode has been exceeded.
2	**Shut_SOURCE5_SMI.** "1" indicates the high limit of SMIOVT _SOURCE4 temperature of SMI# Shut-down mode has been exceeded.
1	**Shut_SOURCE4_SMI.** "1" indicates the high limit of SMIOVT _SOURCE4 temperature of SMI# Shut-down mode has been exceeded.
0	**Shut_SOURCE3_SMI.** "1" indicates the high limit of SMIOVT _SOURCE3 temperature of SMI# Shut-down mode has been exceeded.

9.454 SMI3-8# Mask Register 1 – Index 04h (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved.		SMIOVT8	SMIOVT7	SMIOVT6	SMIOVT5	SMIOVT4	SMIOVT3
DEFAULT	0		1	1	1	1	1	1

BIT	DESCRIPTION	
7-6	**Reserved.**	A one disables the corresponding interrupt status

BIT	DESCRIPTION	
5	**SMIOVT8.**	bit for the SMI interrupt. (See Interrupt Status Register – Index 02h (BankC))
4	**SMIOVT7.**	
3	**SMIOVT6.**	
2	**SMIOVT5.**	
1	**SMIOVT4.**	
0	**SMIOVT3.**	

9.455 SMI3-8# Mask Register 3 – Index 05h (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	CASEOPEN CLEAR0	CASEOPEN CLEAR1	AUXFANIN3	Shut_CPU	Shut_SYS	AUXFANIN2	AUXFANIN1	CASEOPEN1
DEFAULT	0	0	1	1	1	1	1	1

BIT	DESCRIPTION	
7-6	Reserved.	
5	**Shut_SOURCE8_SMI**	"1" disables the corresponding interrupt status bit for the SMI interrupt. (See Interrupt Status Register – Index 03h (Bank C)).
4	**Shut_SOURCE7_SMI**	
3	**Shut_SOURCE6_SMI**	
2	**Shut_SOURCE5_SMI**	
1	**Shut_SOURCE4_SMI**	
0	**Shut_SOURCE3_SMI**	

9.456 SMI/OVT3-8 Control Register – Index 06h (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		DIS_ OVT8	DIS_ OVT7	DIS_ OVT6	DIS_ OVT5	DIS_ OVT4	DIS_ OVT3
DEFAULT	0		0	0	1	0	0	0

BIT	DESCRIPTION
7-6	**Reserved**
5	**DIS_OVT8.** 1: Disable SMIOVT Source8 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source8 temperature OVT output through pin OVT#. (Default)
4	**DIS_OVT7.** 1: Disable SMIOVT Source7 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source7 temperature OVT output through pin OVT#. (Default)
3	**DIS_OVT6.** 1: Disable SMIOVT Source6 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source6 temperature OVT output through pin OVT#. (Default)
2	**DIS_OVT5.** 1: Disable SMIOVT Source5 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source5 temperature OVT output through pin OVT#. (Default)
1	**DIS_OVT4.** 1: Disable SMIOVT Source4 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source4 temperature OVT output through pin OVT#. (Default)
0	**DIS_OVT3.** 1: Disable SMIOVT Source3 temperature sensor over-temperature (OVT) output. 0: Enable SMIOVT Source3 temperature OVT output through pin OVT#. (Default)

9.457 SMIOVT3-8 Temperature Source Configuration Register – Index 07h (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		OVTMOD8	OVTMOD7	OVTMOD6	OVTMOD5	OVTMOD4	OVTMOD3
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Reserved** This bit should be set to zero.
5	**OVTMOD8. SMIOVT8 Mode Select.** 0 : Compare Mode. (Default) 1: Interrupt Mode.
4	**OVTMOD7. SMIOVT7 Mode Select.** 0 : Compare Mode. (Default) 1: Interrupt Mode.
3	**OVTMOD6. SMIOVT6 Mode Select.** 0 : Compare Mode. (Default) 1: Interrupt Mode.
2	**OVTMOD5. SMIOVT5 Mode Select.** 0 : Compare Mode. (Default) 1: Interrupt Mode.
1	**OVTMOD4. SMIOVT4 Mode Select.**

BIT	DESCRIPTION
	0 : Compare Mode. (Default) 1: Interrupt Mode.
0	**OVTMOD3. SMIOVT3 Mode Select.** 0 : Compare Mode. (Default) 1: Interrupt Mode.

9.458 SMIOVT3-8 Temperature Source Configuration Register – Index 08h (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		STOP8	STOP7	STOP6	STOP5	STOP4	STOP3
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**Reserved** This bit should be set to zero.
5	**STOP8.** 0: Monitor SMIOVT8 temperature source. 1: Stop monitoring SMIOVT38 temperature source.
4	**STOP7.** 0: Monitor SMIOVT7 temperature source. 1: Stop monitoring SMIOVT3 temperature source.
3	**STOP6.** 0: Monitor SMIOVT6 temperature source. 1: Stop monitoring SMIOVT6 temperature source..
2	**STOP5.** 0: Monitor SMIOVT5 temperature source. 1: Stop monitoring SMIOVT5 temperature source.
1	**STOP4.** 0: Monitor SMIOVT4 temperature source. 1: Stop monitoring SMIOVT4 temperature source.
0	**STOP3.** 0: Monitor SMIOVT3 temperature source. 1: Stop monitoring SMIOVT3 temperature source.

9.459 Configuration Register – Index 09h (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		EN_WS1	EN_WS3	EN_WS3	EN_WS3	EN_WS3	EN_WS3
DEFAULT	0		0	0	0	0	0	0

BIT	DESCRIPTION
7-6	**RESERVED**
5	**Output type of SMIOVT8** 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode.
4	**Output type of SMIOVT7** 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode.
3	**Output type of SMIOVT6** 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode..
2	**Output type of SMIOVT5** 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode.
1	**Output type of SMIOVT4** 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode.
0	**Output type of SMIOVT3** 1: Enable Shut-down Interrupt Mode. 0: Disable Shut-down Interrupt Mode.

9.460 Configuration Register – Index 0Ah (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	EN_ONE8	EN_ONE7	EN_ONE6	EN_ONE5	EN_ONE3	EN_ONE3	Reserved	
DEFAULT	0	0	0	0	0	0	0	

BIT	DESCRIPTION
7	**Output type of SMIOVT8** 1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
6	**Output type of SMIOVT7** 1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
5	**Output type of SMIOVT6** 1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
4	**Output type of SMIOVT5** 1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
3	**Output type of SMIOVT4**

BIT	DESCRIPTION
	1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
2	**Output type of SMIOVT3** 1: Enable One-Times Interrupt Mode. 0: Disable One-Times Interrupt Mode.
1-0	**RESERVED**

9.461 SMIOVT3-8 Temperature Source Configuration Register – Index 0Ch (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Fault6		Fault5		Fault4		Fault3	
DEFAULT	0		0		0		0	

BIT	DESCRIPTION
7-6	**Fault6.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.
5-4	**Fault5.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.
3-2	**Fault4.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.
1-0	**Fault3.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.

9.462 SMIOVT3-8 Temperature Source Configuration Register – Index 0Dh (Bank C)

Attribute: Read/Write
Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				Fault8		Fault7	
DEFAULT	0				0		0	

BIT	DESCRIPTION
7-4	Reserved.
3-2	**Fault8.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.
1-0	**Fault7.** Number of faults to detect before setting OVT# output. This avoids false strapping due to noise. 0 : Two times. 1 : Three times. 2 : Five times. 3 : Seven times.

9.463 SMIOVT3 Temperature Source Over-temperature (High Byte) Register – Index 1Ah (BankC)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.464 SMIOVT4 Temperature Source Over-temperature (High Byte) Register – Index 1Bh (BankC)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.465 SMIOVT5 Temperature Source Over-temperature (High Byte) Register – Index 1Ch (BankC)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.466 SMIOVT6 Temperature Source Over-temperature (High Byte) Register – Index 1Dh (BankC)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.467 SMIOVT7 Temperature Source Over-temperature (High Byte) Register – Index 1Eh (BankC)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.468 SMIOVT8 Temperature Source Over-temperature (High Byte) Register – Index 1Fh (BankC)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	TOVF<8:1>							
DEFAULT	0	1	0	1	0	0	0	0

BIT	DESCRIPTION
7-0	**TOVF<8:1>.** Over-temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 80°C.

9.469 SMIOVT3 Temperature Source Hysteresis (High Byte) Register – Index 20h (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.470 SMIOVT4 Temperature Source Hysteresis (High Byte) Register – Index 21h (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.471 SMIOVT5 Temperature Source Hysteresis (High Byte) Register – Index 22h (Bank C)

Attribute: Read/Write
Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.472 SMIOVT6 Temperature Source Hysteresis (High Byte) Register – Index 23h (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.473 SMIOVT7 Temperature Source Hysteresis (High Byte) Register – Index 24h (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.474 SMIOVT8 Temperature Source Hysteresis (High Byte) Register – Index 25h (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	THYST<8:1>							
DEFAULT	0	1	0	0	1	0	1	1

BIT	DESCRIPTION
7-0	**THYST<8:1>.** Hysteresis temperature bits 8-1. The nine-bit value is in units of 0.5°C, and the default is 75°C.

9.475 SMIOVT3 Temperature Source Select Register – Index 26 (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT3 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT3 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT3 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SMIOVT3 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SMIOVT3 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SMIOVT3 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SMIOVT3 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as SMIOVT3 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as SMIOVT3 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SMIOVT3 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as SMIOVT3 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SMIOVT3 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT3 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SMIOVT3 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SMIOVT3 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SMIOVT3 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as SMIOVT3 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as SMIOVT3 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as SMIOVT3 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as SMIOVT3 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as SMIOVT3 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as SMIOVT3 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as SMIOVT3 monitoring source.

	1 1 1 0 1: Select **PECI Agent 1 Calibration** as SMIOVT3 monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as SMIOVT3 monitoring source.

9.476 SMIOVT4 Temperature Source Select Register – Index 27 (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT4 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT4 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT4 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SMIOVT4 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SMIOVT4 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SMIOVT4 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SMIOVT4 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as SMIOVT4 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as SMIOVT4 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SMIOVT4 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as SMIOVT4 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SMIOVT4 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT4 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SMIOVT4 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SMIOVT4 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SMIOVT4 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as SMIOVT4 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as SMIOVT4 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as SMIOVT4 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as SMIOVT4 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as SMIOVT4 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as SMIOVT4 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as SMIOVT4 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as SMIOVT4 monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as SMIOVT4 monitoring source.

9.477 SMIOVT5 Temperature Source Select Register – Index 28 (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT5 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT5 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT5 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SMIOVT5 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SMIOVT5 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SMIOVT5 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SMIOVT5 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as SMIOVT5 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as SMIOVT5 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SMIOVT5 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as SMIOVT5 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SMIOVT5 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT5 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SMIOVT5 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SMIOVT5 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SMIOVT5 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as SMIOVT5 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as SMIOVT5 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as SMIOVT5 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as SMIOVT5 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as SMIOVT5 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as SMIOVT5 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as SMIOVT5 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as SMIOVT5 monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as SMIOVT5 monitoring source.

9.478 SMIOVT6 Temperature Source Select Register – Index 29 (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT6 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT6 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT6 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SMIOVT6 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SMIOVT6 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SMIOVT6 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SMIOVT6 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as SMIOVT6 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as SMIOVT6 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SMIOVT6 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as SMIOVT6 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SMIOVT6 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT6 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SMIOVT6 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SMIOVT6 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SMIOVT6 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as SMIOVT6 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as SMIOVT6 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as SMIOVT6 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as SMIOVT6 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as SMIOVT6 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as SMIOVT6 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as SMIOVT6 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as SMIOVT6 monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as SMIOVT6 monitoring source.

9.479 SMIOVT7 Temperature Source Select Register – Index 2A (Bank C)

Attribute: Read/Write
Size: 8 bits

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT7 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT7 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT7 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SMIOVT7 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SMIOVT7 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SMIOVT7 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SMIOVT7 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as SMIOVT7 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as SMIOVT7 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SMIOVT7 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as SMIOVT7 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SMIOVT7 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT7 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SMIOVT7 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SMIOVT7 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SMIOVT7 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as SMIOVT7 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as SMIOVT7 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as SMIOVT7 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as SMIOVT7 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as SMIOVT7 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as SMIOVT7 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as SMIOVT7 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as SMIOVT7 monitoring source. 1 1 1 1 1: Select **Virtual_TEMP** as SMIOVT7 monitoring source.

9.480 SMIOVT8 Temperature Source Select Register – Index 2B (Bank C)

Attribute: Read/Write
Size: 8 bits
Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

BIT	7	6	5	4	3	2	1	0

NAME	RESERVED			SMIOVT_SRC3				
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-5	**RESERVED**
4-0	**SMIOVT8 Temperature selection.** **Bits** **4 3 2 1 0** 0 0 0 0 1: Select **SYSTIN** as SMIOVT8 monitoring source. (Default) 0 0 0 1 0: Select **CPUTIN** as SMIOVT8 monitoring source. 0 0 0 1 1: Select **AUXTIN0** as SMIOVT8 monitoring source. 0 0 1 0 0: Select **AUXTIN1** as SMIOVT8 monitoring source. 0 0 1 0 1: Select **AUXTIN2** as SMIOVT8 monitoring source. 0 0 1 1 0: Select **AUXTIN3** as SMIOVT8 monitoring source. 0 0 1 1 1: Select **AUXTIN4** as SMIOVT8 monitoring source. 0 1 0 0 0: Select **SMBUSMASTER 0** as SMIOVT8 monitoring source. 0 1 0 0 1: Select **SMBUSMASTER 1** as SMIOVT8 monitoring source. 0 1 0 1 0: Reserved. 0 1 0 1 1: Reserved. 0 1 1 0 0: Reserved. 0 1 1 0 1: Reserved. 0 1 1 1 0: Reserved. 0 1 1 1 1: Reserved. 1 0 0 0 0: Select **PECI Agent 0** as SMIOVT8 monitoring source. 1 0 0 0 1: Select **PECI Agent 1** as SMIOVT8 monitoring source. 1 0 0 1 0: Select **PCH_CHIP_CPU_MAX_TEMP** as SMIOVT8 monitoring source. 1 0 0 1 1: Select **PCH_CHIP_TEMP** as SMIOVT8 monitoring source. 1 0 1 0 0: Select **PCH_CPU_TEMP** as SMIOVT8 monitoring source. 1 0 1 0 1: Select **PCH_MCH_TEMP** as SMIOVT8 monitoring source. 1 0 1 1 0: Select **Agent0 Dimm0** as SMIOVT8 monitoring source. 1 0 1 1 1: Select **Agent0 Dimm1** as SMIOVT8 monitoring source. 1 1 0 0 0: Select **Agent1 Dimm0** as SMIOVT8 monitoring source. 1 1 0 0 1: Select **Agent1 Dimm1** as SMIOVT8 monitoring source. 1 1 0 1 0: Select **BYTE_TEMP0** as SMIOVT8 monitoring source. 1 1 0 1 1: Select **BYTE_TEMP1** as SMIOVT8 monitoring source. 1 1 1 0 0: Select **PECI Agent 0 Calibration** as SMIOVT8 monitoring source. 1 1 1 0 1: Select **PECI Agent 1 Calibration** as SMIOVT8 monitoring source. 1 1 1 1 1: Reserved.

9.481 HM Read Only Register

ADDRESS A6-A0	DESCRIPTION
00h	CPUVCORE reading
01h	VIN1 reading
02h	AVSB reading
03h	3VCC reading

ADDRESS A6-A0	DESCRIPTION
04h	VIN0 reading
05h	VIN8 reading
06h	VIN4 reading
07h	3VSB reading
08h	VBAT reading
09h	VTT reading
0Ah	VIN5 reading
0Bh	VIN6 reading
0Ch	VIN2 reading
0Dh	VIN3 reading
0Eh	VIN7 reading
0Fh	VIN9 reading
10h	SYSTIN temperature reading
11h	CPUTIN temperature reading
12h	AUXTIN0 temperature reading
13h	AUXTIN1 temperature reading
14h	AUXTIN2 temperature reading
15h	AUXTIN3 temperature reading
16h	AUXTIN4 temperature reading
17h	Reserved
18h	Reserved
19h	SYSFANOUT fan control temperature reading.
1Ah	CPUFANOUT fan control temperature reading.
1Bh	AUXFANOUT0 fan control temperature reading.
1Ch	AUXFANOUT1 fan control temperature reading.
1Dh	AUXFANOUT2 fan control temperature reading.
1Eh	AUXFANOUT3 fan control temperature reading.
1Fh	Reserved
20h	CPU_Weight temperature reading
21h	Reserved
22h	SYSFAN duty target reading.
23h	CPUFAN duty target reading.
24h	AUXFAN0 duty target reading.
25h	AUXFAN1 duty target reading.
26h	AUXFAN2 duty target reading.
27h	AUXFAN3 duty target reading.
28h	SYSFAN rpm target reading.

ADDRESS A6-A0	DESCRIPTION
29h	CPUFAN rpm target reading.
2Ah	AUXFAN0 rpm target reading.
2Bh	AUXFAN1 rpm target reading.
2Ch	AUXFAN2 rpm target reading.
2Dh	AUXFAN3 rpm target reading.
2Eh	SYSFANIN COUNT High-byte reading
2Fh	SYSFANIN COUNT Low-byte reading
30h	CPUFANIN COUNT High-byte reading
31h	CPUFANIN COUNT Low-byte reading
32h	AUXFANIN0 COUNT High-byte reading
33h	AUXFANIN0 COUNT Low-byte reading
34h	AUXFANIN1 COUNT High-byte reading
35h	AUXFANIN1 COUNT Low-byte reading
36h	AUXFANIN2 COUNT High-byte reading
37h	AUXFANIN2 COUNT Low-byte reading
38h	AUXFANIN3 COUNT High-byte reading
39h	AUXFANIN3 COUNT Low-byte reading
3Ah	SYSFANIN SPEED High-byte (rpm) reading
3Bh	SYSFANIN SPEED Low-byte (rpm) reading
3Ch	CPUFANIN SPEED High-byte (rpm) reading
3Dh	CPUFANIN SPEED Low-byte (rpm) reading
3Eh	AUXFANIN0 SPEED High-byte (rpm) reading
3Fh	AUXFANIN0 SPEED Low-byte (rpm) reading
40h	AUXFANIN1 SPEED High-byte (rpm) reading
41h	AUXFANIN1 SPEED Low-byte (rpm) reading
42h	AUXFANIN2 SPEED High-byte (rpm) reading
43h	AUXFANIN2 SPEED Low-byte (rpm) reading
44h	AUXFANIN3 SPEED High-byte (rpm) reading
45h	AUXFANIN3 SPEED Low-byte (rpm) reading
46h	AUXFANIN4 SPEED High-byte (rpm) reading
47h	AUXFANIN4 SPEED Low-byte (rpm) reading
48h	AUXFANOUT4 Output Value reading
49h	Reserved
4Ah	Reserved
4Bh	Reserved
4Ch	SYSFANOUT Output Value reading
4Dh	CPUFANOUT Output Value reading

ADDRESS A6-A0	DESCRIPTION
4Eh	AUXFANOUT0 Output Value reading
4Fh	AUXFANOUT1 Output Value reading
50h	AUXFANOUT2 Output Value reading
51h	AUXFANOUT3 Output Value reading
52h	PECI Agent 0 reading
53h	Reserved
54h	PECI Agent 1 reading
55h	Reserved
56h	PCH_CHIP_CPU_MAX_TEMP reading
57h	PCH_CHIP_TEMP reading
58h	PCH_CPU_TEMP_H reading
59h	PCH_CPU_TEMP_L reading
5Ah	PCH_MCH_TEMP reading
5Bh	PCH_MCH_TEMP reading
5Ch	Agent0 Dimm0 reading
5Dh	Agent0 Dimm1 reading
5Eh	Agent1 Dimm0 reading
5Fh	Agent1 Dimm1 reading
60h	PCH_TSI0_TEMP_H reading
61h	PCH_TSI0_TEMP_L reading
62h	PCH_TSI1_TEMP_H reading
63h	PCH_TSI1_TEMP_L reading
64h	Reserved
65h	Reserved
66h	Reserved
67h	Reserved
68h	Reserved
69h	Reserved
6Ah	Reserved
6Bh	Reserved
6Ch	Reserved
6Dh	Reserved
6Eh	Reserved
6Fh	ByteTemp_H reading
70h	ByteTemp_L reading
71h	PECI Agent0 Calibration Temp reading
72h	PECI Agent1 Calibration Temp reading

ADDRESS A6-A0	DESCRIPTION
73h	Reserved
74h	Reserved
75h	SMIOVT1 temperature source reading.
76h	SMIOVT2 temperature source reading.

10. UART PORT

10.1 UART Control Register (UCR) (Read/Write)

The UART Control Register defines and controls the protocol for asynchronous data communications; including data length, stop bit, parity, and baud rate selection.

BIT	7	6	5	4	3	2	1	0
NAME	BDLAB	SSE	PBFE	EPE	PBE	MSBE	DLS1	DLS0
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**BDLAB (Baud Rate Divisor Latch Access Bit).** When this bit is set to logic 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud-rate generator during a read or write operation. When this bit is set to logic 0, the Receiver Buffer Register, the Transmitter Buffer Register, and the Interrupt Control Register can be accessed.
6	**SSE (Set Silence Enable).** A logic 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.
5	**PBFE (Parity Bit Fixed Enable).** When PBE and PBFE of UCR are both set to logic 1, (1) if EPE is logic 1, the parity bit is logical 0 when transmitting and checking; (2) if EPE is logic 0, the parity bit is logical 1 when transmitting and checking.
4	**EPE (Even Parity Enable).** When PBE is set to logic 1, this bit counts the number of logic 1's in the data word bits and determines the parity bit. When this bit is set to logic 1, the parity bit is set to logic 1 if an even number of logic 1's are sent or checked. When the bit is set to logic 0, the parity bit is logic 1, if an odd number of logic 1's are sent or checked.
3	**PBE (Parity Bit Enable).** When this bit is set to logic 1, the transmitter inserts a stop bit between the last data bit and the stop bit of the SOUT, and the receiver checks the parity bit in the same position.
2	**MSBE (Multiple Stop Bit Enable).** Defines the number of stop bits in each serial character that is transmitted or received. (1) If MSBE is set to logic 0, one stop bit is sent and checked. (2) If MSBE is set to logic 1 and the data length is 5 bits, one-and-a-half stop bits are sent and checked. (3) If MSBE is set to logic 1 and the data length is 6, 7, or 8 bits, two stop bits are sent and checked.
1	**DLS1 (Data Length Select Bit 1).** Defines the number of data bits that are sent or checked in each serial character.
0	**DLS0 (Data Length Select Bit 0).** Defines the number of data bits that are sent or checked in each serial character.

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits

DLS1	DLS0	DATA LENGTH
1	1	8 bits

The following table identifies the remaining UART registers. Each one is described separately in the following sections.

Table 10-1 Register Summary for UART

Bit Number										
Register Address Base			**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
+ 0 BDLAB = 0	Receiver Buffer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter Buffer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	UFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.
**: These bits are always 0 in 16450 Mode.

10.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of data transfer during communication.

BIT	7	6	5	4	3	2	1	0
NAME	RF EI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
DEFAULT	0	1	1	0	0	0	0	0

BIT	DESCRIPTION
7	**RF EI (RX FIFO Error Indication).** In 16450 mode, this bit is always set to logical 0. In 16550 mode, this bit is set to logical 1 when there is at least one parity-bit error and no stop0bit error or silent-byte detected in the FIFO. In 16550 mode, this bit is cleared to logical 0 by reading from the USR if there are no remaining errors left in the FIFO.
6	**TSRE (Transmitter Shift Register Empty).** In 16450 mode, this bit is set to logical 1 when TBR and TSR are both empty. In 16550 mode, it is set to logical 1 when the transmit FIFO and TSR are both empty. Otherwise, this bit is set to logical 0.
5	**TBRE (Transmitter Buffer Register Empty).** In 16450 mode, when a data character is transferred from TBR to TSR, this bit is set to logical 1. If ETREI of ICR is high, and interrupt is generated to notify the CPU to write next data. In 16550 mode, this bit is set to logical 1 when the transmit FIFO is empty. It is set to logical 0 when the CPU writes data into TBR or the FIFO.
4	**SBD (Silent Byte Detected).** This bit is set to logical 1 to indicate that received data are kept in silent state for the time it takes to receive a full word, which includes the start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
3	**NSER (No Stop Bit Error).** This bit is set to logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
2	**PBER (Parity Bit Error).** This bit is set to logical 1 to indicate that the received data has the wrong parity bit. In 16550 mode, it indicates the same condition for the data on the top of the FIFO. When the CPU reads USR, it sets this bit to logical 0.
1	**OER (Overrun Error).** This bit is set to logical 1 to indicate that the received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition, instead of FIFO full. When the CPU reads USR, it sets this bit to logical 0.
0	**RDR (RBR Data Ready).** This bit is set to logical 1 to indicate that the received data are ready to be read by the CPU in the RBR or FIFO. When no data are left in the RBR or FIFO, the bit is set to logical 0.

10.3 Handshake Control Register (HCR) (Read/Write)

This register controls pins used with handshaking peripherals such as modems and also controls the diagnostic mode of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED			INTERNAL LOOPBACK ENABLE	IRQ ENABLE	LOOPBACK RI INPUT	RTS	DTR
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-5	**Reserved**
4	**Internal Loopback Enable.** When this bit is set to logic 1, the UART enters diagnostic mode, as follows: (1) SOUT is forced to logic 1, and SIN is isolated from the communication link. (2) The modem output pins are set to their inactive state. (3) The modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) →DSR#, RTS (bit 1 of HCR) →CTS#, Loopback RI input (bit 2 of HCR) → RI# and IRQ enable (bit 3 of HCR) →DCD#. Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.
3	**IRQ Enable.** The UART interrupt output is enabled by setting this bit to logic 1. In diagnostic mode, this bit is internally connected to the modem control input DCD#.
2	**Loopback RI Input.** This bit is only used in the diagnostic mode. In diagnostic mode, this bit is internally connected to the modem control input RI#.
1	**RTS (Request to Send).** This bit controls the RTS# output. The value of this bit is inverted and output to RTS#.
0	**DTR (Data Terminal Ready).** This bit controls the DTR# output. The value of this bit is inverted and output to DTR#.

10.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins used with handshake peripherals such as modems and records changes on these pins.

BIT	7	6	5	4	3	2	1	0
NAME	DCD	RI	DSR	CTS	TDCD	FERI	TDSR	TCTS
DEFAULT	NA	NA	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7	**DCD (Data Carrier Detect).** This bit is the inverse of the DCD# input and is equivalent to bit 3 of HCR in Loopback mode.
6	**RI (Ring Indicator).** This bit is the inverse of the RI# input and is equivalent to bit 2 of HCR in Loopback mode.
5	**DSR (Data Set Ready).** This bit is the inverse of the DSR# input and is equivalent to bit 0 of HCR in Loopback mode.
4	**CTS (Clear to Send).** This bit is the inverse of the CTS# input and is equivalent to bit 1 of HCR in Loopback mode.
3	**TDCD (DCD# Toggling).** This bit indicates that the state of the DCD# pin has changed after HSR is read by the CPU.
2	**FERI (RI Falling Edge).** This bit indicates that the RI# pin has changed from low to high after HSR is read by the CPU.
1	**TDSR (DSR# Toggling).** This bit indicates that the state of the DSR# pin has changed after HSR is read by the CPU.
0	**TCTS (CTS# Toggling).** This bit indicates that the state of the CTS# pin has changed after HSR is read by the CPU.

10.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.

BIT	7	6	5	4	3	2	1	0
NAME	MSB	LSB	RESERVED		DMA MODE SELECT	TRANSMITTER FIFO RESET	RECEIVER FIFO RESET	FIFO ENABLE
DEFAULT	0	0	NA	NA	0	0	0	0

BIT	DESCRIPTION	
7	**MSB (RX Interrupt Active Level).**	These two bits are used to set the active level of the receiver FIFO interrupt. The active level is the number of bytes that must be in the receiver FIFO to generate an interrupt.
6	**LSB (RX Interrupt Active Level).**	
5-4	**RESERVED**	
3	**DMS MODE SELECT.** When this bit is set to logic 1, DMA mode changes from mode 0 to mode 1 if UFR bit 0 = 1.	
2	**TRANSMITTER FIFO RESET.** Setting this bit to logic 1 resets the TX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
1	**RECEIVER FIFO RESET.** Setting this bit to logic 1 resets the RX FIFO counter logic to its initial state. This bit is automatically cleared afterwards.	
0	**FIFO ENABLE.** This bit enables 16550 (FIFO) mode. This bit should be set to logic 1 before other UFR bits are programmed.	

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

10.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status.

BIT	7	6	5	4	3	2	1	0
NAME	FIFOS ENABLED		RESERVED		INTERRUPT STATUS BIT 2	INTERRUPT STATUS BIT 1	INTERRUPT STATUS BIT 0	0 IF INTERRUPT PENDING
DEFAULT	0	0	0	0	0	0	0	1

BIT	DESCRIPTION
7-6	**FIFOS ENABLED.** Set to logical 1 when UFR, bit 0 = 1.
5-4	**RESERVED**

3	**INTERRUPT STATUS BIT 2.** In 16450 mode, this bit is logical 0. In 16550 mode, bits 3 and 2 are set to logical 1 when a time-out interrupt is pending. Please see the table below.	
2	**INTERRUPT STATUS BIT 1.**	These two bits identify the priority level of the pending interrupt, as shown in the table below.
1	**INTERRUPT STATUS BIT 0.**	
0	**0 IF INTERRUPT PENDING.** This bit is logic 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit is set to logical 0.	

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

10.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register enables and disables the five types of controller interrupts separately. A selected interrupt can be enabled by setting the appropriate bit to logical 1. The interrupt system can be totally disabled by setting bits 0 through 3 to logical 0.

BIT	7	6	5	4	3	2	1	0
NAME	En_address_byte	RX_ctrl	RESERVED		EHSRI	EUSRI	ETBREI	ERDRI
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**En_address_byte.** 0: Tx block will send data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Tx block will send address byte. (If enable 9bit mode function CRF2 Bit0=1)
6	**RX_ctrl.** 0: Rx block could receive data byte. (If enable 9bit mode function CRF2 Bit0=1) 1: Rx block could receive address byte. (If enable 9bit mode function CRF2 Bit0=1)
5-4	**RESERVED**
3	**EHSRI (Handshake Status Interrupt Enable).** Set this bit to logical 1 to enable the

BIT	DESCRIPTION
	handshake status register interrupt.
2	**EUSRI (UART Receive Status Interrupt Enable).** Set this bit to logical 1 to enable the UART status register interrupt.
1	**ETBREI (TBR Empty Interrupt Enable).** Set this bit to logical 1 to enable the TBR empty interrupt.
0	**ERDRI (RBR Data Ready Interrupt Enable).** Set this bit to logical 1 to enable the RBR data ready interrupt.

10.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divide it by a divisor from 1 to (2^{16} –1). The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table below illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode, the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. As a result, in high-speed mode, the data transmission rate can be as high as 1.5M bps.

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
PRE-DIV: 13 1.8461M HZ	**PRE-DIV:1.625 14.769M HZ**	**PRE-DIV: 1.0 24M HZ**	**DECIMAL DIVISOR USED TO GENERATE 16X CLOCK**	**ERROR PERCENTAGE**
50	400	650	2304	**
75	600	975	1536	**
110	880	1430	1047	0.18%
134.5	1076	1478.5	857	0.099%
150	1200	1950	768	**
300	2400	3900	384	**
600	4800	7800	192	**
1200	9600	15600	96	**
1800	14400	23400	64	**
2000	16000	26000	58	0.53%
2400	19200	31200	48	**
3600	28800	46800	32	**
4800	38400	62400	24	**
7200	57600	93600	16	**
9600	76800	124800	12	**
19200	153600	249600	6	**
38400	307200	499200	3	**
57600	460800	748800	2	**
115200	921600	1497600	1	**

** Unless specified, the error percentage for all of the baud rates is 0.16%.

Note: Pre-Divisor is determined by CRF0 of UART A and B.

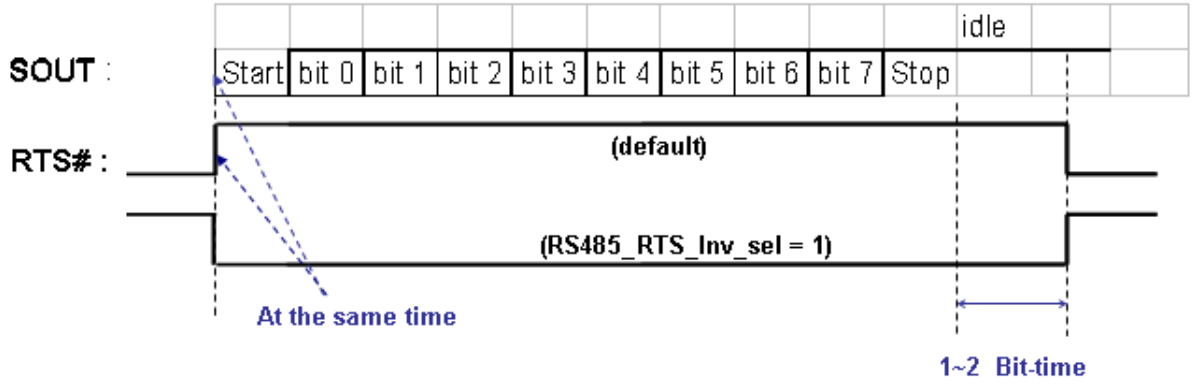
10.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

10.10 UART RS485 Auto Flow Control

NCT6796D supports RS485 auto flow control function for UARTA and UARTB. When enabling the RS485 auto control function, it will automatically drive RTS# pin to logic high or low for UARTA and UARTB when UART TX block transmits the data.

The diagram shown below illustrates the RS485 auto flow control function for UARTA I UARTB.



The default behavior of RTS# pin will drive logic high the time edge between **Start bit** and **bit0** when the UART TX Block start to transmits the data on SOUT pin. Then the RTS# pin will drive logic low later than **Stop bit** about 1~2 x Bit-time when UART TX Block completes the data transmission. The driving behavior of RTS# will be inverted when we set RS485_RTS_inv_sel bit = 1'b1. (Bit-time: Depends on the baud rate of transmission)

The bellowing control register table relates to the RS485 auto flow control function for UARTA and UARTB.

	UARTA	UARTB
RTS485_enable	Logic Device 2, CRF2_Bit7	Logic Device 3, CRF2_Bit7
RTS485_inv_sel	Logic Device 2, CRF2_Bit6	Logic Device 3, CRF2_Bit6

11. PARALLEL PORT

11.1 Printer Interface Logic

The NCT6796D parallel port can be attached to devices that accept eight bits of parallel data at standard TTL level. The NCT6796D supports the IBM XT/AT compatible parallel port (SPP), the bi-directional parallel port (BPP), the Enhanced Parallel Port (EPP), and the Extended Capabilities Parallel Port (ECP).

The following tables show the pin definitions for different modes of the parallel port.

Table 11-1 Pin Descriptions for SPP, EPP, and ECP Modes

HOST CONNECTOR	PIN NUMBER OF NCT6796D	PIN ATTRIBUTE	SPP	EPP	ECP
1	55	O	Nstb	nWrite	nSTB, HostClk[2]
2-9	42-45, 47-50	I/O	PD<7:0>	PD<7:0>	PD<7:0>
10	41	I	nACK	Intr	nACK, PeriphClk[2]
11	40	I	BUSY	nWait	BUSY, PeriphAck[2]
12	39	I	PE	PE	Peerror, nAckReverse[2]
13	38	I	SLCT	Select	SLCT, Xflag[2]
14	54	O	Nafd	nDStrb	nAFD, HostAck[2]
15	53	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	52	O	Ninit	nInit	nINIT[1], nReverseRqst[2]
17	51	O	nSLIN	nAStrb	nSLIN[1], ECPMode[2]

Notes:

n<name > : Active Low

1. Compatible Mode
2. High Speed Mode
3. For more information, please refer to the IEEE 1284 standard.

HOST CONNECTOR	PIN NUMBER OF NCT6796D	PIN ATTRIBUTE	SPP
1	55	O	nSTB
2	50	I/O	PD0
3	49	I/O	PD1
4	48	I/O	PD2
5	47	I/O	PD3
6	45	I/O	PD4
7	44	I/O	PD5
8	43	I/O	PD6
9	42	I/O	PD7
10	41	I	nACK
11	40	I	BUSY
12	39	I	PE
13	38	I	SLCT
14	54	O	nAFD
15	53	I	nERR
16	52	O	nINIT

HOST CONNECTOR	PIN NUMBER OF NCT6796D	PIN ATTRIBUTE	SPP
17	51	O	nSLIN

11.2 Enhanced Parallel Port (EPP)

The following table lists the registers used in the EPP mode and identifies the bit map of the parallel port and EPP registers. Some of the registers are used in other modes as well.

Table 11-2 EPP Register Addresses

A2	A1	A0	REGISTER	NOTE
0	0	0	Data pot (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

1. These registers are available in all modes.
2. These registers are available only in EPP mode.

Table 11-3 Address and Bit Map for SPP and EPP Modes

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	BUSY#	ACK#	PE	SLCT	ERROR#	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1	1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Each register (or pair of registers, in some cases) is discussed below.

11.2.1 Data Port (Data Swapper)

The CPU reads the contents of the printer's data latch by reading the data port.

11.2.2 Printer Status Buffer

The CPU reads the printer status by reading the printer status buffer. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	BUSY#	ACK#	PE	SLCT	ERROR#	RESERVED		TMOUT

DEFAULT	NA	NA	NA	NA	NA	1	1	0

BIT	DESCRIPTION
7	**BUSY#.** This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.
6	**ACK#.** This bit represents the current state of the printer's ACK# signal. A logical 0 means the printer has received a character and is ready to accept another. Normally, this signal is active for approximately 5 μs before BUSY# stops.
5	**PE.** A logical 1 means the printer has detected the end of paper.
4	**SLCT.** A logical 1 means the printer is selected.
3	**ERROR#.** A logical 0 means the printer has encountered an error condition.
2-1	**RESERVED**
0	**TMOUT.** This bit is only valid in EPP mode. A logical 1 indicates that a 10-μs time-out has occurred on the EPP bus; a logical 0 means hat no time-out error has occurred. Writing a logical 1 to this bit clears the time-out status bit; writing a logical 0 has no effect.

11.2.3 Printer Control Latch and Printer Control Swapper

The CPU reads the contents of the printer control latch by reading the printer control swapper. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED		DIR	IRQ ENABLE	SLCT IN	INIT#	AUTO FD	STROBE
DEFAULT	1	1	NA	0	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	**RESERVED** These two bits are always read as logical 1 and can be written.
5	**DIR (Direction Control Bit).** When this bit is logical 1, the parallel port is in the input mode (read). When it is logical 0, the parallel port is in the output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.
4	**IRQ ENABLE.** A logical 1 allows an interrupt to occur when ACK# changes from low to high.
3	**SLCT IN.** a logical 1 selects the printer.
2	**INIT#.** A logical 0 starts the printer (50 microsecond pulse, minimum).
1	**AUTO FD.** A logical 1 causes the printer to line-feed after a line is printed.
0	**STROBE.** A logical 1 generates an active-high pulse for a minimum of 0.5 μs to clock data into the printer. Valid data must be presented for a minimum of 0.5 μs before and after the strobe pulse.

11.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

11.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. The bit definitions for each data port are the same and as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

When any EPP data port is accessed, the contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

11.2.6 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
Nwrite	O	Denotes read or write operation for address or data.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
Nwait	I	Inactivated to acknowledge that data transfer is complete. Activated to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer-select status; same as SPP mode.
NDStrb	O	This signal is active low. It denotes a data read or write operation.
Nerror	I	Error; same as SPP mode.
Ninits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
NAStrb	O	This signal is active low. It denotes an address read or write operation.

11.2.7 EPP Operation

When EPP mode is selected, the PDx bus is in standard or bi-directional mode when no EPP read, write, or address cycle is being executed. In this situation, all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μS have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in status bit 0.

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

11.2.8 EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If nWait is active low, the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, proceeds normally, and is completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle cannot start. It must wait until nWait changes to active low, at which time it starts as described above.

11.2.9 EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it does not finish until nWait changes from active low to inactive high.

11.3 Extended Capabilities Parallel (ECP) Port

This port is software- and hardware-compatible with existing parallel ports, so the NCT6796D parallel port may be used in standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host-to-peripheral) and reverse (peripheral-to-host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port hardware supports run-length-encoded (RLE) decompression. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. RLE compression is required; the hardware support is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

The NCT6796D ECP supports the following modes.

Table 11-4 ECP Mode Description

MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CRF0h to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

The mode selection bits are bits 7-5 of the Extended Control Register.

11.3.1 ECP Register and Bit Map

The next two tables list the registers used in ECP mode and provide a bit map of the parallel port and ECP registers.

Table 11-5 ECP Register Addresses

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR60 and 61, which are determined by configuration register or hardware setting.

Table 11-6 Bit Map of the ECP Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
Dsr	nBusy	nAck	Perror	Select	nFault	1	1	1	1
Dcr	1	1	Directio	ackIntEn	SelectIn	nInit	Autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
Ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

Each register (or pair of registers, in some cases) is discussed below.

11.3.2 Data and ecpAFifo Port

Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input, and the contents of this register are output to PD0-PD7. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. This operation is defined only for the forward direction. The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Address/RLE	Address or RLE						

11.3.3 Device Status Register (DSR)

These bits are logical 0 during a read of the Printer Status Register. The bits of this status register are defined as follows:

BIT	7	6	5	4	3	2	1	0
NAME	nBusy	nAck	Perror	Select	nFault	1	1	1

BIT	DESCRIPTION
7	**nBusy.** This bit reflects the complement of the Busy input.
6	**nAck.** This bit reflects the nAck input.
5	**Perror.** This bit reflects the Perror input.
4	**Select.** This bit reflects the Select input.
3	**nFault.** This bit reflects the nFault input.
2-0	These three bits are not implemented and are always logical 1 during a read.

11.3.4 Device Control Register (DCR)

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	Reserved		Director	ackInEn	SelectIn	nInit	Autofd	Strobe
DEFAULT	1	1	NA	NA	NA	NA	NA	NA

BIT	DESCRIPTION
7-6	**Reserved** These two bits are always read as logical 1 and cannot be written.
5	**Director.** If the mode is 000 or 010, this bit has no effect and the direction is always out. In other modes, 0: The parallel port is in the output mode. 1: The parallel port is in the input mode.
4	**ackInEn** (Interrupt Request Enable). When this bit is set to logical 1, it enables interrupt requests from the parallel port to the CPU on the low-to-high transition on ACK#.
3	**SelectIn.** This bit is inverted and output to the SLIN# output. 0: The printer is not selected. 1: The printer is selected.

BIT	DESCRIPTION
2	**nInit.** This bit is output to the INIT# output.
1	**Autofd.** This bit is inverted and output to the AFD# output.
0	**Strobe.** This bit is inverted and output to the STB# output.

11.3.5 CFIFO (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. Bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte-aligned.

11.3.6 ECPDFIFO (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte-aligned.

When the direction bit is 1, data bytes from the peripheral are read via automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO return bytes of ECP data to the system.

11.3.7 TFIFO (Test FIFO Mode) Mode = 110

Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO is not transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

11.3.8 CNFGA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates that this is an 8-bit implementation.

11.3.9 CNFGB (Configuration Register B) Mode = 111

The bit definitions are as follows:

BIT	7	6	5	4	3	2	1	0
NAME	COMPRESS	intrVALUE	IRQx2	IRQx1	IRQx0	RESERVED		
DEFAULT	0	0	0	0	0	1	1	1

<table>
<tr><th>BIT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td colspan="2">Compress. This bit is read-only. It is logical 0 during a read, which means that this chip does not support hardware RLE compression.</td></tr>
<tr><td>6</td><td colspan="2">intrValue. Returns the value on the ISA IRQ line to determine possible conflicts.</td></tr>
<tr><td>5</td><td>IRQx2.</td><td>Reflects the IRQ resource assigned for ECP port.
<table>
<tr><th>cnfgB[5:3]</th><th>IRQ resource</th></tr>
<tr><td>000</td><td>Reflects other IRQ resources selected by PnP register (default)</td></tr>
</table></td></tr>
</table>

BIT	DESCRIPTION		
4	**IRQx1.**	001	IRQ7
		010	IRQ9
		011	IRQ10
		100	IRQ11
		101	IRQ14
3	**IRQx0.**	110	IRQ15
		111	IRQ5
2-0	**Reserved** These three bits are logical 1 during a read and can be written.		

11.3.10ECR (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:

BIT	7	6	5	4	3	2	1	0
NAME	MODE			nErrIntrEn	dmaEn	ServiceIntr	Full	Empty
DEFAULT	0	0	0	1	0	1	0	1

BIT	DESCRIPTION	
7-5	**Mode.** Read/Write. These bits select the mode.	
	000	Standard Parallel Port (SPP) mode. The FIFO is reset in this mode.
	001	PS/2 Parallel Port mode. This is the same as SPP mode except that direction may be used to tri-state the data lines. Furthermore, reading the data register returns the value on the data lines, not the value in the data register.
	010	Parallel Port FIFO mode. This is the same as SPP mode except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.
	011	ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral using the ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
	100	EPP Mode. EPP mode is activated if the EPP mode is selected.
	101	Reserved
	110	Test Mode. The FIFO may be written and read in this mode, but the data is not transmitted on the parallel port.
	111	Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.
4	**nErrIntrEn.** Read/Write (Valid only in ECP Mode) 0: Enables the interrupt generated on the falling edge of nFault. This prevents interrupts from being lost in the time between the read of the ECR and the write of the ECR. 1: Disables the interrupt generated on the asserting edge of nFault.	

BIT	DESCRIPTION
3	**dmaEn.** Read/Write. 0: Disable DMA unconditionally. 1: Enable DMA.
2	**serviceIntr.** Read/Write. 0: Enable one of the following cases of interrupts. When one of the serviced interrupts occurs, this bit is set to logical 1 by the hardware. This bit must be rest to logical 0 to re-enable the interrupts. (a) dmaEn = 1: During DMA, this bit is set to logical 1 when terminal count is reached. (b) dmaEn = 0, direction = 0: This bit is set to logical 1 whenever there are writeIntr threshold or more bytes free in the FIFO. (c) dmaEn = 0, direction = 1: This bit is set to logical 1 whenever there are readIntr threshold or more valid bytes to be read from the FIFO. 1: Disable DMA and all of the service interrupts. Writing a logical 1 to this bit does not cause an interrupt.
1	**Full.** Read Only. 0: The FIFO has at least one free byte. 1: The FIFO is completely full; it cannot accept another byte.
0	**Empty.** Read Only. 0: The FIFO contains at least one byte of data. 1: The FIFO is completely empty.

11.3.11ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
Nstrobe (HostClk)	O	This pin loads data or address into the slave on its asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contain address, data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. In the reverse direction, it indicates whether the data lines contain ECP command information or data. Normal data are transferred when Busy (PeriphAck) is high, and an 8-bit command is transferred when it is low.
Perror (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on-line.
NautoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. In the forward direction, this signal indicates whether the data lines contain ECP address or data. Normal data are transferred when nAutoFd (HostAck) is high, and an 8-bit command is transferred when it is low.

NAME	TYPE	DESCRIPTION
nFault (nPeriphReuqest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

11.3.12 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits.

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

I Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

0 Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

11.3.12.1. Mode Switching

The software must handle P1284 negotiation and all operations prior to a data transfer in SPP or PS/2 modes (000 or 001). The hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port, only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

In extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode, the software should wait for all the data to be read from the FIFO before changing back to mode 000 or 001.

11.3.12.2. Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high, and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high, and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

11.3.12.3. Data Compression

The NCT6796D hardware supports RLE decompression and can transfer compressed data to a peripheral. Odd (RLE) compression is not supported in the hardware, however. In order to transfer data in ECP mode, the compression count is written to ecpAFifo and the data byte is written to ecpDFifo.

11.3.13FIFO Operation

The FIFO threshold is set in CR5. All data transferred to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used in Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

11.3.14DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or Cfifo. DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA empties or fills the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated, and serviceIntr is asserted, which will disable the DMA.

11.3.15Programmed I/O (NON-DMA) Mode

The ECP and parallel port FIFOs can also be operated using interrupt-driven, programmed I/O. Programmed I/O transfers are

1. To the ecpDFifo at 400H and ecpAFifo at 000H
2. From the ecpDFifo located at 400H
3. To / from the tFifo at 400H.

The host must set dmaEn and serviceIntr to 0 and also must set the direction and state accordingly in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O empties or fills the FIFO using the appropriate direction and mode.

12. KEYBOARD CONTROLLER

The NCT6796D KBC (8042 with licensed KB BIOS) circuit is designed to provide the functions needed to interface a CPU with a keyboard and/or a PS/2 mouse and can be used with IBM®-compatible personal computers or PS/2-based systems. The controller receives serial data from the keyboard or PS/2 mouse, checks the parity of the data, and presents the data to the system as a byte of data in its output buffer. Then, the controller asserts an interrupt to the system when data are placed in its output buffer. The keyboard and PS/2 mouse are required to acknowledge all data transmissions. No transmission should be sent to the keyboard or PS/2 mouse until an acknowledgement is received for the previous data byte.

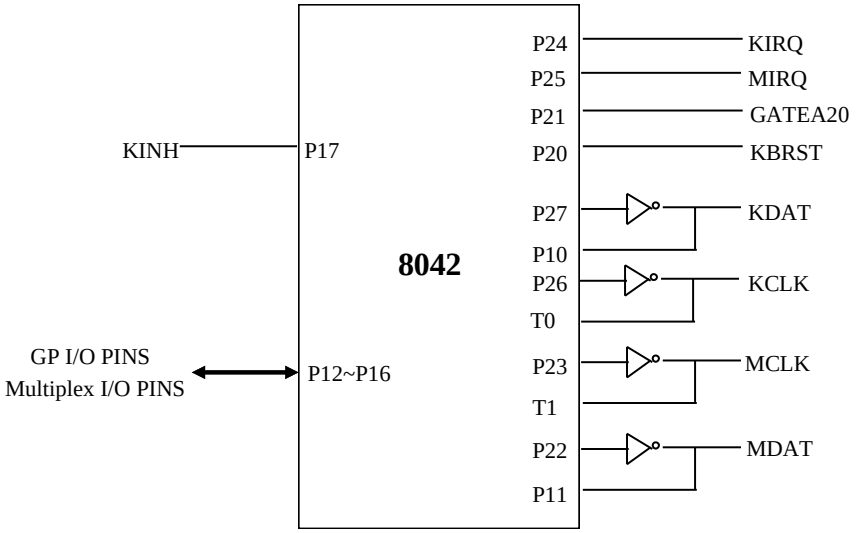


Figure 12-1 Keyboard and Mouse Interface

12.1 Output Buffer

The output buffer is an 8-bit, read-only register at I/O address 60H (Default, PnP programmable I/O address LD5-CR60 and LD5-CR61). The keyboard controller uses the output buffer to send the scan code (from the keyboard) and required command bytes to the system. The output buffer can only be read when the output buffer full bit in the register (in the status register) is logical 1.

12.2 Input Buffer

The input buffer is an 8-bit, write-only register at I/O address 60h or 64h (Default, PnP programmable I/O address LD5-CR60, LD5-CR61, LD5-CR62, and LD5-CR63). Writing to address 60h sets a flag to indicate a data write; writing to address 64h sets a flag to indicate a command write. Data written to I/O address 60h is sent to the keyboard (unless the keyboard controller is expecting a data byte) through the controller's input buffer only if the input buffer full bit (in the status register) is logical 0.

12.3 Status Register

The status register is an 8-bit, read-only register at I/O address 64h (Default, PnP programmable I/O address LD5-CR62 and LD5-CR63) that holds information about the status of the keyboard controller and interface. It may be read at any time.

Table 12-1 Bit Map of Status Register

BIT	BUT FUNCTION	DESCRIPTION
0	Output Buffer Full	0: Output buffer empty 1: Output buffer full
1	Input Buffer Full	0: Input buffer empty 1: Input buffer full
2	System Flag	This bit may be set to 0 or 1 by writing to the system flag bit in the command byte of the keyboard controller. It defaults to 0 after a power-on reset.
3	Command/Data	0: Data byte 1: Command byte
4	Inhibit Switch	0: Keyboard is inhibited 1: Keyboard is not inhibited
5	Auxiliary Device Output Buffer	0: Auxiliary device output buffer empty 1: Auxiliary device output buffer full
6	General Purpose Time-out	0: No time-out error 1: Time-out error
7	Parity Error	0: Odd parity 1: Even parity (error)

12.4 Commands

Table 12-2 KBC Command Sets

<table>
<tr><th>COMMAND</th><th>FUNCTION</th></tr>
<tr><td>20h</td><td>Read Command Byte of Keyboard Controller</td></tr>
<tr><td>60h</td><td>Write Command Byte of Keyboard Controller
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>7</td><td>Reserved</td></tr>
<tr><td>6</td><td>IBM Keyboard Translate Mode</td></tr>
<tr><td>5</td><td>Disable Auxiliary Device</td></tr>
<tr><td>4</td><td>Disable Keyboard</td></tr>
<tr><td>3</td><td>Reserve</td></tr>
<tr><td>2</td><td>System Flag</td></tr>
<tr><td>1</td><td>Enable Auxiliary Interrupt</td></tr>
<tr><td>0</td><td>Enable Keyboard Interrupt</td></tr>
</table></td></tr>
<tr><td>A4h</td><td>Test Password
Returns 0Fah if Password is loaded
Returns 0F1h if Password is not loaded</td></tr>
<tr><td>A5h</td><td>Load Password
Load Password until a logical 0 is received from the system</td></tr>
<tr><td>A6h</td><td>Enable Password
Enable the checking of keystrokes for a match with the password</td></tr>
<tr><td>A7h</td><td>Disable Auxiliary Device Interface</td></tr>
<tr><td>A8h</td><td>Enable Auxiliary Device Interface</td></tr>
<tr><td>A9h</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Auxiliary Device "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Auxiliary Device "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Auxiliary Device "Data" line is stuck low</td></tr>
</table></td></tr>
<tr><td>Aah</td><td>Self-test
Returns 055h if self-test succeeds</td></tr>
<tr><td>Abh</td><td>Interface Test
<table>
<tr><th>BIT</th><th>BIT DEFINITION</th></tr>
<tr><td>00</td><td>No Error Detected</td></tr>
<tr><td>01</td><td>Keyboard "Clock" line is stuck low</td></tr>
<tr><td>02</td><td>Keyboard "Clock" line is stuck high</td></tr>
<tr><td>03</td><td>Keyboard "Data" line is stuck low</td></tr>
<tr><td>04</td><td>Keyboard "Data" line is stuck high</td></tr>
</table></td></tr>
</table>

COMMAND	FUNCTION
Adh	Disable Keyboard Interface
Aeh	Enable Keyboard Interface
C0h	Read Input Port (P1) and send data to the system
C1h	Continuously puts the lower four bits of Port1 into the STATUS register
C2h	Continuously puts the upper four bits of Port1 into the STATUS register
D0h	Send Port 2 value to the system
D1h	Only set / reset GateA20 line based on system data bit 1
D2h	Send data back to the system as if it came from the Keyboard
D3h	Send data back to the system as if it came from Auxiliary Device
D4h	Output next received byte of data from system to Auxiliary Device
E0h	Reports the status of the test inputs
FXh	Pulse only RC (the reset line) low for 6μs if the Command byte is even

12.5 Hardware GATEA20/Keyboard Reset Control Logic

The KBC includes hardware control logic to speed-up GATEA20 and KBRESET. This control logic is controlled by LD5-CRF0 as follows:

12.5.1 KB Control Register (Logic Device 5, CR[F0])

BIT	7	6	5	4	3	2	1	0
NAME	KCLKS1	KCLKS0	RESERVED			P92EN	HGA20	HKBRST#
DEFAULT	1	0	0	0	0	0	0	0

BIT	DESCRIPTION	
7	**KCLKS1.**	Select the KBC clock rate. **Bits** **7 6** 0 0: Reserved 0 1: Reserved 1 0: KBC clock input is 12 MHz. 1 1: Reserved
6	**KCLKS0.**	
5-3	**RESERVED**	
2	**P92EN (Port 92 Enable).** 1: Enables Port 92 to control GATEA20 and KBRESET. 0: Disables Port 92 functions.	
1	**HGA20 (Hardware GATEA 20).** 1: Selects hardware GATE A20 control logic to control GATE A20 signal. 0: Disables GATEA20 control logic functions.	
0	**HKBRST# (Hardware Keyboard Reset).** 1: Selects hardware KB RESET control logic to control KBRESET signal. 0: Disables hardware KB RESET control logic function.	

When the KBC receives data that follows a “D1” command, the hardware control logic sets or clears GATEA20 according to received data bit 1. Similarly, the hardware control logic sets or clears KBRESET depending on received data bit 0. When the KBC receives an “FE” command, the KBRESET is pulse low for 6 μs (Min.) with a 14 μs (Min.) delay.

GATEA20 and KBRESET are controlled by either software or hardware logic, and they are mutually exclusive. Then, GATEA20 and KBRESET are merged with Port92 when the P92EN bit is set.

12.5.2 Port 92 Control Register (Default Value = 0x00)

BIT	7	6	5	4	3	2	1	0
NAME	RESERVED						SGA20	PLKBRST#
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-2	**RESERVED.**
1	**SGA20 (Special GATE A20 Control)** 1: Drives GATE A20 signal to high. 0: Drives GATE A20 signal to low.
0	**PLKBRST# (Pulled-low KBRESET).** A logical 1 on this bit causes KBRESET to drive low for 6 µS(Min.) with a 14 µS(Min.) delay. Before issuing another keyboard-reset command, the bit must be cleared.

13. CONSUMER INFRARED REMOTE (CIR)

Regarding the receiving of IR Block, the hardware uses the sampling rates of 1us, 25us, 50us and 100us to calculate the widths of H Level and L Level. The results are saved/stored in 32*8 RX FIFO. The max widths of H Level and L Level will be determined by Sample Limit Count Register. During the receiving, the hardware will reflect the FIFO status in RX FIFO Status Register. In addition, the hardware also generates status, such as Data Ready, Trigger Level Reach, FIFO Overrun and FIFO underrun, in RC Status Register.

13.1 CIR Register Table

Table 13-1 CIR Register Table

RC Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
base+0	IRCON	Reserved			RXEN	Reserved	RXINV	Sample Period Select	
base+1	IRSTS	RDR	RTR	PE	RFO	Reserved			GH
base+2	IREN	RDR	RTR	PE	RFO	Reserved			GH
base+3	RXFCONT	RXFIFO Count							
base+4	CP	Reserved							
base+5	CC	Reserved							
base+6	SLCH	Sample Limit Count High Byte							
base+7	SLCL	Sample Limit Count Low Byte							
base+8	FIFOCON	R				RXFIFOCLR	R	Rx Trigger Level	
base+9	IRFIFOSTS	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	Reserved		
base+A	SRXFIFO	Sample RX FIFO							
base+B	TXFCONT	Reserved							
base+C	STXFIFO	Reserved							
base+D	FCCH	Reserved							
base+E	FCCL	Reserved							
base+F	IRFSM	R	Decoder FSM			Reserved			

13.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Received			RXEN	Reserved	RXINV	Sample Period Select	
DEFAULT	0	0	0	0	0	1	0	0

BIT	DESCRIPTION
7-5	**Reserved**
4	**RX Enable**
3	**Reserved**
2	**IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1-0	**Sample Period Select** 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

13.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
Name	RDR	RTR	PE	RFO	Reserved			GH
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RX Data Ready** (Writing 1 will clear the bit).
6	**RX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
5	**Packet End** (Writing 1 will clear the bit).
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3-1	**Reserved**
0	**Min Length Detected** (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.

13.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	Reserved			GH
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	**RX Data Ready**
6	**RX FIFO Trigger Level Reach**
5	**Packet End**
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated).
3-1	**Reserved**
0	**Min Length Detected**

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

13.1.4 RX FIFO Count– Base Address + 3

Attribute: Read Only
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7-0	**RX FIFO Count**

13.1.5 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6

Attribute: Read/Write
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the high byte of the limited count in the IR RX mode.

13.1.6 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7

Attribute: Read/Write
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

13.1.7 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**Reserved**
3	**RX FIFO Cleared**.
2	**Reserved**

1-0	**RX Trigger Level** **Bits** **1 0** 0 0: 1 0 1: 8 1 0: 16 1 1: 24

13.1.8 IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	IR_Pending	RX_GS	RX_FTA	RX_Empty	RX_Full	Reserved		
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**IR Pending** 1: No Interrupt 0: Interrupt issue
6	**Minimum Length Detect Status**. This bit will be cleared when Packet End appears.
5	**RX FIFO Trigger Level Active**.
4	**RX FIFO Empty Flag**.
3	**RX FIFO Full Flag**.
2-0	**Reserved**

13.1.9 IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7	**Voltage Level** 0: Low, 1: High
6-0	**RX data length** (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

13.1.10 IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Decoder FSM			Reserved			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Reserved**
6	**Decoder over status**
5	**Decoder continuing status**
4	**Decoder wait H status** 1: idle, 0: RX busy
3-0	**Encoder Level Output Status**

13.1.11 IR Minimum Length Register – Base Address + F

Attribute: Write Only
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Min Length Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**Min Length Register**. Set up the shortest expected length of each carrier on the RX receiver (Unit: Sample Clock).

14. CONSUMER INFRARED REMOTE (CIR) WAKE-UP

One of the features of the NCT6796D is system boot-up by a remote controller. The hardware will store a specifically appointed key command from the IR remote controller in the FIFO of 67Byte.

The same key is required to re-boot the system after the computer shut-down. Such way can be applied to any remote controllers. Learning is necessary only at the first time.

14.1 CIR WAKE-UP Register Table

RC Block									
ExtAddr	**Name**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
base+0	IRCON	DEC_RST	Mode[1]	Mode[0]	RXEN	IgnoreEN	RXINV	Sample Period Select	
base+1	IRSTS	RDR	RTR	PE	RFO	GH	R	R	IR Pending
base+2	IREN	RDR	RTR	PE	RFO	GH	R		
Base+3		FIFO_COMPARE_DEEP							
base+4		FIFO_COMPARE_TOLERANCE							
base+5		FIFO_Count							
Base+6	SLCH	Sample Limit Count High Byte							
base+7	SLCL	Sample Limit Count Low Byte							
base+8	FIFOCON	R				RXFIFOCLR	R	Rx Trigger Level	
base+9	SRXFSTS	GS	FTA	Empty	Full	R			
base+A		Sample RX FIFO							
base+B		WR_FIFO_DATA							
Base+C		Read FIFO Only							
Base+D		Read FIFO Only Index							
Base+E		FIFO_Ignore							
Base+F	IRFSM	R	Decoder FSM			R			Wakeup Event

14.1.1 IR Configuration Register – Base Address + 0

Attribute: Read/Write
Size: 8 bits
Power Well: VRTC
Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	**DEC_RST**	**Mode[1]**	**Mode[0]**	**RXEN**	**Received**	**RXINV**	**Sample Period Select**	
DEFAULT	0	0	1	0	0	1	1	0

BIT	DESCRIPTION
7	**Reset CIR DECODER** (Write 1 to clear)
6	**Mode[1]** : 0: FIFO can't be written 1: FIFO can be written
5	**Mode[0]** 0: Learning Mode 1: Wake up Mode (Before enter in Power S3 state, this bit should be set) This bit reset by VCC.
4	**RX Enable**
3	**Ignore Bit Enable**
2	**IR Rx Invert Enable** 0: Dongle Carrier ON is high, OFF (Idle) is low. 1: Dongle Carrier ON is low, OFF (Idle) is high.
1-0	**Sample Period Select** 00:1us, 01: 25us, 10: 50us, 11: 100us Note: In the 1us mode, the pulse mode will not function due to the IR regulations.

14.1.2 IR Status Register – Base Address + 1

Attribute: Read/Write
Size: 8 bits
Power Well: VSB
Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Received		IR_Pending
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**RX Data Ready** (Writing 1 will clear the bit).
6	**RX FIFO Trigger Level Reach** (Writing 1 will clear the bit).
5	**Packet End** (Writing 1 will clear the bit).
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated. Writing 1 will clear the bit).
3	**Min Length Detected** (Writing 1 will clear the bit) 1: The IR Data length received is shorter than the default value. 0: The IR Data length received is longer than the default value.
2-1	**Reserved**
0	**IR Pending** 1: No Interrupt 0: Interrupt issue

14.1.3 IR Interrupt Configuration Register – Base Address + 2

Attribute: Read/Write
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	RDR	RTR	PE	RFO	GH	Reserved		
DEFAULT	0	0	0	0	0	0	0	0

1: Enable interrupt; 0: Disable interrupt

BIT	DESCRIPTION
7	**RX Data Ready**
6	**RX FIFO Trigger Level Reach**
5	**Packet End**
4	**RX FIFO Overrun** (Overrun and Data Ready will be simultaneously generated).
3	**Min Length Detected**
2-0	**Reserved**

Note. When an Interrupt occurs, it only can be cleared by writing IR Status Register to 1.

14.1.4 IR TX Configuration Register – Base Address + 3

Attribute: Read/Write
Size: 8 bits
Power Well: VRTC
Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Deep							
DEFAULT	0	1	0	0	0	0	1	1

1: Enable; 0: Disable

BIT	DESCRIPTION
7-0	When in S3 state, how many bytes need to compare. Default is 67 bytes.

14.1.5 IR FIFO Compare Tolerance Configuration Register – Base Address + 4

Attribute: Read/Write
Size: 8 bits
Power Wel: VRTC
Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Compare Tolerance							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	**FIFO Data Tolerance between Learning mode and Wakeup mode**. (Every byte) FIFO Date Tolerance = (Learning mode data) – (Wakeup mode data)

14.1.6 RX FIFO Count– Base Address + 5

Attribute: Read
Size: 8 bits
Power Wel: VRTC
Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Count							
DEFAULT	0	0	0	0	0	0	0	0

1: Enable; 0: Disable

BIT	DESCRIPTION
7-0	RX FIFO Count

14.1.7 IR RX Sample Limited Count High Byte Register (RCLCH) – Base Address + 6

Attribute: Read/Write
Size: 8 bits
Power Wel: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count High Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the high byte of the limited count in the IR RX mode.

14.1.8 IR RX Sample Limited Count Low Byte Register (RCLCL) – Base Address + 7

Attribute: Read/Write
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Sample Limited Count low Byte							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	This byte is defined as the low byte of the limited count in the IR RX mode.

Note. (RCLCH, RCLCL) is defined as 16 bits value of the limited count in the IR RX mode. When the RX date length reaches the limited count, Packet End status will appear.

14.1.9 IR FIFO Configuration Register (FIFOCON) – Base Address + 8

Attribute: Read/Write
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Reserved				RXFIFOCLR	Reserved	RX Trigger Level	
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-4	**Reserved**
3	**RX FIFO Cleared.**
2	**Reserved**
1-0	**RX Trigger Level** **Bits** **1 0** 0 0: 67 0 1: 66 1 0: 65 1 1: 64

14.1.10 IR Sample RX FIFO Status Register – Base Address + 9

Attribute: Read Only
Size: 8 bits
Power Well: VSB
Reset by:RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	GS	FTA	Empty	Full	Reserved			
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	**Minimum Length Detect Status**. This bit will be cleared when Packet End appears.
6	**RX FIFO Trigger Level Active.**
5	**RX FIFO Empty Flag**.
4	**RX FIFO Full Flag**.
3-0	**Reserved**

14.1.11 IR Sample RX FIFO Register – Base Address + A

Attribute: Read Only
Size: 8 bits
Power Well: VRTC
Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7	**Voltage Level** 0: Low, 1: High
6-0	**RX data length** (Unit : Sample Period) Note: 1. 0x80 is Packet End. The hardware enters the Idle state after checking Rx Channel. 2. When 0x00 represents the glitch packet, it means pulses shorter than 3/4 sample period are received. 3. Pulses that are shorter than 1/4 sample periods will be ignored automatically.

14.1.12 Write FIFO – Base Address + B

Attribute: Write Only
Size: 8 bits
Power Well: VRTC
Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Write Sample RX FIFO						

BIT	DESCRIPTION
7	**Voltage Level** 0: Low, 1: High

BIT	DESCRIPTION
6-0	**RX data length** (Unit : Sample Period)

Note. Before writing FIFO Data, mode[1] register should be set.

14.1.13 Read FIFO Only – Base Address + C

Attribute: Read Only
Size: 8 bits
Power Well: VRTC
Reset by: Battery reset

BIT	7	6	5	4	3	2	1	0
NAME	Voltage Level	Sample RX FIFO						

BIT	DESCRIPTION
7	**Voltage Level** 0: Low, 1: High
6-0	RX data length (Unit : Sample Period)

Note. Only Read FIFO Data.

14.1.14 Read FIFO Index – Base Address + D

Attribute: Read Only
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	FIFO Index							

BIT	DESCRIPTION
7-0	Indicate that FIFO Index when only read FIFO data(Base Address + C)

Note. Only Read FIFO Data.

14.1.15 Reserved – Base Address + E

14.1.16 IR FSM Status Register (IRFSM) – Base Address + F

Attribute: Read Only
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0

NAME	Reserved	Decoder FSM			Reserved			Wake up event
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7	Reserved
6-4	CIR State Machine
3-1	Reserved
0	**Wake up event:** 0: CIR wake up event has not been triggered. 1: CIR wake up event has been triggered. (Wake up event Read clear.)

14.1.17 IR Minimum Length Register – Base Address + F

Attribute: Write Only
Size: 8 bits
Power Well: VSB
Reset by: RSMRST#

BIT	7	6	5	4	3	2	1	0
NAME	Min Length Register							
DEFAULT	0	0	0	0	0	0	0	0

BIT	DESCRIPTION
7-0	Min Length Register. Set up the shortest expected length of each carrier on the RX receiver (Unit: Sample Clock).

15. POWER MANAGEMENT EVENT

The PME# signal is connected to the South Bridge and is used to wake up the system from S1 ~ S5 sleeping states.

One control bit and four registers in the NCT6796D are associated with the PME function. The control bit is at Logical Device A, CR[F2h], bit[0] and is for enabling or disabling the PME function. If this bit is set to "0", the NCT6796D won't output any PME signal when any of the wake-up events has occurred and is enabled. The four registers are divided into PME status registers and PME interrupt registers of wake-up events Note.1.

2) The PME status registers of wake-up event:
   - At Logical Device A, CR[F3h] and CR[F4h]
   - Each wake-up event has its own status
   - The PME status should be cleared by writing a "1" before enabling its corresponding bit in the PME interrupt registers
3) The PME interrupt registers of wake-up event:
   - At Logical Device A, CR[F6h] and CR[F7h]
   - Each wake-up event can be enabled / disabled individually to generate a PME# signal

Note.1 PME wake-up events that the NCT6796D supports include:

- Mouse event*
- Keyboard event*
- GP41, GP46, GP31, GP32 events *
- CIR*
- Printer IRQ event
- UART A IRQ event
- UART B IRQ event
- IR IRQ event
- Hardware Monitor IRQ event
- WDT1 event
- RIA (UARTA Ring Indicator) event
- RIB (UARTB Ring Indicator) event

Note.2 All the above support both S0 and S1 states. Events with the "*" mark also support S3 ~ S5 states.

15.1 Power Control Logic

This chapter describes how the NCT6796D implements its ACPI function via these power control pins: PSIN#, PSOUT#, SLP_S3# and PSON#. The following figure illustrates the relationships.

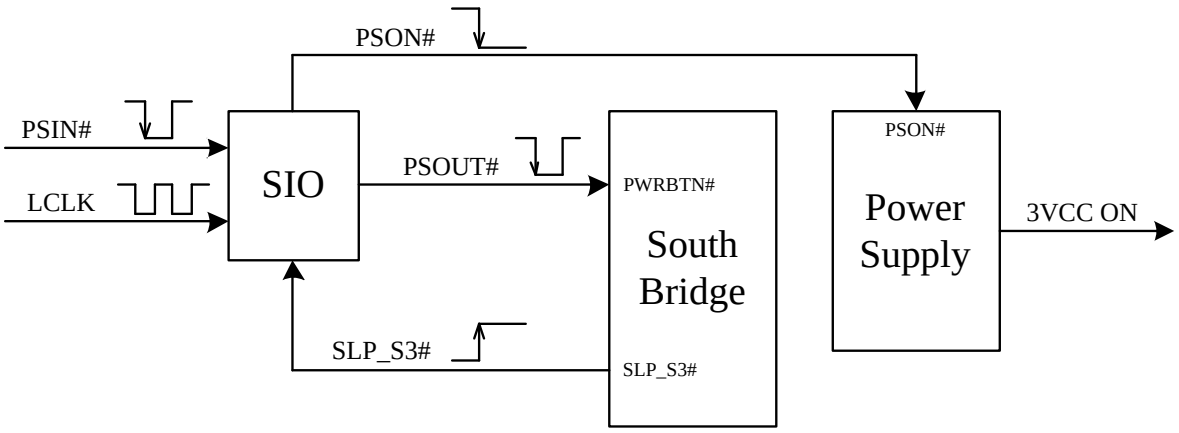


Figure 15-1 Power Control Mechanism

15.1.1 PSON# Logic

15.1.1.1. Normal Operation

The PSOUT# signal will be asserted low if the PSIN# signal is asserted low. The PSOUT# signal is held low for as long as the PSIN# is held low. The South Bridge controls the SLP_S3# signal through the PSOUT# signal. The PSON# is directly connected to the power supply to turn on or off the power.

Figure 15-2 shows the power on and off sequences.

The ACPI state changes from S5 to S0, then to S5

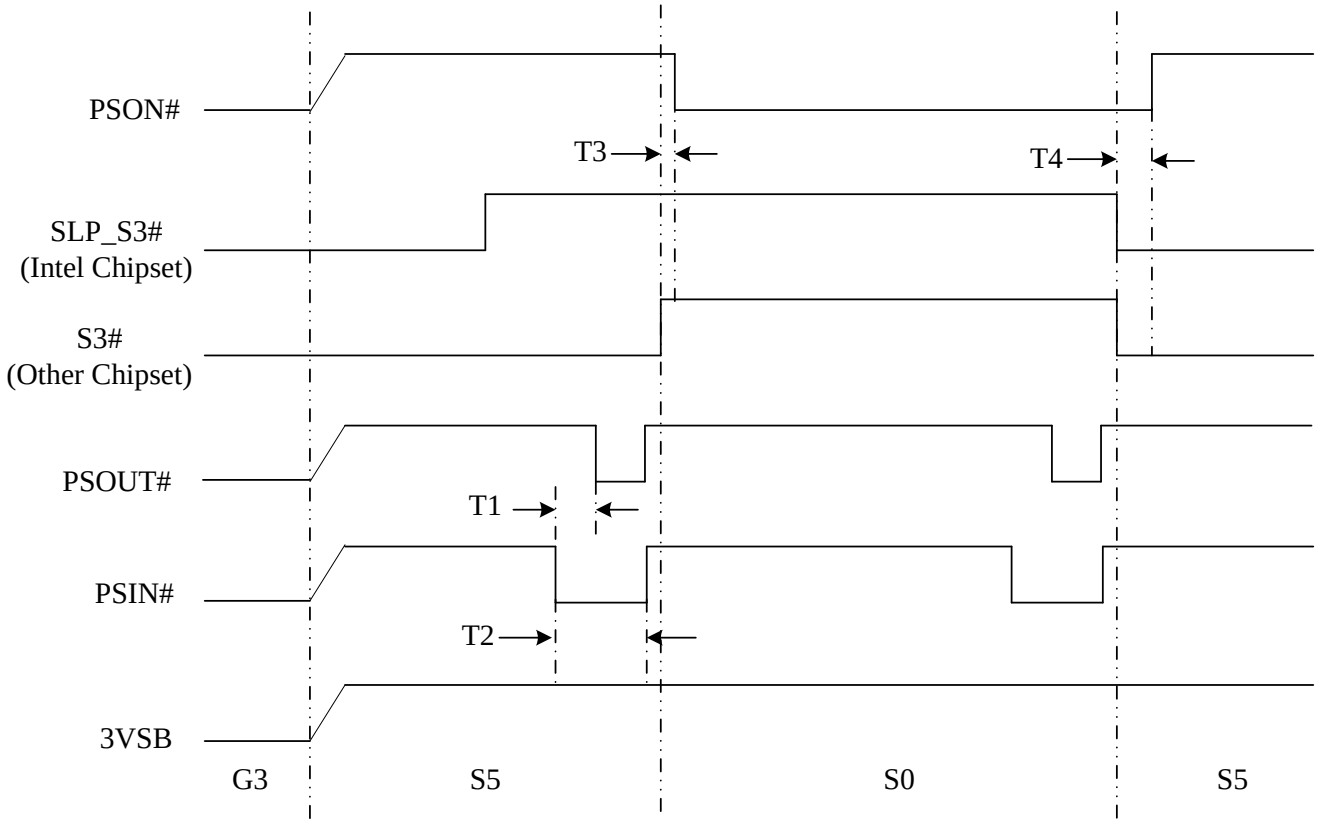


Figure 15-2 Power Sequence from S5 to S0, then Back to S5

15.1.2 AC Power Failure Resume

By definition, AC power failure means that the standby power is removed. The power failure resume control logic of the NCT6796D is used to recover the system to a pre-defined state after AC power failure. Two control bits at Logical Device A, CR[E4h], bits[6:5] indicate the pre-defined state. The definition of these two bits is listed in the following table:

Table 15-1 Bit Map of Logical Device A, CR[E4h], Bits[6:5]

LOGICAL DEVICE A, CR[E4H], BITS[6 :5]	DEFINITION
00	System always turns off when it returns from AC power failure
01	System always turns on when it returns from AC power failure
10	System turns off / on when it returns from power failure depending on the state before the power failure. (Please see Note 1)
11	User defines the state before the power failure. (The previous state is set at CRE6[4]. Please see Note 2)

Note1. The NCT6796D detects the state before power failure (on or off) through the SLP_S3# signal and the 3VCC power. The relation is illustrated in the following two figures.

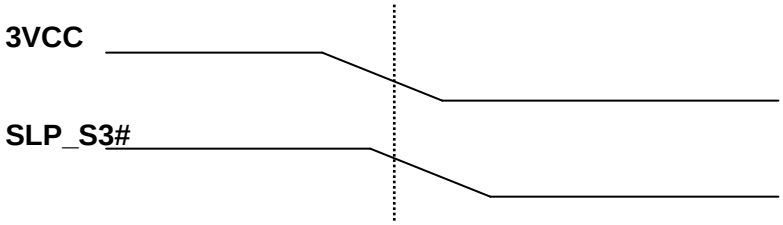


Figure 15-3 The previous state is “on”

3VCC falls to 2.6V and SLP_S3# keeps at 2.0V.

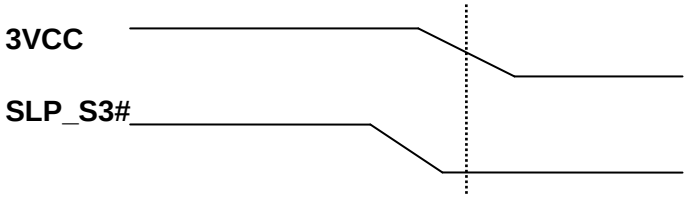


Figure 15-4 The previous state is “off”.

3VCC falls to 2.6V and SLP_S3# keeps at 0.8V.

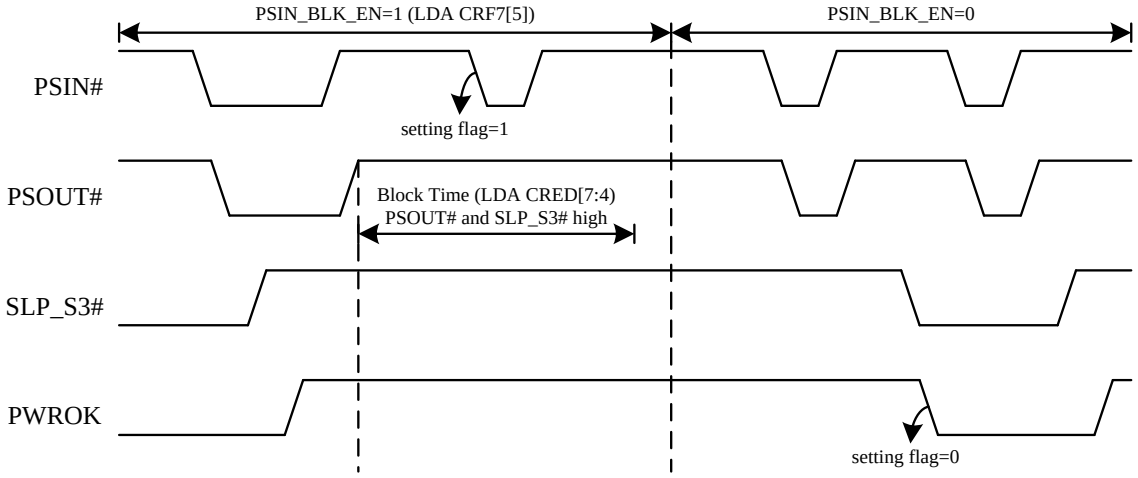
Note 2.

Logical Device A, CR[E6h] bit [4]	Definition
0	User defines the state to be “on”
1	User defines the state to be “off”

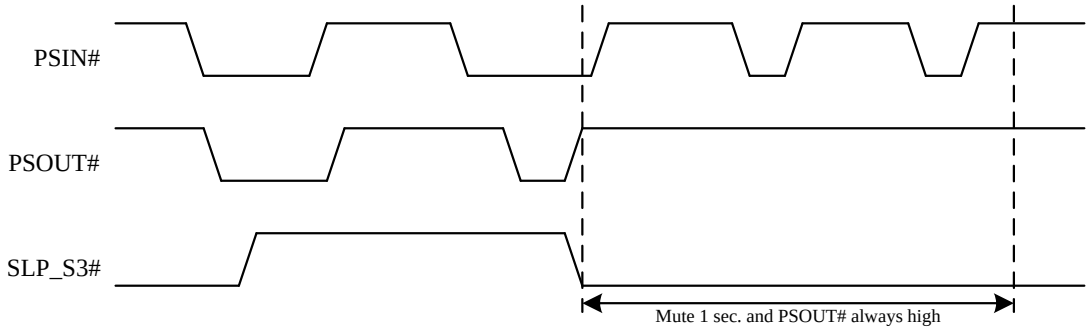
To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT6796D adds the option of “user define mode” for the pre-defined state before AC power failure. BIOS can set the pre-defined state to be “On” or “Off”. According to this setting, the system is returned to the pre-defined state after the AC power recovery.

15.1.3 PSOUT Blocking Time

When PSOUT# and SLP_S3# signal is given, the time set by the user to block, the PSIN# signal will be not reaction PSOUT#, but can be recorded. When the system was S0 back to S5 and SLP_S3# Low, PSIN# signal will be isolated in one second, then PSOUT for high.



When the system was S0 back to S5 and SLP_S3 Low, PSIN# signal will be isolated in one second, the PSOUT# for high.



15.2 Wake Up the System by Keyboard and Mouse

The NCT6796D generates a low pulse through the PSOUT# pin to wake up the system when it detects a key code pressed or mouse button clicked. The following sections describe how the NCT6796D works.

15.2.1 Waken up by Keyboard events

The keyboard Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 6 to “1”.

There are two keyboard events can be used for the wake-up

1) Any key – Set bit 0 at Logical Device A, CR[E0h] to “1” (Default).
2) Specific keys (Password) – Set bit 0 at Logical Device A, CR[E0h] to “0”.

Three sets of specific key combinations are stored at Logical Device A. CR[E1h] is an index register to indicate which byte of key code storage (0x00h ~ 0x0Eh, 0x30h ~ 0x3Eh, 0x40h ~ 0x4Eh) is going to be read or written through CR[E2h]. According to IBM 101/102 keyboard specification, a complete key code contains a 1-byte make

code and a 2-byte break code. For example, the make code of “0” is 0x45h, and the corresponding break code is 0xF0h, 0x45h.

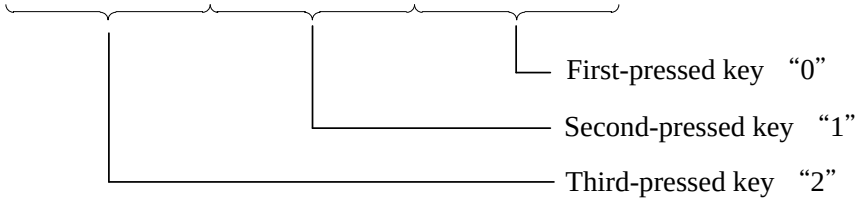
First sets of specific key can be set to serial or simultaneous password mode, second and third sets of specific keys only serial password mode. In simultaneous password mode, assume that we want to set “L Ctrl + L Alt + A” or “R Ctrl + R Alt + A” as the password (the password of simultaneous mode must be avoid ghost keys). The storage only fill the make code, except for the prefixed scan code of the password. The detail setting shows as below. Serial password mode descript as under section.

Index (CRE1)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Data (CRE2)	14	11	1C	00	00	00	00	00	00	00	00	00	00	00	00

- L Ctrl / R Ctrl : 0x14h, 0xF0h, 0x14h / 0xE0h, 0x14h, 0xE0h, 0xF0h, 0x14h
- L Alt / R Alt : 0x11h, 0xF0h, 0x11h / 0xE0h, 0x11h, 0xE0h, 0xF0h, 0x11h
- A : 0x1Ch, 0xF0h, 0x1Ch

The approach to implement Keyboard Password Wake-Up Function is to fill key codes into the password storage. Assume that we want to set “012” as the password. The storage should be filled as below. Please note that index 0x09h ~ 0x0Eh must be filled as 0x00h since the password has only three numbers.

Index (CRE1)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Data (CRE2)	1E	F0	1E	16	F0	16	45	F0	45	00	00	00	00	00	00



15.2.2 Waken up by Mouse events

The mouse Wake-Up function is enabled by setting Logical Device A, CR[E0h], bit 5 to “1”.

The following specific mouse events can be used for the wake-up:

- Any button clicked or any movement
- One click of the left or the right button
- One click of the left button
- One click of the right button
- Two clicks of the left button
- Two clicks of the right button.

Three control bits (ENMDAT_UP, MSRKEY, MSXKEY) define the combinations of the mouse wake-up events. Please see the following table for the details.

Table 15-2 Definitions of Mouse Wake-Up Events

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT

ENMDAT_UP (LOGICAL DEVICE A, CR[E6H], BIT 7)	MSRKEY (LOGICAL DEVICE A, CR[E0H], BIT 4)	MSXKEY (LOGICAL DEVICE A, CR[E0H], BIT 1)	WAKE-UP EVENT
1	x	1	Any button clicked or any movement.
1	x	0	One click of the left or right button.
0	0	1	One click of the left button.
0	1	1	One click of the right button.
0	0	0	Two clicks of the left button.
0	1	0	Two clicks of the right button.

15.3 Resume Reset Logic

The RSMRST# signal is a reset output and is used as the VSB power on reset signal for the South Bridge.

When the NCT6796D detects the 3VSB voltage rises to “V1”, it then starts a delay – “t1” before the rising edge of RSMRST# asserting. If the 3VSB voltage falls below “V2”, the RSMRST# de-asserts immediately.

Timing and voltage parameters are shown in Figure 15-5 and Table 15-3.

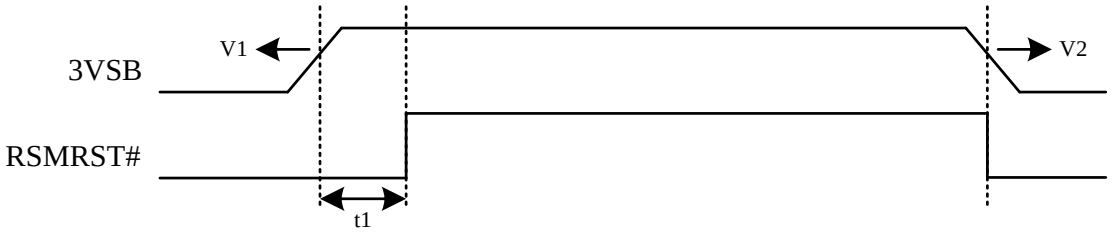


Figure 15-5 Mechanism of Resume Reset Logic

Table 15-3 Timing and Voltage Parameters of RSMRST#

NAME	PARAMETER	MIN.	MAX.	UNIT
V1	3VSB Valid Voltage	2.94	3.00	V
V2	3VSB Ineffective Voltage	2.90	2.96	V
t1	Valid 3VSB to RSMRST# inactive	200	300	mS

16. SERIALIZED IRQ

The NCT6796D supports a serialized IRQ scheme. This allows a signal line to be used to report the parallel interrupt requests. Since more than one device may need to share the signal serial SERIRQ signal, an open drain signal scheme is employed. The clock source is the PCI clock. The serialized interrupt is transferred on the SERIRQ signal, one cycle consisting of three frames types: the Start Frame, the IRQ/Data Frame, and the Stop Frame.

16.1 Start Frame

There are two modes of operation for the SERIRQ Start Frame: Quiet mode and Continuous mode.

In the Quiet mode, the NCT6796D drives the SERIRQ signal active low for one clock, and then tri-states it. This brings all the state machines of the NCT6796D from idle to active states. The host controller (the South Bridge) then takes over driving SERIRQ signal low in the next clock and continues driving the SERIRQ low for programmable 3 to 7 clock periods. This makes the total number of clocks low 4 to 8 clock periods. After these clocks, the host controller drives the SERIRQ high for one clock and then tri-states it.

In the Continuous mode, the START Frame can only be initiated by the host controller to update the information of the IRQ/Data Frame. The host controller drives the SERIRQ signal low for 4 to 8 clock periods. Upon a reset, the SERIRQ signal is defaulted to the Continuous mode for the host controller to initiate the first Start Frame.

Please see the diagram below for more details.

Start Frame Timing with source sampled a low pulse on IRQ1.

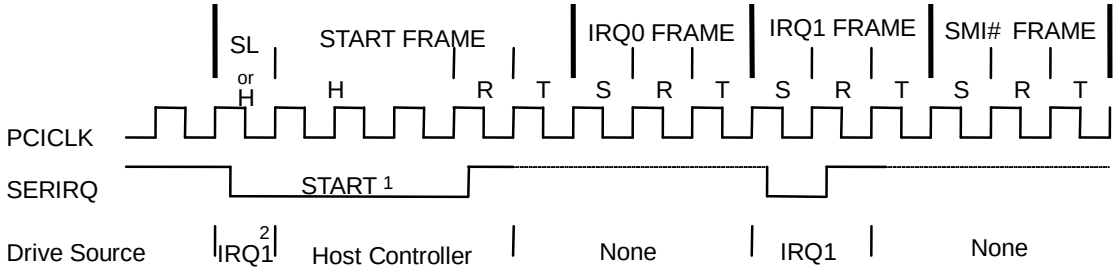


Figure 16-1 Start Frame Timing with Source Sampled A Low Pulse on IRQ1

H=Host Control SL=Slave Control R=Recovery T=Turn-around S=Sample

Note:

1. The Start Frame pulse can be 4-8 clocks wide.
2. The first clock of Start Frame is driven low by the NCT6796D because IRQ1 of the NCT6796D needs an interrupt request. Then the host takes over and continues to pull the SERIRQ low.

16.2 IRQ/Data Frame

Once the Start Frame has been initiated, the NCT6796D must start counting frames based on the rising edge of the start pulse. Each IRQ/Data Frame has three clocks: the Sample phase, the Recovery phase, and the Turn-around phase.

During the Sample phase, the NCT6796D drives SERIRQ low if the corresponding IRQ is active. If the corresponding IRQ is inactive, then SERIRQ must be left tri-stated. During the Recovery phase, the NCT6796D device drives the SERIRQ high. During the Turn-around phase, the NCT6796D device leaves the SERIRQ tri-stated. The NCT6796D starts to drive the SERIRQ line from the beginning of “IRQ0 FRAME” based on the rising edge of PCICLK.

The IRQ/Data Frame has a specific numeral order, as shown in Table 16-1.

Table 16-1 SERIRQ Sampling Periods

SERIRQ SAMPLING PERIODS			
IRQ/DATA FRAME	**SIGNAL SAMPLED**	**# OF CLOCKS PAST START**	**EMPLOYED BY**
1	IRQ0	2	Reserved
2	IRQ1	5	Keyboard
3	SMI#	8	H/W Monitor & SMI
4	IRQ3	11	IR
5	IRQ4	14	UART A
6	IRQ5	17	-
7	IRQ6	20	FDC
8	IRQ7	23	LPT
9	IRQ8	26	-
10	IRQ9	29	-
11	IRQ10	32	-
12	IRQ11	35	-
13	IRQ12	38	Mouse
14	IRQ13	41	Reserved
15	IRQ14	44	-
16	IRQ15	47	-
17	IOCHCK#	50	-
18	INTA#	53	-
19	INTB#	56	-
20	INTC#	59	-
21	INTD#	62	-
32:22	Unassigned	95	-

16.3 Stop Frame

After all IRQ/Data Frames have completed, the host controller will terminates SERIRQ with a Stop frame. Only the host controller can initiate the Stop Frame by driving SERIRQ low for 2 or 3 clocks. If the Stop Frame is low for 2 clocks, the Sample mode of next SERIRQ cycle's Sample mode is the Quiet mode. If the Stop Frame is low for 3 clocks, the Sample mode of next SERIRQ cycle is the Continuous mode.

Please see the diagram below for more details.

Stop Frame Timing with Host Using 17 SERIRQ sampling period.

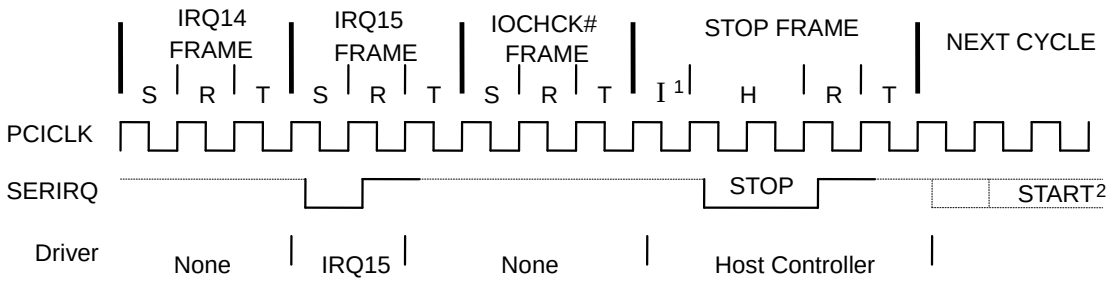


Figure 16-2 Stop Frame Timing with Host Using 17 SERIRQ Sampling Period

H=Host Control R=Recovery T=Turn-around S=Sample I= Idle.

Note:

1. There may be none, one or more Idle states during the Stop Frame.
2. The Start Frame pulse of next SERIRQ cycle may or may not start immediately after the turn-around clock of the Stop Frame.

17. WATCHDOG TIMER

The Watchdog Timer 1 of the NCT6796D consists of an 8-bit programmable time-out counter and a control and status register. GPIO0, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7 provides an alternative WDT1 function. This function can be configured by the relative GPIO control register. The units of Watchdog Timer counter can be selected at Logical Device 8, CR[F5h], bit[3]. The time-out value is set at Logical Device 8, CR[F6h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

When Watchdog Timer 1 time-out event is occurring, GPIO0, GPIO2, GPIO4, GPIO6, bit[0],[4], GPIO3, bit[3], GPIO7, bit[0], PWROK and RESETCONO# will trigger a low pulse apporx 100mS or low level by Logical Device 8 CR[F5h], bit[0] and RSMRST# will trigger a low pulse electi 250ms. The PWROK, SLP_S3# and RSMRST# event also relate to acpi sequence, that can be control by Logical Device D, CR[F0h], bit[7] and bit[0], Logical Device D, CR[F0h], bit[7] and bit[0] as 2'b00 is normal acpi function, others timing illustrations are define in Figure 17-1 to Figure 17-3 In other words, when the value is counted down to zero, the timer stops, and the NCT6796D sets the WDT1 status bit in Logical Device 8, CR[F7h], bit[4]. Writing a zero will clear the status bit. It. This bit will also be cleared if LRESET# or PWROK signal is asserted.

The Watchdog Timer 3 of the NCT6796D consists of an 8-bit programmable time-out counter and a control and status register. The units of Watchdog Timer counter can be selected at Logical Device 8, CR[F8h], bit[3]. The time-out value is set at Logical Device 8, CR[F9h]. Writing zero disables the Watchdog Timer function. Writing any non-zero value to this register causes the counter to load this value into the Watchdog Timer counter and start counting down.

When Watchdog Timer 3 time-out event is occurring, PWROK and RESETCONO# will trigger a low pluse apporx 100mS or low level by Logical Device 8 CR[F8h], bit[0]. In other words, when the value is counted down to zero, the timer stops, and the NCT6796D sets the WDT3 status bit in Logical Device 8, CR[Fah], bit[4]. Writing a zero will clear the status bit. It. This bit will also be cleared if LRESET# or PWROK signal is asserted.

The Watchdog Timer 4 of the NCT6796D consists of an status register (Logic Device D, CR[E7h] bit[6]). The timeout event will trigger RESETCONO pin to gerenate a pulse when RSTWDT_EN set to oen. CR[2Dh], bit[0] is RSTWDT_EN enable bit. When RSTWDT_EN set to one, if VCC3V is good, the timer will start count down, after 5 second, the timer time-out and to issue about 100ms low pulse to trigger pin.

Watchdog Timer Time-Out Trigger Event	Watchdog Timer 1	Watchdog Timer 3	Watchdog Timer 4
			WDTRST_EN strapping, 5sec to issue RESETCON# if VCC3V is High
KBRST#	✓	×	×
PWROK	×	✓	×
GPIO Pin	✓	×	×
RESETCONO# Pin	✓	✓	✓
RSMRST# Event	✓	×	×
PWROK Event Then Into Deep S5	✓	×	×
Internal SLP_S3# Event Then Into Deep S5	✓	×	×

Table 17-1 Watchdog Timer 1/3/4 Time-Out Trigger event

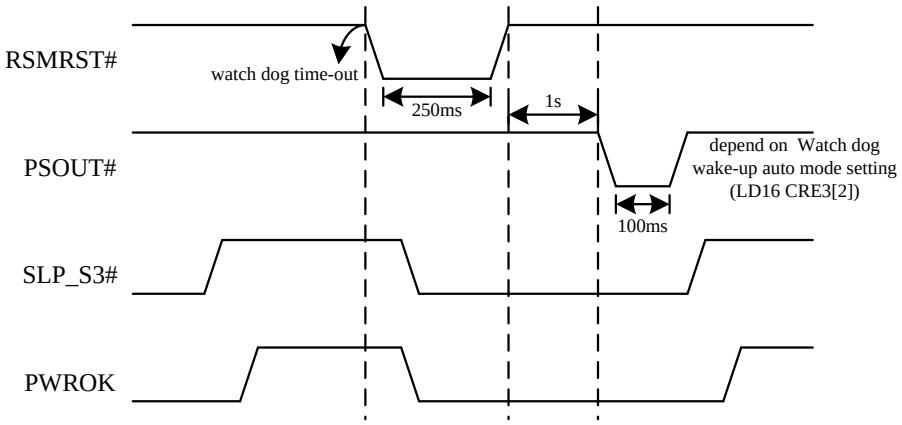


Figure 17-1 RSMRST# Event When Logical Device D CRF0 Bit[7] and Bit[0] as 2'b01

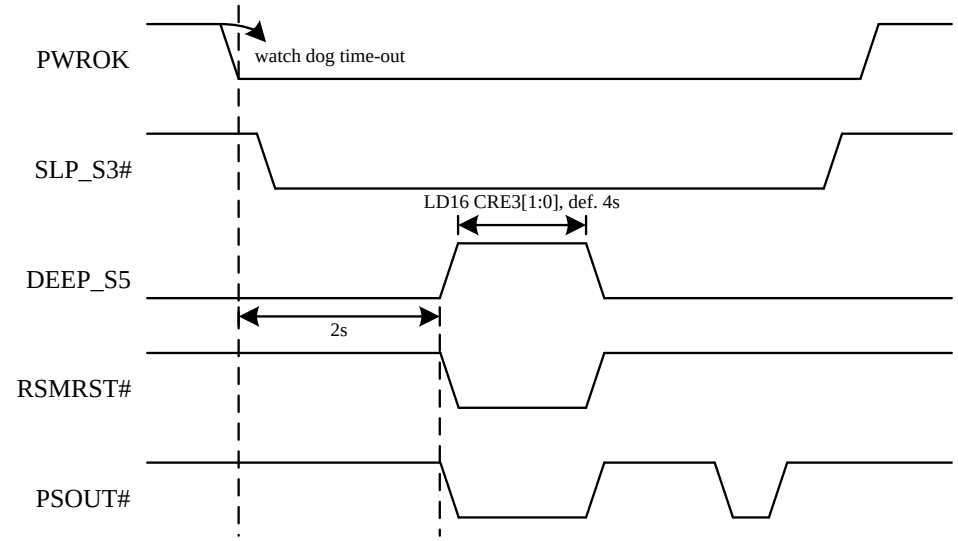


Figure 17-2 PWROK Event When Logical Device D CRF0 Bit[7] and Bit[0] as 2'b10

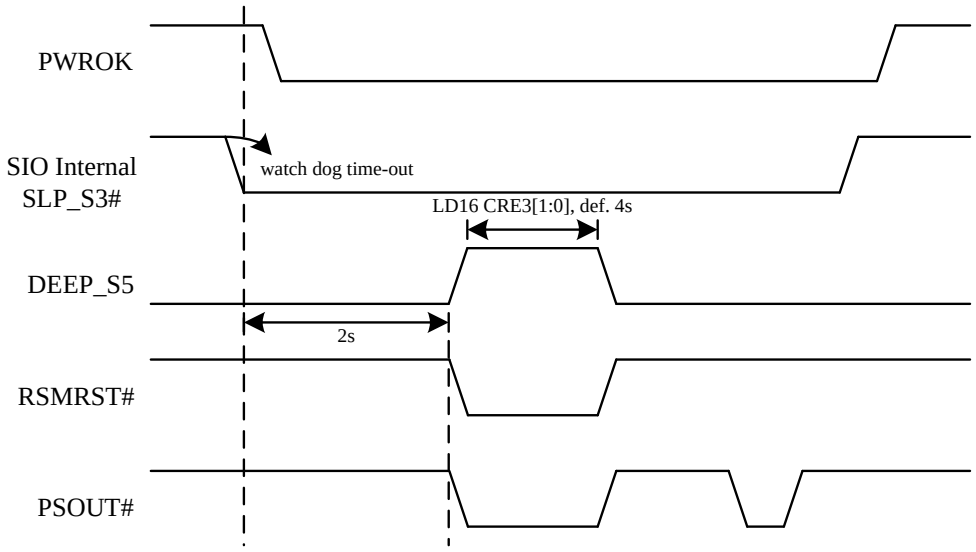


Figure 17-3 SLP_S3# Event When Logical Device D CRF0 Bit[7] and Bit[0] as 2'b11

18. GENERAL PURPOSE I/O

18.1 GPIO ARCHITECTURE

The NCT6796D provides 71 input/output ports that can be individually configured to perform a simple basic I/O function or alternative, pre-defined function. Users can configure each individual port to be an input or output port by programming respective bit in selection register (0 = output, 1 = input). Invert port value by setting inversion register (0 = non–inverse, 1 = inverse). Port value is read/write through data register.

In addition, only **GP41, GP46, GP31 and GP32** are designed to be able to assert **PSOUT# or PME#** signal to wake up the system if any of them has falling transitions. The following table gives more detailed register map on GP41, GP46, GP31 and GP32.

Table 18-1 Relative Control Registers of GP41, 46, 31 and 32 that Support Wake-Up Function

	EVENTROUTE I (PSOUT#) **0 : DISABLE** **1 : ENABLE**	**EVENTROUTE II (PME#)** **0 : DISABLE** **1 : ENABLE**
GP41	LDA, CR[Feh] bit[7]	LDA, CR[Feh] bit[3]
GP46	LDA, CR[Feh] bit[6]	LDA, CR[Feh] bit[2]
GP31	LDA, CR[Feh] bit[5]	LDA, CR[Feh] bit[1]
GP32	LDA, CR[Feh] bit[4]	LDA, CR[Feh] bit[0]

Table 18-2 GPIO Group Programming Table

18.2 ACCESS CHANNELS

There are two different channels to set up/access the GPIO ports. The first one is the indirect access via register 2E/2F (4E/4F, it depends by HEFRAS trapping). The registers can be read / written only when the respective logical device ID and port number are selected.

The other is the direct access through GPIO register table that can be configured by {CR61, CR60} of logic device 8. The mapped 7 registers are defined in table 18-3. Base address plus 0 to 4 are GPIO registers, base address plus 5 to 7 are watchdog registers.Since the base address is set, the GPIO number can be selected by writing the group number to GSR [INDEX] (GPIO Select Register, #0~#8 for GPIO0 ~ GPIO8 respectively). Then the I/O register, the Data register and the Inversion register are mapped to addresses Base+0, Base+1 and Base+2 respectively. Only one GPIO can be accessed at one time.

Table 18-3 GPIO Register Addresses

ADDRESS	ABBR	BIT NUMBER							
		7	6	5	4	3	2	1	0
Base + 0	GSR	Reserved				INDEX			
Base + 1	IOR	GPIO I/O Register							
Base + 2	DAT	GPIO Data Register							
Base + 3	INV	GPIO Inversion Register							
Base + 4	DST	GPIO Status Register							
Base + 5	Wdtmod	Watchdog Timer 1 (WDT1) and KBC P20 Control Mode Register							
Base + 6	Wdttim	Watchdog Timer 1 (WDT1) Control Register							
Base + 7	Wdtsts	Watchdog Timer 1 (WDT1) Status Register							

19. SMBUS MASTER INTERFACE

19.1 General Description

The SMBus interface module is two wire serial interface compatible to the SMBus physical layer. It is also compatible with Intel's SMBus and Philips' I^2C bus.

The rest of this section introduces the various features of the SMBus master capability. These features are divided into the following sections:

- SMBus and I^2C compliant
- AMD-TSI
- PCH
- SMBus master

19.2 Introduction to the SMBus Master

19.2.1 Data Transfer Format

Every byte transferred on the bus consists of 8 bits. After the start condition, the master places the 7-bit address to the slave device it wants to address on the bus. The address followed an eight bit indicating the direction of the data transfer (R/W#); a zero indicates a transmission for data while a one indicates a request for data. Each byte is transferred with the most significant bit first, and after each byte, an acknowledge signal must follow. A data transfer is always terminated by stop condition generated by master.

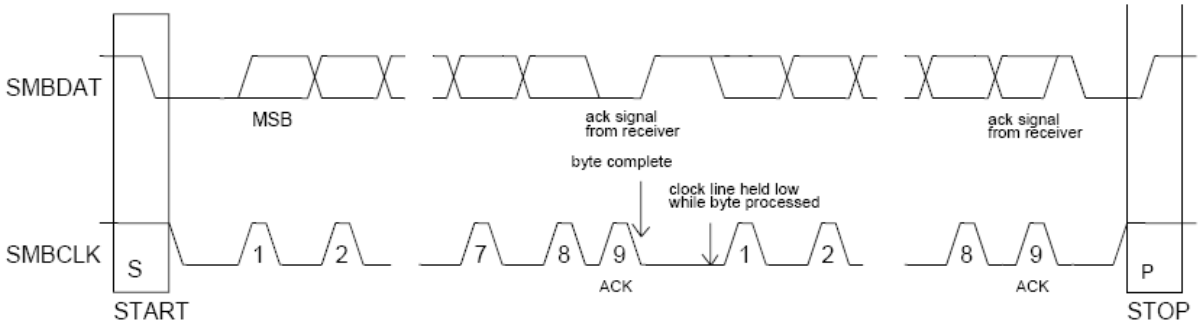


Figure 19-1 Data Transfer Format

19.2.2 Arbitration

Arbitration takes place on the SMBDAT data line while the SMBCLK line is high. Two devices may generate a start condition at the same time and enter the arbitration procedure. Arbitration continues until one master generates a HIGH level on the SMBDAT line while another competing master generates a LOW level on the SMBDAT line while SMBCLK is high. The master device which generated the HIGH level on SMBDAT loses arbitration. If a device loses arbitration during the first byte following a start condition i.e. while transmitting a slave address it becomes a slave receiver and monitors the address for a potential match. Arbitration may also be lost in the master receive mode during the acknowledge cycle.

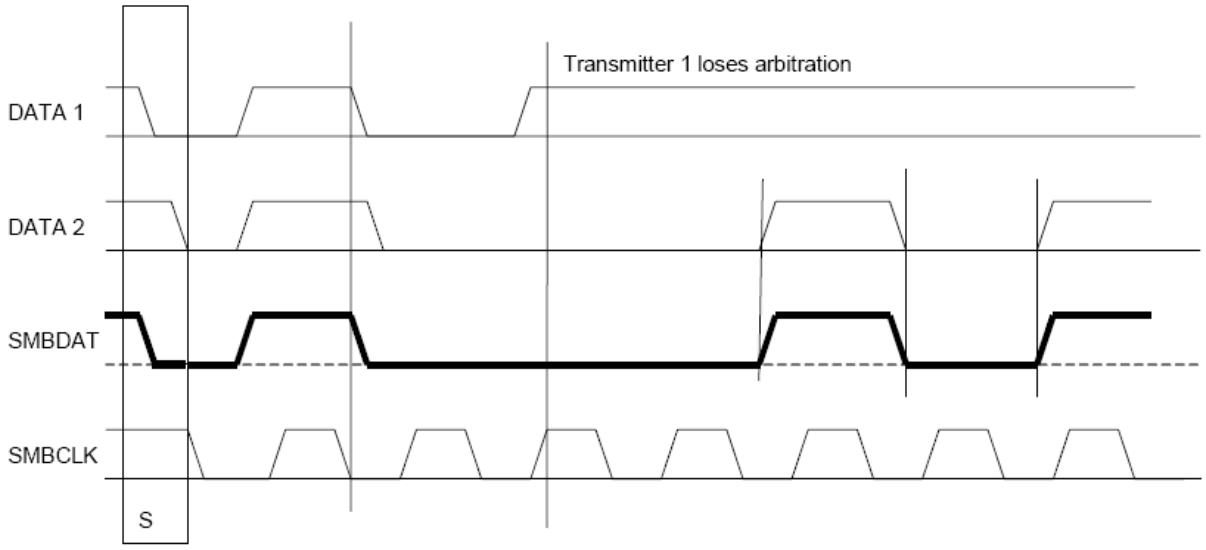


Figure 19-2 SMBus Arbitration

19.2.3 Clock Synchronization

Clock synchronization is performed while the arbitration procedure described above is in effect. Clock Synchronization takes place between two competing devices by utilizing the wired-AND nature of the SMBCLK line. The SMBCLK line will go low as soon as the master with the shortest high time pulls SMBCLK low. SMBCLK will remain low until the device with the longest SMBCLK low time relinquishes the SMBCLK line. Therefore the SMBCLK high time is determined by device with the shortest high time while the SMBCLK low time is determined by the device with the longest low time.

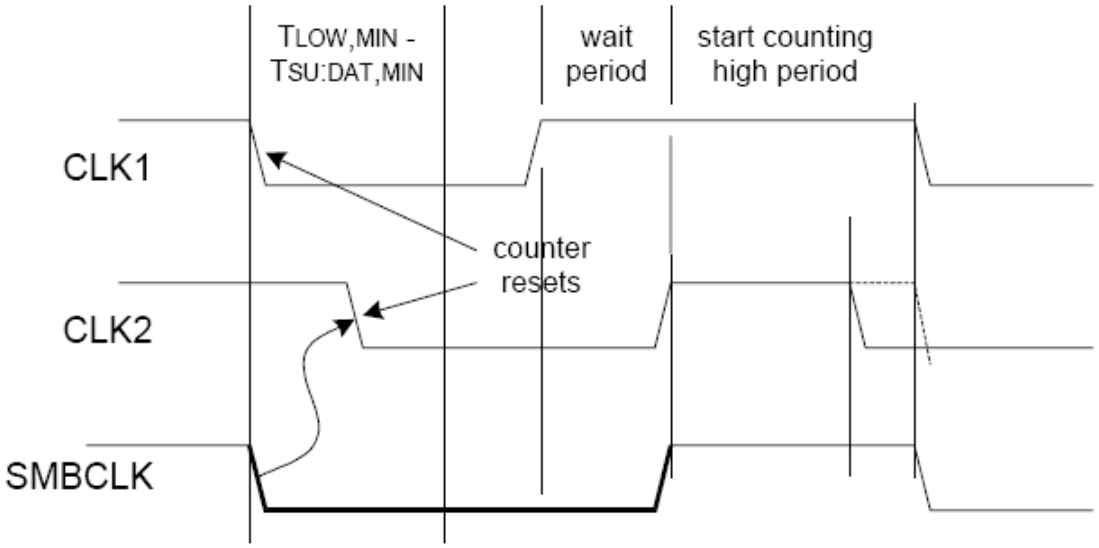


Figure 19-3 Clock synchronization

19.3 SB-TSI

The combined-format repeated start sequence is not supported in standard-mode and fast-mode.

- Only 7-bit SMBus addresses are supported.
- SB-TSI implements the Send/Receive Byte and Read/Write Byte protocols.
- SB-TSI registers can only by written using a write byte command.
- Address Resolution Protocol (ARP) is not implemented.
- Packet Error Checking (PEC) is not supported.

19.3.1 SB-TSI Address

The SMBus address is really 7 bits. The SB-TSI address is normally 98h or 4Ch. The address could vary with address select bits.

Table 19-1 SB-TSI Address Encoding

Address Select Bits	SB-TSI Address
000b	98h
001b	9Ah
010b	9Ch
011b	9Eh
100b	90h
101b	92h
110b	94h
111b	96h

19.4 PCH

The PCH provide system thermal data to EC. The EC can manage the fans and other cooling elements based on this data. A subset of the thermal collection is that the PCH and be programmed to alert the EC when a device has gone outside of its temperature limits.

19.4.1 Command Summary

Table 19-2 PCH Command Summary

Trans-action	Slave Addr.	Data Byte 0 =Command	Data Byte 1 =Byte Count	Data Byte 2	Data Byte 3	Data Byte 4	Data Byte 5	Data Byte 6	Data Byte 7
Write STS Preferences	I2C	0x41	0x6	STS [47:40]	STS [39:32]	STS [31:24]	STS [23:16]	STS [15:8]	STS [7:0]
Write CPU Temp Limits	I2C	0x42	0x6	Lower Limit [15:8]	Lower Limit [7:0]	Upper Limit [15:8]	Upper Limit [15:8]		

Write MCH Temp Limits	I2C	0x43	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write IBX Temp Limits	I2C	0x44	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write DIMM Temp Limits	I2C	0x45	0x2	Lower Limit [7:0]	Upper Limit [7:0]	na	na		
Write MPC CPU Power Clamp	I2C	0x50	0x2	Lower Limit [7:0]	Power Clamp [7:0]				
Block Read	Block Read Address	0x40	Block Read Address	Byte Count	Data 0	Data N	PEC (optional)		

19.5 SMBus Master

19.5.1 Block Diagram

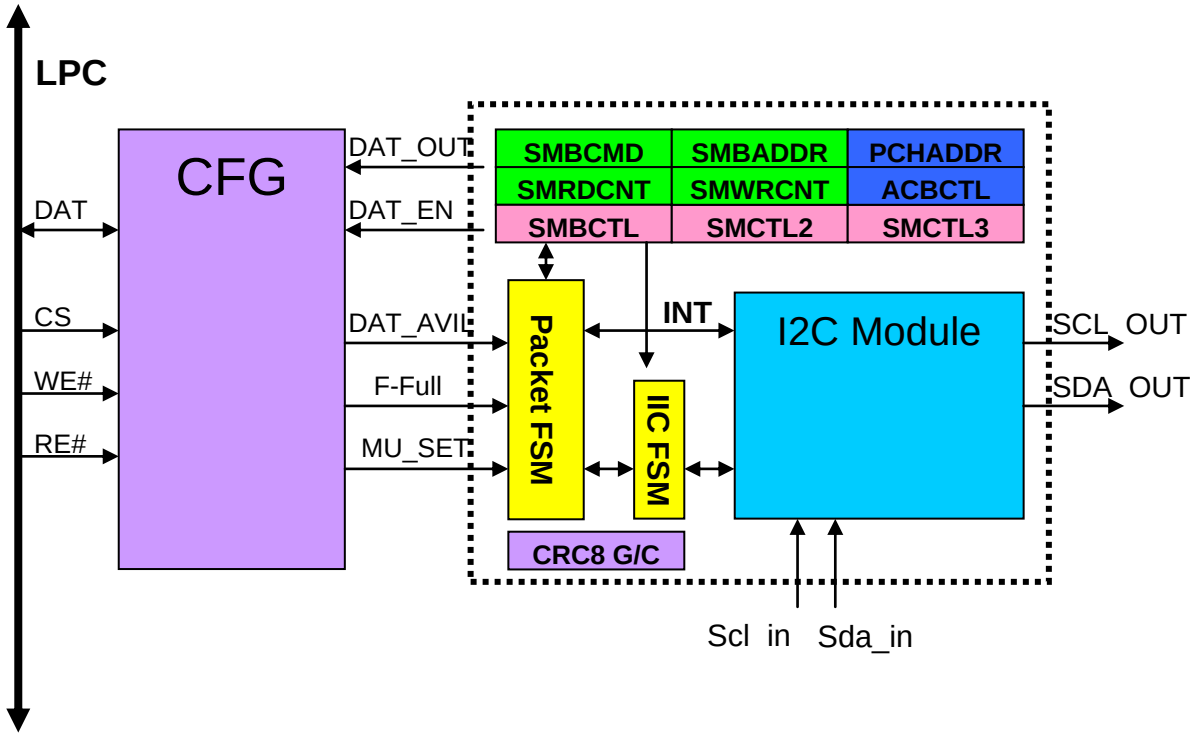


Figure 19-4 SMBus Master Block Diagram

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19.5.2 Programming Flow

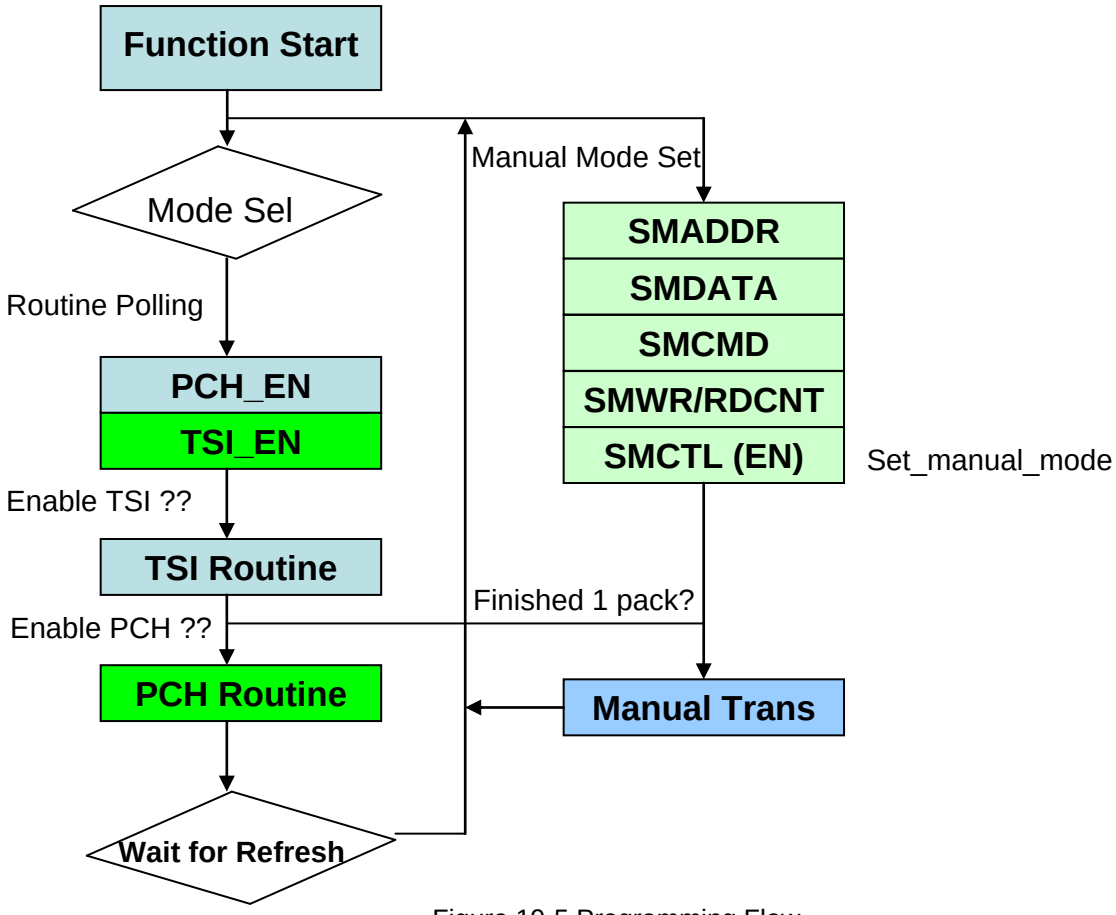

Figure 19-5 Programming Flow

19.5.3 TSI Routine

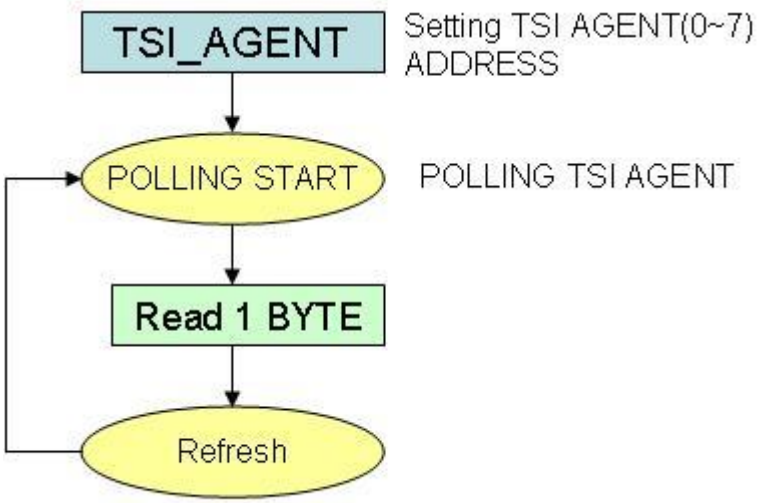

Figure 19-6 TSI Routine

19.5.4 PCH Routine

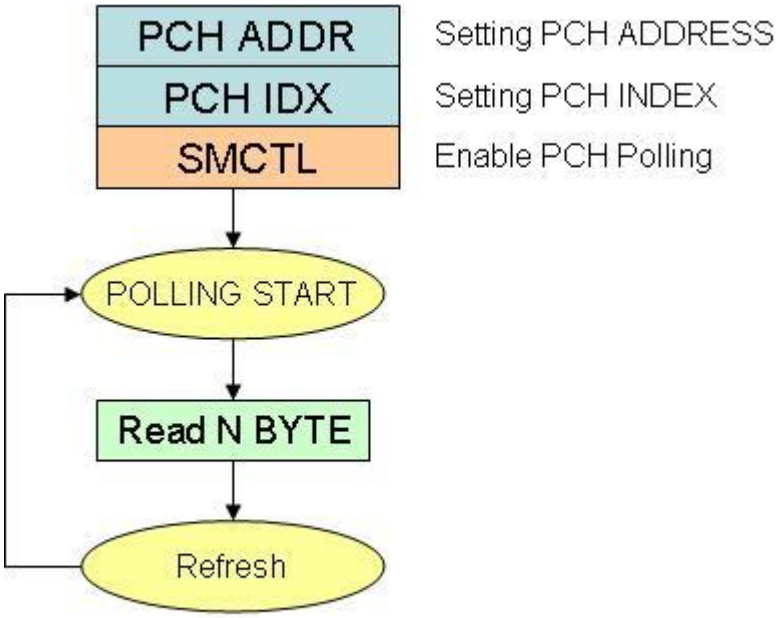

Figure 19-7 PCH Routine

19.5.5 BYTE Ruttine

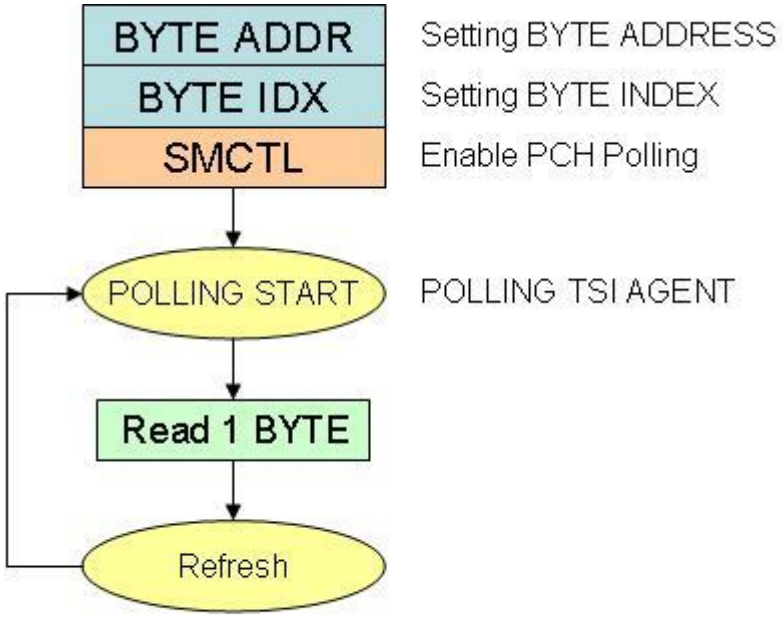

Figure 19-8 PCH Routine

19.5.6 Manual Mode interface

The SMBus host supports Block/Word/Byte Write and Block/Word/Byte read with PEC. The SMBus host can use the interface to access the smbus slave. The timing diagrams below illustrate how to use the smbus interface to write the data or read the data to the smbus slave.

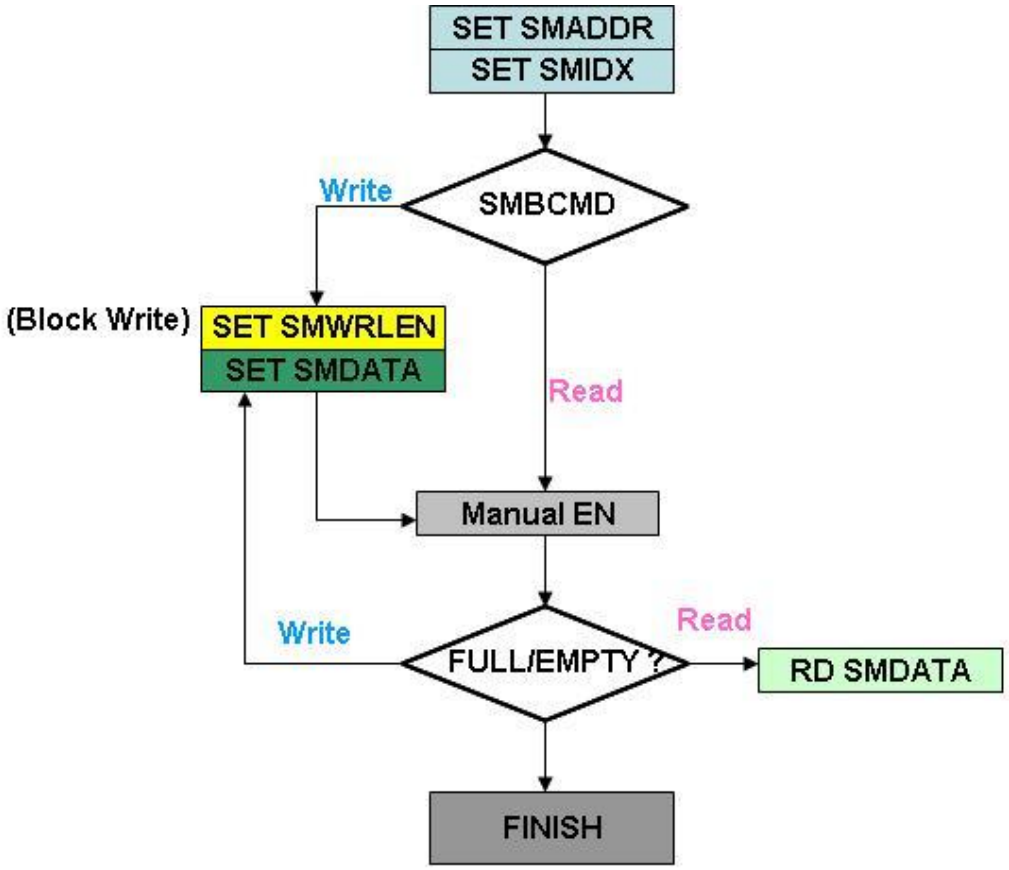

Figure 19-9 Manual Mode Programming Flow

19.6 Register Type Abbreviations

The following abbreviations are used to indicate the Register Type:

- R/W = Read/Write.
- R = Read from register.
- W = Write.
- RO = Read-only.

To program the SMBus master configuration registers, the following configuration procedures must be followed in sequence:

(1). Enter the Extended Function Mode.

(2). Configure the configuration registers.

19.6.1 Enter the Extended Function Mode

To place the chip into the Extended Function Mode, two successive writes of 0x26 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

19.6.2 Configure the Configuration Registers

The chip selects the Logical Device and activates the desired Logical Devices through Extended Function Index Register (EFIR) and Extended Function Data Register (EFDR). The EFIR is located at the same address as the EFER, and the EFDR is located at address (EFIR+1).

First, write the Logical Device Number (i.e. 0x07) to the EFIR and then write the number of the desired Logical Device to the EFDR. If accessing the Chip (Global) Control Registers, this step is not required.

Secondly, write the address of the desired configuration register within the Logical Device to the EFIR and then write (or read) the desired configuration register through the EFDR.

19.7 SMBus Master Register Set

19.7.1 SMBus Register Map

SMBus Master base address in register Logic Device B CR62h(MSB), CR63h(LSB).

Table 19-3 SMBus Master Bank 0 Registers

Offset	Type	Name	Section
0	R/W	**SMBus Data**	19.7.2
1	R/W	**SMBus Write Data Size**	19.7.3
2	R/W	**SMBus Command**	19.7.4
3	R/W	**SMBus Index**	19.7.5
4	R/W	**SMBus Control**	19.7.6
5	R/W	**SMBus Address**	19.7.7
6	R/W	**SMBCLK Frequency**	19.7.8
7	RO	**Reserved**	--
8	R/W	**PCH Address**	19.7.9
9	R/W	**Error status**	19.7.10
A	R/W	**Reserved**	--
B	R/W	**PCH Command**	19.7.11
D	R/W	**TSI Agent Enable**	19.7.12
E	R/W	**SMBus Control 3 Register**	19.7.13
F	R/W	**SMBus Control 3 Register**	19.7.14
10	R/W	**BYTE_ADDR**	19.7.15
11	R/W	**BYTE Index High Byte**	19.7.16
12	R/W	**BYTE Index Low Byte**	19.7.17
13-15	R/W	**Reserved**	
16	R/W	**TSI AGENT0 Address**	19.7.19
17	R/W	**TSI AGENT1 Address**	19.7.20

19.7.2 SMBus Data (SMDATA) – Bank 0

This 32 bits register is the data in and out register of SMBus data register. Before writing to SMDATA register, this register contains the input data, after writing to SMDATA register, this register contains the output data.

Attribute: Read/Write
Offset: 0h
Power Well: VSB
Reset by: LRESET#

Byte	3	2	1	0
Name	**SMFIFO3**	**SMFIFO2**	**SMFIFO1**	**SMFIFO0**
Default	00h	00h	00h	00h

Byte	Description
3	**SMFIFO3 (SMBus FIFO 3).** This byte represents the high byte of the 32 bits SMBus data.
2	**SMFIFO2 (SMBus FIFO 2).** This byte represents the second byte of the 32 bits SMBus data.
1	**SMFIFO1 (SMBus FIFO 1).** This byte represents the first byte of the 32 bits SMBus data.
0	**SMFIFO0 (SMBus FIFO 0).** This byte represents the low byte of the 32 bits SMBus data.

19.7.3 SMBus Write Data Size (SMWRSIZE) – Bank 0

Attribute: Read/Write
Offset: 1h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**			**SMWRSIZE**				
Default	0	0	0	0	0	0	0	0

Byte	Description
7-5	**Reserved**
4-0	**SMWRSIZE (SMBus Write Byte Counter).** This field sets the write byte counter, the max counter size is 32 bytes, and the minimal size is bytes.

19.7.4 SMBus Command (SMCMD) – Bank 0

Attribute: Read/Write
Offset: 2h
Power Well: VSB

Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
NAME	**REV**				**SMBus CMD**			
Default	0	0	0	0	0	0	0	0

Byte	Description
7-4	**Reserved**
3-0	**SMBCMD (SMBus Command).** This field sets SMBus Command: 0000 : Read Byte (Default) 0001 : Read Word 0010 : Read Block 0011 : Block Write and Read Process Call 0100 : Process Call 1000 : Write Byte 1001 : Write Word 1010 : Write Block

19.7.5 SMBus INDEX (SMIDX) – Bank 0

Attribute: Read/Write
Offset: 3h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**SMCMD**							
Default	0	0	0	0	0	0	0	0

Byte	Description
7-0	**SMIDX (SMBus INDEX).** This field represents the index data of the SMBus.

19.7.6 SMBus Control (SMCTL) – Bank 0

Attribute: Read/Write
Offset: 4h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**MMODE_S**	**S_RST**	**CRC8_EN**	**REFLASH_CLK**			**BYTE_EN**	**PCH_EN**
Default	0	0	0	0	0	0	0	0

Byte	Description
7	**MMODE_S (Manual Mode Set).** 0 : Disable. 1 : Enable.
6	**S_RST (Soft Reset SMBus).** 1 : Disable. 1 : Enable.
5	**CRC8_EN (CRC8 Enable).** 2 : CRC8 function is disable. 1 : CRC8 function is enable.
4-2	**REFRASH_CLK (Refrash Clock Select).** 000, 100 – 128ms 001, 101 – 256ms 010, 110 – 512ms 011, 111 – 64ms (1KHz)
1	**BYTE_EN (BYTE Enable).** 3 : BYTE function is disable. 1 : BYTE function is enable.
0	**PCH_EN (PCH Enable).** 4 : PCH function is disable. 1 : PCH function is enable.

19.7.7 SMBus Address (SMADDR) – Bank 0

Attribute: Read/Write
Offset: 5h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**SMADDR**							**REV**
Default	0	0	0	0	0	0	0	0

Byte	Description
7-1	**SMADDR (SMBus Address).** AMD-TSI only supports 7-bit SMBus address.
0	**Reserved:** 0 : Write. If the protocol is write, the WR_SIZE can't be zero. (Default)

19.7.8 SCL FREQ (SCLFREQ) – Bank 0

Attribute: Read/Write
Offset: 6h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**Reserved:**				**SCLFREQ**			
Default	0	0	0	0	0	1	1	1

Byte	Description
7-4	Reserved
3-0	**SCLFQ (SMBCLK Frequency).** This field defines the SMBCLK period (low time and high time). The clock low time and high time ate defined as follows: 0000 : 365KHz 0001 : 261KHz 0010 : 200KHz 0011 : 162KHz 0100 : 136KHz 0101 : 117KHz 0110 : 103KHz 0111 : 99KHz (Default) 1000 : 83KHz 1001 : 76KHz 1010 : 71KHz 1011 : 65KHz 1100 : 61KHz 1101 : 57KHz 1110 : 53KHz 1111 : 47KHz

19.7.9 PCH Address (PCHADDR) – Bank 0

Attribute: Read/Write
Offset: 8h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**PCHADDR**							**REV**
Default	1	0	0	1	0	1	0	0

Byte	Description

7-1	**PCHADDR (PCH Address).** PCH supports 8-bit SMBus address. The default address is 94h. The last bit is read or write bit. It needs to set to “0”.

19.7.10 SMBus Error Status (Error_status) – Bank 0

Attribute: Read/Write
Offset: 9h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**REV**		**ADNACK**	**Timeout**	**Reserved**	**BER**	**NACK**	**REV**
Default	1	0	0	1	0	1	0	0

Byte	Description
7-6	**Reserved**
5	**ADDR Non ACK.** This bit reflects SMBus occurred ADDRESS NON ACK in Manual mode..
4	**Timeout.** This bit reflects when SMBus occurs timeout.
3	**Reserved**
2	**BER (Bus Error).** This bit reflects when a start or stop condition is detected during data transfer, or when an arbitration problem is detected.
1	**NACK (Negative acknowledge).** This bit is set by hardware when a transmission is not acknowledged on the ninth clock. While NACK is set SCL will be drive low and subsequent bus transactions are stalled until NACK is cleared.
0	**Reserved**

19.7.11 PCH Command (PCHCMD) – Bank 0

Attribute: Read/Write
Offset: Bh
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**PCHCMD**							
Default	0	1	0	0	0	0	0	0

Byte	Description
7-0	**PCHCMD (PCH Command).** This field represents the command data of the PCH. The default command is block read (40h).

19.7.12 TSI Agent Enable Register (TSI_AGENT) – Bank

Attribute: Read/Write
Offset: Dh
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	Reserved						AG1	AG0
Default	0	0	0	0	0	0	0	0

Byte	Description
7-2	**Reserved**
1	**TSI AGENT1 Enable. :** This bit reflects AMD-TSI Agent elect. 0: Diable 1: Enable
0	**TSI AGENT0 Enable. :** This bit reflects AMD-TSI Agent elect. 0: Diable 1: Enable

19.7.13 SMBus Control 3 Register (SMCTL3) – Bank 0

Attribute: Read Only
Offset: Eh
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**				**CRC_CHK**	**M_MODE**	**F_FULL**	**F_EMPT**
Default	0	0	0	0	0	0	0	0

Byte	Description
7-4	**Reserved**
3	**CRC_CHK (CRC Check).** 5 : incorrect 1 : correct
2	**M_MODE (Manual Mode).** 6 : Non-active 1 : Active
1	**F_FULL (fifo_full). :** This bit reflects SMBus data fifo is full. 7 : Non-full 1 : Full

0	**F_EMPT (fifo empty). :** This bit reflects the SMBus data fifo is empty. 8 : Non-empty 1 : Empty

19.7.14 SMBus Control 2 Register (SMCTL2) – Bank 0

Attribute: Read/Write
Offset: Fh
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**Reserved**		**INT_LCH_E**	**Reserved**		**BYTE_SEL**	**BANKSEL**	
Default	0	0	0	0	0	0	0	0

Byte	Description
7-6	**Reserved**
5	**INT_LCH_E (Interrupt Latch Enable). :** This bit will latch the I2CSTA register. 9 : Disable. 1 : Enable.
4-3	**Reserved**
2	**BYTE_SEL :**This field represents byte polling 8-bit/16bit select bits. 0: BYTE_TEMP is 16 bit data 1: BYTE_TEMP is 8 bit data
1-0	**BANKSEL (Bank Select).** 00 – Bank 0. 01 – Bank 1. 10 – Bank 2.

19.7.15 BYTE ADDRESS0 (BYTE ADDR) – Bank 0

Attribute: Read/Write
Offset: 10h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_ADDRESS**							
Default	0	0	0	0	0	0	0	0

Byte	Description

7-0	**BYTE ADDRESS (BYTE ADDR).** This field represents the address data of the BYTE.

19.7.16 BYTE ADDRESS1 (BYTE ADDR) – Bank 0

Attribute: Read/Write
Offset: 11h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_ADDRESS**							
Default	0	0	0	0	0	0	0	0

Byte	Description
7-0	**BYTE ADDRESS1 (BYTE ADDR).** This field represents the address data of the BYTE.

19.7.17 BYTE INDEX0 (BYTE_IDX0) – Bank 0

Attribute: Read/Write
Offset:12h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_IDX_H**							
Default	0	0	0	0	0	0	0	1

Byte	Description
7-0	**BYTE_IDX_H (High BYTE INDEX).** This field represents the high byte index of the Byte polling. The default command is byte read (01h).

19.7.18 BYTE INDEX1 (BYTE_IDX1) – Bank 0

Attribute: Read/Write
Offset: 13h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**BYTE_IDX_L**							

Default	0	0	0	1	0	0	0	0

Byte	Description
7-0	**BYTE_IDX_L (LOW BYTE INDEX).** This field represents the low byte index of the Byte polling. The default command is byte read (10h).

19.7.19 TSI AGENT0 ADDRESS (TSI_AGENT0 ADDR) – Bank 0

Attribute: Read/Write
Offset: 16h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**TSI_AGNET0_ADDRESS**							
Default	1	0	0	1	1	0	0	0

Byte	Description
7-1	**TSI AGENT0 ADDRESS (TSI AGENT0 ADDR).** This field represents the address data of the BYTE.
0	**Reserved**

19.7.20 SI AGENT1 ADDRESS (TSI_AGENT1 ADDR) – Bank 0

Attribute: Read/Write
Offset: 17h
Power Well: VSB
Reset by: LRESET#

Bit	7	6	5	4	3	2	1	0
Name	**TSI_AGNET1_ADDRESS**							
Default	1	0	0	1	1	0	1	0

Byte	Description
7-1	**TSI AGENT1 ADDRESS (TSI AGENT1 ADDR).** This field represents the address data of the BYTE.
0	**Reserved**

The EC may read thermal information from IBX using the SMBus block read command. The IBX doesn't support byte-read or word-read SMBus commands. The read use a different address that the writes. The address must be different so that the IBX knows which target Is intended, either the I2C target or the block read buffer.

The IBX and EC are set up by BIOS with the length of the read that is supported by the platform. The EC must always do reads of the lengths set up by BIOS. There is no way to change the length of the read after BIOS has set things up.

An EC that only wants the single highest temperature among MCH, and CPU could read one byte. A 2 byte read would provide both IBX and CPU/MCH package temperature. An EC that wanted each components temperature would do a 4 byte read. An EC that also wanted DIMM information would read 9 bytes. If an EC wanted to read the HOST STS status, it must read 19 bytes. An EC can also read the energy data provided by the CPU by reading 12 bytes.

20. OVP & UVP DETECT

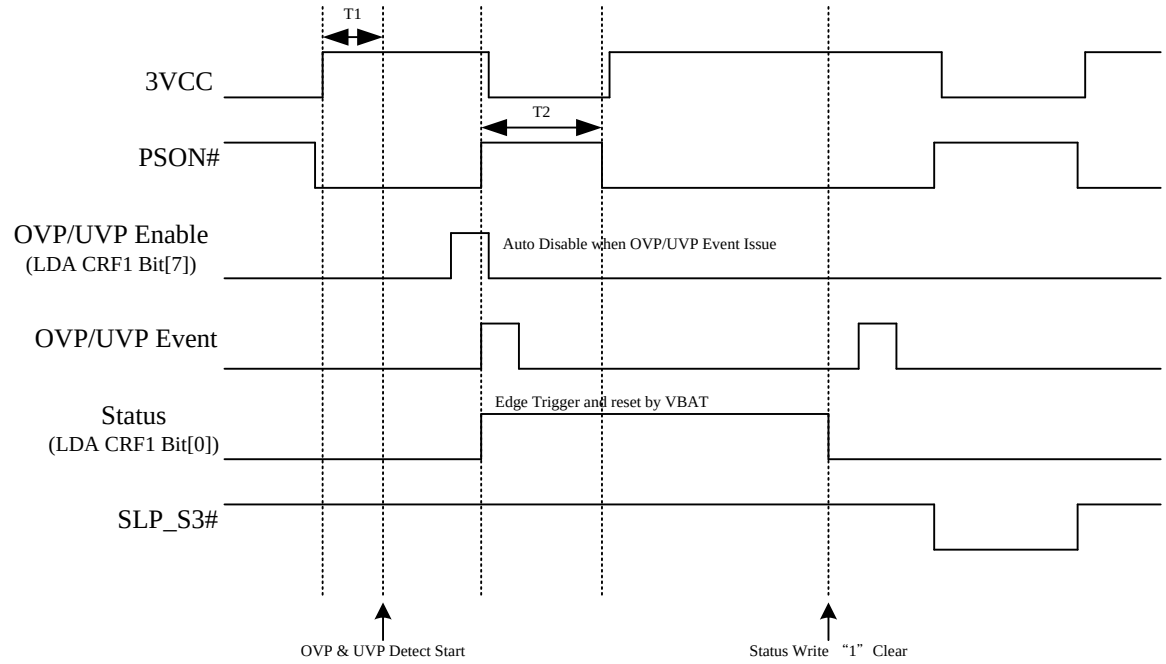

Figure 20-1 OVP & UVP Detect when SLP_S3# = 1

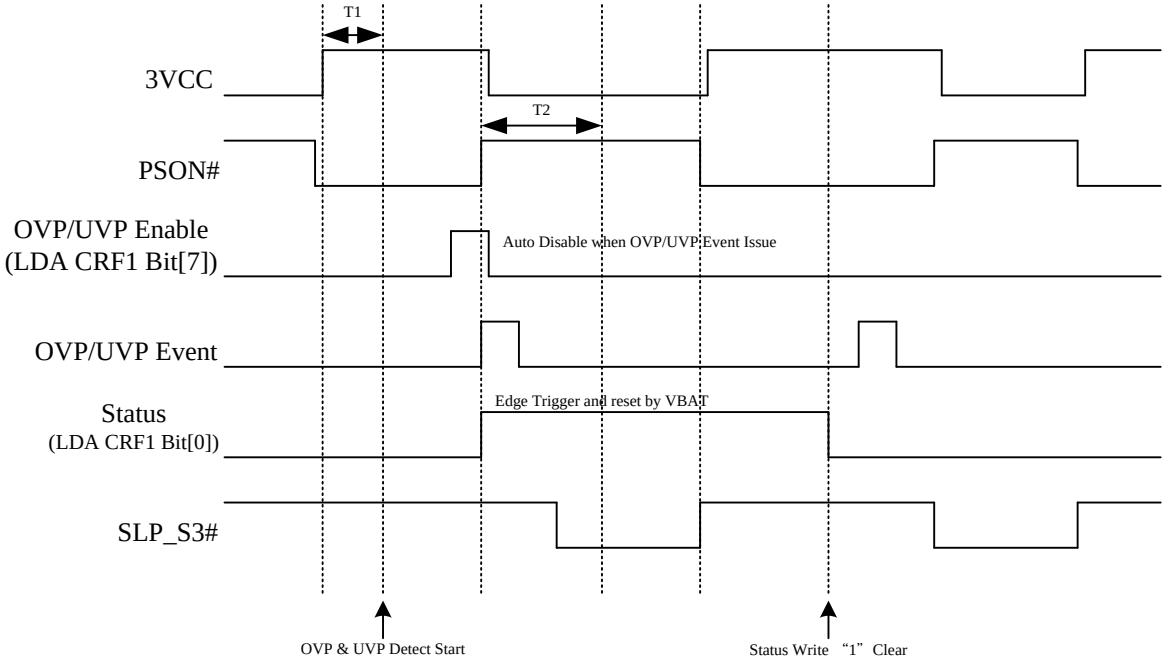

Figure 20-2 OVP & UVP Detect when SLP_S3# = 0

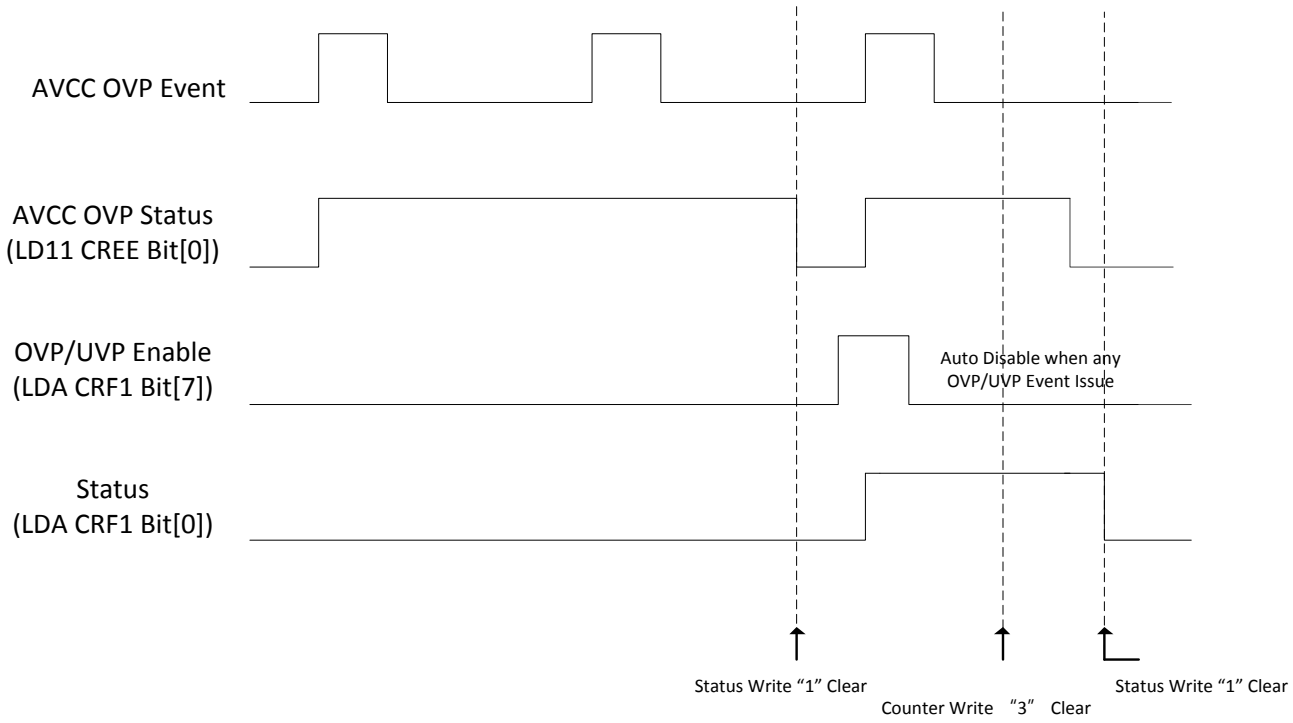

Figure 20-3 AVCC OVP Detect

Table 20-1 Timing Parameters of OVP/UVP

TIMING	PARAMETER
T1	3VCC to OVP/UVP Detect Start (See LDA CRF1 Bit6-5)
T2	PSON# inactive to SLP_S3# Detect (See LDA CRF1 Bit4-3)

21. PORT80 TO UART

The NCT6796D provides UART interface to transfer PORT80 information to other peripheral devices. Default baud rate is 115200Hz for universal UART protocol and it could be change by LD14 CRE2 and LD14 CRE3. When BIOS program PORT80 LED, in proportion to UART baud rate, it changes very frequently. Thus, some information might be lose. But we make sure the last one would be send.

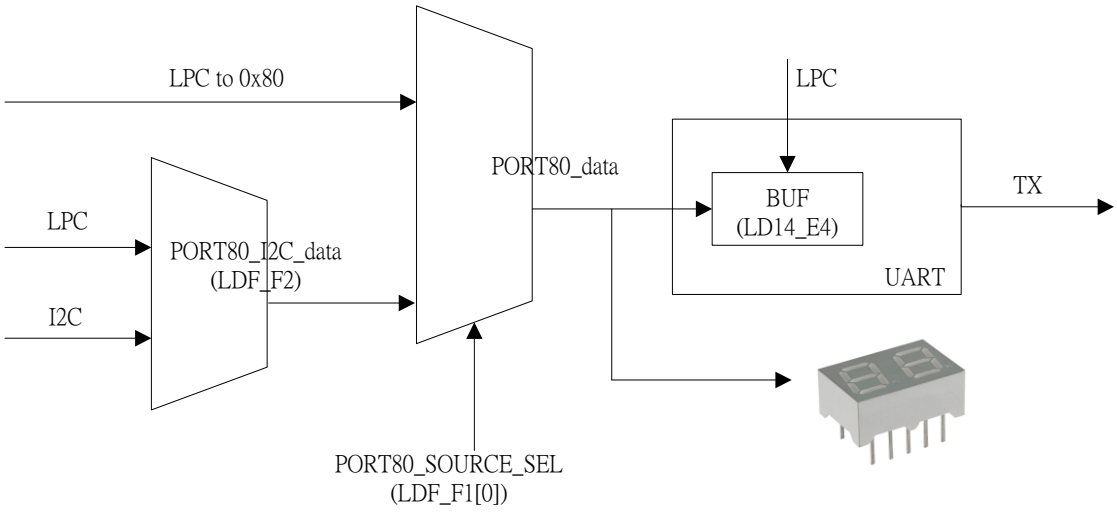

Figure 21-1 PORT80 to UART Block Diagram

After enter OS, we support other root to control PORT80 LED by write LDF CRF2 and LDF CRF1 to change other path. The UART could be control by other root, too. It is set by LD14 CRE4.

22. FADING LED

The NCT6796D provide Fading led interface that can be change led speed of bright or dark througt different frequency or duty cycle. Furthermore, the constrast of led bright or dark can be decided by maximum duty cycle, minimum duty cycle, and middle value.

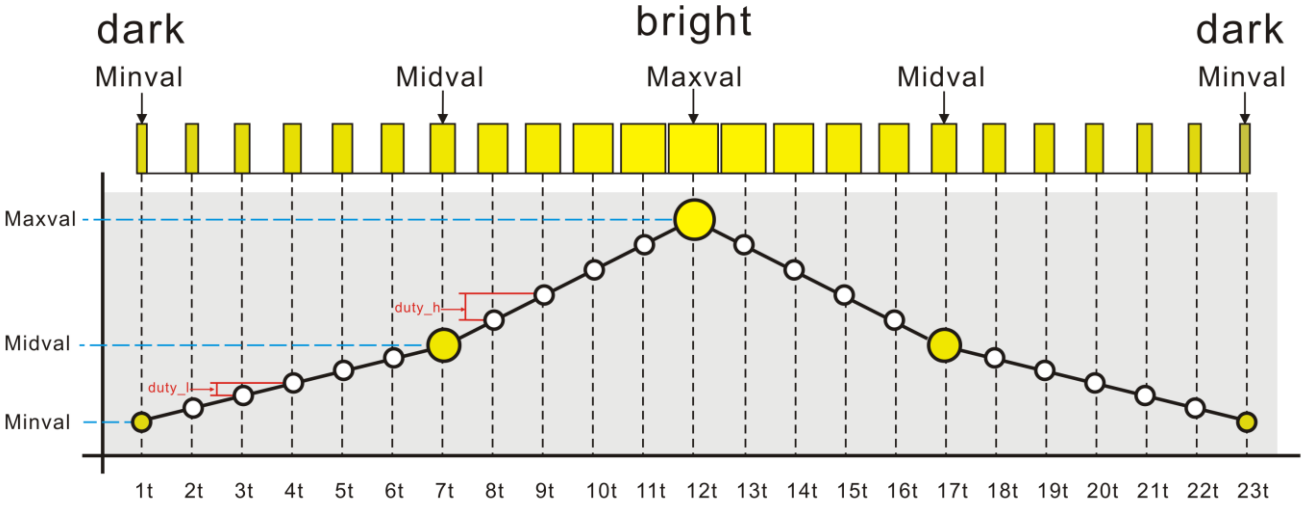

Figure 28-1 Example of Fading LED

NCT6796D GRN/YLW, MLED and FDLED1~4 supports fading led function. The duty cycle can be increase and decrease contrl by LD15 CRF3, CRF4, CRF9 and CRFA, as table 29-1. Besides LD15 CRF7 also supports dark extend control, as table 29-2.

Table 29-1 Duty cycle increase/decrease time

LD15 CRF3	LD15 CRF4	LD15 CRF9	LD15 CRFA	Increase Time	Decrease Time
0x0D	0x0E	0x03	0x03	0.61 sec	2.90 sec
0x08	0x08	0x08	0x08	1.06 sec	1.06 sec
0x06	0x05	0x06	0x05	1.57 sec	1.57 sec (default)
0x04	0x04	0x04	0x04	2.15 sec	2.15 sec

Table 29-2 Dark extend time

LD15 CRF7	Dark extend Time
0x0F	0.96 sec (default)
0x17	1.47 sec
0x1E	1.92 sec

23. OSCILLATOR FREE

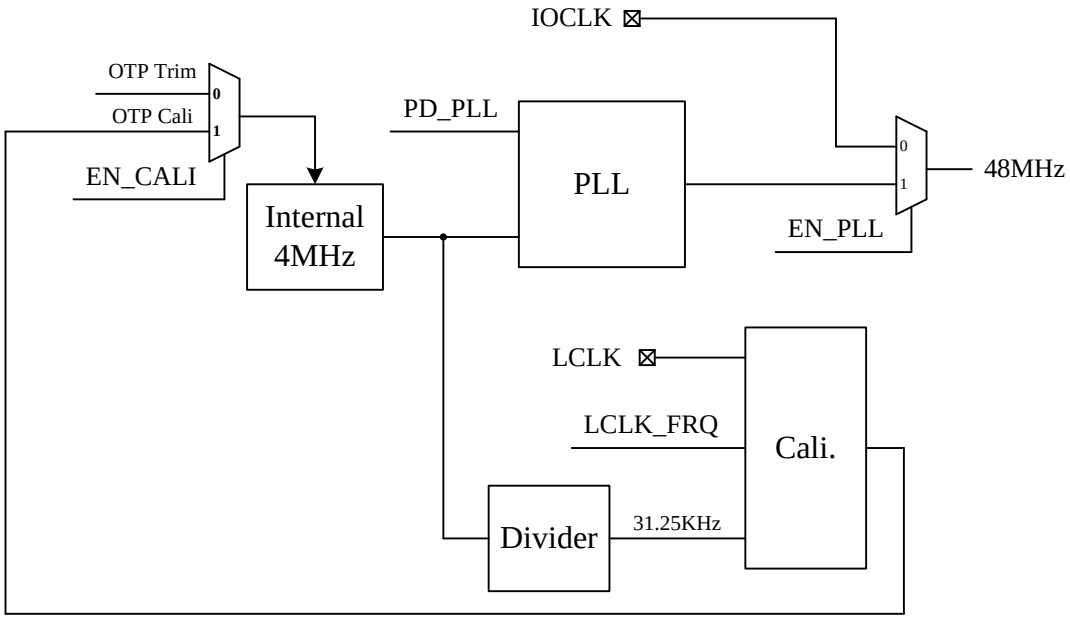

Figure 30-1 Oscillator free architecture

24. CONFIGURATION REGISTER

24.1 Chip (Global) Control Register

Default Value of Global Control Register:

Register	Default	Register	Default	Register	Default
CR 07h	00h	CR 20h	D4h (ID_H)	CR 2Bh	00h
CR 10h	FFh	CR 21h	21h (ID_L)	CR 2Ch	01h
CR 11h	FFh	CR 22h	FFh	CR 2Dh	0ss0_0000b
CR 13h	00h	CR 24h	04h	CR 2Fh	ssss_sss0b
CR 14h	00h	CR 25h	00h		
CR 1Ah	30h	CR 26h	0s00_0000b		
CR 1Bh	18h	CR 27h	03h		
CR 1Ch	00h	CR 28h	00h		
CR 1Dh	00h	CR 2Ah	C0h		

Note. The value of “s” means hardware strapping result: strapping high will report 1; strapping low will report 0.
In addition, BIOS can write the value of strapping result after hardware strapping.

Note. The CR21h is low-byte of the Chip-ID; the “X” means IC version. EX. 11=A version, 12=B version, 13=C version.

Reserved Registers of Global Control Register:

Register	Default	Register	Default
CR 02h	00h	CR 1Eh	FFh
CR 12h	FFh	CR 1Fh	FFh
CR 15h	FFh	CR 23h	00h
CR 16h	FFh	CR 29h	FFh
CR 17h	FFh	CR 2Eh	00h
CR 18h	FFh		
CR 19h	FFh		

Note. All reserved registers must keep default value.

Note. Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 07h. Logical Device Selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Logical Device Number.

CR 10h. Device IRQ TYPE Selection

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	PRT IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
5	R / W	UARTA IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4	R / W	UARTB IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
3	R / W	KBC IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
2	R / W	MOUSE IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
1	R / W	CIR IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	R / W	CIRWAKUP IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 11h. Device IRQ TYPE Selection

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	R / W	HM IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
6	R / W	WDT1 IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.

BIT	READ / WRITE	DESCRIPTION
5	R / W	WDT3 IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
4-2	Reserved	
1	R / W	SMI IRQ TYPE SELECT (note1.) 0: Edge. 1: Level.
0	Reserved	

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 13h. Device IRQ Polarity Selection

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<15:8> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 14h. Device IRQ Polarity Selection

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	IRQ Channel<7:0> Polarity (note1.) 0: High. 1: Low.

Note1: Before accessing CR10, CR11, CR13 and CR14, CR26 [Bit4] must be set to logic 1.

CR 1Ah.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 30h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td>R / W</td><td>Pin83 function selection
<table>
<tr><th>LD12 CREB[Bit6]</th><th>CR1A [Bit7-6]</th><th>Pin83</th></tr>
<tr><td>1</td><td>x</td><td>CIRRX</td></tr>
<tr><td>0</td><td>00</td><td>RESETCONI#</td></tr>
<tr><td>0</td><td>01</td><td>GP30</td></tr>
<tr><td>0</td><td>10</td><td>OVT#_1</td></tr>
<tr><td>0</td><td>11</td><td>SMI#_1</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin76 function selection
<table>
<tr><th>CR1B [Bit0]</th><th>LD12 CRE0[Bit4]</th><th>CR1A [Bit5]</th><th>Pin76</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>MSDA</td></tr>
<tr><td>0</td><td>1</td><td>X</td><td>AUXFANOUT2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SDA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP31</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>Pin75 function selection
<table>
<tr><th>CR1B [Bit0]</th><th>LD12 CRE0[Bit3]</th><th>CR1A [Bit4]</th><th>Pin75</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>MSCL</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>AUXFANIN2#</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SCL</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP32</td></tr>
</table></td></tr>
<tr><td>3-2</td><td>R / W</td><td>Pin52 function selection
<table>
<tr><th>CR27 [Bit4]</th><th>CR1A [Bit3-2]</th><th>Pin52</th></tr>
<tr><td>1</td><td>xx</td><td>INIT#</td></tr>
<tr><td>0</td><td>00</td><td>MSCL</td></tr>
<tr><td>0</td><td>01</td><td>SCL</td></tr>
<tr><td>0</td><td>10</td><td>GP41</td></tr>
</table></td></tr>
<tr><td>1</td><td colspan="2">Reserved</td></tr>
<tr><td>0</td><td>R / W</td><td>GA20M and KBRST# output type selection
0: Push Pull
1: OD</td></tr>
</table>

CR 1Bh.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 10h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin37 function selection
<table>
<tr><td>CR27 [Bit6]</td><td>CR1B [Bit7]</td><td>Pin37</td></tr>
<tr><td>0</td><td>0</td><td>RESETCONO#</td></tr>
<tr><td>0</td><td>1</td><td>GP47</td></tr>
<tr><td>1</td><td>x</td><td>FDLED4</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin39 function selection
<table>
<tr><td>CR27 [Bit4]</td><td>LDD CRE1 [Bit4]</td><td>CR1B [Bit6]</td><td>Pin39</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>PE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP45</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>YLW_LED</td></tr>
</table>
Pin40 function selection
<table>
<tr><td>CR27 [Bit4]</td><td>LDD CRE1 [Bit4]</td><td>CR1B [Bit6]</td><td>Pin40</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>BUSY</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP44</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GRN_LED</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin86 function Selection
<table>
<tr><td>DDR4_EN</td><td>CR1B [Bit5]</td><td>Pin86</td></tr>
<tr><td>0</td><td>0</td><td>GP57</td></tr>
<tr><td>1</td><td>0</td><td>VPP_EN</td></tr>
<tr><td>x</td><td>1</td><td>AUXFANIN2</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>Pin95 function selection
<table>
<tr><td>DDR4_EN</td><td>CR1B [Bit4]</td><td>CR27 [Bit3]</td><td>Pin95</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>VPP_PG</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>CIRRX</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP24</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>IRRX1</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>3</td><td>R / W</td><td>Pin103 function selection
<table>
<tr><td>CR1B [Bit3]</td><td>LDD CRE2 [Bit1-0]</td><td>Pin103</td></tr>
<tr><td>0</td><td>00</td><td>GP40</td></tr>
<tr><td>0</td><td>01</td><td>SMI#_2</td></tr>
<tr><td>0</td><td>1x</td><td>OVT#_2</td></tr>
<tr><td>1</td><td>xx</td><td>GP40</td></tr>
</table></td></tr>
<tr><td>2-1</td><td>R / W</td><td>Pin51 function selection
<table>
<tr><td>CR27 [Bit4]</td><td>CR1B [Bit2-1]</td><td>Pin51</td></tr>
<tr><td>1</td><td>x</td><td>SLIN#</td></tr>
<tr><td>0</td><td>00</td><td>MSDA</td></tr>
<tr><td>0</td><td>01</td><td>SDA</td></tr>
<tr><td>0</td><td>10</td><td>BEEP</td></tr>
<tr><td>0</td><td>11</td><td>GP42</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin75 function selection
<table>
<tr><td>CR1B [Bit0]</td><td>LD12 CRE0[Bit3]</td><td>CR1A [Bit4]</td><td>Pin75</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>MSCL</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>AUXFANIN2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SCL</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP32</td></tr>
</table>
Pin76 function selection
<table>
<tr><td>CR1B [Bit0]</td><td>LD12 CRE0[Bit4]</td><td>CR1A [Bit5]</td><td>Pin76</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>MSDA</td></tr>
<tr><td>0</td><td>1</td><td>X</td><td>AUXFANOUT2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SDA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP31</td></tr>
</table></td></tr>
</table>

CR 1Ch.
Attribute: Read/Write
Power Well: VSB
Reset by: PWROK
Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin5 function selection
<table>
<tr><td>CR1C [Bit7]</td><td>Pin5</td></tr>
<tr><td>0</td><td>AUXFANIN2</td></tr>
<tr><td>1</td><td>GP06</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R / W</td><td>Pin4 function selection
<table>
<tr><td>CR1C [Bit6]</td><td>Pin4</td></tr>
<tr><td>0</td><td>AUXFANIN1</td></tr>
<tr><td>1</td><td>GP05</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin3 function selection
<table>
<tr><td>CR1C [Bit5]</td><td>Pin3</td></tr>
<tr><td>0</td><td>AUXFANIN0</td></tr>
<tr><td>1</td><td>GP04</td></tr>
</table></td></tr>
<tr><td>4-3</td><td>R / W</td><td>Pin2 function selection
<table>
<tr><td>LDD_CRE1[Bit1]</td><td>CR1C [Bit4-3]</td><td>Pin2</td></tr>
<tr><td>1</td><td>xx</td><td>RESERVE</td></tr>
<tr><td>0</td><td>00</td><td>GP03</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin123 function selection
<table>
<tr><td>CR1C [Bit2]</td><td>Pin123</td></tr>
<tr><td>0</td><td>AUXFANOUT2</td></tr>
<tr><td>1</td><td>GP02</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin122 function selection
<table>
<tr><td>CR1C [Bit1]</td><td>Pin122</td></tr>
<tr><td>0</td><td>AUXFANOUT1</td></tr>
<tr><td>1</td><td>GP01</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin6 function selection
<table>
<tr><td>CR1C [Bit0]</td><td>Pin6</td></tr>
<tr><td>0</td><td>AUXFANOUT0</td></tr>
<tr><td>1</td><td>GP00</td></tr>
</table></td></tr>
</table>

CR 1Dh.
Attribute: Read/Write
Power Well: VSB
Reset by: PWROK(Bit7-5, 0), RSMRST#(Bit4-1)
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	RESERVE	
4	R / W	0: Disable ANTISURGE event route to KBRST# 1: Enable ANTISURGE event route to KBRST#

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>3-1</td><td>R / W</td><td>Pin66 function selection
<table>
<tr><td>CR1D [Bit3-1]</td><td>Pin66</td></tr>
<tr><td>000</td><td>AUXFANOUT4</td></tr>
<tr><td>001</td><td>AUXFANOUT4</td></tr>
<tr><td>011</td><td>GP73</td></tr>
<tr><td>100</td><td>Tri-state</td></tr>
<tr><td>111</td><td>Tri-state</td></tr>
</table></td></tr>
<tr><td>0</td><td>Reserved</td><td></td></tr>
</table>

CR 20h. Chip ID (High Byte)

Attribute: Read Only
Power Well: VSB
Reset by: None
Default : D4h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = D4h (high byte).

CR 21h. Chip ID (Low Byte)

Attribute: Read Only
Power Well: VSB
Reset by: None
Default : 21h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only	Chip ID number = 21h (low byte)

CR 22h. Device Power Down

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	UARTB Power Down. 0: Powered down. 1: Not powered down.
4	R / W	UARTA Power Down. 0: Powered down. 1: Not powered down.
3	R / W	PRT Power Down. 0: Powered down. 1: Not powered down.
2-0	Reserved	

CR 24h.

Attribute: Read/Write

Power Well: VSB
Reset by: LRESET#
Default : 04h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Select output type of AUXFANOUT2
=0 AUXFANOUT2 is Open-drain.
=1 AUXFANOUT2 is Push-pull.</td></tr>
<tr><td>6</td><td>R / W</td><td>Select output type of AUXFANOUT1
=0 AUXFANOUT1 is Open-drain.
=1 AUXFANOUT1 is Push-pull.</td></tr>
<tr><td>5</td><td>R / W</td><td>Select output type of AUXFANOUT0
=0 AUXFANOUT0 is Open-drain.
=1 AUXFANOUT0 is Push-pull.</td></tr>
<tr><td>4</td><td>R / W</td><td>Select output type of SYSFANOUT
=0 SYSFANOUT is Open-drain.
=1 SYSFANOUT is Push-pull.</td></tr>
<tr><td>3</td><td>R / W</td><td>Select output type of CPUFANOUT
=0 CPUFANOUT is Open-drain.
=1 CPUFANOUT is Push-pull.</td></tr>
<tr><td>2</td><td>R / W</td><td>Pin128 function selection
<table>
<tr><th>CR24 [Bit2]</th><th>CR25 [Bit4]</th><th>Pin128</th></tr>
<tr><td>0</td><td>0</td><td>OVT#_1</td></tr>
<tr><td>0</td><td>1</td><td>GP07</td></tr>
<tr><td>1</td><td>x</td><td>SMI#_1</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Select output type of AUXFANOUT3
=0 AUXFANOUT3 is Open-drain.
=1 AUXFANOUT3 is Push-pull.</td></tr>
<tr><td>0</td><td>R / W</td><td>PNPCVS =>
= 0 The compatible PNP address-select registers have default values.
= 1 The compatible PNP address-select registers have no default values.</td></tr>
</table>

CR 25h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-5</td><td colspan="2">Reserved</td></tr>
<tr><td>4</td><td>R / W</td><td>Pin128 function selection
<table>
<tr><td>CR24 [Bit2]</td><td>CR25 [Bit4]</td><td>Pin128</td></tr>
<tr><td>0</td><td>0</td><td>OVT#_1</td></tr>
<tr><td>0</td><td>1</td><td>GP07</td></tr>
<tr><td>1</td><td>x</td><td>SMI#_1</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>UARTBTRI</td></tr>
<tr><td>2</td><td>R / W</td><td>UARTATRI</td></tr>
<tr><td>1</td><td>R / W</td><td>PRTTRI</td></tr>
<tr><td>0</td><td>R / W</td><td>Select output type of AUXFANOUT4
=0 AUXFANOUT4 is Open-drain.
=1 AUXFANOUT4 is Push-pull.</td></tr>
</table>

CR 26h. s: value by strapping
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 0s00_0000b

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	HEFRAS => = 0 Write 87h to location 2E twice. = 1 Write 87h to location 4E twice. The corresponding power-on strapping pin is RTSA#.
5	R / W	LOCKREG => = 0 Enable R/W configuration registers. = 1 Disable R/W configuration registers.
4-3	Reserved	
2	R / W	DSPRLGRQ => = 0 Enable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is effective when selecting IRQ. = 1 Disable PRT legacy mode for IRQ and DRQ selection. Then DCR register (base address + 2) bit 4 is not effective when selecting IRQ.

BIT	READ / WRITE	DESCRIPTION
1	R / W	DSUALGRQ => = 0 Enable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable UART A legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.
0	R / W	DSUBLGRQ => = 0 Enable IR legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is effective when selecting IRQ. = 1 Disable IR legacy mode for IRQ selection. Then HCR register (base address + 4) bit 3 is not effective when selecting IRQ.

CR 27h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 03h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin82 function selection
<table>
<tr><th>CR27 [Bit7]</th><th>LD12 CREB [Bit0]</th><th>Pin82</th></tr>
<tr><td>0</td><td>0</td><td>PWROK</td></tr>
<tr><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>1</td><td>x</td><td>FDLED1</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin37 function selection
<table>
<tr><th>CR27 [Bit6]</th><th>CR1B [Bit7]</th><th>Pin37</th></tr>
<tr><td>0</td><td>0</td><td>RESETCONO#</td></tr>
<tr><td>0</td><td>0</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>GP47</td></tr>
<tr><td>1</td><td>x</td><td>FDLED4</td></tr>
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<tr><td>5</td><td colspan="2">Reserved</td></tr>
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<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>
Pin38 function selection
<table>
<tr><td>CR27 [Bit4]</td><td>LDD CRE1 [Bit5]</td><td>Pin38</td></tr>
<tr><td>0</td><td>0</td><td>GP46</td></tr>
<tr><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>1</td><td>x</td><td>SLCT</td></tr>
</table>
Pin39 function selection
<table>
<tr><td>CR27 [Bit4]</td><td>LDD CRE1 [Bit4]</td><td>CR1B [Bit6]</td><td>Pin39</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>PE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP45</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>YLW_LED</td></tr>
</table>
Pin40 function selection
<table>
<tr><td>CR27 [Bit4]</td><td>LDD CRE1 [Bit4]</td><td>CR1B [Bit6]</td><td>Pin40</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>BUSY</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP44</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GRN_LED</td></tr>
</table>
Pin41 function selection
<table>
<tr><td>P80_EN</td><td>CR27 [Bit4]</td><td>Pin41</td></tr>
<tr><td>1</td><td>x</td><td>DGL0#</td></tr>
<tr><td>0</td><td>0</td><td>GP43</td></tr>
<tr><td>0</td><td>1</td><td>ACK#</td></tr>
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</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>
Pin42 function selection
<table>
<tr><td>P80_EN</td><td>CR27 [Bit4]</td><td>Pin42</td></tr>
<tr><td>1</td><td>x</td><td>DGH0#</td></tr>
<tr><td>0</td><td>0</td><td>GP67</td></tr>
<tr><td>0</td><td>1</td><td>PD7</td></tr>
</table>
Pin43 function selection
<table>
<tr><td>P80_EN</td><td>CR27 [Bit4]</td><td>Pin43</td></tr>
<tr><td>1</td><td>x</td><td>LED_G</td></tr>
<tr><td>0</td><td>0</td><td>GP66</td></tr>
<tr><td>0</td><td>1</td><td>PD6</td></tr>
</table>
Pin44 function selection
<table>
<tr><td>P80_EN</td><td>CR27 [Bit4]</td><td>Pin44</td></tr>
<tr><td>1</td><td>x</td><td>LED_F</td></tr>
<tr><td>0</td><td>0</td><td>GP65</td></tr>
<tr><td>0</td><td>1</td><td>PD5</td></tr>
</table>
Pin45 function selection
<table>
<tr><td>P80_EN</td><td>CR27 [Bit4]</td><td>Pin45</td></tr>
<tr><td>1</td><td>x</td><td>LED_E</td></tr>
<tr><td>0</td><td>0</td><td>GP64</td></tr>
<tr><td>0</td><td>1</td><td>PD4</td></tr>
</table>
Pin47 function selection
<table>
<tr><td>P80_EN</td><td>CR27 [Bit4]</td><td>Pin47</td></tr>
<tr><td>1</td><td>x</td><td>LED_D</td></tr>
<tr><td>0</td><td>0</td><td>GP63</td></tr>
<tr><td>0</td><td>1</td><td>PD3</td></tr>
</table>
Pin48 function selection
<table>
<tr><td>P80_EN</td><td>CR27 [Bit4]</td><td>Pin48</td></tr>
<tr><td>1</td><td>x</td><td>LED_C</td></tr>
<tr><td>0</td><td>0</td><td>GP62</td></tr>
<tr><td>0</td><td>1</td><td>PD2</td></tr>
</table>
Pin49 function selection
<table>
<tr><td>P80_EN</td><td>CR27 [Bit4]</td><td>Pin49</td></tr>
<tr><td>1</td><td>x</td><td>LED_B</td></tr>
<tr><td>0</td><td>0</td><td>GP61</td></tr>
<tr><td>0</td><td>1</td><td>PD1</td></tr>
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<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>
Pin50 function selection
<table>
<tr><td>P80_EN</td><td>CR27 [Bit4]</td><td>Pin50</td></tr>
<tr><td>1</td><td>x</td><td>LED_A</td></tr>
<tr><td>0</td><td>0</td><td>GP60</td></tr>
<tr><td>0</td><td>1</td><td>PD0</td></tr>
</table>
Pin51 function selection
<table>
<tr><td>CR27 [Bit4]</td><td>CR1B [Bit2-1]</td><td>Pin51</td></tr>
<tr><td>1</td><td>x</td><td>SLIN#</td></tr>
<tr><td>0</td><td>00</td><td>MSDA</td></tr>
<tr><td>0</td><td>01</td><td>SDA</td></tr>
<tr><td>0</td><td>10</td><td>BEEP</td></tr>
<tr><td>0</td><td>11</td><td>GP42</td></tr>
</table>
Pin52 function selection
<table>
<tr><td>CR27 [Bit4]</td><td>CR1A [Bit3-2]</td><td>Pin52</td></tr>
<tr><td>1</td><td>xx</td><td>INIT#</td></tr>
<tr><td>0</td><td>00</td><td>MSCL</td></tr>
<tr><td>0</td><td>01</td><td>SCL</td></tr>
<tr><td>0</td><td>10</td><td>GP41</td></tr>
</table>
Pin53 function selection
<table>
<tr><td>LD12 CREC [Bit2]</td><td>CR27 [Bit4]</td><td>LDD CRE1 [Bit6]</td><td>Pin53</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>DGL1#</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP36</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>ERR#</td></tr>
</table>
Pin54 function selection
<table>
<tr><td>LD12 CREC [Bit2]</td><td>CR27 [Bit4]</td><td>LDD CRE1 [Bit6]</td><td>Pin54</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>DGH1#</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP35</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>AFD#</td></tr>
</table>
</td></tr>
<tr><td>4</td><td>R / W</td><td>
Pin55 function selection
<table>
<tr><td>CR27 [Bit4]</td><td>LDD CRE1 [Bit5]</td><td>Pin55</td></tr>
<tr><td>0</td><td>0</td><td>GP34</td></tr>
<tr><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>1</td><td>x</td><td>STB#</td></tr>
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</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>3</td><td>R / W</td><td>Pin95 function selection
<table>
<tr><td>DDR4_EN</td><td>CR1B [Bit4]</td><td>CR27 [Bit3]</td><td>Pin95</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>VPP_PG</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>CIRRX</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP24</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>IRRX1</td></tr>
</table>
Pin96 function selection
<table>
<tr><td>CR27 [Bit3]</td><td>Pin96</td></tr>
<tr><td>0</td><td>GP25</td></tr>
<tr><td>1</td><td>IRTX1</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin11 function selection
<table>
<tr><td>TEST_MODE0_EN</td><td>CR27 [Bit2]</td><td>CR2A [Bit6]</td><td>Pin11</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>VRM_PG</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>IRRX0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SINB</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP13</td></tr>
</table>
Pin12 function selection
<table>
<tr><td>CR27 [Bit2]</td><td>CR2A [Bit6]</td><td>Pin12</td></tr>
<tr><td>1</td><td>x</td><td>IRTX0</td></tr>
<tr><td>0</td><td>0</td><td>SOUTB</td></tr>
<tr><td>0</td><td>1</td><td>GP12</td></tr>
</table></td></tr>
<tr><td>1-0</td><td colspan="2">Reserved</td></tr>
</table>

CR 28h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4	R / W	HM IO space lock enable 0 : Disable 1 : Enable
3	Reserved	

BIT	READ / WRITE	DESCRIPTION
2-0	R / W	PRTMODS2 ~ 0 => **Bits** **2 1 0** = 0 x x Parallel Port Mode. = 1 x x Reserved

CR 2Ah.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#, GP2X_MRST(Bit1-0)

Default : C0h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>
Pin29 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin29</td></tr>
<tr><td>0</td><td>CTSA#</td></tr>
<tr><td>1</td><td>GP80</td></tr>
</table>
Pin30 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin30</td></tr>
<tr><td>0</td><td>DSRA#</td></tr>
<tr><td>1</td><td>GP81</td></tr>
</table>
Pin31 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin31</td></tr>
<tr><td>0</td><td>RTSA#</td></tr>
<tr><td>1</td><td>GP82</td></tr>
</table>
Pin32 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin32</td></tr>
<tr><td>0</td><td>DTRA#</td></tr>
<tr><td>1</td><td>GP83</td></tr>
</table>
Pin33 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin33</td></tr>
<tr><td>0</td><td>SINA</td></tr>
<tr><td>1</td><td>GP84</td></tr>
</table>
Pin34 function selection
<table>
<tr><td>UARTA_P80_EN</td><td>CR2A [Bit7]</td><td>Pin34</td></tr>
<tr><td>1</td><td>x</td><td>SOUTA_P80</td></tr>
<tr><td>0</td><td>0</td><td>SOUTA</td></tr>
<tr><td>0</td><td>1</td><td>GP85</td></tr>
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<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin35 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin35</td></tr>
<tr><td>0</td><td>DCDA#</td></tr>
<tr><td>1</td><td>GP86</td></tr>
</table>
Pin36 function selection
<table>
<tr><td>CR2A [Bit7]</td><td>Pin36</td></tr>
<tr><td>0</td><td>RIA#</td></tr>
<tr><td>1</td><td>GP87</td></tr>
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<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R / W</td><td>
Pin7 function selection
<table>
<tr><td>TEST_MODE0_EN</td><td>LD12 CRE0 [Bit7]</td><td>CR2A [Bit6]</td><td>Pin7</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>PWM_R</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>CTSB#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP17</td></tr>
</table>
Pin8 function selection
<table>
<tr><td>TEST_MODE0_EN</td><td>LD12 CRE0 [Bit6]</td><td>CR2A [Bit6]</td><td>Pin8</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>PWM_G</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DSRB#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP16</td></tr>
</table>
Pin9 function selection
<table>
<tr><td>CR2A [Bit6]</td><td>Pin9</td></tr>
<tr><td>0</td><td>RTSB#</td></tr>
<tr><td>1</td><td>GP15</td></tr>
</table>
Pin10 function selection
<table>
<tr><td>CR2A [Bit6]</td><td>Pin10</td></tr>
<tr><td>0</td><td>DTRB#</td></tr>
<tr><td>1</td><td>GP14</td></tr>
</table>
Pin11 function selection
<table>
<tr><td>TEST_MODE0_EN</td><td>CR27 [Bit2]</td><td>CR2A [Bit6]</td><td>Pin11</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>IRRX0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SINB</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP13</td></tr>
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Pin12 function selection
<table>
<tr><td>CR27 [Bit2]</td><td>CR2A [Bit6]</td><td>Pin12</td></tr>
<tr><td>1</td><td>x</td><td>IRTX0</td></tr>
<tr><td>0</td><td>0</td><td>SOUTB</td></tr>
<tr><td>0</td><td>1</td><td>GP12</td></tr>
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<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R / W</td><td>
Pin13 function selection
<table>
<tr><th>TEST_MODE0_EN</th><th>LD12 CRE0 [Bit5]</th><th>CR2A [Bit6]</th><th>Pin13</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>PWM_B</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DCDB#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP11</td></tr>
</table>
Pin14 function selection
<table>
<tr><th>TEST_MODE0_EN</th><th>CR2A [Bit6]</th><th>Pin14</th></tr>
<tr><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>RIB#</td></tr>
<tr><td>0</td><td>1</td><td>GP10</td></tr>
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</td></tr>
<tr><td>5</td><td>R / W</td><td>
Pin69 function selection
<table>
<tr><th>CR2A [Bit5]</th><th>Pin69</th></tr>
<tr><td>0</td><td>GP70</td></tr>
<tr><td>1</td><td>Tri-state</td></tr>
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<tr><td>4</td><td>R / W</td><td>
Pin92 function selection
<table>
<tr><th>DSW_EN</th><th>LD12 CRED [Bit4]</th><th>CR2A [Bit4]</th><th>Pin92</th></tr>
<tr><td>1</td><td>0</td><td>x</td><td>5VDUAL</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>GP51</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>AUXFANIN3</td></tr>
<tr><td>0</td><td>x</td><td>0</td><td>GP51</td></tr>
<tr><td>0</td><td>x</td><td>1</td><td>AUXFANIN3</td></tr>
</table>
</td></tr>
<tr><td>3</td><td>R / W</td><td>
Pin90 function selection
<table>
<tr><th>DSW_EN</th><th>LD12 CRED [Bit2]</th><th>CR2A [Bit3]</th><th>Pin90</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>SUSWARN_5VDUAL</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>FDLED2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>GP53</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>AUXFANOUT3</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>FDLED2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>GP53</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>AUXFANOUT3</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>2</td><td>R/W</td><td>Enable Over Temperature shutdown Protection (OVT#)
= 0 The thermal shutdown function is disabled. (Default)
= 1 Enable thermal shutdown function.
(If set this bit to 1, the relative registers of OVT# event are:
Bank0, CR18 ,Bit6 → SMIOVT1 OVT# (Default SYSTIN)
Bank0, CR4C ,Bit4 → SMIOVT3 OVT# (Default AUXTIN0)
Bank0, CR4C ,Bit3 → SMIOVT2 OVT# (Default CPUTIN)
If current temperature exceeds high-limit setting, OVT# event will be triggered and PSON# will inactive immediately.)</td></tr>
<tr><td>1</td><td>R / W</td><td>Pin56 function selection
<table>
<tr><td>LD12 CREB [Bit2]</td><td>CR2A [Bit1]</td><td>Pin56</td></tr>
<tr><td>0</td><td>0</td><td>MCLK</td></tr>
<tr><td>0</td><td>1</td><td>GP23</td></tr>
<tr><td>1</td><td>x</td><td>AUXFANOUT3</td></tr>
</table>
Pin57 function selection
<table>
<tr><td>LD12 CREB [Bit3]</td><td>CR2A [Bit1]</td><td>Pin57</td></tr>
<tr><td>0</td><td>0</td><td>MDAT</td></tr>
<tr><td>0</td><td>1</td><td>GP22</td></tr>
<tr><td>1</td><td>x</td><td>AUXFANIN3</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin58 function selection
<table>
<tr><td>LD12 CREB [Bit4]</td><td>CR2A [Bit0]</td><td>Pin58</td></tr>
<tr><td>0</td><td>0</td><td>KCLK</td></tr>
<tr><td>0</td><td>1</td><td>GP21</td></tr>
<tr><td>1</td><td>0</td><td>AUXFANOUT2</td></tr>
<tr><td>1</td><td>1</td><td>CIRRX</td></tr>
</table>
Pin59 function selection
<table>
<tr><td>LD12 CREB [Bit5]</td><td>CR2A [Bit0]</td><td>Pin59</td></tr>
<tr><td>0</td><td>0</td><td>KDAT</td></tr>
<tr><td>0</td><td>1</td><td>GP20</td></tr>
<tr><td>1</td><td>x</td><td>AUXFANIN2</td></tr>
</table></td></tr>
</table>

CR 2Bh.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td>R / W</td><td>Pin77 function selection
<table>
<tr><td>CR2B [Bit7-6]</td><td>Pin77</td></tr>
<tr><td>00</td><td>RSTOUT2#</td></tr>
<tr><td>01</td><td>GP76</td></tr>
<tr><td>10</td><td>MLED</td></tr>
<tr><td>11</td><td>RESERVE</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>R / W</td><td>Pin78 function selection
<table>
<tr><td>CR2B [Bit5-4]</td><td>Pin78</td></tr>
<tr><td>00</td><td>RSTOUT1#</td></tr>
<tr><td>01</td><td>GP75</td></tr>
<tr><td>10</td><td>Tri-state</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin79 function selection
<table>
<tr><td>CR2B [Bit3]</td><td>Pin79</td></tr>
<tr><td>0</td><td>RSTOUT0#</td></tr>
<tr><td>1</td><td>GP74</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin67 function selection
<table>
<tr><td>CR2B [Bit2]</td><td>Pin67</td></tr>
<tr><td>0</td><td>AUXFANIN4</td></tr>
<tr><td>1</td><td>GP72</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>R / W</td><td>Pin68 function selection
<table>
<tr><td>UARTB_P80_EN</td><td>LDD CRE1[Bit1]</td><td>CR2B [Bit1-0]</td><td>Pin68</td></tr>
<tr><td>0</td><td>0</td><td>00</td><td>GP71</td></tr>
<tr><td>0</td><td>1</td><td>00</td><td>RESERVE</td></tr>
<tr><td>1</td><td>x</td><td>00</td><td>SOUTB_P80</td></tr>
<tr><td>x</td><td>x</td><td>01</td><td>GP71</td></tr>
<tr><td>x</td><td>x</td><td>11</td><td>Tri-state</td></tr>
</table></td></tr>
</table>

CR 2Ch.

Attribute: Read/Write

Power Well: VSB, VRTC(Bit0)

Reset by: RSMRST#, Battery reset(Bit0)

Default : 01h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td colspan="2">Reserved.</td></tr>
<tr><td>6-5</td><td>R / W</td><td>Pin71 function selection
<table>
<tr><td>CR2C [Bit6-5]</td><td>Pin71</td></tr>
<tr><td>00</td><td>3VSBSW#</td></tr>
<tr><td>01</td><td>GP33</td></tr>
<tr><td>10</td><td>Tri-state</td></tr>
<tr><td>11</td><td>3VSBSW#</td></tr>
</table></td></tr>
<tr><td>4-3</td><td>R / W</td><td>Pin98 function selection
<table>
<tr><td>CR2C [Bit4-3]</td><td>Pin98</td></tr>
<tr><td>00</td><td>GP27</td></tr>
<tr><td>01</td><td>RESERVE</td></tr>
<tr><td>11</td><td>RESERVE</td></tr>
<tr><td>10</td><td>MLED</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin65 function selection
<table>
<tr><td>CR2C [Bit2]</td><td>Pin65</td></tr>
<tr><td>0</td><td>THERMTRIP#_IN</td></tr>
<tr><td>1</td><td>PME#</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin119 function selection
<table>
<tr><td>LDD CRE1 [Bit3]</td><td>CR2C [Bit1]</td><td>CR2C [Bit0]</td><td>Pin119</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>TSIC</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP26</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>RESERVE</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin119 function selection
<table>
<tr><td>LDD CRE1 [Bit3]</td><td>CR2C [Bit1]</td><td>CR2C [Bit0]</td><td>Pin119</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>TSIC</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP26</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>RESERVE</td></tr>
</table>
Pin121 function selection
<table>
<tr><td>CR2C [Bit0]</td><td>Pin121</td></tr>
<tr><td>0</td><td>PECI</td></tr>
<tr><td>1</td><td>TSID</td></tr>
</table></td></tr>
</table>

CR 2Dh.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#(Bit6), RSMRST#(Bit7, Bit5, Bit0)

Default : 0ss0_0000b

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin87 function Selection
<table>
<tr><th>DDR4_EN</th><th>CR2D [Bit7]</th><th>Pin87</th></tr>
<tr><td>0</td><td>0</td><td>GP56</td></tr>
<tr><td>1</td><td>0</td><td>VDDQ_EN</td></tr>
<tr><td>x</td><td>1</td><td>AUXFANOUT2</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>STRP_KEY_LOCK Strapping result reading</td></tr>
<tr><td>5</td><td>R / W</td><td>ESPI_EN Strapping result reading</td></tr>
<tr><td>4-0</td><td colspan="2">Reserved</td></tr>
<tr><td>0</td><td>R / W</td><td>0: RSTWDT_EN is inactive
1: RSTWDT_EN is active</td></tr>
</table>

CR 2Fh. Strapping Function Result

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#(Bit5-2), LRESET#(Bit7-6), PWROK(Bit1)

Default : ssss_sss0b

BIT	READ / WRITE	DESCRIPTION
7	R / W	UARTB_P80_EN Strapping result reading
6	R / W	UARTA_P80_EN Strapping result reading
5	R / W	TEST_MODE0_EN Strapping result reading
4	R / W	DDR4_EN Strapping result reading
3	R / W	DSW_EN Strapping result reading
2	Reserved	
1	R / W	P80_EN Strapping result reading
0	Reserved	

Note . All Strapping results can be programming by LPC Interface. There are three conditions below:

4) VSB Strapping result can be programming by LPC, and reset by RSMRST#
5) VCC Strapping result can be programming by LPC, and reset by PWROK
6) LRESET Strapping (2E_4E_SEL) : No change

24.2 Logical Device 1

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: The PRT logical device is inactive. 1: The PRT logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 03h, 78h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select PRT I/O base address. <100h: FFCh> on 4 bytes boundary (EPP not supported) or <100h: FF8h> on 8 bytes boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR 70h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 07h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for PRT.

CR 74h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2-0	R / W	These bits select DRQ resource for PRT. 000: DMA0. 001: DMA1. 010: DMA2. 011: DMA3. 1xx: No DMA active.

CR F0h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 3Fh

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-3	R / W	ECP FIFO Threshold.
2-0	R / W	Parallel Port Mode selection (CR28 bit2 PRTMODS2 = 0). **Bits** **2 1 0** 0 0 0: Standard and Bi-direction (SPP) mode. 0 0 1: EPP – 1.9 and SPP mode. 0 1 0: ECP mode. 0 1 1: ECP and EPP – 1.9 mode. 1 0 0: Printer Mode. 1 0 1: EPP – 1.7 and SPP mode. 1 1 0: Reserved 1 1 1: ECP and EPP – 1.7 mode.

24.3 Logical Device 2

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: The UARTA logical device is inactive. 1: The UARTA logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 03h, F8h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select Serial Port 1 I/O base address <100h: FF8h> on 8 bytes boundary.

CR 70h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for Serial Port 1.

CR F0h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5-2	Reserved	

BIT	READ / WRITE	DESCRIPTION
1-0	R / W	**Bits** **1 0** 0 0: UART A clock source is 1.8462 MHz (24 MHz / 13). 0 1: UART A clock source is 2 MHz (24 MHz / 12). 1 0: UART A clock source is 24 MHz (24 MHz / 1). 1 1: UART A clock source is 14.769 MHz (24 MHz / 1.625).

CR F2h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**UARTA_RS485_enable** 0: Disable RS485 auto flow control function for UARTA 1: Enable RS485 auto flow control function for UARTA
6	R / W	**UARTA_RS485_inv_sel** (Available only when CRF2_Bit7=1) 0: Do not invert the behavior of RTSA# pin for RS485 auto flow control. 1: Invert the behavior of RTSA# pin for RS485 auto flow control.
5-0	Reserved	

24.4 Logical Device 3

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: The UARTB logical device is inactive. 1: The UARTB logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 02h, F8h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select IR I/O base address <100h: FF8h> on eight-byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 03h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for IR.

CR F0h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	0: IRQ is the level mode. 1: IRQ is the pulse mode for IRQ sharing function.
5-2	Reserved	

BIT	READ / WRITE	DESCRIPTION
1-0	R / W	**Bits** **1 0** 0 0: IR clock source is 1.8462 MHz (24 MHz / 13). 0 1: IR clock source is 2 MHz (24 MHz / 12). 1 0: IR clock source is 24 MHz (24 MHz / 1). 1 1: IR clock source is 14.769 MHz (24 MHz / 1.625).

CR F1h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	IRLOCSEL => IR I/O pins' location selection. 0: Reserved 1: Through IRRX / IRTX.
5-3	R / W	IRMODE => IR function mode selection. See the table below.
2	R / W	IR half / full duplex function selection. 0: IR function is Full Duplex. 1: IR function is Half Duplex.
1	R / W	0: IRTX pin of IR function in normal condition. 1: Inverse IRTX pin of IR function.
0	R / W	0: IRRX pin of IR function in normal condition. 1: Inverse IRRX pin of IR function.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	Tri-state	High
010*	IrDA	Active pulse 1.6 μS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	Routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

CR F2h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**UARTB_RS485_enable** 0: Disable RS485 auto flow control function for UARTB 1: Enable RS485 auto flow control function for UARTB
6	R / W	**UARTB_RS485_inv_sel** (Available only when CRF2_Bit7=1) 0: Do not invert the behavior of RTSB# pin for RS485 auto flow control. 1: Invert the behavior of RTSB# pin for RS485 auto flow control.
5-0	Reserved	

24.5 Logical Device 5

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: The KBC logical device is inactive. 1: The KBC logical device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the first KBC I/O base address <100h: FFFh> on 1-byte boundary.

CR 62h, 63h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the second KBC I/O base address <100h: FFFh> on 1 byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for KINT. (Keyboard interrupt)

CR 72h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for MINT. (PS/2 Mouse interrupt)

CR F0h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 43h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	KBC clock rate selection **Bits** **7 6** 0 0: Reserved 0 1: 8MHz 1 0: Reserved 1 1: Reserved
5-3	Reserved	
2	R / W	0: Port 92 disabled. 1: Port 92 enabled.
1	R / W	0: Gate A20 software control. 1: Gate A20 hardware speed up.
0	R / W	0: KBRST# software control. 1: KBRST# hardware speed up.

24.6 Logical Device 6

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: CIR Interface is inactive. 1: CIR Interface is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for CIR.

24.7 Logical Device 7

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION	
7-3	Reserved		
2	R / W	0: GPIO8 is inactive.	1: GPIO8 is active.
1	R / W	0: GPIO7 is inactive.	1: GPIO7 is active.
0	R / W	0: GPIO6 is inactive.	1: GPIO6 is active.

CR E0h. GPIO7 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO7 I/O register 0: The respective GPIO7 PIN is programmed as an output port 1: The respective GPIO7 PIN is programmed as an input port.

CR E1h. GPIO7 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO7 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. GPIO7 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO7 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. GPIO7 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO7 Event Status Bit 7-0 corresponds to GP77-GP70, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR E4h. GPIO8 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 I/O register 0: The respective GPIO8 PIN is programmed as an output port 1: The respective GPIO8 PIN is programmed as an input port.

CR E5h. GPIO8 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E6h. GPIO8 Inversion Registe

Attribute: Read/Write
Power Well: VSB
Reset by: GP8X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO8 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E7h. GPIO8 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP8X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO8 Event Status Bit 7-0 corresponds to GP87-GP80, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR ECh. GPIO7 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO77 1: GPIO77 → MLED (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO76 1: GPIO76 → MLED (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO75 1: GPIO75 → BEEP (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO74 1: GPIO74 → GRN (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO73 1: GPIO73 → WDT1 (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO72 1: GPIO72 → SMI (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO71 1: GPIO71 → BEEP (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO70 1: GPIO70 → GRN (Please also set this GPIO to “output” type.)

CR EDh. GPIO8 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB

Reset by: GP8X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO87 1: GPIO87 → YLW
6	R / W	0: GPIO86 1: GPIO86 → BEEP
5	R / W	0: GPIO85 1: GPIO85 → SMI
4	R / W	0: GPIO84 1: GPIO84 → GRN
3	R / W	0: GPIO83 1: GPIO83 → YLW
2	R / W	0: GPIO82 1: GPIO82 → BEEP
1	R / W	0: GPIO81 1: GPIO81 → YLW
0	R / W	0: GPIO80 1: GPIO80 → WDT1

CR F4h. GPIO6 I/O Register
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 I/O register 0: The respective GPIO6 PIN is programmed as an output port 1: The respective GPIO6 PIN is programmed as an input port.

CR F5h. GPIO6 Data Register
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F6h. GPIO6 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO6 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F7h. GPIO6 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO6 Event Status Bit 7-0 corresponds to GP67-GP60, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR F8h. GPIO6 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO67 1: GPIO67 → MLED (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO66 1: GPIO66 → BEEP (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO65 1: GPIO65 → SMI (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO64 1: GPIO64 → WDT1 (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO63 1: GPIO63 → MLED (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO62 1: GPIO62 → BEEP (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO61 1: GPIO61 → SMI (Please also set this GPIO to “output” type.)

BIT	READ / WRITE	DESCRIPTION
0	R / W	0: GPIO60 1: GPIO60 → WDT1 (Please also set this GPIO to “output” type.)

24.8 Logical Device 8

CR 30h.

Attribute: Read/Write
Power Well: VSB, VSB
Reset by: LRESET#, RSMRST# (Bit7)
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO1 is inactive. 1: GPIO1 is active.
6-5	Reserved	
4	R / W	0: WDT3 is inactive. 1: WDT3 is active.
3	R / W	0: GPIO Base Address mode is inactive 1: GPIO Base Address mode is active
2	Reserved	
1	R / W	0: GPIO0 is inactive. 1: GPIO0 is active.
0	R / W	0: WDT1 is inactive. 1: WDT1 is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select GPIO Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR E0h. GPIO0 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 I/O register 0: The respective GPIO0 PIN is programmed as an output port 1: The respective GPIO0 PIN is programmed as an input port.

CR E1h. GPIO0 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR E2h. GPIO0 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO0 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR E3h. GPIO0 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO0 Event Status Bit 7-0 corresponds to GP07-GP00, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR E4h. GPIO0 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO07 1: GPIO07 → MLED (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO06 1: GPIO06 → BEEP (Please also set this GPIO to “output” type.)

BIT	READ / WRITE	DESCRIPTION
5	R / W	0: GPIO05 1: GPIO05 → SMI (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO04 1: GPIO04 → WDT1 (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO03 1: GPIO03 → MLED (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO02 1: GPIO02 → BEEP (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO01 1: GPIO01 → SMI (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO00 1: GPIO00 → WDT1 (Please also set this GPIO to “output” type.)

CR F0h. GPIO1 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 I/O register 0: The respective GPIO1 PIN is programmed as an output port 1: The respective GPIO1 PIN is programmed as an input port.

CR F1h. GPIO1 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Data register For output ports, the respective bits can be read/written and produced to pins.
	Read Only	For input ports, the respective bits can be read only from pins. Write accesses will be ignored.

CR F2h. GPIO1 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO1 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Both Input & Output ports)

CR F3h. GPIO1 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO1 Event Status Bit 7-0 corresponds to GP17-GP10, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR F4h. GPIO1 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO17 1: GPIO17 → YLW (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO16 1: GPIO16 → GRN (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO15 1: GPIO15 → YLW (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO14 1: GPIO14 → GRN (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO13 1: GPIO13 → YLW (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO12 1: GPIO12 → GRN (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO11 1: GPIO11 → YLW (Please also set this GPIO to “output” type.)

BIT	READ / WRITE	DESCRIPTION
0	R / W	0: GPIO10 1: GPIO10 → GRN (Please also set this GPIO to “output” type.)

CR F5h. Watchdog Timer 1(WDT1) and KBC P20 Control Mode Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CRE7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W Write “1” Only	Disable / Enabel RESETCONO# One Shooting bit. This bit is self-clearing. 0: Disable 1: Enable
4	R / W	Watchdog Timer 1 count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is 0, the count mode is 1/1000 seconds mode.) (If bit-3 is 1, the count mode is 1/1000 minutes mode.)
3	R / W	Select Watchdog Timer 1 count mode. 0: Second Mode. 1: Minute Mode.
2	Reversed	
1	R / W	Disable / Enable the Watchdog Timer 1 output low pulse to the KBRST# pin 0: Disable. 1: Enable.
0	R / W	Pulse or Level mode select 0: Pulse mode 1: Level mode

CR F6h. Watchdog Timer 1(WDT1) Counter Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CRE7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watch Dog Timer I Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watch Dog Counter and start counting down. The accuracy of watchgdog timer 1 about oen cycle deviation. If CR F7h, bits 7 and 6 are set, any Mouse Interrupt or Keyboard Interrupt event causes the previously-loaded, non-zero value to be reloaded to the Watch Dog Counter and the count down resumes. Reading this register returns the current value in the Watch Dog Counter, not the Watch Dog Timer Time-out value. 00h: Time-out Disable 01h: Time-out occurs after one cycle time, the cycle time is base on LD8 CRF5, bit[3], by analogy.

CR F7h. Watchdog Timer 1(WDT1) Control & Status Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CRE7[3])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mouse interrupt reset enables watch-dog timer reload 0: Watchdog Timer 1 is not affected by mouse interrupt. 1: Watchdog Timer 1 is reset by mouse interrupt.
6	R / W	Keyboard interrupt reset enables watch-dog timer reload 0: Watchdog Timer 1 is not affected by keyboard interrupt. 1: Watchdog Timer 1 is reset by keyboard interrupt.
5	Write “1” Only	Trigger Watchdog Timer 1 event. This bit is self-clearing.
4	R / W Write “0” Clear	Watchdog Timer 1 status bit 0: Watchdog Timer 1 is running. 1: Watchdog Timer 1 issues time-out event.
3-0	R / W	These bits select the IRQ resource for the Watchdog Timer 1

CR F8h. Watchdog Timer 3(WDT3) Control Mode Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CREE[2])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	

BIT	READ / WRITE	DESCRIPTION
4	R / W	Watchdog Timer 3 count mode is 1000 times faster. 0: Disable. 1: Enable. (If bit-3 is 0, the count mode is 1/1000 seconds mode.) (If bit-3 is 1, the count mode is 1/1000 minutes mode.)
3	R / W	Select Watchdog Timer 3 count mode. 0: Second Mode. 1: Minute Mode.
2-1	Reserved	
0	R / W	Pulse or Level mode select 0: Pulse mode 1: Level mode

CR F9h. Watchdog Timer 3(WDT3) Counter Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CREE[2])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Watchdog Timer 3 Time-out value. Writing a non-zero value to this register causes the counter to load the value into the Watchdog Counter and start counting down. The accuracy of watchgdog timer 3 about oen cycle deviation. Reading this register returns the current value in the Watchdog Counter, not the Watchdog Timer 3 Time-out value. 00h: Time-out Disable 01h: Time-out occurs after one cycle time, the cycle time is base on LD8 CRF8, bit[3], by analogy.

CR FAh. Watchdog Timer 3(WDT3) Control & Status Register

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET# or PWROK(see LDA CREE[2])

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W Write “1” Only	Trigger Watchdog Timer 3 event. This bit is self-clearing.
4	R / W Write “0” Clear	Watchdog Timer 3 status bit 0: Watchdog Timer 3 is running. 1: Watchdog Timer 3 issues time-out event.
3-0	R / W	These bits select the IRQ resource for Watchdog Timer 3

CR FEh. Watchdog Timer 1(WDT1) Timeout Counter Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W Write “1” Clear	Watchdog Timer 1 Timeout Counter.

CR FFh. Watchdog Timer 3(WDT3) Timeout Counter Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W Write “1” Clear	Watchdog Timer 3 Timeout Counter.

24.9 Logical Device 9

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION	
7-4	Reserved		
3	R / W	0: GPIO5 is inactive.	1: GPIO5 is active
2	R / W	0: GPIO4 is inactive.	1: GPIO4 is active.
1	R / W	0: GPIO3 is inactive.	1: GPIO3 is active.
0	R / W	0: GPIO2 is inactive.	1: GPIO2 is active.

CR E0h. GPIO2 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 I/O register 0: The respective GPIO2 PIN is programmed as an output port 1: The respective GPIO2 PIN is programmed as an input port.

CR E1h. GPIO2 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E2h. GPIO2 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO2 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E3h. GPIO2 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO2 Event Status Bit 7-0 corresponds to GP27-GP20, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR E4h. GPIO3 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GPIO3 I/O register 0: The respective GPIO3 PIN is programmed as an output port 1: The respective GPIO3 PIN is programmed as an input port.

CR E5h. GPIO3 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	

BIT	READ / WRITE	DESCRIPTION
6-0	R / W	GPIO3 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR E6h. GPIO3 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GPIO3 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E7h. GPIO3 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP3X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	Read Only Read-Clear	GPIO3 Event Status Bit 6-0 corresponds to GP36-GP30, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR E9h. GPIO2 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO27 1: GPIO27 → GRN (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO26 1: GPIO26 → BEEP (Please also set this GPIO to “output” type.)

BIT	READ / WRITE	DESCRIPTION
5	R / W	0: GPIO25 1: GPIO25 → SMI (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO24 1: GPIO24 → MLED (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO23 1: GPIO23 → GRN (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO22 1: GPIO22 → YLW (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO21 1: GPIO21 → SMI (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO20 1: GPIO20 → WDT1 (Please also set this GPIO to “output” type.)

CR EAh. GPIO3 Multi-function Select Register

Attribute: Read/Write

Power Well: VSB

Reset by: GP3X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	0: GPIO36 1: GPIO36 → GRN (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO35 1: GPIO35 → BEEP (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO34 1: GPIO34 → SMI (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO33 1: GPIO33 → WDT1 (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO32 1: GPIO32 → GRN (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO31 1: GPIO31 → YLW (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO30 1: GPIO30 → WDT1 (Please also set this GPIO to “output” type.)

CR EBh. GPIO5 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO57 1: GPIO57 → YLW (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO56 1: GPIO56 → GRN (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO55 1: GPIO55 → SLPS5_Lch (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO54 1: GPIO54 →FDLED1 (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO53 1: GPIO53 → YLW (Please also set this GPIO to “output” type.)
2	R / W	0: GPIO52 1: GPIO52 → GRN (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO51 1: GPIO51 → YLW (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO50 1: GPIO50 → GRN (Please also set this GPIO to “output” type.)

CR F0h. GPIO4 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 I/O register 0: The respective GPIO4 PIN is programmed as an output port 1: The respective GPIO4 PIN is programmed as an input port.

CR F1h. GPIO4 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Data register For output ports, the respective bits can be read and written by the pins.

BIT	READ / WRITE	DESCRIPTION
	Read Only	For Input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR F2h. GPIO4 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO4 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR E8h. GPIO4 Status Register

Attribute: Read Only
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO4 Event Status Bit 7-0 corresponds to GP47-GP40, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

CR EEh. GPIO4 Multi-function Select Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: GPIO47 1: GPIO47 → BEEP (Please also set this GPIO to “output” type.)
6	R / W	0: GPIO46 1: GPIO46 → BEEP (Please also set this GPIO to “output” type.)
5	R / W	0: GPIO45 1: GPIO45 → SMI (Please also set this GPIO to “output” type.)
4	R / W	0: GPIO44 1: GPIO44 → WDT1 (Please also set this GPIO to “output” type.)
3	R / W	0: GPIO43 1: GPIO43 → YLW (Please also set this GPIO to “output” type.)

BIT	READ / WRITE	DESCRIPTION
2	R / W	0: GPIO42 1: GPIO42 → BEEP (Please also set this GPIO to “output” type.)
1	R / W	0: GPIO41 1: GPIO41 → SMI (Please also set this GPIO to “output” type.)
0	R / W	0: GPIO40 1: GPIO40 → WDT1 (Please also set this GPIO to “output” type.)

CR F4h. GPIO5 I/O Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 I/O register 0: The respective GPIO5 PIN is programmed as an output port 1: The respective GPIO5 PIN is programmed as an input port.

CR F5h. GPIO5 Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 Data register For output ports, the respective bits can be read and written by the pins.
	Read Only	For input ports, the respective bits can only be read by the pins. Write accesses are ignored.

CR F6h. GPIO5 Inversion Register

Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GPIO5 Inversion register 0: The respective bit and the port value are the same. 1: The respective bit and the port value are inverted. (Applies to both input and output ports)

CR F7h. GPIO5 Status Register

Attribute: Read Only

Power Well: VSB

Reset by: GP5X_MRST

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	Read Only Read-Clear	GPIO5 Event Status Bit 7-0 corresponds to GP57-GP50, respectively. 0 : No active edge has been detected 1 : An active edge has been detected Read the status bit clears it to 0.

24.10 Logical Device A

CR E0h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 01h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>DIS_PSIN => Disable the panel switch input to turn on the system power supply.
0: PSIN is wire-AND and connected to PSOUT#.
1: PSIN is blocked and cannot affect PSOUT#.</td></tr>
<tr><td>6</td><td>R / W</td><td>Enable KBC wake-up
0: Disable keyboard wake-up function via PSOUT#.
1: Enable keyboard wake-up function via PSOUT#.</td></tr>
<tr><td>5</td><td>R / W</td><td>Enable Mouse wake-up
0: Disable mouse wake-up function via PSOUT#.
1: Enable mouse wake-up function via PSOUT#.</td></tr>
<tr><td>4</td><td>R / W</td><td>MSRKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the following table for the details.
<table>
<tr><th>ENMDAT_UP</th><th>MSRKEY</th><th>MSXKEY</th><th>Wake-up event</th></tr>
<tr><td>1</td><td>x</td><td>1</td><td>Any button clicked or any movement.</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>One click of left or right button.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>One click of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>One click of the right button.</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Two clicks of the left button.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Two clicks of the right button.</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Enable CIR wake-up
0: Disable CIR wake-up function via PSOUT#.
1: Enable CIR wake-up function via PSOUT#.</td></tr>
<tr><td>2</td><td>R / W</td><td>Keyboard / Mouse swap enable
0: Normal mode.
1: Keyboard / Mouse ports are swapped.</td></tr>
<tr><td>1</td><td>R / W</td><td>MSXKEY =>
Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please check out the table in CRE0[4] for the detailed.</td></tr>
<tr><td>0</td><td>R / W</td><td>KBXKEY =>
0: Only the pre-determined key combination in sequence can wake up the system.
1: Any character received from the keyboard can wake up the system.</td></tr>
</table>

CR E1h. KBC Wake-Up Index Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up index register. This is the index register of CRE2, which is the access window for the keyboard's pre-determined key key-combination characters. The first set of wake-up keys is in of 0x00 – 0x0E, the second set 0x30 – 0x3E, and the third set 0x40 – 0x4E. Incoming key combinations can be read through 0x10 – 0x1E.

CR E2h. KBC Wake-Up Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Keyboard wake-up data register. This is the data register for the keyboard's pre-determined key-combination characters, which is indexed by CRE1.

CR E3h. Event Status Register

Attribute: Read Only
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4	Read Only Read-Clear	This status flag indicates VSB power off/on.
3	Read Only Read-Clear	Thermal shutdown status. 0: No thermal shutdown event issued. 1: Thermal shutdown event issued.
2	Read Only Read-Clear	PSIN_STS 0: No PSIN event issued. 1: PSIN event issued.
1	Read Only Read-Clear	MSWAKEUP_STS => The bit is latched by the mouse wake-up event. 0: No mouse wake-up event issued. 1: Mouse wake-up event issued.
0	Read Only Read-Clear	KBWAKEUP_STS => The bit is latched by the keyboard wake-up event. 0: No keyboard wake-up event issued. 1: Keyboard wake-up event issued.

CR E4h.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset, PWROK(Bit4), LRESET#(Bit3-2)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-5	R / W	Power-loss control [Note] (These two bits will determine the system turn on or off after AC resume, from G3 to S5 state.) **Bits** **6 5** 0 0: Always turn off. 0 1: Always turn on. (PSON# will active when S3# is high.) 1 0: Pre-state. (System turns On or Off which depends on the state before the power loss. Pease check the definition of the pre-state is "ON" or "OFF" in chapter 26.2.) 1 1: User defined mode for power loss last-state. (The last-state flag is located on "CRE6h, bit4.")
4	R / W	3VSBSW# enable bit 0: Disable. 1: Enable.
3	R / W	Keyboard wake-up options. 0: Password or sequence hot keys programmed in the registers. 1: Any key.
2	R / W	Enable the hunting mode for wake-up events set in CRE0. This bit is cleared when any wake-up event is captured. (Note. This bit is use for KB and MS to generate PSOUT# while VCC valid, for example, wake-up from S1 to S0 via PSOUT#.) 0: Disable.(Default) 1: Enable.
1-0	Reserved	

Note. Whether "Always turn on", "Pre-state" or "User defined mode", the PSON#'s active condition for system to turn-on is S3# goes high. For south-bridge which S3# default is low while AC resume, please refer "CRE7h, bit4" to achieve the power-loss control application.

CR E5h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 02h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	GP8X_MRST 0: GP8X reset by RSMRST#. (Default) 1: GP8X reset by SLPS5.

BIT	READ / WRITE	DESCRIPTION
4	R / W	GP7X_MRST 0: GP7X reset by RSMRST#. (Default) 1: GP7X reset by SLPS5.
3	R / W	GP6X_MRST 0: GP6X reset by RSMRST#. (Default) 1: GP6X reset by SLPS5.
2	R / W	RESETCONO# signal to control PWROK 0: Disable (Default) 1: Enable
1	R / W	Route to PWROK source selection. 0: PSON#. 1: SLP_S3#. (Default)
0	R / W	ATXPGD signal to control PWROK 0: Enable. (Default) 1: Disable.

CR E6h.

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#(Bit7, Bit5, Bit3-1), Battery reset(Bit6, Bit4)

Default : 1Ah

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENMDAT => Three keys (ENMDAT_UP, CRE6[7]; MSRKEY, CRE0[4]; MSXKEY, CRE0[1]) define the combinations of the mouse wake-up events. Please see the table in CRE0, bit 4 for the details.
6	Read Only	SKTOCC# Status. This bit is '1' when SKTOCC# = 1.
5	R / W	CASEOPEN0 Clear Control. Write 1 to this bit to clear CASEOPEN0 status. This bit will clear the status itself.
4	R / W	Power-loss Last State Flag. 0: ON 1: OFF. (Default)

BIT	READ / WRITE	DESCRIPTION
3-1	R / W	PWROK_DEL Set the delay time when rising from 3VCC to PWROK **Bits** **3 2 1** 0 0 0: 50mS 0 0 1: 100mS 0 1 0: 150mS 0 1 1: 200mS 1 0 0: 250mS 1 0 1: 300mS (Default) 1 1 0: 500mS 1 1 1: 700mS
0	Reserved	

CR E7h.

Attribute: Read/Write

Power Well: VRTC

Reset by: RSMRST#(Bit7-5, Bit3), Battery reset(Bit4, Bit1-0)

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	ENKD3 => Enable the third set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 40h to 4eh. 0: Disable the third set of the key combinations. 1: Enable the third set of the key combinations.
6	R / W	ENKD2 => Enable the second set of keyboard wake-up key combination. Its values are accessed through keyboard wake-up index register (CRE1) and keyboard wake-up data register (CRE2) at the index from 30h to 3eh. 0: Disable the second set of the key combinations. 1: Enable the second set of the key combinations.
5	R / W	ENWIN98KEY => Enable Win98 keyboard dedicated key to wake-up system via PSOUT# when keyboard wake-up function is enabled. 0: Disable Win98 keyboard wake-up. 1: Enable Win98 keyboard wake-up.
4	R / W	EN_ONPSOUT **(VBAT)** Disable/Enable to issue a 0.5s delay PSOUT# level when system returns from power loss state and is supposed to be on as described in CRE4[6:5], logic device A. (For southbridge which S3# default is low when AC resume, like VIA …etc.) 0: Disable. (Default) 1: Enable.

BIT	READ / WRITE	DESCRIPTION
3	R / W	Select Watchdog Timer 1 Reset Source 0: Watchdog timer 1 is reset by LRESET#. 1: Watchdog timer 1 is reset by PWROK.
2	Reserved	
1	R / W	SKTOCC# Clear Control. Write 1 to this bit to clear SKTOCC# status. This bit will clear the status itself.
0	R / W	Hardware Monitor RESET source select 0: PWROK or internal PWROK (LDA CRED[3]). 1: LRESET#.

CR E9h. GPIOs Reset Source Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	GP5X_MRST 0: GP5X reset by RSMRST#. 1: GP5X reset by SLPS5.
4	R / W	GP4X_MRST 0: GP4X reset by RSMRST#. 1: GP4X reset by SLPS5.
3	R / W	GP3X_MRST 0: GP3X reset by RSMRST#. 1: GP3X reset by SLPS5.
2	R / W	GP2X_MRST 0: GP2X reset by RSMRST#. 1: GP2X reset by SLPS5.
1	R / W	GP1X_MRST 0: GP1X reset by RSMRST#. 1: GP1X reset by SLPS5.
0	R / W	GP0X_MRST 0: GP0X reset by LRESET#. 1: GP0X reset by PWROK.

CR ECh. ACPI Control and Status Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R	PSIN real time Status
6-5	R / W	Select PSOUT Delay time from GPO (GP73) to PSOUT. 00: 1ms 01: 2ms 10: 3ms 11: 4ms
4	R / W	Enable PSOUT Delay function from GPO (GP73) to PSOUT. 0: Disable. 1: Enable.

BIT	READ / WRITE	DESCRIPTION
3	R / W	Auto clear PSOUT# to disconnect to PSIN# function select 0: Disable. Clear by RSMRST 1: Enable. Clear by PSIN rising and RSMRST
2	R / W1C	Block PSIN# event, when PSOUT blocking time and push PSIN. (write “1” clear, and clear by PWROK) 0: No PSIN# event. 1: Have PSINT# event.
1	R / W	Enable to disconnect PSIN to PSOUT 0: Disable , PSOUT will bypass PSIN. 1: Enable.
0	R / W1C	PSIN# 4 sec status when PSIN is low and SLPS3 is high. (write “1” clear) 0: No 4 sec power down event. 1: 4 sec power down event

CR EDh.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	PSIN# blocking time register from S5 to S0. 1bit for 0.5sec.. Min: 0.5sec Max: 8sec
3	R / W	Hardware monitor reset source select. 0: internal PWROK (no delay). 1: PWROK.
2-1	Reserved	
0	R / W	RSMRST reset source select. 0: VSB and PSOUT/PCHVSB 1: VSB and PSOUT/PCHVSB and Deep_S5_Ctrl

CR EEh.

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	RESCON Reset source selection. 0: LRESET_L 1: PWROK
6	R / W	RIA Wakeup Enable 0: Disable 1: Enable

BIT	READ / WRITE	DESCRIPTION
5	R / W	RIB Wakeup Enable 0: Disable 1: Enable
4-3	Reserved	
2	R / W	Watchdog Timer 3 Reset Source Selection 0: LRESET_L 1: PWROK
1	R / W	CASEOPEN polarity 0: None inverse CASEOPEN0/1 INPUT 1: Inverse CASEOPEN0/1 INPUT
0	R / W	CASEOPEN1 Clear Control. Write 1 to this bit to clear CASEOPEN1 status. This bit will clear the status itself.

CR F0h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-5	R / W	**Pin70** function selection LDA CRF0 [Bit7-5] / Pin70 000 / DEEP_S5_0 001 / 3VSBSW 010 / Tri-state 011 / ATXPGDO 1xx / PWROK
4	R / W	**Pin72** function selection LDA CRF0 [Bit4] / Pin72 0 / CASEOPEN1# 1 / DEEP_S5_1
3	Reserved	
2	R / W	SUSACK_L source select 0: Actice by 5VDUAL. 1: Active by 5VDUAL and SUS_WARN.
1	R / W	PSIN de-bounce 0: 62.4ms 1: 206ms
0	R / W	Keyboard Auto-Swap Detect Enable. 0: Disable 1: Enable

CR F2h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 5Eh

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W	Block SLP_S3# to PSON# 0: Disable 1: Enable
4	R / W	Enable RSTOUT2# function. 0: Disable RSTOUT2#. 1: Enable RSTOUT2#. (Default)
3	R / W	Enable RSTOUT1# function. 0: Disable RSTOUT1#. 1: Enable RSTOUT1#. (Default)
2	R / W	Enable RSTOUT0# function. 0: Disable RSTOUT0#. 1: Enable RSTOUT0#. (Default)
1	R / W	Enable S3# Debounce function. 0: Disable Debounce. 1: Enable Debounce.
0	R / W	EN_PME 0 : Disable PME. (Default) 1 : Enable PME.

CR F3h.
Attribute: Read/Write
Power Well: VSB
Reset by: WDT_L_RST(bit6), RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W Write “1” Clear	Watchdog Timer 4 status. When this bit is set to 1, it means timeout event occurs.
5	R / W-Clear	PME status of the Mouse event. Write 1 to clear this status.
4	R / W-Clear	PME status of the KBC event. Write 1 to clear this status.
3	R / W-Clear	PME status of the PRT IRQ event. Write 1 to clear this status.
2	Reserved	

BIT	READ / WRITE	DESCRIPTION
1	R / W-Clear	PME status of the URA IRQ event. Write 1 to clear this status.
0	R / W-Clear	PME status of the URB IRQ event. Write 1 to clear this status.

CR F4h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W-Clear	PME status of the GP41 event. Write 1 to clear this status.
6	R / W-Clear	PME status of the GP46 event. Write 1 to clear this status.
5	R / W-Clear	PME status of the GP31 event. Write 1 to clear this status.
4	R / W-Clear	PME status of the GP32 event. Write 1 to clear this status.
3	R / W-Clear	PME status of the HM IRQ event. Write 1 to clear this status.
2	R / W-Clear	PME status of the WDT1 event. Write 1 to clear this status.
1	R / W-Clear	PME status of the RIA event. Write 1 to clear this status.
0	R / W-Clear	PME status of the RIB event. Write 1 to clear this status.

CR F5h.

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3	R / W	Virtual 8048 Enable bit. This bit is used for KBC emulation without PS/2 keyborad and PS/2 mouse. When set “1” to auto response KBC command.
2-0	Reserved	

CR F6h.

Attribute: Read/Write

Power Well: VSB

Reset by: LRESET#(Bit7), RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable KB, MS interrupt of the KBC password event. 1: Enable KB, MS interrupt of the KBC password event.
6	Reserved	
5	R / W	0: Disable PME interrupt of the Mouse event. 1: Enable PME interrupt of the Mouse event.
4	R / W	0: Disable PME interrupt of the KBC event. 1: Enable PME interrupt of the KBC event.
3	R / W	0: Disable PME interrupt of the PRT IRQ event. 1: Enable PME interrupt of the PRT IRQ event.
2	Reserved	
1	R / W	0: Disable PME interrupt of the URA IRQ event. 1: Enable PME interrupt of the URA IRQ event.
0	R / W	0: Disable PME interrupt of the URB IRQ event. 1: Enable PME interrupt of the URB IRQ event.

CR F7h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : C0h

BIT	READ / WRITE	DESCRIPTION
7	R / W	RSTOUT2# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)
6	R / W	RSTOUT1# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)
5	R / W	PSIN_BLK_EN. When S5->S0 or S0->S5, SIO will filter PSIN# a specific time. 0: Disable 1: Enable
4	R / W	0: Disable PME interrupt of the CIRWAKEUP event. 1: Enable PME interrupt of the CIRWAKEUP event.
3	R / W	0: Disable PME interrupt of the HM event. 1: Enable PME interrupt of the HM event.
2	R / W	0: Disable PME interrupt of the WDT1 event. 1: Enable PME interrupt of the WDT1 event.
1	R / W	0: Disable PME interrupt of the RIA event. 1: Enable PME interrupt of the RIA event.
0	R / W	0: Disable PME interrupt of the RIB event. 1: Enable PME interrupt of the RIB event.

CR FCh.

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 80h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2	R / W	TIME_PWRD (Power Fault and ANTISURGE function) 00: 3us ~ 4us(LDA CRFC[2]=0), 20ms ~35ms(LDA CRFC[2]=1) 01: 1.5s ~ 2s 10: 93.75ms ~ 125ms (Default) 11: 187.5ms ~ 250ms
1-0	Reserved	

CR FEh. GP41, GP46, GP31 and GP32 Event Route Selection Register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable GP41 event route to PSOUT#. 1: Enable GP41 event route to PSOUT#.
6	R / W	0: Disable GP46 event route to PSOUT#. 1: Enable GP46 event route to PSOUT#.
5	R / W	0: Disable GP31 event route to PSOUT#. 1: Enable GP31 event route to PSOUT#.
4	R / W	0: Disable GP32 event route to PSOUT#. 1: Enable GP32 event route to PSOUT#.
3	R / W	0: Disable GP41 event route to PME#. 1: Enable GP41 event route to PME#.
2	R / W	0: Disable GP46 event route to PME#. 1: Enable GP46 event route to PME#.
1	R / W	0: Disable GP31 event route to PME#. 1: Enable GP31 event route to PME#.
0	R / W	0: Disable GP32 event route to PME#. 1: Enable GP32 event route to PME#.

24.11 Logical Device B

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: Hardware Monitor & SB-TSI device is inactive. 1: Hardware Monitor & SB-TSI device is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the HM base address <100h : FFEh> along a two-byte boundary.

CR 62h, 63h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the SB-TSI base address <100h : FFEh> along a two-byte boundary.

CR 64h, 65h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select the read-only HM base address <100h : FFEh> along a two-byte boundary.

CR 70h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select the IRQ resource for HM.

CR E0h. SYSFAN Duty Cycle Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 99h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	SYSFAN Duty Cycle Register

CR E1h. CPUFAN Duty Cycle Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 99h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	CPUFAN Duty Cycle Register

CR E2h. AUXFAN0 Duty Cycle Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 99h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN0 Duty Cycle Register

CR E3h. AUXFAN1 Duty Cycle Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 99h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN1 Duty Cycle Register

CR E4h. AUXFAN2 Duty Cycle Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 99h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN2 Duty Cycle Register

CR E5h. ANTISURGE Voltage Channel Confiugration Register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : A8h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	3VCC high / low limit voltage setting 00: UV -10%, OV +9.8% 01: UV -15%, OV +14.8% 10: UV -19.9%, OV +19.8% 11: UV -24.9%, OV + 24.1%
5-4	R / W	VIN0 high / low limit voltage setting 00: UV -9.9%, OV +9.6% 01: UV -15%, OV +14.7% 10: UV -20.1%, OV +19.8% 11: UV -25.2%, OV + 24.9%
3-2	R / W	VIN1 high / low limit voltage setting 00: UV -9.9%, OV +9.6% 01: UV -15%, OV +14.7% 10: UV -20.1%, OV +19.8% 11: UV -25.2%, OV + 24.9%
1	R / W	ANTISURGE Voltage Channel selection 0: VIN0 and VIN1 1: VIN2 and VIN3
0	Reserved	

CR E6h. Configuration Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#(Bit7, Bit4-0), WDT1&PWROK(Bit6)
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	CR2A Bit1-0 reset source selection 0: WDT1 & PWROK 1: RSMRST#

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>6</td><td>R / W</td><td>RESETCONI# and PSIN# input block
0: Enable
1: Disable</td></tr>
<tr><td>5</td><td colspan="2">Reserved</td></tr>
<tr><td>4</td><td>R / W</td><td>Block OVP/UVP detect signal by S5#.
0: Disable
1: Enable</td></tr>
<tr><td>3</td><td>R / W</td><td>Pin88 function selection
<table>
<tr><th>DSW_EN</th><th>LD12 CRED [Bit0]</th><th>LDD CRE1 [Bit2]</th><th>LDB CRE6 [Bit3]</th><th>Pin88</th></tr>
<tr><td>1</td><td>0</td><td>x</td><td>x</td><td>SLP_SUS_FET</td></tr>
<tr><td>1</td><td>1</td><td>x</td><td>0</td><td>GP55</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>GP55</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin93 function selection
<table>
<tr><th>LDE CRFA [Bit1]</th><th>DSW_EN</th><th>LD12 CRED [Bit5]</th><th>LDD CRE1 [Bit0]</th><th>LDB CRE6 [Bit2]</th><th>Pin93</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>VW_SUSWARN#</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>x</td><td>x</td><td>SUSWARN#</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>x</td><td>0</td><td>GP50</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>x</td><td>1</td><td>RSTOUT3#</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>0</td><td>0</td><td>GP50</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>0</td><td>1</td><td>RSTOUT3#</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin91 function selection
<table>
<tr><th>DSW_EN</th><th>LD12 CRED [Bit3]</th><th>LDD CRE1 [Bit0]</th><th>LDB CRE6 [Bit1]</th><th>Pin91</th></tr>
<tr><td>1</td><td>0</td><td>x</td><td>0</td><td>SUSACK#</td></tr>
<tr><td>1</td><td>0</td><td>x</td><td>1</td><td>GP52</td></tr>
<tr><td>1</td><td>1</td><td>x</td><td>0</td><td>FDLED3</td></tr>
<tr><td>1</td><td>1</td><td>x</td><td>1</td><td>RSTOUT4</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td>GP52</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>0</td><td>FDLED3</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>1</td><td>RSTOUT4#</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Block OVP/UVP detect signal by VCC or S3#.
0: VCC and S3#
1: VCC</td></tr>
</table>

CR E7h. AUXFAN3 Duty Cycle Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN3 Duty Cycle Register

CR EDh.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 81h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4	R / W	THERMTRIP Active Flag (write 1 clear) 0: No THERMTRIP event. 1: THERMTRIP Active event
3	R / W	THERMTRIP Deep S5 Enable 0: Disable. When THERMTRIP active at S0 state, system will go into S5 state. 1: Enable. When THERMTRIP active at S0 state, system will go into DeepS5 state.
2:0	Reserved	

CR F0h. FANIN De-bouncer Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#(Bit7), LRESET#(Bit6-1)
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	1: Enable AUXFANIN4 input de-bouncer. 0: Disable AUXFANIN4 input de-bouncer.
6	R / W	1: Enable AUXFANIN3 input de-bouncer. 0: Disable AUXFANIN3 input de-bouncer.
5	R / W	1: Enable AUXFANIN2 input de-bouncer. 0: Disable AUXFANIN2 input de-bouncer.
4	R / W	1: Enable AUXFANIN1 input de-bouncer. 0: Disable AUXFANIN1 input de-bouncer.
3	R / W	1: Enable AUXFANIN0 input de-bouncer. 0: Disable AUXFANIN0 input de-bouncer.

BIT	READ / WRITE	DESCRIPTION
2	R / W	1: Enable CPUFANIN input de-bouncer. 0: Disable CPUFANIN input de-bouncer.
1	R / W	1: Enable SYSFANIN input de-bouncer. 0: Disable SYSFANIN input de-bouncer.
0	Reserved	

CR F5h. SMBus de-bouncer Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: Disable debug port. 1: Enable debug port.
6-5	Reserved	
4	R / W	1: Enable Antisurge input de-bouncer. 0: Disable Antisurge input de-bouncer.
3	R / W	1: Enable SDA0 input de-bouncer. 0: Disable SDA0 input de-bouncer.
2	R / W	1: Enable SCL0 input de-bouncer. 0: Disable SCL0 input de-bouncer.
1	R / W	1: Enable SCL input de-bouncer 160ns. 0: Disable SCL input de-bouncer.
0	R / W	1: Enable SDA input de-bouncer 160ns. 0: Disable SDA input de-bouncer.

CR F6h. Deep S5 Front Panel Green & Yellow LED control register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	**Deep S5**_YLW_BLK_FREQ bits (This function affects by LDB CRF9 Bit 5) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: YLW_LED outputs 0.0625Hz. 0010: YLW_LED outputs 0.125Hz. 0011: YLW_LED outputs 0.25Hz. 0100: YLW_LED outputs 0.5Hz 0101: YLW_LED outputs 1Hz. 0110: YLW_LED outputs 2Hz. 0111: YLW_LED outputs low. 1XXX: Fading LED.
3-0	R / W	**Deep S5**_GRN_BLK_FREQ bits (This function affects by LDB CRF9 Bit 4) 0000: High-Z. (The output type of YLW_LED is open-drain.) (Default) 0001: GRN_LED outputs 0.0625Hz. 0010: GRN_LED outputs 0.125Hz. 0011: GRN_LED outputs 0.25Hz. 0100: GRN_LED outputs 0.5Hz 0101: GRN_LED outputs 1Hz. 0110: GRN_LED outputs 2Hz. 0111: GRN_LED outputs low. 1XXX: Fading LED.

CR F7h. Front Panel Green LED (GRN_LED) control register

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 87h

BIT	READ / WRITE	DESCRIPTION
7	R / W	**AUTO_EN** (Powered by VBAT , default = 1) 0: GRN_LED and YLW_LED are controlled by GRN_ LED_ RST or SLP_S3# and SLP_S5#. 1: GRN_LED is controlled by SLP_S3# and YLW_LED is controlled by SLP_S3# and SLP_S5#.
6	R / W	**GRN_LED_RST#** (Default= 0) 0: GRN_BLK_FREQ will be set to “0000” (High-Z) when into S3~S5 state. 1: GRN_BLK_FREQ will be kept when into S3~S5 state.
5	R / W	**GRN_LED_POL** 0: GRN_LED output is the same. (Default) 1: GRN_LED output is inverted.
4	Reserved	

BIT	READ / WRITE	DESCRIPTION
3-0	R / W	**GRN_BLK_FREQ** bits (The reset depends on bit6, GRN_LED_RST#) 0000: High-Z. (The output type of YLW_LED is open-drain.) 0001: GRN_LED outputs 0.0625Hz. 0010: GRN_LED outputs 0.125Hz. 0011: GRN_LED outputs 0.25Hz. 0100: GRN_LED outputs 0.5Hz 0101: GRN_LED outputs 1Hz. 0110: GRN_LED outputs 2Hz. 0111: GRN_LED outputs low. (Default) 1XXX: Fading LED.

CR F8h. Front Panel Yellow LED (YLW_LED) control register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 47h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	**YLW_LED_RST#** (Default =1) 0: YLW_BLK_FREQ will be set to “0000” (High-Z) when into S3~S5 state. 1: YLW_BLK_FREQ will be kept when into S3~S5 state.
5	R / W	**YLW_LED_POL** 0: YLW_LED output is the same. (Default) 1: YLW_LED output is inverted.
4	Reserved	
3-0	R / W	**YLW_BLK_FREQ** bits (The reset depends on bit6,YLW_LED_RST#) 0000: High-Z. (The output type of YLW_LED is open-drain.) 0001: YLW_LED outputs 0.0625Hz. 0010: YLW_LED outputs 0.125Hz. 0011: YLW_LED outputs 0.25Hz. 0100: YLW_LED outputs 0.5Hz 0101: YLW_LED outputs 1Hz. 0110: YLW_LED outputs 2Hz. 0111: YLW_LED outputs low. (Default) 1XXX: Fading LED.

CR F9h. Deep Sleep LED Eanble register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	RESERVE	
5	R / W	Deep S5_YLW_BLK_FREQ : 0: Depend on setting of CRF6h, bit7~4. 1: Always output high.
4	R / W	Deep S5_GRN_BLK_FREQ : 0: Depend on setting of CRF2h, bit3~0. 1: Always output high.
3	Reserved	
2-0	R / W	RSMRST# V1/V2 adjust register 000: normal V1/V2 001: -3% ~ -6% of normal 011: -6% ~ -9% of normal 111: -9% ~ -12% of normal

CR FAh.RESETCONO# and PWROK active Pulse width selection

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-2	R / W	RESETCONO# and PWROK active Pulse width selection 00:50ms ~ 60ms 01:100ms ~ 130ms 10:200ms ~ 260ms 11:200ms ~ 260ms
1-0	Reserved	

24.12 Logical Device D

CR E1h.

Attribute: Read/Write

Power Well: VSB

Reset by: PWROK (DEFAULT) OR LRESET# (LOGIC DEVICE A, CR[E7], BIT[0]=1)

Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>Reserved</td><td></td></tr>
<tr><td>6</td><td>R / W</td><td>
Pin54 function selection
<table>
<tr><th>LD12 CREC [Bit2]</th><th>CR27 [Bit4]</th><th>LDD CRE1 [Bit6]</th><th>Pin54</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>DGH1#</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP35</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>AFD#</td></tr>
</table>
Pin53 function selection
<table>
<tr><th>LD12 CREC [Bit2]</th><th>CR27 [Bit4]</th><th>LDD CRE1 [Bit6]</th><th>Pin53</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>DGL1#</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP36</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>ERR#</td></tr>
</table>
</td></tr>
<tr><td>5</td><td>R / W</td><td>
Pin55 function selection
<table>
<tr><th>CR27 [Bit4]</th><th>LDD CRE1 [Bit5]</th><th>Pin55</th></tr>
<tr><td>0</td><td>0</td><td>GP34</td></tr>
<tr><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>1</td><td>x</td><td>STB#</td></tr>
</table>
Pin38 function selection
<table>
<tr><th>CR27 [Bit4]</th><th>LDD CRE1 [Bit5]</th><th>Pin38</th></tr>
<tr><td>0</td><td>0</td><td>GP46</td></tr>
<tr><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>1</td><td>x</td><td>SLCT</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>R / W</td><td>
Pin40 function selection
<table>
<tr><th>CR27 [Bit4]</th><th>LDD CRE1 [Bit4]</th><th>CR1B [Bit6]</th><th>Pin40</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>BUSY</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP44</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GRN_LED</td></tr>
</table>
Pin39 function selection
<table>
<tr><th>CR27 [Bit4]</th><th>LDD CRE1 [Bit4]</th><th>CR1B [Bit6]</th><th>Pin39</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>PE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP45</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>YLW_LED</td></tr>
</table>
</td></tr>
<tr><td>3</td><td>R / W</td><td>
Pin119 function selection
<table>
<tr><th>LDD CRE1 [Bit3]</th><th>CR2C [Bit1]</th><th>CR2C [Bit0]</th><th>Pin119</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>TSIC</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>GP26</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>RESERVE</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>R / W</td><td>
Pin88 function selection
<table>
<tr><th>DSW_EN</th><th>LD12 CRED [Bit0]</th><th>LDD CRE1 [Bit2]</th><th>LDB CRE6 [Bit3]</th><th>Pin88</th></tr>
<tr><td>1</td><td>0</td><td>x</td><td>x</td><td>SLP_SUS_FET</td></tr>
<tr><td>1</td><td>1</td><td>x</td><td>0</td><td>GP55</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>GP55</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
</table>
Pin89 function selection
<table>
<tr><th>DSW_EN</th><th>LDD CRE1 [Bit2]</th><th>LD12 CRED [Bit1]</th><th>Pin89</th></tr>
<tr><td>0</td><td>0</td><td>x</td><td>GP54</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>SLP_SUS#</td></tr>
<tr><td>1</td><td>x</td><td>1</td><td>GP54</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>R / W</td><td>
Pin2 function selection
<table>
<tr><th>LDD CRE1[Bit1]</th><th>CR1C [Bit4-3]</th><th>Pin2</th></tr>
<tr><td>1</td><td>xx</td><td>RESERVE</td></tr>
<tr><td>0</td><td>00</td><td>GP03</td></tr>
</table>
Pin68 function selection
<table>
<tr><th>UARTB_P80_EN</th><th>LDD CRE1[Bit1]</th><th>CR2B [Bit1-0]</th><th>Pin68</th></tr>
<tr><td>0</td><td>0</td><td>00</td><td>GP71</td></tr>
<tr><td>0</td><td>1</td><td>00</td><td>RESERVE</td></tr>
<tr><td>1</td><td>x</td><td>00</td><td>SOUTB_P80</td></tr>
<tr><td>1</td><td>x</td><td>00</td><td>SOUTB_P80</td></tr>
<tr><td>x</td><td>x</td><td>01</td><td>GP71</td></tr>
<tr><td>x</td><td>x</td><td>10</td><td>SOUTB_P80</td></tr>
<tr><td>x</td><td>x</td><td>11</td><td>Tri-state</td></tr>
</table>
</td></tr>
<tr><td>0</td><td>R / W</td><td>
Pin91 function selection
<table>
<tr><th>DSW_EN</th><th>LD12 CRED [Bit3]</th><th>LDD CRE1 [Bit0]</th><th>LDB CRE6 [Bit1]</th><th>Pin91</th></tr>
<tr><td>1</td><td>0</td><td>x</td><td>0</td><td>SUSACK#</td></tr>
<tr><td>1</td><td>0</td><td>x</td><td>1</td><td>GP52</td></tr>
<tr><td>1</td><td>1</td><td>x</td><td>0</td><td>FDLED3</td></tr>
<tr><td>1</td><td>1</td><td>x</td><td>1</td><td>RSTOUT4</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td>GP52</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>0</td><td>FDLED3</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>1</td><td>RSTOUT4#</td></tr>
</table>
Pin93 function selection
<table>
<tr><th>LDE CRFA [Bit1]</th><th>DSW_EN</th><th>LD12 CRED [Bit5]</th><th>LDD CRE1 [Bit0]</th><th>LDB CRE6 [Bit2]</th><th>Pin93</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>VW_SUSWARN#</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>x</td><td>x</td><td>SUSWARN#</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>x</td><td>0</td><td>GP50</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>x</td><td>1</td><td>RSTOUT3#</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>0</td><td>0</td><td>GP50</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>0</td><td>1</td><td>RSTOUT3#</td></tr>
</table>
</td></tr>
</table>

CR E2h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1-0	R / W	**Pin103** function selection

CR1B [Bit3]	LDD CRE2 [Bit1-0]	Pin103
0	00	GP40
0	01	SMI#_2
0	1x	OVT#_2
1	xx	GP40

CR E3h. AUXFAN4 Duty Cycle Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	AUXFAN4 Duty Cycle Register

CR E7h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-5	Reserved	
4	R / W	RSTOUT0# Push-Pull/OD select 0: Open Drain 1: Push-Pull (Default)
3~0	Reserved	

CR F0h. Watchdog Timer Mask Register
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W	Mask Watchdog Timer 1 to affect PWROK, then enter Deep_S5 0: Mask enable. (WDT1 not affect PWROK) 1: Mask disable. (WDT1 default affect PWROK)
6	R / W	Mask Watchdog Timer 1 to affect RESETCONO# 0: Mask enable. (WDT1 not affect RESETCONO#) 1: Mask disable. (WDT1 default affect RESETCONO#)
5	R / W	DIS WAKEUP ESPI ESPI virtual wire WAKE# is controlled by SIO glue logic 0: Disable. 1: Enable.
4	R / W	Mask Watchdog Timer 3 to affect PWROK 0: Mask enable. (WDT3 not affect PWROK) 1: Mask disable. (WDT3 default affect PWROK)
3	R / W	Mask Watchdog Timer 3 to affect RESETCONO# 0: Mask enable. (WDT3 not affect RESETCONO#) 1: Mask disable. (WDT3 default affect RESETCONO#)
2-1	Reserved	
0	R / W	Mask Watchdog Timer 1 to affect RSMRST# 0: Mask enable. (WDT1 not affect RSMRST #) 1: Mask disable. (WDT1 default affect RSMRST#)

CR F3h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7~1	Reversed	
0	R	KBC Auto-Swap Detect Status. 0: Keyboard 1: Mouse

24.13 Logical Device E

CR 30h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	0: CIR Wake-up is inactive. 1: CIR Wake-up Interface is active.

CR 60h, 61h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h, 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	These two registers select CIR Wake-up Interface I/O base address <100h: FF8h> on 1 byte boundary.

CR 70h.

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	These bits select IRQ resource for CIR Wake-up.

CR F0h.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 02h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	OOB Destination Slave Address.

CR F1h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 1Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	OOB Source Slave Address.

CR F4h.
Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R / W	Read OOB Temperature Enable.
0	Reserved	

CR F6h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 17h

BIT	READ / WRITE	DESCRIPTION
7-3	R / W	OOB Power-ON Configuration [Bit7-3]
2	R / W	Core OOB Channel Enable. This Bit reflect in OOB Channel is ready. 0: Not Ready 1: Ready
1	R / W	Core Virtual Wire Channel Enable. This Bit reflect in Virtual Wire Channel is ready. 0: Not Ready 1: Ready
0	R / W	Core Peripheral Channel Enable. This Bit reflect in Peripheral Channel is ready. 0: Not Ready 1: Ready

CR F7h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 0Bh

BIT	READ / WRITE	DESCRIPTION
7-5	R / W	OOB Power-ON Configuration [Bit15-13]

BIT	READ / WRITE	DESCRIPTION
4-2	R / W	MAXFREQ (Maximum Frequency Supported) 000: 20MHz 001: 25MHz 010: 33MHz(Default) 011: 50MHz Others: Reserved
1-0	R / W	IO Mode Support. This field is reflected in IO Mode Support field of the Gerneral Purpose Capabilities Configurations register. 00: Single IO 01: Single and Dual IO 10: Single and Quad IO 11: Single, Dual and Quad IO

CR F8h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	OOB Power-ON Configuration [Bit23-16]

CR F9h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 07h

BIT	READ / WRITE	DESCRIPTION
7-3	R / W	OOB Power-ON Configuration [Bit31-27]
2	R / W	OOB Channel Support Control Bit. 0: OOB Channel is not support 1: OOB Channel is support
1	R / W	Virtual Wire Channel Support Control Bit. 0: Virtual Wire Channel is not support 1: Virtual Wire Channel is support
0	R / W	Peripheral Channel Support Control Bit. 0: Peripheral Channel is not support 1: Peripheral Channel is support

CR FAh.

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-3</td><td colspan="2">Reserved</td></tr>
<tr><td>2</td><td>R / W</td><td>ESPI S5/S4 SEL
If LDE CRFA [Bit0] = 1
0: Pin84 will drive SLP_S5# by espi internal signal
1: Pin84 will drive SLP_S4# by espi internal signal
If LDE CRFA [Bit0] = 0
This bit will be don’t care.</td></tr>
<tr><td>1</td><td>R / W</td><td>Pin93 function selection
<table>
<tr><th>LDE CRFA [Bit1]</th><th>DSW_EN</th><th>LD12 CRED [Bit5]</th><th>LDD CRE1 [Bit0]</th><th>LDB CRE6 [Bit2]</th><th>Pin93</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>VW_SUSWARN#</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>x</td><td>x</td><td>SUSWARN#</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>x</td><td>0</td><td>GP50</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>x</td><td>1</td><td>RSTOUT3#</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>0</td><td>0</td><td>GP50</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>0</td><td>1</td><td>RSTOUT3#</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>ESPI OUT SEL
0: Pin64, Pin84 will be input pin
1: Pin64, Pin84 will be output pin that drive by espi internal signal of SLP_S3# and SLP_S5#.</td></tr>
</table>

24.14 Logical Device F

CR E0h.

Attribute: Read/Write
Power Well: VSB
Reset by: GP1X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP1 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E1h.

Attribute: Read/Write
Power Well: VSB
Reset by: GP2X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP2 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E2h.

Attribute: Read/Write
Power Well: VSB
Reset by: GP3X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6-0	R / W	GP3 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E3h.

Attribute: Read/Write
Power Well: VSB
Reset by: GP4X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP4 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E4h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP5X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP5 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E5h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP6X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP6 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E6h.
Attribute: Read/Write
Power Well: VSB
Reset by: GP7X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP7 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E7h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP8 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR E9h.

Attribute: Read/Write
Power Well: VSB
Reset by: GP0X_MRST
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	GP0 Push-Pull/OD select 0:Push-Pull 1:Open Drain

CR F0h. I2C Control & Address Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 9Dh

BIT	READ / WRITE	DESCRIPTION
7	R / W	Enable I2C_Slave
6-0	R / W	I2C Address

CR F1h. I2C to 80PORT Control Register

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#, SLP_S5#(Bit2),
Default : 04h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R / W	80PORT Display 0: Enable 1: Disable
0	R / W	LPC or I2C to 80PORT switch

CR F2h. I2C to 80PORT Data Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	I2C to 80PORT Data

24.15 Logical Device 11

CR E0h.

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 08h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2	R / W	PSIN_4S_EN 0: Disable. When PSIN# low over 4 sec, system will go into S5 state 1: Enable. When PSIN# low over 3.8 sec, system will go into DeepS5 state
1	R / W	0: There is no relationship between SKTOCC# and PSON# 1: SKTOCC# releated to PSON#
0	R / W	**Pin100** function selection LD11_CRE0 [Bit0] / Pin100 0 / THERMTRIP#_IN 1 / CASEOPEN0#

CR E1h. GPIO, RI PSOUT Wake-Up Status Register

Attribute: Read/Write
Power Well: VRTC
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	R / W-Clear	PSOUT status of the GP41 event. Write 1 to clear this status.
6	R / W-Clear	PSOUT status of the GP46 event. Write 1 to clear this status.
5	R / W-Clear	PSOUT status of the GP31 event. Write 1 to clear this status.
4	R / W-Clear	PSOUT status of the GP32 event. Write 1 to clear this status.
3	R / W-Clear	PSOUT status of the RIA event. Write 1 to clear this status.
2	R / W-Clear	PSOUT status of the RIB event. Write 1 to clear this status.
1-0	Reserved.	

CR E2h. GPIO, RI PSOUT Wake-Up Control Register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R / W	GPIO and RI PSOUT Wake-Up Group Select. 0: GPIO 1: GPIO+RI
0	R / W	GPIO and RI PSOUT Wake-Up Mode Select 0: Sleep 1: Sleep+Deep

CR EEh. AVCC, VIN0, VIN1 Status Register

Attribute: Read/Write
Power Well: VRTC
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5	R / W-Clear	VIN1 status of the UV event. Write 1 to clear this status.
4	R / W-Clear	VIN1 status of the OV event. Write 1 to clear this status.
3	R / W-Clear	VIN0 status of the UV event. Write 1 to clear this status.
2	R / W-Clear	VIN0 status of the OV event. Write 1 to clear this status.
1	R / W-Clear	AVCC status of the UV event. Write 1 to clear this status.
0	R / W-Clear	AVCC status of the OV event. Write 1 to clear this status.

24.16 Logical Device 12

CR E0h.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>R / W</td><td>Pin7 function selection
<table>
<tr><th>TEST_MODE0_EN</th><th>LD12 CRE0 [Bit7]</th><th>CR2A [Bit6]</th><th>Pin7</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>CTSB#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP17</td></tr>
</table></td></tr>
<tr><td>6</td><td>R / W</td><td>Pin8 function selection
<table>
<tr><th>TEST_MODE0_EN</th><th>LD12 CRE0 [Bit6]</th><th>CR2A [Bit6]</th><th>Pin8</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DSRB#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP16</td></tr>
</table></td></tr>
<tr><td>5</td><td>R / W</td><td>Pin13 function selection
<table>
<tr><th>TEST_MODE0_EN</th><th>LD12 CRE0 [Bit5]</th><th>CR2A [Bit6]</th><th>Pin13</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DCDB#</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP11</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>Pin76 function selection
<table>
<tr><th>CR1B [Bit0]</th><th>LD12 CRE0[Bit4]</th><th>CR1A [Bit5]</th><th>Pin76</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>MSDA</td></tr>
<tr><td>0</td><td>1</td><td>X</td><td>AUXFANOUT2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SDA</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP31</td></tr>
</table></td></tr>
<tr><td>3</td><td>R / W</td><td>Pin75 function selection
<table>
<tr><th>CR1B [Bit0]</th><th>LD12 CRE0[Bit3]</th><th>CR1A [Bit4]</th><th>Pin75</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>MSCL</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>AUXFANIN2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>SCL</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>GP32</td></tr>
</table></td></tr>
<tr><td>2-0</td><td colspan="2">RESERVE</td></tr>
</table>

CR E4h. MLED & FDLED1 Control Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	FDLED1 Frequency 0000: always high 0001: always low 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 1/2 Hz 0110: 1/4 Hz 0111: 1/8 Hz 1xxx: fading led
3-0	R / W	MLED Frequency 0000: always high 0001: always low 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 1/2 Hz 0110: 1/4 Hz 0111: 1/8 Hz 1xxx: fading led

CR E5h. FDLED2 & FDLED3 Control Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	FDLED3 Frequency 0000: always high 0001: always low 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 1/2 Hz 0110: 1/4 Hz 0111: 1/8 Hz 1xxx: fading led

BIT	READ / WRITE	DESCRIPTION
3-0	R / W	FDLED2 Frequency 0000: always high 0001: always low 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 1/2 Hz 0110: 1/4 Hz 0111: 1/8 Hz 1xxx: fading led

CR E6h. FDLED4 Control Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	FDLED4 Frequency 0000: always high 0001: always low 0010: 4 Hz 0011: 2 Hz 0100: 1 Hz 0101: 1/2 Hz 0110: 1/4 Hz 0111: 1/8 Hz 1xxx: fading led

CR E7h. KBC Short Detection Register

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved.	
0	R / W	KBC Short Detection Enable. 0: Disable KBC Short Detection. 1: Enable KBC Short Detection.

CR EAh. PORT80 Control Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#, LRESET#(Bit3)
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved.	
1-0	R / W	Extend PSON time When system power off (S0->S3/S5), PSON# can keep high for a certain time to avoid power on signal coming immediately. 00: 0 sec 01: 2 sec 10: 3 sec 11: 4 sec

CR EBh.

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7	Reserved	
6	R / W	**Pin83** function selection LD12 CREB[Bit6] / CR1A [Bit7-6] / Pin83 1 / x / CIRRX 0 / 00 / RESETCONI# 0 / 01 / GP30 0 / 10 / OVT#_1 0 / 11 / SMI#_1
5	R / W	**Pin59** function selection LD12 CREB [Bit5] / CR2A [Bit0] / Pin59 0 / 0 / KDAT 0 / 1 / GP20 1 / x / AUXFANIN2
4	R / W	**Pin58** function selection LD12 CREB [Bit4] / CR2A [Bit0] / Pin58 0 / 0 / KCLK 0 / 1 / GP21 1 / 0 / AUXFANOUT2 1 / 1 / CIRRX

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>3</td><td>R / W</td><td>Pin57 function selection
<table>
<tr><td>LD12 CREB [Bit3]</td><td>CR2A [Bit1]</td><td>Pin57</td></tr>
<tr><td>0</td><td>0</td><td>MDAT</td></tr>
<tr><td>0</td><td>1</td><td>GP22</td></tr>
<tr><td>1</td><td>x</td><td>AUXFANIN3</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin56 function selection
<table>
<tr><td>LD12 CREB [Bit2]</td><td>CR2A [Bit1]</td><td>Pin56</td></tr>
<tr><td>0</td><td>0</td><td>MCLK</td></tr>
<tr><td>0</td><td>1</td><td>GP23</td></tr>
<tr><td>1</td><td>x</td><td>AUXFANOUT3</td></tr>
</table></td></tr>
<tr><td>1</td><td colspan="2">Reserved</td></tr>
<tr><td>0</td><td>R / W</td><td>Pin82 function selection
<table>
<tr><td>CR27 [Bit7]</td><td>LD12 CREB [Bit0]</td><td>Pin82</td></tr>
<tr><td>0</td><td>0</td><td>PWROK</td></tr>
<tr><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>1</td><td>x</td><td>FDLED1</td></tr>
</table></td></tr>
</table>

CR ECh.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#, LRESET#(Bit7-6)

Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-3</td><td colspan="2">Reserved</td></tr>
<tr><td>2</td><td>R / W</td><td>Pin54 function selection
<table>
<tr><td>LD12 CREC [Bit2]</td><td>CR27 [Bit4]</td><td>LDD CRE1 [Bit6]</td><td>Pin54</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>DGH1#</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP35</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>AFD#</td></tr>
</table>
Pin53 function selection
<table>
<tr><td>LD12 CREC [Bit2]</td><td>CR27 [Bit4]</td><td>LDD CRE1 [Bit6]</td><td>Pin53</td></tr>
<tr><td>1</td><td>x</td><td>x</td><td>DGL1#</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>GP36</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>ERR#</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>1-0</td><td>R / W</td><td>Pin74 function selection
<table>
<tr><th>TEST_MODE1_EN</th><th>LD12 CREC [Bit1-0]</th><th>Pin74</th></tr>
<tr><td>0</td><td>00</td><td>Output low</td></tr>
<tr><td>1</td><td>00</td><td>RESERVE</td></tr>
<tr><td>x</td><td>10</td><td>GP77</td></tr>
<tr><td>x</td><td>11</td><td>Tri-state</td></tr>
</table></td></tr>
</table>

CR EDh.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>7-6</td><td colspan="2">Reserved</td></tr>
<tr><td>5</td><td>R / W</td><td>Pin93 function selection
<table>
<tr><th>LDE CRFA [Bit1]</th><th>DSW_EN</th><th>LD12 CRED [Bit5]</th><th>LDD CRE1 [Bit0]</th><th>LDB CRE6 [Bit2]</th><th>Pin93</th></tr>
<tr><td>1</td><td>x</td><td>x</td><td>x</td><td>x</td><td>VW_SUSWARN#</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>x</td><td>x</td><td>SUSWARN#</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>x</td><td>0</td><td>GP50</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>x</td><td>1</td><td>RSTOUT3#</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>0</td><td>0</td><td>GP50</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>0</td><td>1</td><td>RSTOUT3#</td></tr>
</table></td></tr>
<tr><td>4</td><td>R / W</td><td>Pin92 function selection
<table>
<tr><th>DSW_EN</th><th>LD12 CRED [Bit4]</th><th>CR2A [Bit4]</th><th>Pin92</th></tr>
<tr><td>1</td><td>0</td><td>x</td><td>5VDUAL</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>GP51</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>AUXFANIN3</td></tr>
<tr><td>0</td><td>x</td><td>0</td><td>GP51</td></tr>
<tr><td>0</td><td>x</td><td>1</td><td>AUXFANIN3</td></tr>
</table></td></tr>
</table>

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>3</td><td>R / W</td><td>Pin91 function selection
<table>
<tr><th>DSW_EN</th><th>LD12 CRED [Bit3]</th><th>LDD CRE1 [Bit0]</th><th>LDB CRE6 [Bit1]</th><th>Pin91</th></tr>
<tr><td>1</td><td>0</td><td>x</td><td>0</td><td>SUSACK#</td></tr>
<tr><td>1</td><td>0</td><td>x</td><td>1</td><td>GP52</td></tr>
<tr><td>1</td><td>1</td><td>x</td><td>0</td><td>FDLED3</td></tr>
<tr><td>1</td><td>1</td><td>x</td><td>1</td><td>RSTOUT4</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td>GP52</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>0</td><td>FDLED3</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>1</td><td>RSTOUT4#</td></tr>
</table></td></tr>
<tr><td>2</td><td>R / W</td><td>Pin90 function selection
<table>
<tr><th>DSW_EN</th><th>LD12 CRED [Bit2]</th><th>CR2A [Bit3]</th><th>Pin90</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>SUSWARN_5VDUAL</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>FDLED2</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>GP53</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>AUXFANOUT3</td></tr>
<tr><td>0</td><td>0</td><td>x</td><td>FDLED2</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>GP53</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>AUXFANOUT3</td></tr>
</table></td></tr>
<tr><td>1</td><td>R / W</td><td>Pin89 function selection
<table>
<tr><th>DSW_EN</th><th>LDD CRE1 [Bit2]</th><th>LD12 CRED [Bit1]</th><th>Pin89</th></tr>
<tr><td>0</td><td>0</td><td>x</td><td>GP54</td></tr>
<tr><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
<tr><td>1</td><td>x</td><td>0</td><td>SLP_SUS#</td></tr>
<tr><td>1</td><td>x</td><td>1</td><td>GP54</td></tr>
</table></td></tr>
<tr><td>0</td><td>R / W</td><td>Pin88 function selection
<table>
<tr><th>DSW_EN</th><th>LD12 CRED [Bit0]</th><th>LDD CRE1 [Bit2]</th><th>LDB CRE6 [Bit3]</th><th>Pin88</th></tr>
<tr><td>1</td><td>0</td><td>x</td><td>x</td><td>SLP_SUS_FET</td></tr>
<tr><td>1</td><td>1</td><td>x</td><td>0</td><td>GP55</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>GP55</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>x</td><td>RESERVE</td></tr>
</table></td></tr>
</table>

CR EFh.

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : 40h

BIT	READ / WRITE	DESCRIPTION
7-6	R / W	RSMRST# inactive Timing 00: 90~130 ms 01: 190~230 ms 10: 290~330 ms 11: 390~430 ms
5-4	R / W	DPWROK# inactive Timing 00: 90~130 ms 01: 190~230 ms 10: 290~330 ms 11: 390~430 ms
3-0	Reserved	

24.17 Logical Device 14

CR E0h. PORT80 UART Control Register

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 80h

BIT	READ / WRITE	DESCRIPTION
7	R / W	TxEN (Transmit enable)
6-5	Reserved	
4	R / W	PARE (Parity enable)
3	R / W	PARS (Parity Selection) 0: odd parity 1: even parity
2	R / W	STPS (Stop bit length election) 0: 1 stop bit 1: 2 stop bits
1	R / W	CHAS (Character length selection) 0: 8 bits 1: 7bits
0	Reserved	

CR E1h. PORT80 UART Status Register

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-2	Reserved	
1	R	TD (Transmit done status) When UART finish transmit, it would be 1 and auto clear by hardware
0	R	TBF (Transmit buffer full flag) 0: UART is idle 1: UART is transmitting

CR E2h. PORT80 UART Baud Rate Generator High Byte

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator high byte)

CR E3h. PORT80 UART Baud Rate Generator Low Byte

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	BRGL (Baud rate generator low byte) Baud Rate = 2MHz / ({BRGH, BRGL} + 1)

CR E4h. PORT80 UART Transmit Buffer

Attribute: Read/Write
Power Well: VSB
Reset by: LRESET#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	UARTBUF (UART Transmit buffer)

24.18 Logical Device 15

CR F0h. Fading Led Maximun Duty Cycle Value Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : FFh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_led_maxval This byte reference Led frequency select, CRF5 bit[1] and fading led enable, CRF5 bit[0], Led frequency select bit has higher priority, the combination of Led frequency select and fading led enable describe below. When solid led mode, this byte is duty cycle control register, and frequency control by CRF8. Led frequency before divider select = 1 and fading led enable = 1 is fading led The maximum duty cycle value. Led frequency before divider select = 0 **or** fading led enable = 0 is solid led **maxval ratio Duty cycle** 0x01 1/255 = 0.3% 0x02 2/255 = 0.7% … 0x40 64/255 = 25.1% … 0xFF 255/255 = 100%

CR F1h. Fading Led Middle Duty Cycle Value Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 7Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_led_midval This byte is the turning point duty cycle value between minimum and maximum duty cycle value.

CR F2h. Fading Led Minimun Duty Cycle Value Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_led_minval This byte is the minimum duty cycle value.

CR F3h. Fading Led Increase Duty Cycle Value Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 06h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_led_duty_inc_l The increased duty cycle value between the minimum duty cycle value and turning point.

CR F4h. Fading Led Increase Duty Cycle Value Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 05h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_led_duty_inc_h The increased duty cycle value between the turning point and the maximum duty cycle value.

CR F5h. Fading Led Control Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 17h

BIT	READ / WRITE	DESCRIPTION
7-4	R / W	Fading_led_prgval Repeat each duty cycle value for a few times.
3-2	R / W	Fading led extend enable bits 00 : No extend. 01 : Only extend the minimum duty cycle. 10 : Only extend the maximum duty cycle. 11 : Both extend the minimum and the maximum duty cycle.
1	R / W	Led frequency before frequency divider select Fading led is **only** allowed when this bit select 1 (1kHz). When this bit turn to 0 (4Hz). It force to solid led mode regardless Fading led enable bit (LD15 CRF5 Bit0). 0 : 4Hz 1 : 1kHz (default)

<table>
<tr><th>BIT</th><th>READ / WRITE</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>R / W</td><td>Fading led enable
0 : Solid Led
1 : Fading Led
<table>
<tr><th>LD15 CRF5 bit[1:0]</th><th>Led mode</th></tr>
<tr><td>00</td><td>Solid led and 4Hz before divide</td></tr>
<tr><td>01</td><td>Solid led and 4Hz before divide</td></tr>
<tr><td>10</td><td>Solid led and 1kHz before divide</td></tr>
<tr><td>11</td><td>Fading led and 1kHz before divide</td></tr>
</table></td></tr>
</table>

CR F6h. Fading Led Light Extend Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	This byte is the time for extend the maximum duty cycle value. The extend time reference to fading led frequency : Extend time = (extend value * 4) / fading led frequency

CR F7h. Fading Led Dark Extend Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 0Fh

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	This byte is the time for extend the minimum duty cycle value. The extend time reference to fading led frequency : Extend time = (extend value * 4) / fading led frequency

CR F8h. Fading Led Frequency Divider Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 10h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading led frequency divide factor when fading frequency before divider select = 1 (It can select fading or solid mode depend on LD15 CRF5 bit0) led frequency 0x01: 1kHz/1 = 1kHz 0x02: 1kHz/2 = 500Hz … 0x10: 1kHz/16 = 62Hz (default) … 0xFF: 1kHz/255 = 4Hz When fading led frequency before divider select = 0 (It force to solid led mode) Solid led frequency 0x00: Output low 0x01: High-z 0x02: 4Hz 0x03: 2Hz 0x04: 1Hz 0x05: 1/2Hz 0x06: 1/4Hz 0x07: Output low others High-z

CR F9h. Fading Led Decrease Duty Cycle Value Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 06h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_led_duty_dec_l The decreased duty cycle value between the turning point and the minimum duty cycle value.

CR FAh. Fading Led Decrease Duty Cycle Value Register

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 05h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	Fading_led_duty_dec_h The decreased duty cycle value between the maximum duty cycle value and the turning point.

24.19 Logical Device 16

CR 30h. Deep Sleep Configuration Register

Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : A0h

BIT	READ / WRITE	DESCRIPTION
7	R / W	DIS_SLPSUS_PULLUP (test mode) 0: Enable SLP_SUS# internal pull-up. 1: Disable SLP_SUS# internal pull-up.
6-1	Reserved	
0	R / W	Deep S5 Enable 0: Disable Deep S5 function when into S5 state (SLP_S5#). 1: Enable Deep S5 function when into S5 state (SLP_S5#).

CR E0h. Deep Sleep wake up PSOUT# delay time

Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : **20h** (Default: 512ms)

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	
5-0	R / W	Deep Sleep wake up PSOUT# delay time. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT# after SYS_3VSB and wait a delay time. DELAY TIME = (Setting Value) * 16ms Example : maximum delay time = $(3F)_{hex}$ * 16ms = 1008ms

CR E1h. Deep Sleep wake up PSOUT# pulse width

Attribute: Read/Write

Power Well: VSB

Reset by: RSMRST#

Default : **04h** (Default: 128 ms)

BIT	READ / WRITE	DESCRIPTION
7-4	Reserved	
3-0	R / W	Deep Sleep wake up PSOUT# pulse width. When system wake up from deep sleep state, IO will issue a low pulse via PSOUT#.. Pulse Width = (Setting Value) * **32ms** Example : maximum pulse width = $(F)_{hex}$ * **32ms** = 480ms

CR E2h. Deep Sleep Delay Time Control

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 05h

BIT	READ / WRITE	DESCRIPTION
7	R / W	0: The unit of deep sleep delay time is second. 1: The unit of deep sleep delay time is Minute.
6-0	R / W	Deep Sleep Delay Time Control. When system leaves S0 State, IO will wait a delay time before entering into Deep Sleep State. Example: maximum delay time = 127 second/minute

CR E3h. WDT1 to Deep Sleep Delay Time Control

Attribute: Read/Write

Power Well: VRTC

Reset by: Battery reset

Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2	R / W	Watchdog Timer 1 wake up auto mode. 0: SIO will not wake up system after RSMRST release 1: SIO will wake up system after RSMRST release.
1-0	R / W	Deep Sleep Watchdog Timer 1 Delay Time Control. When system will enter Deeps5 by watchdog timer 1, SIO will set a delay time to control. Delay time: 2, 4, 6, 8 sec = register: 0, 1, 2, 3

CR F3h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 80h

BIT	READ / WRITE	DESCRIPTION
7-0	R / W	LCLK_FRQ[7:0] LCLK / (31.25KHz * 2) = LCLK_FRQ Example: 33MHz / (31.25KHz *2) = 11'h210 = 11'd528 24MHz / (31.25KHz *2) = 11'h180 = 11'd384

CR F4h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 01h

BIT	READ / WRITE	DESCRIPTION
7-3	Reserved	
2-0	R / W	LCLK_FRQ[10:8] LCLK / (31.25KHz * 2) = LCLK_FRQ Example: 33MHz / (31.25KHz *2) = 11'h210 = 11'd528 24MHz / (31.25KHz *2) = 11'h180 = 11'd384

CR F5h.
Attribute: Read/Write
Power Well: VSB
Reset by: RSMRST#
Default : 00h

BIT	READ / WRITE	DESCRIPTION
7-1	Reserved	
0	R / W	EN_CALI 0: Disable Oscillator free calibrate 1: Enable Oscillator free calibrate

CR F8h.
Attribute: Read/Write
Power Well: VRTC
Reset by: Battery reset
Default : 20h

BIT	READ / WRITE	DESCRIPTION
7-6	Reserved	

BIT	READ / WRITE	DESCRIPTION
5	R / W	EN_PLL 0: Disable Oscillator free 1: Enable Oscillator free
4-0	Reserved	

25. SPECIFICATIONS

25.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNIT
3VCC	Power Supply Voltage (3.3V)	-0.3 to 3.6	V
VI	Input Voltage	-0.3 to 3VCC+0.3	V
	Input Voltage (5V tolerance)	-0.3 to 5.5	V
TA	Operating Temperature	0 to +70	°C
TSTG	Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

25.2 DC CHARACTERISTICS

(T_A = 0°C to +70°C, V_{DD} = 3.3V ± 5%, V_{DD} = 1.8V ± 5%, V_{SS} = 0V)

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Battery Quiescent Current	IBAT			2.4	µA	VBAT = 2.5 V
ACPI Stand-by Power Supply Quiescent Current	IVSB			8.0	mA	VSB = 3.3 V, All ACPI pins are not connected.
VCC Quiescent Current	IVCC			25	mA	VSB (AVSB)= 3.3 V VCC= 3.3 V LRESET = High CASEOPEN Pull-Up to VBAT
VTT Quiescent Current	IVTT			1	mA	VSB (AVSB)= 3.3 V VCC= 3.3 V VTT = 1.2V LRESET = High CASEOPEN Pull-Up to VBAT
AIN – Analog input						
AOUT – Analog output						
In_{tp3} – 3.3V TTL-level input pin						
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	

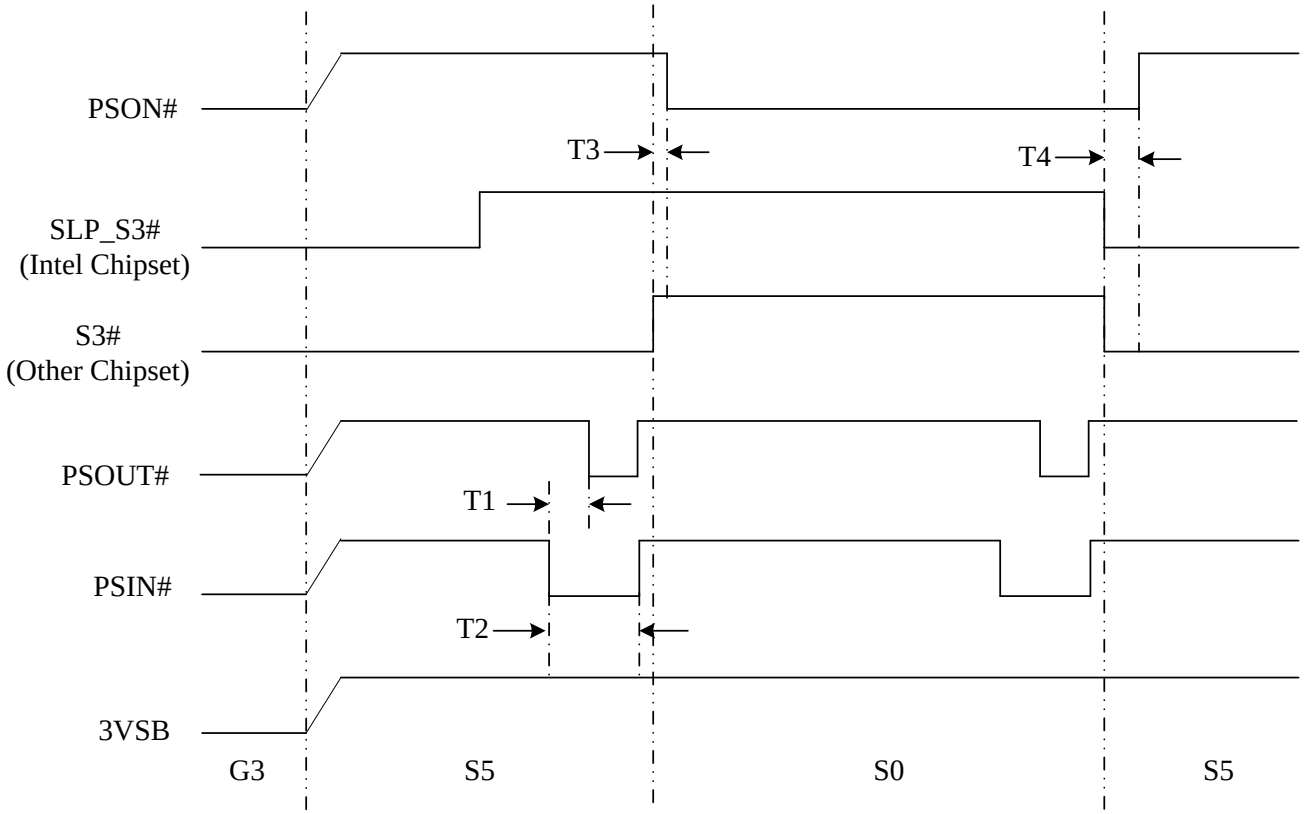
PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{sp3} – 3.3V Schmitt-trigger input for AMD SB-TSI						
Input Low Threshold Voltage	V_{t-}			0.4*V_{TT}	V	
Input High Threshold Voltage	V_{t+}	0.6*V_{TT}			V	
Hystersis	V_{TH}		0.2*V_{TT}		V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{TT}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{tp318} – 3.3V/1.8V input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	1.5			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{sp318} – 3.3V/1.8V Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.8	0.9	1.1	V	
Input High Threshold Voltage	V_{t+}	1.1	1.2	1.4	V	
Hystersis	V_{TH}		0.2		V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{gp3} – 3.3V GTL-level input pin						
Input Low Voltage	V_{IL}		0.72		V	
Input High Voltage	V_{IH}		0.72		V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{tp5} – 5V TTL-level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{tscup5} – 5V TTL-level, Schmitt-trigger input buffer with controllable pull-up						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{IN} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{IN} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{IN} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{tsp5} – 5V TTL-level, Schmitt-trigger input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{IN} = 3.3 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{IN} = 3.3 V
Hystersis	V_{TH}	0.5	1.2		V	V_{IN} = 3.3 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3 V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
In_{tdp5} – 5V TTL-level input pin with internal pull-down resistor						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = 3.3V
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
O_8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA
OD_8 – Open-drain output pin with 8mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
OX_8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -8 mA, PAD_VDD=3.3V
Output High Voltage	V_{OH}	1.31			V	I_{OH} = -8 mA, PAD_VDD=1.8V
ODX_8 – Output pin with 8mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
O_{12} – Output pin with 12mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_{12} – Open-drain output pin with 12mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
O_{16} – Output pin with 16mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -16 mA
OD_{16} – Open-drain output pin with 16mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 16 mA
O_{24} – Output pin with 24mA source-sink capability						

PARAMETER	SYM	MIN	TYP	MAX.	UNIT	CONDITIONS
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -24 mA
OD_{24} – Open-drain output pin with 24mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 24 mA
O_{48} – Output pin with 48mA source-sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -48 mA
OD_{48} – Open-drain output pin with 48mA sink capability						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
I/O_{V3} – Bi-direction pin with source capability of 6 mA and sink capability of 1 mA for INTEL® PECI						
Input Low Voltage	V_{IL}	$0.275*V_{TT}$		$0.5*V_{TT}$	V	
Input High Voltage	V_{IH}	$0.55*V_{TT}$		$0.725*V_{TT}$	V	
Output Low Voltage	V_{OL}			$0.25*V_{TT}$	V	
Output High Voltage	V_{OH}	$0.75*V_{TT}$			V	
Hysterisis	V_{Hys}	$0.1*V_{TT}$			V	
O_{12cu} – Output pin 12mA source-sink capability with controllable pull-up						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_{12cu} – Open-drain 12mA sink capability output pin with controllable pull-up						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA

26. AC CHARACTERISTICS

26.1 Power On / Off Timing

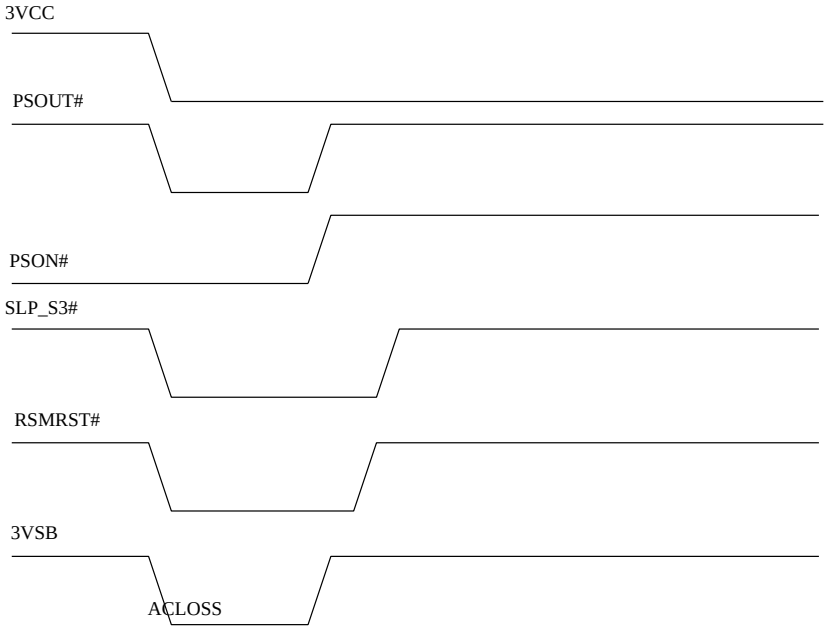


	T1	T2	T3	T4
IDEAL TIMING	48ms~66ms	Over 64ms at least	< 200ns	15ms~32ms

26.2 AC Power Failure Resume Timing

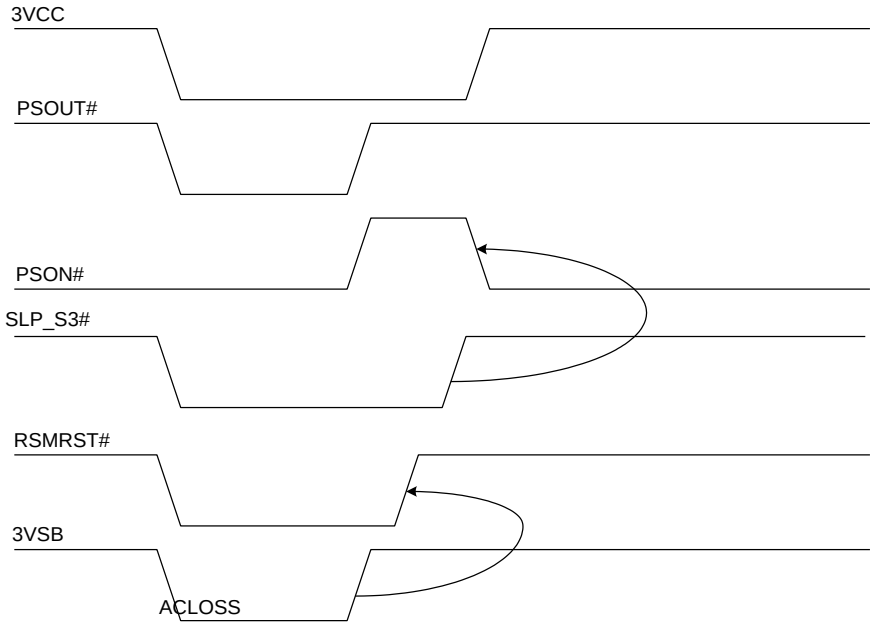
(1) Logical Device A, CR [E4h] bits [6:5] =00 means “OFF” state

(“OFF” means the system is always turned off after the AC power loss recovered.)



(2) Logical Device A, CR [E4h] bits [6:5]=01 means “ON” state.

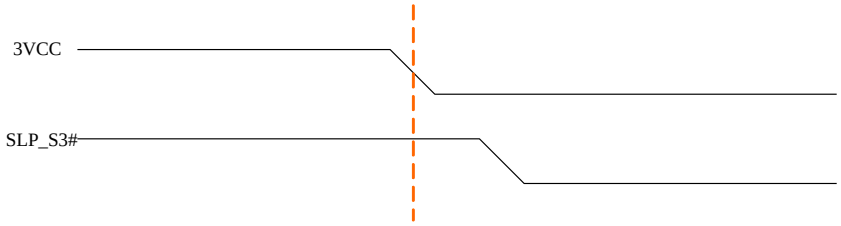
(“ON” means the system is always turned on after AC power loss recovered.)



**** What's the definition of former state at AC power failure?**

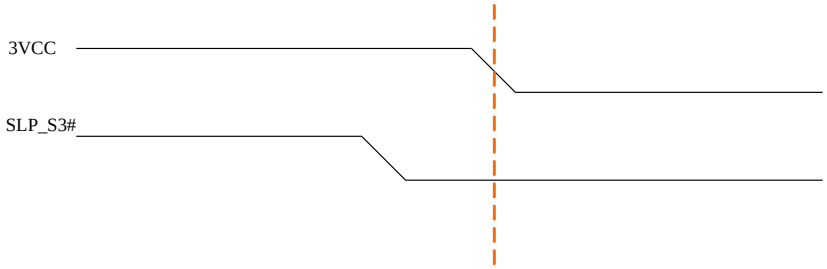
1) The previous state is "ON"

VCC falls to 2.6V and SLP_S3# keeps at VIH 2.0V



2) The previous state is "OFF"

VCC fall to 2.6V and SLP_S3# keeps at VIL 0.8V



To ensure that VCC does not fall faster than VSB in various ATX Power Supplies, the NCT6796D adds the option of "user define mode" for the pre-defined state before AC power failure. BIOS can set the pre-defined state for the system to be "On" or "Off". According to this setting, the system chooses the state after the AC power recovery.

Please refer to the descriptions of bit 6~5 of CR E4h and bit 4 of CR E6h in Logical Device A.

CR E4h

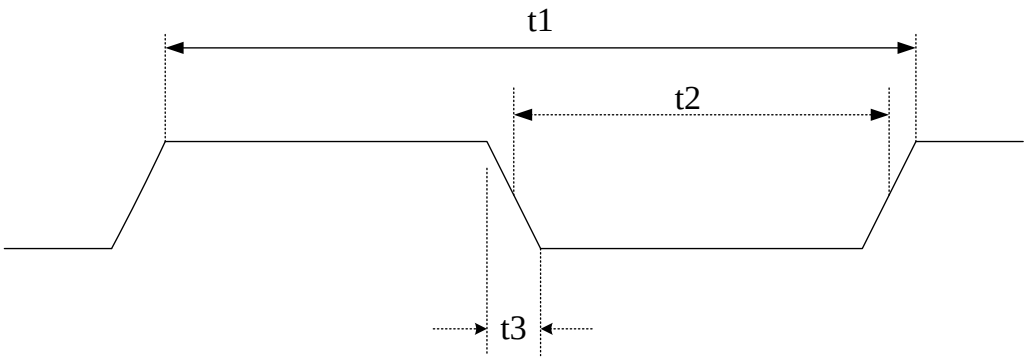
BIT	READ/WRITE	DESCRIPTION
6~5	R / W	Power-loss control bits => (VBAT) 0 0: System always turns off when it returns from power-loss state. 0 1: System always turns on when it returns from power-loss state. 1 0: System turns off / on when it returns from power-loss state depending on the state before the power loss. 1 1: User defines the resuming state before power loss.(refer to Logic Device A, CRE6[4])

CR E6h

BIT	READ/WRITE	DESCRIPTION
4	R / W	Power loss Last State Flag. **(VBAT)** 0: ON 1: OFF

26.3 Clock Input Timing

PARAMETER	48MHZ / 24MHZ		UNIT
	MIN	MAX	
Cycle to cycle jitter		300/500	ps
Duty cycle	45	55	%



PARAMETER	DESCRIPTION	48MHZ / 24MHZ			UNIT
		MIN	TYP	MAX	
t1	Clock cycle time		20.8 / 41.7		ns
t2	Clock high time/low time	9 / 19	10 / 21		ns
t3	Clock rising time/falling time (0.4V~2.4V)			3	ns

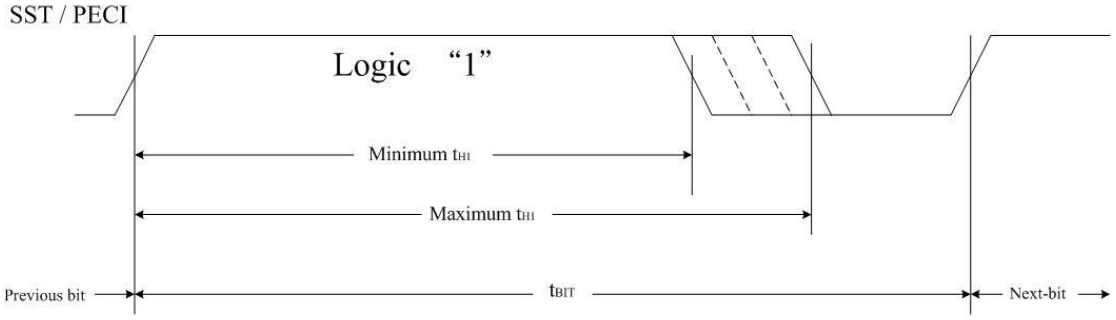
26.4 PCICLK_OUT delay

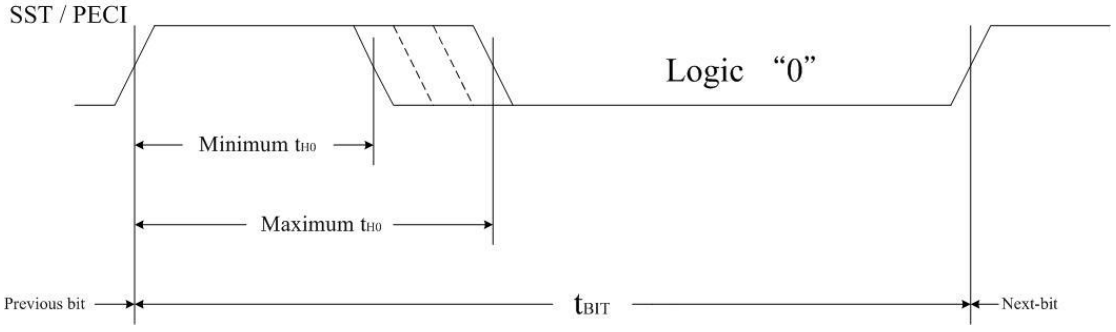
CLKOUT Delay	Min.	Max.	Unit
Propagation delay	0.5	1.2	nsec
Ron	6.7	15.3	ohm

26.5 LPC timing

Symbol	Parameter	MIN	Typical	MAX	Units
PCICLK	Clock frequency	19.2		36	MHz
T_{CO}	Tx Rising Clock to Data Output Delay	3.5		8.5	ns
T_{SU}	Rx Data Setup Time to CLK Rising Edge	18			ns
T_{HD}	Rx Data Hold Time to CLK Rising Edge	-7.6			ns

26.6 PECI Timing

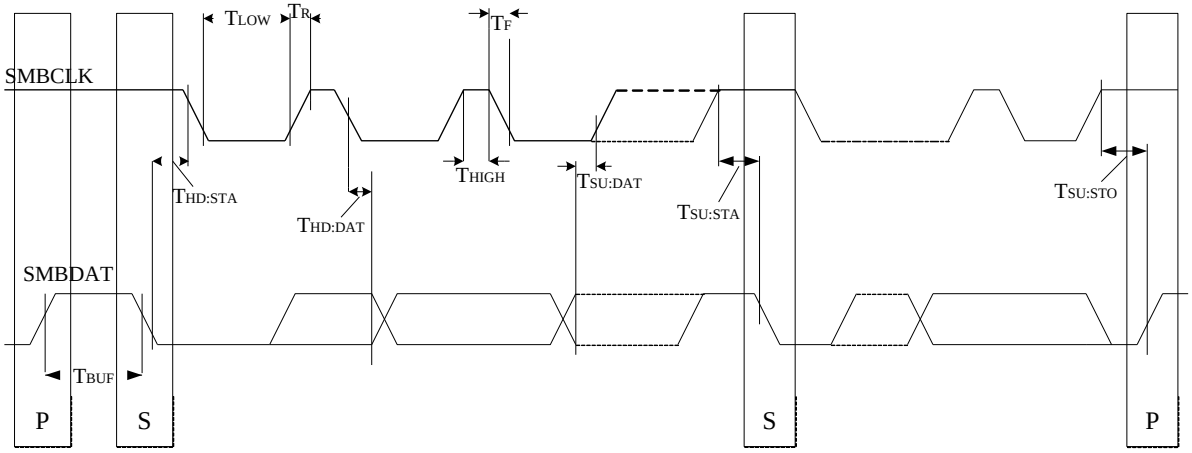




SYMBOL	MIN	TYP	MAX	UNITS

t_{BIT}	Client	0.495		500	μs
	Originator	0.495		250	
t_{H1}		0.6	3/4	0.8	× t_{BIT}
t_{H0}		0.2	1/4	0.4	× t_{BIT}

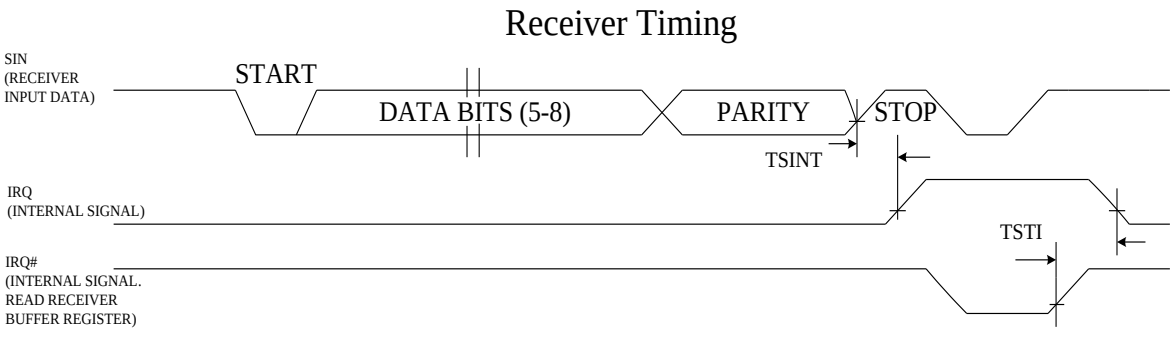
26.7 SMBus Timing



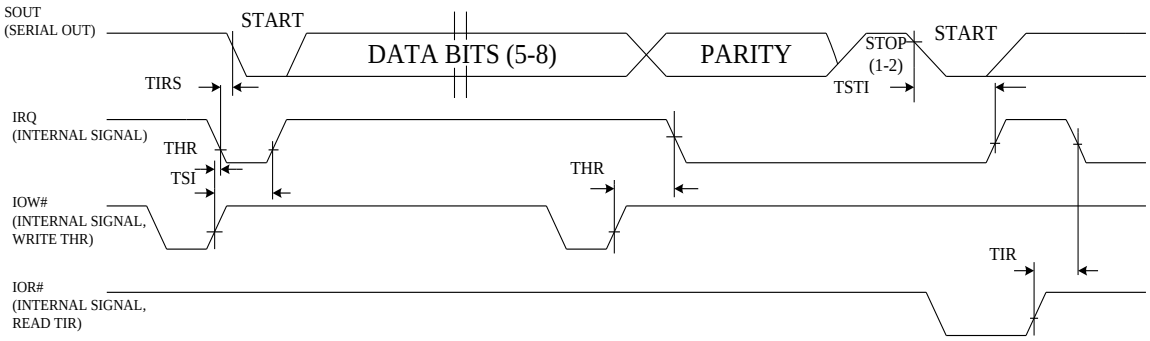
26.8 UART/Parallel Port

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Delay from Stop to Set Interrupt	TSINT		9/16		Baud Rate
Delay from $\overline{IOR}$ Reset Interrupt	TRINT		9	1000	nS
Delay from Initial IRQ Reset to Transmit Start	TIRS		1/16	8/16	Baud Rate
Delay from to Reset interrupt	THR			175	nS
Delay from Initial $\overline{IOW}$ to interrupt	TSI		9/16	16/16	Baud Rate
Delay from Stop to Set Interrupt	TSTI			8/16	Baud Rate
Delay from $\overline{IOR}$ to Reset Interrupt	TIR		8	250	nS
Delay from $\overline{IOR}$ to Output	TMWO		6	200	nS
Set Interrupt Delay from Modem Input	TSIM		18	250	nS
Reset Interrupt Delay from $\overline{IOR}$	TRIM		9	250	nS
Baud Divisor	N	100 pF Loading		2^{16}-1	

UART Receiver Timing

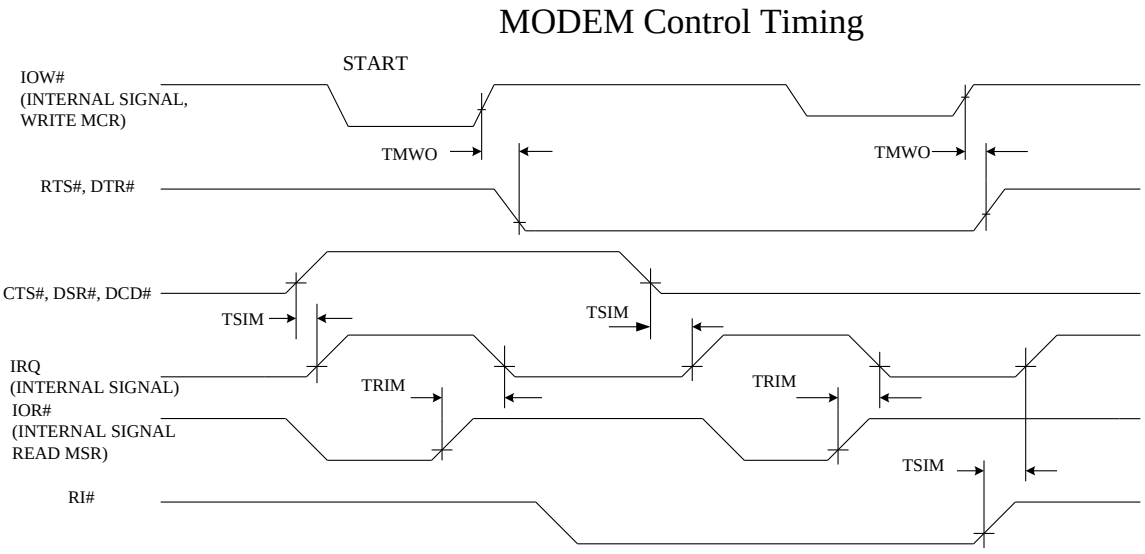


UART Transmitter Timing



26.9 Modem Control Timing

Modem Control Timing



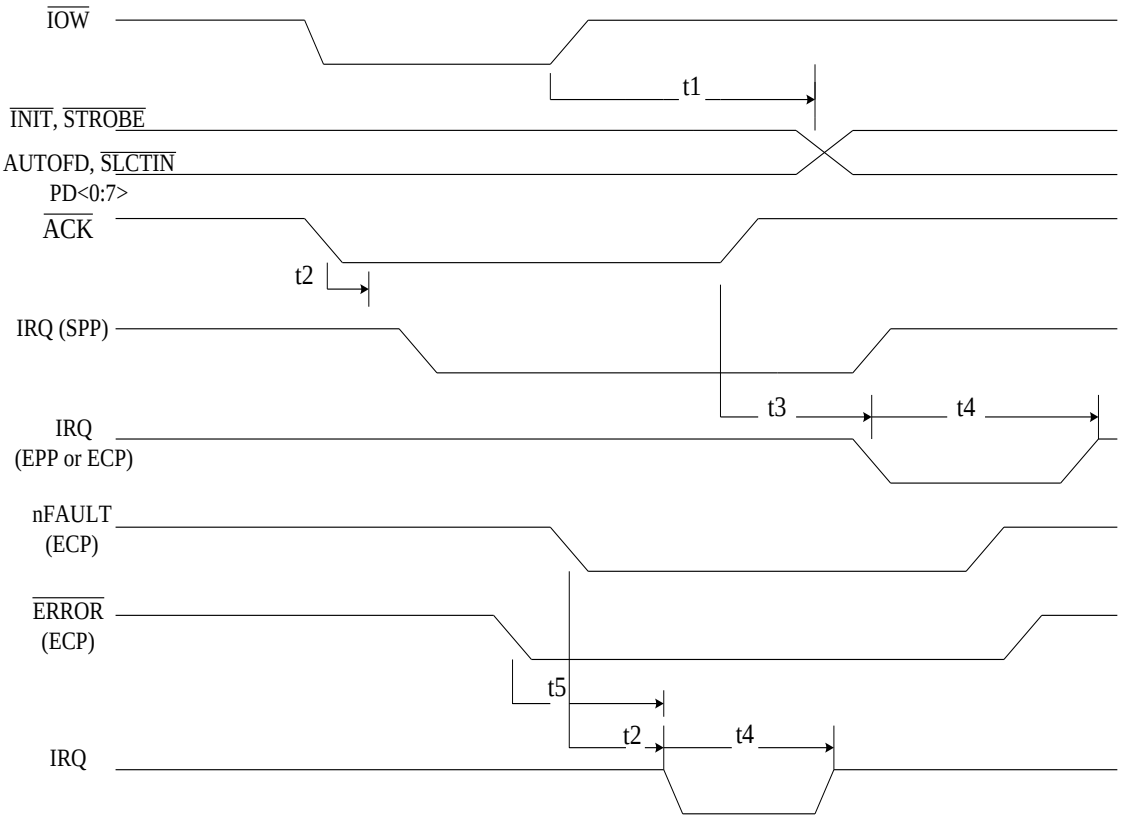
26.10 Parallel Port Mode Parameters

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS

$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS
PARAMETER	**SYM.**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
PD0-7, $\overline{\text{INDEX}}$, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFD}}$ Delay from $\overline{\text{IOW}}$	t1			100	nS
IRQ Delay from $\overline{\text{ACK}}$, nFAULT	t2			60	nS
IRQ Delay from $\overline{\text{IOW}}$	t3			105	nS
IRQ Active Low in ECP and EPP Modes	t4	200		300	nS
$\overline{\text{ERROR}}$ Active to IRQ Active	t5			105	nS

26.10.1Parallel Port Timing

Parallel Port Timing



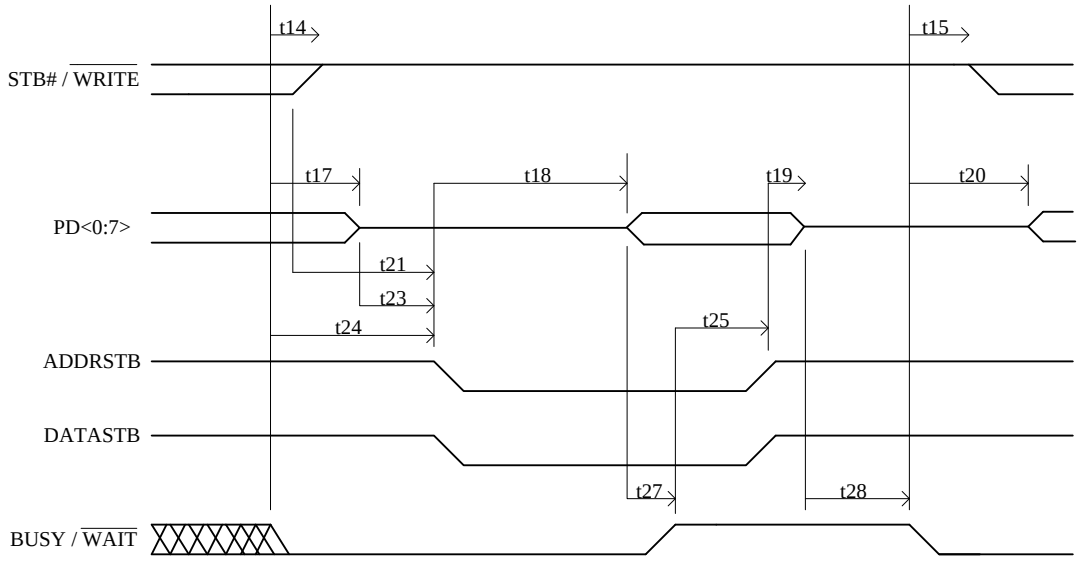
26.10.2EPP Data or Address Read Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS
PARAMETER	**SYM.**	**MIN.**	**MAX.**	**UNIT**
Ax Valid to $\overline{\text{IOR}}$ Asserted	t1	40		nS
IOCHRDY Deasserted to $\overline{\text{IOR}}$ Deasserted	t2	0		nS
$\overline{\text{IOR}}$ Deasserted to Ax Valid	t3	10	10	nS
$\overline{\text{IOR}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t4	40		
$\overline{\text{IOR}}$ Asserted to IOCHRDY Asserted	t5	0	24	nS
PD Valid to SD Valid	t6	0	75	nS
$\overline{\text{IOR}}$ Deasserted to SD Hi-Z (Hold Time)	t7	0	40	µS
SD Valid to IOCHRDY Deasserted	t8	0	85	nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t9	60	160	nS
PD Hi-Z to PDBIR Set	t10	0		nS
$\overline{\text{WRITE}}$ Deasserted to $\overline{\text{IOR}}$ Asserted	t13	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Deasserted	t14	0	185	nS
Deasserted to $\overline{\text{WRITE}}$ Modified	t15	60	190	nS
$\overline{\text{IOR}}$ Asserted to PD Hi-Z	t16	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Hi-Z	t17	60	180	nS
Command Asserted to PD Valid	t18	0		nS
Command Deasserted to PD Hi-Z	t19	0		nS
$\overline{\text{WAIT}}$ Deasserted to PD Drive	t20	60	190	nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{\text{WRITE}}$ Deasserted to Command	t21	1		nS
PBDIR Set to Command	t22	0	20	nS
PD Hi-Z to Command Asserted	t23	0	30	nS
Asserted to Command Asserted	t24	0	195	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t25	60	180	nS
Time out	t26	10	12	nS
PD Valid to $\overline{\text{WAIT}}$ Deasserted	t27	0		nS
PD Hi-Z to $\overline{\text{WAIT}}$ Deasserted	t28	0		µS

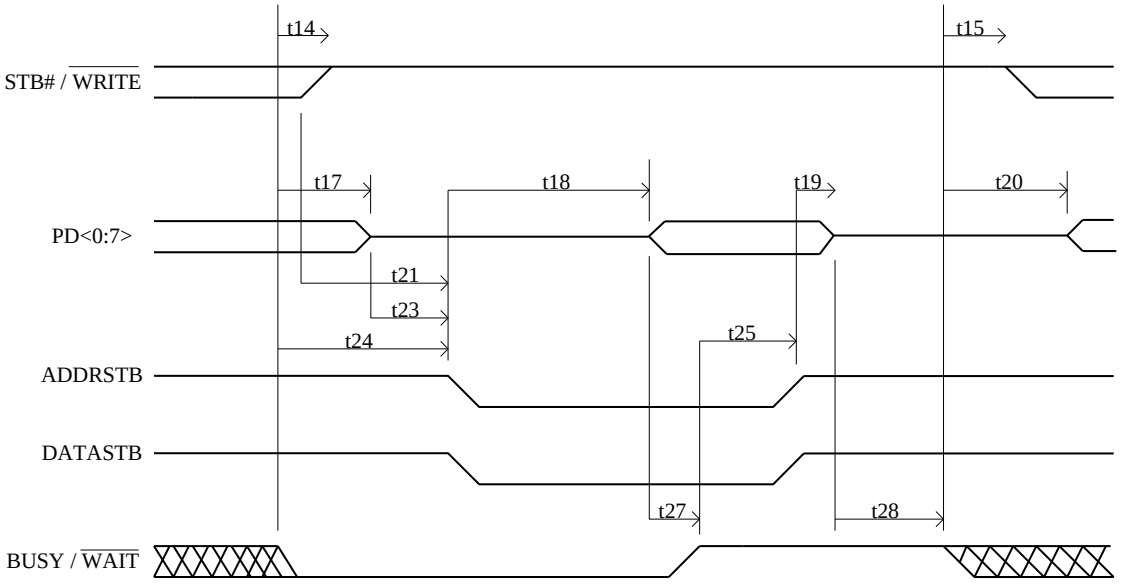
26.10.3EPP Data or Address Read Cycle (EPP Version 1.9)

EPP Data or Address Read Cycle (EPP Version 1.9)



26.10.4EPP Data or Address Read Cycle (EPP Version 1.7)

EPP Data or Address Read Cycle (EPP Version 1.7)



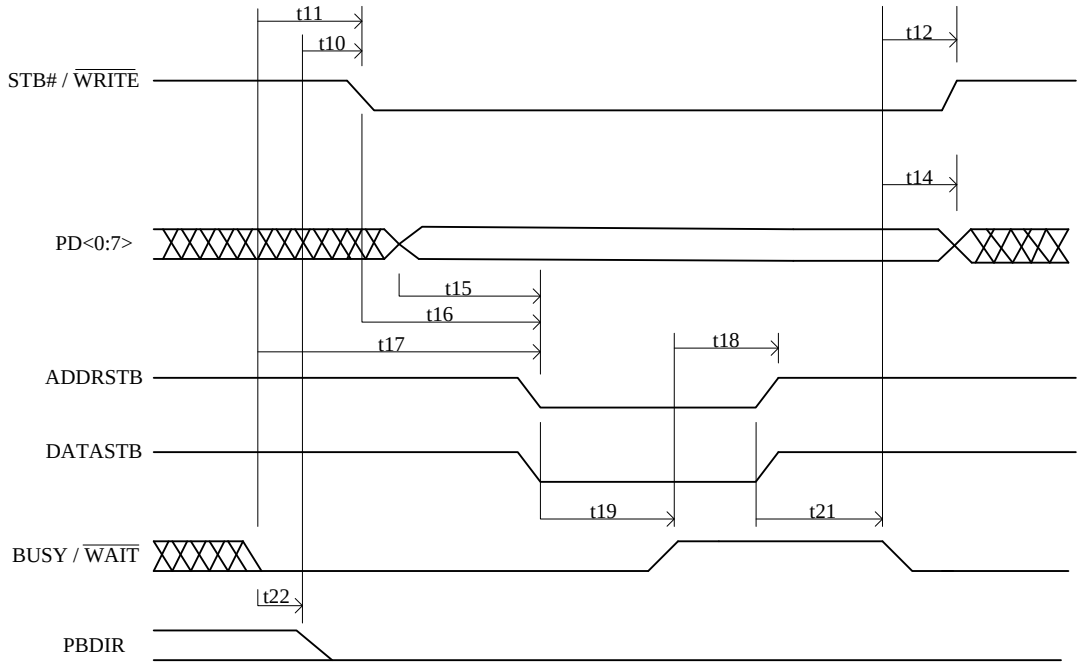
26.10.5EPP Data or Address Write Cycle Timing Parameters

PARAMETER	SYM.	MIN.	MAX.	UNIT
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS
PARAMETER	**SYM.**	**MIN.**	**MAX.**	**UNIT**
Ax Valid to $\overline{\text{IOW}}$ Asserted	t1	40		nS
SD Valid to Asserted	t2	10		nS
$\overline{\text{IOW}}$ Deasserted to Ax Invalid	t3	10		nS
$\overline{\text{WAIT}}$ Deasserted to IOCHRDY Deasserted	t4	0		nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t5	10		nS
$\overline{\text{IOW}}$ Deasserted to $\overline{\text{IOW}}$ or $\overline{\text{IOR}}$ Asserted	t6	40		nS
IOCHRDY Deasserted to $\overline{\text{IOW}}$ Deasserted	t7	0	24	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t8	60	160	nS
$\overline{\text{IOW}}$ Asserted to $\overline{\text{WAIT}}$ Asserted	t9	0	70	nS
PBDIR Low to $\overline{\text{WRITE}}$ Asserted	t10	0		nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Asserted	t11	60	185	nS
$\overline{\text{WAIT}}$ Asserted to $\overline{\text{WRITE}}$ Change	t12	60	185	nS
$\overline{\text{IOW}}$ Asserted to PD Valid	t13	0	50	nS
$\overline{\text{WAIT}}$ Asserted to PD Invalid	t14	0		nS
PD Invalid to Command Asserted	t15	10		nS
$\overline{\text{IOW}}$ to Command Asserted	t16	5	35	nS
$\overline{\text{WAIT}}$ Asserted to Command Asserted	t17	60	210	nS
$\overline{\text{WAIT}}$ Deasserted to Command Deasserted	t18	60	190	nS
Command Asserted to $\overline{\text{WAIT}}$ Deasserted	t19	0	10	µS
Time out	t20	10	12	µS
Command Deasserted to $\overline{\text{WAIT}}$ Asserted	t21	0		nS

PARAMETER	SYM.	MIN.	MAX.	UNIT
$\overline{IOW}$ Deasserted to $\overline{WRITE}$ Deasserted and PD invalid	t22	0		nS
$\overline{WRITE}$ to Command Asserted	t16	5	35	nS

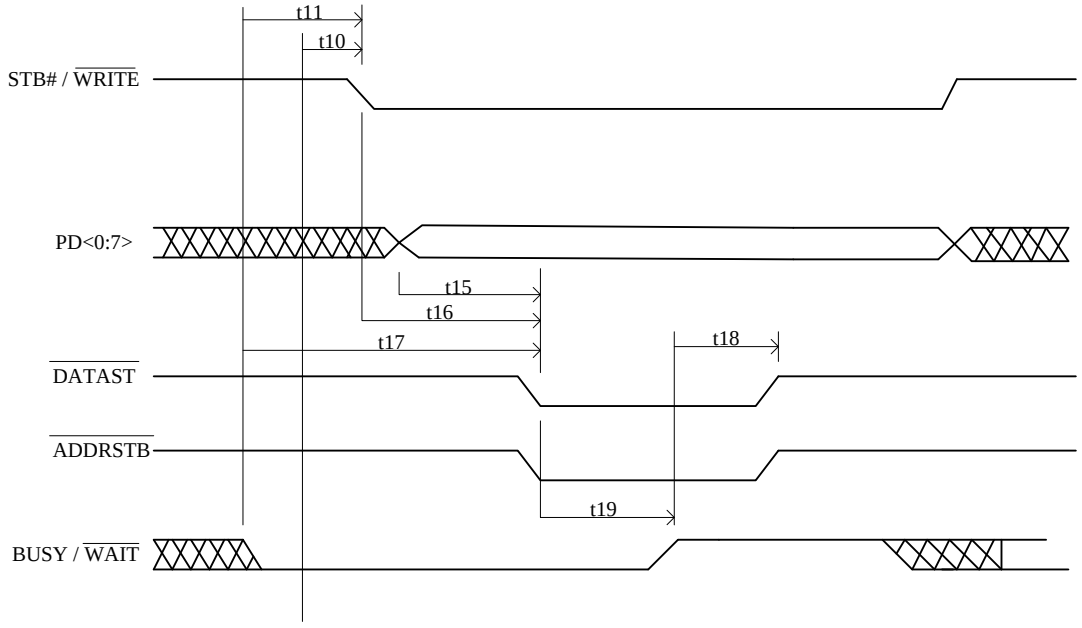
26.10.6EPP Data or Address Write Cycle (EPP Version 1.9)

EPP Data or Address Write Cycle (EPP Version 1.9)



26.10.7EPP Data or Address Write Cycle (EPP Version 1.7)

EPP Data or Address Write Cycle (EPP Version 1.7)

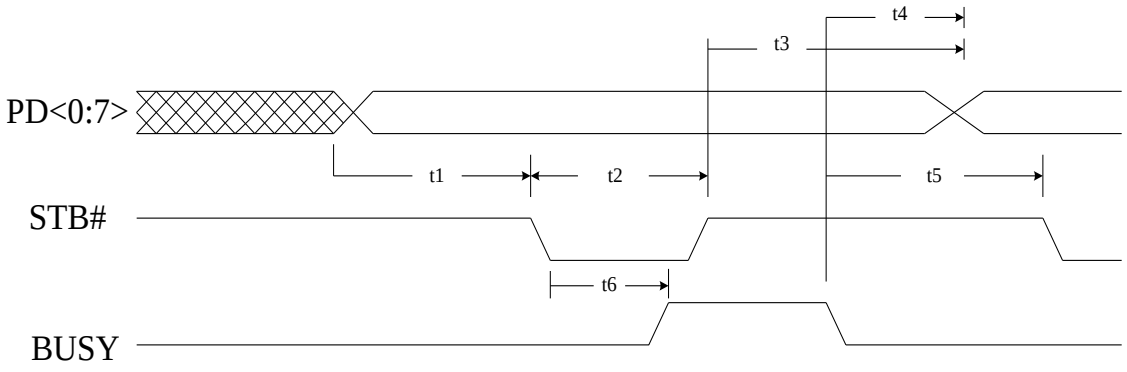


26.10.8Parallel Port FIFO Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DATA Valid to nSTROBE Active	t1	600		nS
nSTROBE Active Pulse Width	t2	600		nS
DATA Hold from nSTROBE Inactive	t3	450		nS
BUSY Inactive to PD Inactive	t4	80		nS
BUSY Inactive to nSTROBE Active	t5	680		nS
nSTROBE Active to BUSY Active	t6		500	nS

26.10.9Parallel FIFO Timing

Parallel FIFO Timing

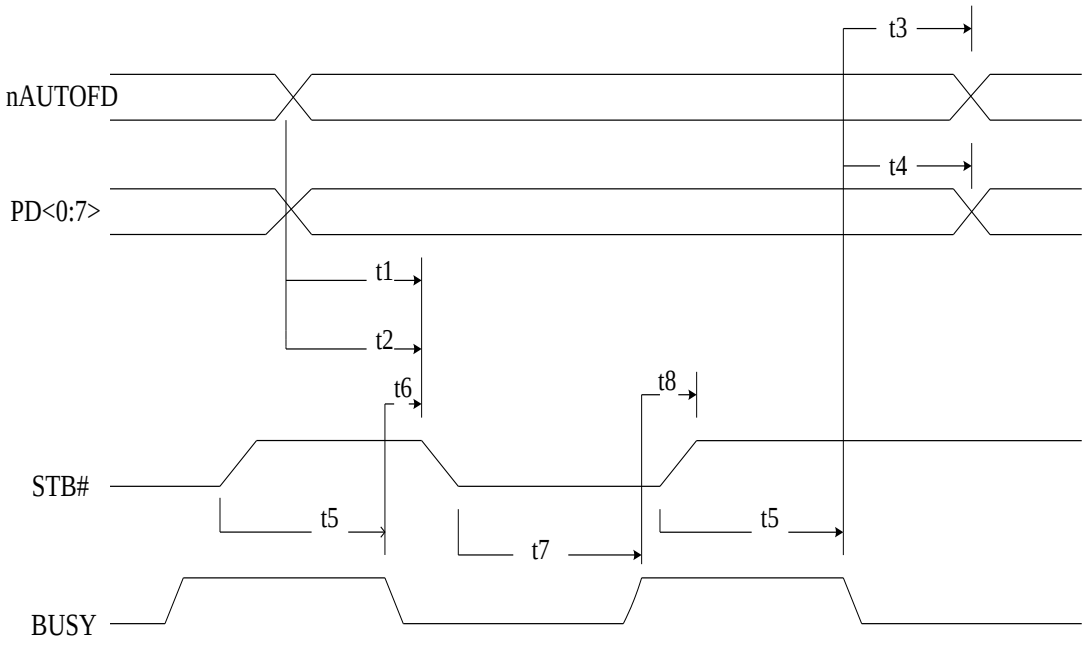


26.10.10 ECP Parallel Port Forward Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
nAUTOFD Valid to nSTROBE Asserted	t1	0	60	nS
PD Valid to nSTROBE Asserted	t2	0	60	nS
BUSY Deasserted to nAUTOFD Changed	t3	80	180	nS
BUSY Deasserted to PD Changed	t4	80	180	nS
nSTROBE Deasserted to BUSY Deasserted	t5	0		nS
BUSY Deasserted to nSTROBE Asserted	t6	80	200	nS
nSTROBE Asserted to BUSY Asserted	t7	0		nS
BUSY Asserted to nSTROBE Deasserted	t8	80	180	nS

26.10.11 ECP Parallel Port Forward Timing

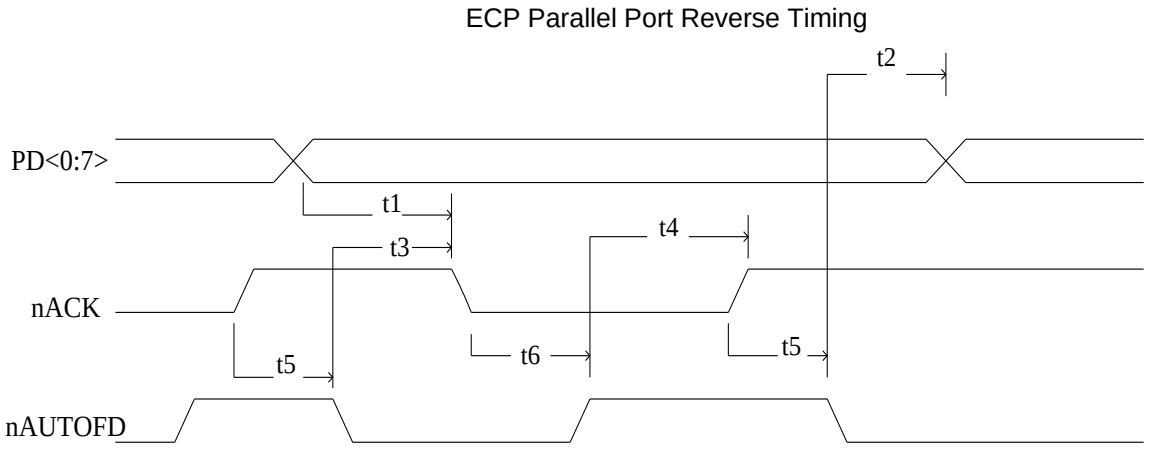
ECP Parallel Port Forward Timing



26.10.12 ECP Parallel Port Reverse Timing Parameters

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
PD Valid to nACK Asserted	t1	0		nS
nAUTOFD Deasserted to PD Changed	t2	0		nS
nAUTOFD Asserted to nACK Asserted	t3	0		nS
nAUTOFD Deasserted to nACK Deasserted	t4	0		nS
nACK Deasserted to nAUTOFD Asserted	t5	80	200	nS
PD Changed to nAUTOFD Deasserted	t6	80	200	nS

26.10.13 ECP Parallel Port Reverse Timing

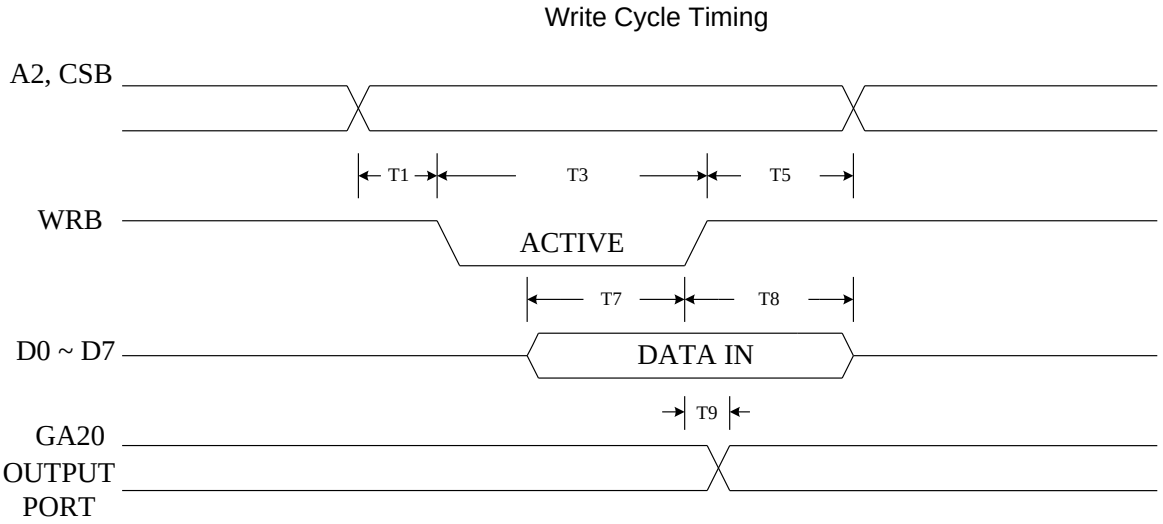


26.10.14 KBC Timing Parameters

NO.	DESCRIPTION	MIN.	MAX.	UNIT
T1	Address Setup Time from WRB	0		nS
T2	Address Setup Time from RDB	0		nS
T3	WRB Strobe Width	20		nS
T4	RDB Strobe Width	20		nS
T5	Address Hold Time from WRB	0		nS
T6	Address Hold Time from RDB	0		nS
T7	Data Setup Time	50		nS
T8	Data Hold Time	0		nS
T9	Gate Delay Time from WRB	10	30	nS
T10	RDB to Drive Data Delay		40	nS
T11	RDB to Floating Data Delay	0	20	nS
T12	Data Valid After Clock Falling (SEND)		4	µS
T13	K/B Clock Period	20		µS
T14	K/B Clock Pulse Width	10		µS
T15	Data Valid Before Clock Falling (RECEIVE)	4		µS
T16	K/B ACK After Finish Receiving	20		µS
T19	Transmit Timeout		2	mS
T20	Data Valid Hold Time	0		µS
T21	Input Clock Period (6–16 Mhz)	63	167	nS

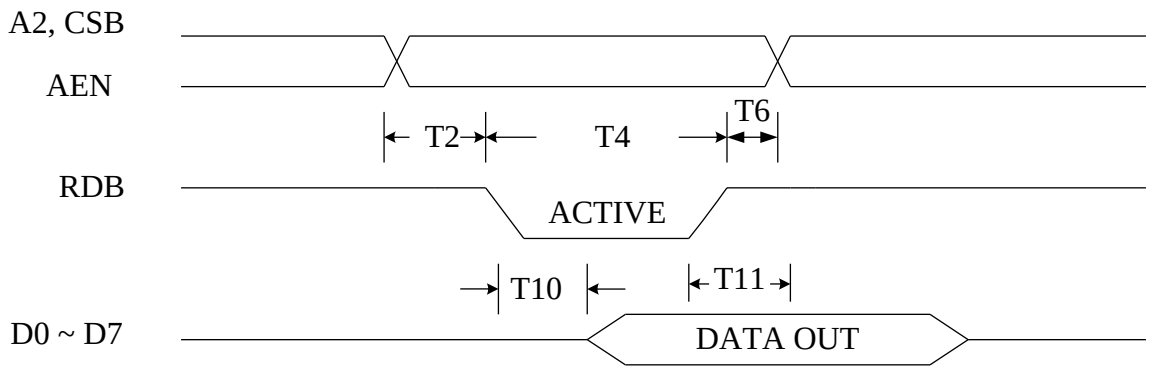
NO.	DESCRIPTION	MIN.	MAX.	UNIT
T22	Duration of CLK inactive	30	50	µS
T23	Duration of CLK active	30	50	µS
T24	Time from inactive CLK transition, used to time when the auxiliary device sample DATA	5	25	µS
T25	Time of inhibit mode	100	300	µS
T26	Time from rising edge of CLK to DATA transition	5	T28-5	µS
T27	Duration of CLK inactive	30	50	µS
T28	Duration of CLK active	30	50	µS
T29	Time from DATA transition to falling edge of CLK	5	25	µS

26.10.15 Writing Cycle Timing



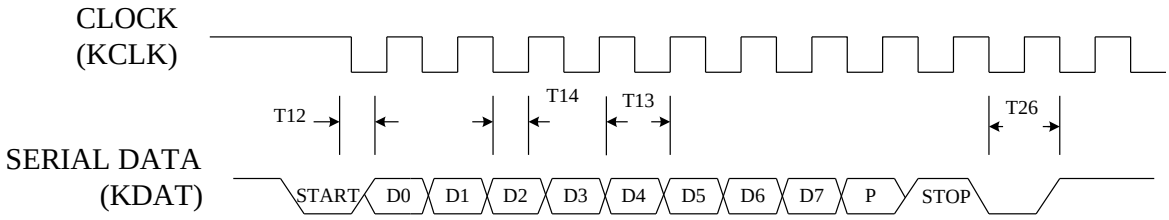
26.10.16 Read Cycle Timing

Read Cycle



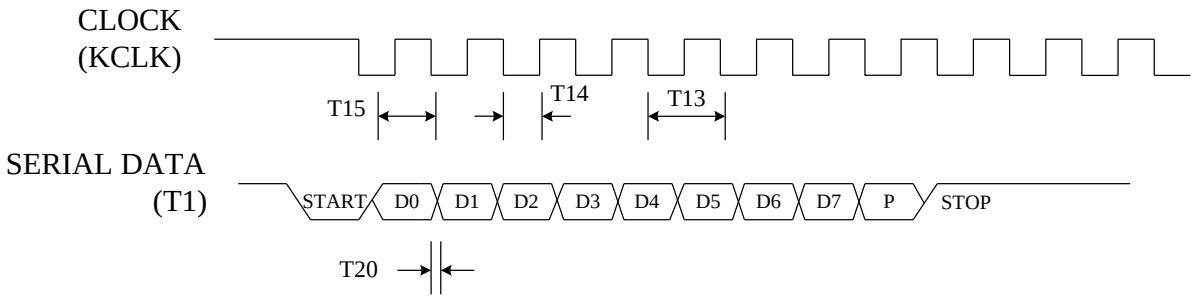
26.10.17 Send Data to K/B

Send Data to K/B



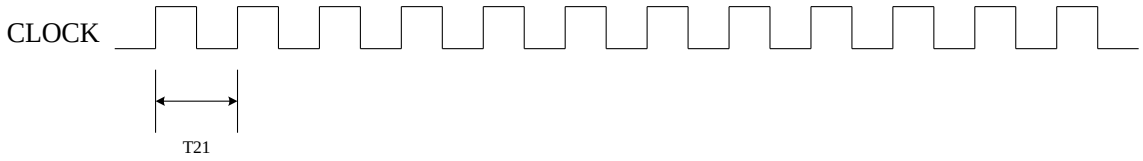
26.10.18 Receive Data from K/B

Receive Data from K/B



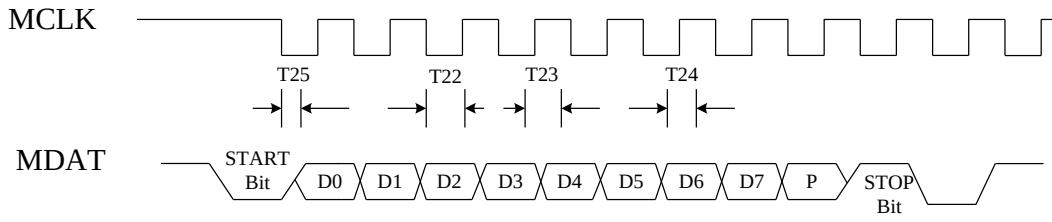
26.10.19 Input Clock

Input Clock



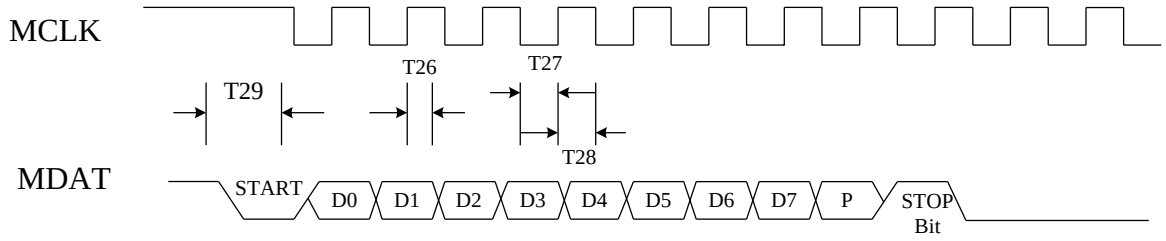
26.10.20 Send Data to Mouse

Send Data to Mouse



26.10.21 Receive Data from Mouse

Receive Data from Mouse



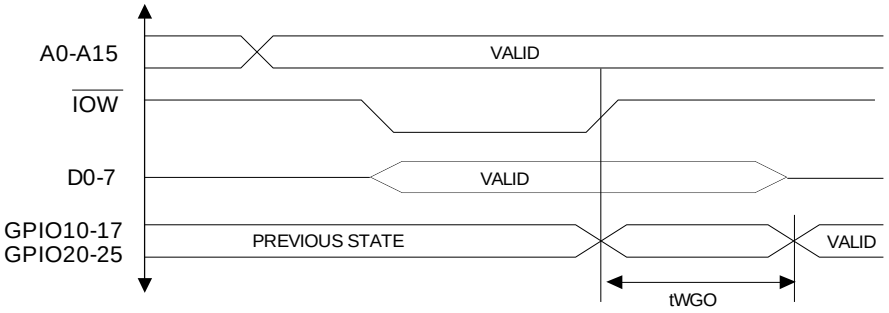
26.11 GPIO Timing Parameters

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
t_{WGO}	Write data to GPIO update		300(Note 1)	ns

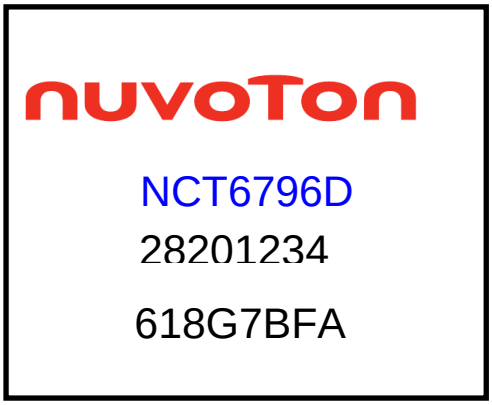
Note: Refer to Microprocessor Interface Timing for Read Timing.

26.11.1 GPIO Write Timing

GPIO Write Timing diagram



27. TOP MARKING SPECIFICATIONS



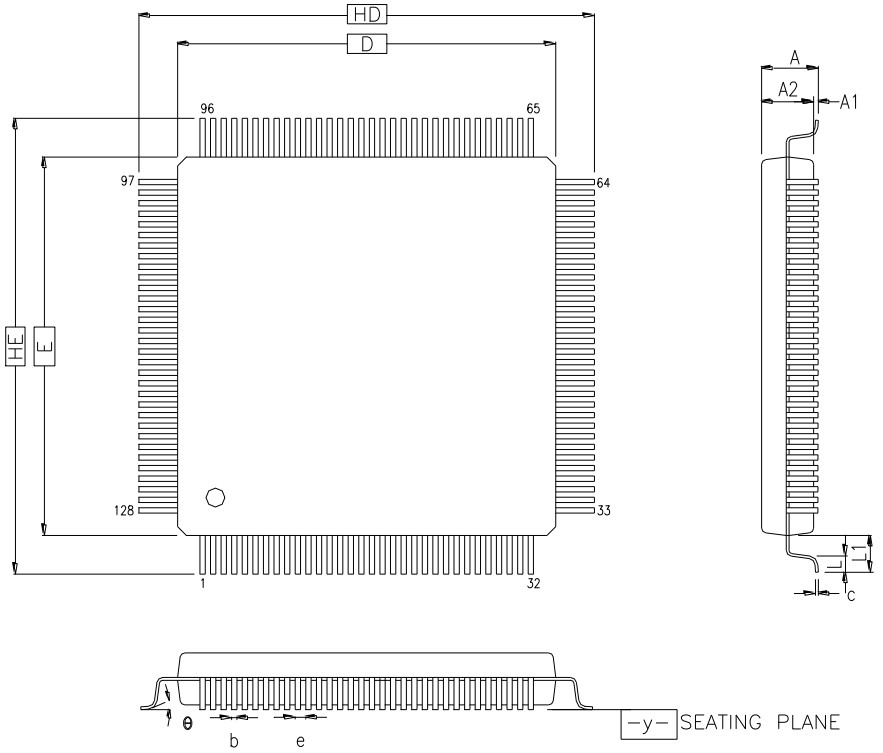
1st line: Nuvoton logo
2nd line: part number NCT6796D
3rd line: wafer production series lot number 28201234
4th line: tracking code 618G7AFA

618: packages made in 2016, week 18
G: assembly house ID; G means GR, A means ASE, etc.
7: code version; 7 means code 007
B: IC revision; A means version A; B means version B, and C means version C
FA: Nuvoton internal use.

28. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
NCT6796D	128Pin LQFP (Green package)	Commercial, 0°C to +70°C

29. PACKAGE SPECIFICATION



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

128-pin LQFP (14mm x 14mm x 1.4mm)

30. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.1	10/03/2016	N.A.	Draft datasheet to define features and pin configuration
0.2	02/16/2017	N.A.	Correct information
0.3	04/05/2017	7 ~ 28, 58, 272 39 87, 88 377 474	1. Modify Pin description and remove Pin 103 strapping function. 2. Modify Hardware monitor register 3. Modify PWROK Block Diagram 4. Modify SYSFANOUT DC output formula 5. Modify SMIOVT# Relative Register 6. Modify reset source 7. Add PCICLK_OUT delay time
0.4	05/05/2017	6,18, 250, 419, 422,427, 428,430, 449	1. Modify PWR_FAULT# function 2. Correct typo in Chapter 9.433, AUXFANIN3 -> AUXFANIN4
0.5	05/26/2017	376, 377,	1. Modify Chapter 24.1, CR 2Ch, bit 3 & bit 4 2. Modify Chapter 24.1, CR 2Fh, bit 2 3. Modify Chapter 24.12, Logical Device D, CR E1h, bit 3
0.6		473 59	1. Add LPC AC Specification. 2. Modify VIN9 and VIN8 register address.

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All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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