Arpan Swaroop

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Education

Purdue University — West Lafayette, IN
M.S. Computer Engineering, Elmore Family School of Electrical and Computer Engineering — *Aug. 2025 – Present*

University of Illinois at Urbana Champaign — Urbana Champaign, IL
B.S. Computer Engineering, Grainger College of Engineering — *Aug. 2021 – May 2025*

Relevant Coursework: Computer Organization and Design, Computer Systems Engineering, Distributed Systems, Database Systems, Multimedia Signal Processing, Digital Signal Processing, Data Structures and Algorithms

Technical Skills

Languages: Python, C/C++, Java, SQL (MySQL), JavaScript, HTML/CSS, System Verilog, x86 asm, Golang, Rust
Technologies: Jenkins CI/CD, Google Cloud Platform, ROS, Synopsis VCS
Developer Tools: Git, Docker, Linux

Experience

Software engineering intern — May 2025 - Aug 2025
Riverbed

- Parallelized fingerprinting algorithm across CPU cores and optimized SIMD execution with Intel AVX-512, boosting duplicate string detection efficiency in network acceleration infrastructure.
- Measured performance improvements using iperf, demonstrating 13% increased throughput in network traffic and reduction in retransmissions via reference-based messaging.
- Developed automated testing framework integrating KUnit harnesses, GTests, Valgrind/Helgrind, and Coccinelle static analysis, improving detection of race conditions and ensuring design-pattern compliance.
- Performed coverage analysis to validate kernel modifications, increasing test completeness and reducing regression risk.
- Migrated product release pipeline from Scientific Linux 2.6 to AlmaLinux Kernel 6.6, modernizing build environment and ensuring long-term supportability.
- Architected hierarchical Jenkins CI/CD jobs with Triggerbox builds, fully automating build/test workflows and accelerating release cycles.
- Enabled continuous integration and regression testing, cutting manual release overhead and significantly improving product launch reliability.

Research Assistant — Feb 2023 – Aug 2023
Advanced Controls Laboratory

- Implemented path planning algorithms in quadcopters to enable autonomous flight using Euclidean signed distance fields for flexible local planning.
- Developed rapidly exploring random tree (RRT) algorithm for efficient pathfinding and obstacle avoidance.
- Integrated depth-sense cameras into planning stack using ROS, enabling robust real-time localization.
- Prototyped on Nvidia Xavier NX, optimizing for embedded hardware constraints.

Projects

Out of Order RISC-V processor | *System Verilog, Synopsis VCS*

- Designed and tested an out of order processor using the explicit register renaming architecture
- Achieved third highest maximum frequency in class wide design competition with an Fmax of 630Mhz
- Achieved 0.4 IPC on the Coremark IM benchmark, with high instruction level parallelism
- Incorporated an instruction and data cache utilizing pipelined 4-way set associative caches
- Implemented integral components such as: Free list, reservation stations, register alias table, retirement register alias table, physical register file, mult/div functional unit, return order buffer, load store queue
- Incorporated dynamic branch prediction with a G-share branch predictor along with a Branch Target buffer
- Developed additional advanced features such as a split load store queue for out of order loads, as well as a next line prefetcher

Unix Like 32-bit x86 Operating System | *C, x86 asm*

- Architected a minimalistic multitasking operating system for x86 hardware, prioritizing efficiency and reliability
- Devised an interrupt-driven, time-slice-based CPU scheduling algorithm to schedule process execution
- Supported virtual memory using paging data-structures
- Developed a custom filesystem that supports basic file operations, utilizing storage, and I/O principles
- Implemented device drivers for keyboard, Real Time Clock, Programmable Interrupt Controller, and Programmable Interval Timer