Arpan Swaroop

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Education

University of Illinois at Urbana Champaign Urbana Champaign, IL
B.S. Computer Engineering, Grainger College of Engineering *Aug. 2021 – May 2025*
Relevant Coursework: Computer Organization and design, Computer Systems Engineering, Distributed systems, Database systems, Multimedia Signal Processing, Digital Signal Processing, Data structures and Algorithms

Technical Skills

Languages: Python, C/C++, System Verilog, Rust, x86 asm, RISC-V asm, Java, SQL(MySQL), JavaScript, HTML/CSS
Technologies: Cargo, Node.js, Express, Google Cloud Platform, Spring Framework, ROS, Synopsis VCS
Developer Tools: Git, Docker, Linux, Vim, Tmux

Experience

Web Developer Intern Jun 2024 – Aug 2024
Avermatix LLC.
- Redesigned landing page to include more modern and minimal UI/UX using Figma
- Implemented these changes using HTML/CSS and Javascript on the frontend
- Created a custom form, and connected it to a REST API written in Java using the Spring Boot framework
- Architected the integration of a relational database, designing the schema, and writing custom queries to handle user data for 100s of users
- Wrote a comprehensive business report about the impact of generative AI on low-code app building services

Embedded developer for ECTF Jan 2024 – May 2024
University of Illinois At Urbana Champaign
- Designed a secure embedded system for a medical device, in an intercollegiate embedded security competition
- Led the build subteam to design a secure hardware abstraction layer for the MAX78000FTHR microcontroller
- Implemented a secure interface to interact with the TRNG and the I2C communication protocol
- Created an automated attack platform to attack common vulnerabilities present in other teams' designs
- University of Illinois received 2nd place out of 76 teams

Research Assistant Feb 2023 – Aug 2023
Advanced Controls laboratory
- Implemented path planning algorithms in quad-copters, to allow for autonomous flight
- Developed these algorithms using Euclidean signed distance fields for fast and flexible local planning
- Implemented the rapidly exploring random trees algorithm for efficient path planning
- Utilized ROS to integrate the depth sense cameras used for localization and planning
- Developed on the Nvidia Xavier nx platform

Projects

Out of Order RISC-V processor | *System Verilog, Synopsis VCS*
- Designed and tested an out of order processor using the explicit register renaming architecture
- Achieved third highest maximum frequency in class wide design competition with an Fmax of 630Mhz
- Acheived 0.4 IPC on the Coremark IM benchmark, with high instruction level parallelism
- Incorporated an instruction and data cache utilizing pipelined 4-way set associative caches
- Implemented integral components such as: Free list, reservation stations, register alias table, retirement register alias table, physical register file, mult/div functional unit, return order buffer, load store queue
- Incorporated dynamic branch prediction with a G-share branch predictor along with a Branch Target buffer
- Developed additional advanced features such as a split load store queue for out of order loads, as well as a next line prefetcher

Unix Like 32-bit x86 Operating System | *C, x86 asm*
- Architected a minimalistic multitasking operating system for x86 hardware, prioritizing efficiency and reliability
- Devised an interrupt-driven, time-slice-based CPU scheduling algorithm to schedule process execution
- Supported virtual memory using paging data-structures
- Developed a custom filesystem that supports basic file operations, utilizing storage, and I/O principles
- Implemented device drivers for keyboard, Real Time Clock, Programmable Interrupt Controller, and Programmable Interval Timer