

# Arpan Swaroop

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## EDUCATION

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### Purdue University

*M.S. Computer Engineering, Elmore Family School of Electrical and Computer Engineering*

West Lafayette, IN

*Aug. 2025 – Present*

### University of Illinois at Urbana Champaign

*B.S. Computer Engineering, Grainger College of Engineering*

Urbana Champaign, IL

*Aug. 2021 – May 2025*

**Relevant Coursework:** Computer Organization and Design, Computer Systems Engineering, Distributed Systems, Database Systems, Multimedia Signal Processing, Digital Signal Processing, Data Structures and Algorithms

## TECHNICAL SKILLS

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**Languages:** Python, C/C++, Java, SQL (MySQL), JavaScript, HTML/CSS, System Verilog, x86 asm, Golang, Rust

**Technologies:** Node.js, Express, Google Cloud Platform, Spring Framework, ROS, Synopsis VCS

**Developer Tools:** Git, Docker, Linux

## EXPERIENCE

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### Software engineering intern

May 2025 - Aug 2025

*Riverbed*

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- Architected CI/CD pipeline for new product release
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### Research Assistant

Feb 2023 – Aug 2023

*Advanced Controls Laboratory*

- Implemented path planning algorithms in quad-copters, to allow for autonomous flight
- Developed these algorithms using Euclidean signed distance fields for fast and flexible local planning
- Implemented the rapidly exploring random trees algorithm for efficient path planning
- Utilized ROS to integrate the depth sense cameras used for localization and planning
- Developed on the Nvidia Xavier nx platform

## PROJECTS

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### Out of Order RISC-V processor | *System Verilog, Synopsis VCS*

- Designed and tested an out of order processor using the explicit register renaming architecture
- Achieved third highest maximum frequency in class wide design competition with an Fmax of 630Mhz
- Achieved 0.4 IPC on the Coremark IM benchmark, with high instruction level parallelism
- Incorporated an instruction and data cache utilizing pipelined 4-way set associative caches
- Implemented integral components such as: Free list, reservation stations, register alias table, retirement register alias table, physical register file, mult/div functional unit, return order buffer, load store queue
- Incorporated dynamic branch prediction with a G-share branch predictor along with a Branch Target buffer
- Developed additional advanced features such as a split load store queue for out of order loads, as well as a next line prefetcher

### Unix Like 32-bit x86 Operating System | *C, x86 asm*

- Architected a minimalistic multitasking operating system for x86 hardware, prioritizing efficiency and reliability
- Devised an interrupt-driven, time-slice-based CPU scheduling algorithm to schedule process execution
- Supported virtual memory using paging data-structures
- Developed a custom filesystem that supports basic file operations, utilizing storage, and I/O principles
- Implemented device drivers for keyboard, Real Time Clock, Programmable Interrupt Controller, and Programmable Interval Timer