

| Tool Version : Vivado v.2022.2 (win64) Build 3671981 Fri Oct 14 05:00:03 MDT 2022
| Date   : Tue Dec 23 13:23:35 2025
| Host   : aswin-iiitkottayam-iiitkottayam-ac-in running 64-bit major release (build 9200)
| Command   : report_utilization -file baud_gen_utilization_synth.rpt -pb baud_gen_utilization_synth.pb
| Design   : baud_gen
| Device   : xc7a12ticsg325-1L
| Speed File   : -1L
| Design State : Synthesized

Utilization Design Information

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1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	28	0	0	8000	0.35
LUT as Logic	28	0	0	8000	0.35
LUT as Memory	0	0	0	5000	0.00
Slice Registers	34	0	0	16000	0.21
Register as Flip Flop	34	0	0	16000	0.21
Register as Latch	0	0	0	16000	0.00
F7 Muxes	0	0	0	7300	0.00
F8 Muxes	0	0	0	3650	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation, is typically lower. Run opt_design after synthesis, if not already completed, for a more realistic count.
Warning! LUT value is adjusted to account for LUT combining.

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	_	-	-
0	_	-	Set
0	_	-	Reset
0	_	Set	-
0	_	Reset	-
0	Yes	-	-
0	Yes	-	Set
34	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Prohibited	Available	Util%
Block RAM Tile	0	0	0	20	0.00
RAMB36/FIFO*	0	0	0	20	0.00
RAMB18	0	0	0	40	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	0	0	0	40	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	4	0	0	150	2.67
Bonded IPADs	0	0	0	10	0.00
Bonded OPADs	0	0	0	4	0.00
PHY_CONTROL	0	0	0	3	0.00
PHASER_REF	0	0	0	3	0.00
OUT_FIFO	0	0	0	12	0.00
IN_FIFO	0	0	0	12	0.00
IDELAYCTRL	0	0	0	3	0.00
IBUFDS	0	0	0	144	0.00
GTPE2_CHANNEL	0	0	0	2	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	12	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	12	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	150	0.00
IBUFDS_GTE2	0	0	0	2	0.00
ILOGIC	0	0	0	150	0.00
OLOGIC	0	0	0	150	0.00

5. Clocking

Site Type	Used	Fixed	Prohibited	Available	Util%
BUFGCTRL	1	0	0	32	3.13
BUFIO	0	0	0	12	0.00
MMCME2_ADV	0	0	0	3	0.00
PLLE2_ADV	0	0	0	3	0.00
BUFMRCE	0	0	0	6	0.00
BUFHCE	0	0	0	48	0.00
BUFR	0	0	0	12	0.00

6. Specific Feature

Site Type	Used	Fixed	Prohibited	Available	Util%
BSCANE2	0	0	0	4	0.00
CAPTUREE2	0	0	0	1	0.00
DNA_PORT	0	0	0	1	0.00
EFUSE_USR	0	0	0	1	0.00
FRAME_ECCE2	0	0	0	1	0.00
ICAPE2	0	0	0	2	0.00
PCIE_2_1	0	0	0	1	0.00

| STARTUPE2 | 0 | 0 | 0 | 1 | 0.00 |
| XADC | 0 | 0 | 0 | 1 | 0.00 |

7. Primitives

Ref Name	Used	Functional Category
FDCE	34	Flop & Latch
LUT3	32	LUT
CARRY4	8	CarryLogic
LUT4	5	LUT
LUT6	3	LUT
LUT5	3	LUT
OBUF	2	IO
IBUF	2	IO
LUT1	1	LUT
BUFG	1	Clock

8. Black Boxes

Ref Name	Used

9. Instantiated Netlists

Ref Name	Used