100 Days of RTL

DAY 2

Structural Modelling

Achutha Aswin Naick

Introduction

Structural modelling in Verilog represents digital circuits in terms of their gate-level connections rather than describing their behaviour. In this project, basic logic gates (AND, OR, NOT, NAND, NOR, XOR, and XNOR) were implemented using structural modelling in Verilog. A corresponding testbench was developed to simulate the circuit and verify its correctness.

Implementation Details

The logic gate module, logic_gates, takes two input signals (a and b) and produces outputs corresponding to the seven basic logic operations. Unlike behavioural modelling, structural modelling uses assign statements to continuously assign values to the output signals based on Boolean expressions. Since these assignments are continuous, the outputs are declared as wire instead of reg.

The testbench module, logic_gate_tb, is used to verify the functionality of the logic_gates module. The testbench instantiates the design under test (DUT) and applies different input combinations with time delays (#10). The outputs are declared as wire since they are driven by the DUT.

Code Explanation

The main module and testbench include:

- **Input and Output Declaration:** Inputs (a and b) are declared as input types, while outputs (and_gate, or_gate, etc.) are declared as output wire since they are continuously assigned values.
- **Continuous Assignment (assign Statements):** Used to define logic functions without procedural blocks, ensuring real-time updates of the outputs.
- **Boolean Operations:** The bitwise operators (&, |, ~, ^) are used to define the logical relationships.
- **Instantiation in Testbench:** The DUT is instantiated with named mapping to connect signals.

- **Simulation Execution:** The initial block runs only once and assigns different values to the inputs over time to simulate different conditions.

Simulation and Results

The testbench applies four input combinations (00, 01, 10, 11) at 10-time unit intervals. The expected outputs for each logic operation are observed using waveform simulation. The results confirm that the structural model correctly implements the logic gates.

Conclusion

This project successfully demonstrates the implementation of logic gates using structural modelling in Verilog. The use of continuous assignments highlights how hardware components are interconnected at the gate level.

Future Enhancements

Future enhancements could include additional gates and more complex combinational logic circuits.