**1 Marks Questions (ANSWERS HIGHLIGHTED IN RED)**

1. **For a pipelined CPU with a single ALU, consider the following situations  
   1.The j+1th instruction uses the result of the jth instruction as an operand  
   2.The execution of a conditional jump instruction  
   3. The jth and j+1 instruction require the ALU  at the same time**

**Which of the above can cause a hazard?**

|  |  |
| --- | --- |
|  | 1and 2 only |
|  | 2and 3 only |
|  | 3 only |
|  | All the Three |

1. **Comparing the time T1 taken for a single instruction on a pipelined CPU with time T2 taken on a non-pipelined but identical CPU, we can say that**

|  |  |
| --- | --- |
|  | T1≤T2 |
|  | **T1≥T2** |
|  | T1<T2 |
|  | T1 is T2 plus the time taken for one instruction fetch cycle |

1. **Register renaming is done in pipelined processors**

|  |  |
| --- | --- |
|  | as an alternative to register allocation at compile time |
|  | for efficient access to function parameters and local variables |
|  | **to handle certain kinds of hazards** |
|  | as part of address translation |

A

1. **Marks Questions**
2. **Suppose the functions F and G can be computed in 5 and 3 nanoseconds by functional units UF and UG, respectively. Given two instances of UF and two instances of UG, it is required to implement the computation**

**F (G (Xi)) for 1≤i≤10.**

**Ignoring all other delays, the minimum time required to complete this computation is \_\_\_\_\_\_\_\_\_\_\_\_\_ nanoseconds.**

Correct Answer is **28**

1. **Consider a 3 GHz (gigahertz) processor with a three-stage pipeline and stage latencies τ1, τ2, and τ3 such that τ1=3τ2/4=2τ3. If the longest pipeline stage is split into two pipeline stages of equal latency, the new frequency is \_\_\_\_\_\_\_\_\_\_\_\_ GHz, ignoring delays in the pipeline registers.**

Correct answer is between **3.9**and **4.1**

1. **The stage delays in a 4 -stage pipeline are 800,500,400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput increase of the pipeline is \_\_\_\_\_\_\_ percent.**

Correct answer is between **33**and **34**

**5 Marks Questions**

1. **Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate-**
2. **Pipeline cycle time**
3. **Non-pipeline execution time**
4. **Speed up ratio**
5. **Pipeline time for 1000 tasks**
6. **Sequential time for 1000 tasks**
7. **Throughput**

**Solution-**

Given-

Four stage pipeline is used

Delay of stages = 60, 50, 90 and 80 ns

Latch delay or delay due to each register = 10 ns

**Cycle time**

= Maximum delay due to any stage + Delay due to its register

= Max { 60, 50, 90, 80 } + 10 ns

= 90 ns + 10 ns= 100 ns

**Non-Pipeline Execution Time-**

Non-pipeline execution time for one instruction

= 60 ns + 50 ns + 90 ns + 80 ns= 280 ns

**Speed Up Ratio-**

Speed up

= Non-pipeline execution time / Pipeline execution time

= 280 ns / Cycle time = 280 ns / 100 ns= 2.8

**Pipeline Time for 1000 Tasks**

= Time taken for 1st task + Time taken for remaining 999 tasks

= 1 x 4 clock cycles + 999 x 1 clock cycle

= 4 x cycle time + 999 x cycle time

= 4 x 100 ns + 999 x 100 ns

= 400 ns + 99900 ns = 100300 ns

**Sequential Time for 1000 Tasks**

Non-pipeline time for 1000 tasks

= 1000 x Time taken for one task

= 1000 x 280 ns = 280000 ns

**Throughput**

Throughput for pipelined execution

= Number of instructions executed per unit time

= 1000 tasks / 100300 ns

1. **Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I1, I2, I3… I12 is executed in this pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is**

**(A) 132  
(B) 165  
(C) 176  
(D) 328**

**Solution**

Pipeline will have to be stalled till Ei stage of I4 completes, as Ei stage will tell whether to take branch or not.

After that I4 (WO) and I9 (Fi) can go in parallel and later the following instructions.

So, till I4 (Ei) completes : 7 cycles \* (10 + 1 ) ns = 77ns

From I4(WO) or I9(Fi) to I12(WO) : 8 cycles \* (10 + 1)ns = 88ns

Total = 77 + 88 = 165 ns

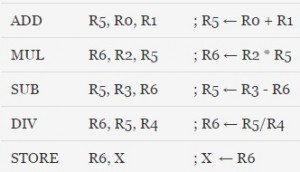
1. **The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. The number of clock cycles required for completion of execution of the sequence of instruction is \_\_\_\_\_\_ .**
2. **219 (B) 104 (C) 115 (D) 220**

**Solution**

Given, total number of instructions (n) = 100  
Number of stages (k) = 5  
Since, if n instructions take c cycle, so (c-1) stalls will occur for these instructions.

Therefore, the number of clock cycles required = Total number of cycles required in general case + Extra cycles required (here, in PO stage)  
= (n + k – 1) + Extra cycles  
= (100 + 5 -1) + 40\*(3-1)+35\*(2-1)+20\*(1-1)  
= (100 + 4) + 40\*2+35\*1+20\*0= 104 + 115= 219 cycles

1. **A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement X = (S – R \* (P + Q))/T is given below. The values of variables P, Q, R, S and T are available in the registers R0, R1, R2, R3 and R4 respectively, before the execution of the instruction sequence.**



**The number of Read-After-Write (RAW) dependencies, Write-After-Read( WAR) dependencies, and Write-After-Write (WAW) dependencies in the sequence of instructions are, respectively,  
(A) 2, 2, 4  
(B) 3,2,3  
(C) 4,2,2  
(D) 3,3,2**

**Solution:**

 Read After Write:  
1. ADD ->MUL (R5)  
2. MUL -> SUB (R6)  
3. SUB-> DIV (R5)  
4. DIV->STORE (R6)  
Write After Read  
1. MUL -> SUB (R5)  
2. DIV -> STORE (R6)  
Write After Write  
1. ADD -> SUB (R5)  
2. MUL – DIV (R6)

1. **An instruction pipeline has five stages where each stage takes 22 nanoseconds and all instructions use all five stages. Branch instructions are not overlapped, i.e., the instruction after the branch is not fetched till the branch instruction is completed. Under ideal conditions,**
2. **Calculate the average instruction execution time assuming that 2020% of all instruction executed are branch instructions. Ignore the fact that some branch instructions may be conditional.**
3. **If a branch instruction is a conditional branch instruction, the branch need not be taken. If the branch is not taken, the following instructions can be overlapped. When 8080% of all branch instructions are conditional branch instructions, and 5050% of the conditional branch instructions are such that the branch is taken, calculate the average instruction execution time.**

**Solution:**

(a) Average instruction execution time =3.6 ns

(b) Average instruction execution time = 2.96 ns

1. **A four stage pipeline has the stage delays as 150, 120, 160 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, the total time taken to process 1000 data items on the pipeline will be-**
2. **120.4 microseconds**
3. **160.5 microseconds**
4. **165.5 microseconds**
5. **590.0 microseconds**

**Solution:**

Given-

Four stage pipeline is used

Delay of stages = 150, 120, 160 and 140 ns

Delay due to each register = 5 ns

1000 data items or instructions are processed

 Cycle time

= Maximum delay due to any stage + Delay due to its register

= Max {150, 120, 160, 140 } + 5 ns

= 160 ns + 5 ns= 165 ns

Pipeline time to process 1000 data items

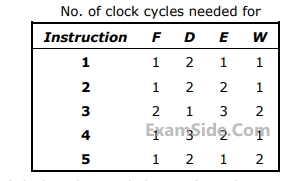
= Time taken for 1st data item + Time taken for remaining 999 data items

= 1 x 4 clock cycles + 999 x 1 clock cycle

= 4 x cycle time + 999 x cycle time

= 4 x 165 ns + 999 x 165 ns= 660 ns + 164835 ns== 165495 ns= 165.5 μs

Thus, Option (C) is correct.

1. **An instruction pipeline consists of 4 stages: Fetch (F), Decode field (D), Execute (E), and Result-Write (W). The 5 instructions in a certain instruction sequence need these stages for the different number of clock cycles as shown by the table below.**

**Find the number of clock cycles needed to perform the 5 instructions**

**Solution:** 15 Cycles.

1. **Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of 4. The same processor is upgraded to a pipelined processor with five stages but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume there are no stalls in the pipeline. The speed up achieved in this pipelined processor is-**
2. **3.2**
3. **3.0**
4. **2.2**
5. **2.0**

## Solution-

 Cycle Time in Non-Pipelined Processor-

 Frequency of the clock = 2.5 gigahertz

Cycle time= 1 / frequency= 1 / (2.5 gigahertz)= 1 / (2.5 x 109 hertz)= 0.4 ns

 Non-Pipeline Execution Time-

 Non-pipeline execution time to process 1 instruction

= Number of clock cycles taken to execute one instruction

= 4 clock cycles= 4 x 0.4 ns= 1.6 ns

### Cycle Time in Pipelined Processor-

 Frequency of the clock = 2 gigahertz

Cycle time= 1 / frequency= 1 / (2 gigahertz)= 1 / (2 x 109 hertz)= 0.5 ns

**Pipeline Execution Time**

 Since there are no stalls in the pipeline, so ideally one instruction is executed per clock cycle. So,Pipeline execution time= 1 clock cycle= 0.5 ns

 Speed Up= Non-pipeline execution time / Pipeline execution time

= 1.6 ns / 0.5 ns= 3.2

Thus, Option (A) is correct.

1. **The stage delays in a 4 stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds.**

**The throughput increase of the pipeline is \_\_\_\_\_%.**

## Solution-

**Execution Time in 4 Stage Pipeline-**

 Cycle time

= Maximum delay due to any stage + Delay due to its register

= Max { 800, 500, 400, 300 } + 0

= 800 picoseconds

Thus, Execution time in 4 stage pipeline = 1 clock cycle = 800 picoseconds.

**Throughput in 4 Stage Pipeline-**

 = Number of instructions executed per unit time

= 1 instruction / 800 picoseconds

**Execution Time in 2 Stage Pipeline-**

 Cycle time

= Maximum delay due to any stage + Delay due to its register

= Max { 600, 350 } + 0= 600 picoseconds

Thus, Execution time in 2 stage pipeline = 1 clock cycle = 600 picoseconds.

### ****Throughput in 2 Stage Pipeline-****

 Throughput

= Number of instructions executed per unit time

= 1 instruction / 600 picoseconds

### ****Throughput Increase-****

 Throughput increase

= { (Final throughput – Initial throughput) / Initial throughput } x 100

= { (1 / 600 – 1 / 800) / (1 / 800) } x 100

= { (800 / 600) – 1 } x 100

= (1.33 – 1) x 100

= 0.3333 x 100

= 33.33 %

1. **A non-pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 ns, 1.5 ns, 2 ns, 1.5 ns and 2.5 ns respectively. The delay of the latches is 0.5 sec.**

**The speed up of the pipeline processor for a large number of instructions is-**

1. **4.5**
2. **4.0**
3. **3.33**
4. **3.0**

**Solution-**

### ****Cycle Time in Non-Pipelined Processor-****

 Frequency of the clock = 100 MHz

Cycle time= 1 / frequency= 1 / (100 MHz)= 1 / (100 x 106 hertz)= 0.01 μs

### ****Non-Pipeline Execution Time-****

 Non-pipeline execution time to process 1 instruction

= Number of clock cycles taken to execute one instruction

= 1 clock cycle= 0.01 μs= 10 ns

**Cycle Time in Pipelined Processor-**

 Cycle time

= Maximum delay due to any stage + Delay due to its register

= Max { 2.5, 1.5, 2, 1.5, 2.5 } + 0.5 ns

= 2.5 ns + 0.5 ns= 3 ns

### ****Pipeline Execution Time-****

 Pipeline execution time

= 1 clock cycle

= 3 ns

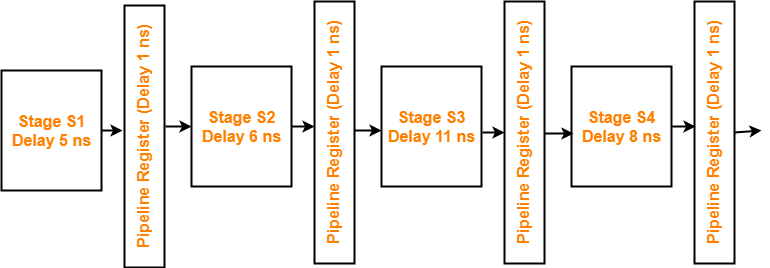
 Speed Up-

Speed up= Non-pipeline execution time / Pipeline execution time

= 10 ns / 3 ns= 3.33

Thus, Option (C) is correct.

1. **Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure-**



**What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?**

1. **4.0**
2. **2.5**
3. **1.1**
4. **3.0**

**Solution-**

### ****Non-Pipeline Execution Time-****

 Non-pipeline execution time for 1 instruction

= 5 ns + 6 ns + 11 ns + 8 ns

= 30 ns

### ****Cycle Time in Pipelined Processor-****

 Cycle time

= Maximum delay due to any stage + Delay due to its register

= Max { 5, 6, 11, 8 } + 1 ns= 11 ns + 1 ns= 12 ns

### ****Pipeline Execution Time-****

Pipeline execution time

= 1 clock cycle= 12 ns

**Speed Up-**

 Speed up

= Non-pipeline execution time / Pipeline execution time

= 30 ns / 12 ns= 2.5

Thus, Option (B) is correct.

1. **Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3 and I4 in stages S1, S2, S3 and S4 is shown below-**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **S1** | **S2** | **S3** | **S4** |
| **I1** | **2** | **1** | **1** | **1** |
| **I2** | **1** | **3** | **2** | **2** |
| **I3** | **2** | **1** | **1** | **3** |
| **I4** | **1** | **2** | **2** | **2** |

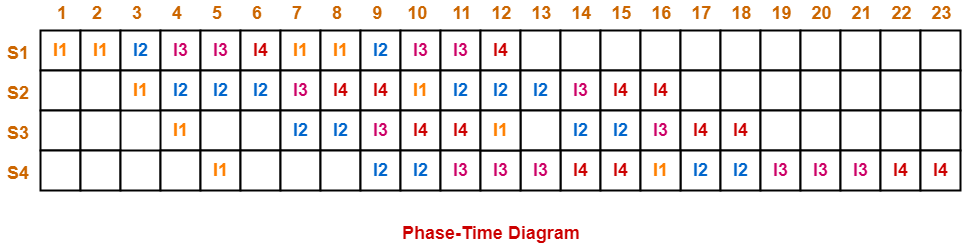
**What is the number of cycles needed to execute the following loop?**

**for(i=1 to 2) { I1; I2; I3; I4; }**

1. 16
2. 23
3. 28
4. 30

## Solution-

 The phase-time diagram is-



From here, number of clock cycles required to execute the loop = 23 clock cycles.

Thus, Option (B) is correct.

1. **Consider a pipelined processor with the following four stages-**

**IF : Instruction Fetch**

**ID : Instruction Decode and Operand Fetch**

**EX : Execute**

**WB : Write Back**

**The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction need 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?**

**ADD R2, R1, R0      R2 ← R0 + R1**

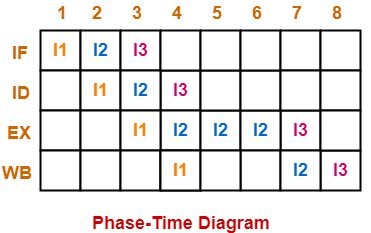
**MUL R4, R3, R2      R4 ← R3 + R2**

**SUB R6, R5, R4      R6 ← R5 + R4**

1. **7**
2. **8**
3. **10**
4. **14**

**Solution-**

The phase-time diagram is-



From here, number of clock cycles required to execute the instructions = 8 clock cycles.

Thus, Option (B) is correct.

1. **Consider the following procedures. Assume that the pipeline registers have zero latency.**

**P1 : 4 stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns**

**P2 : 4 stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns**

**P3 : 5 stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns**

**P4 : 5 stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns**

**Which procedure has the highest peak clock frequency?**

1. **P1**
2. **P2**
3. **P3**
4. **P4**

**Solution-**

 It is given that pipeline registers have zero latency. Thus,

Cycle time

= Maximum delay due to any stage + Delay due to its register

= Maximum delay due to any stage

### ****For Processor P1:****

 Cycle time

= Max { 1 ns, 2 ns, 2 ns, 1 ns }

= 2 ns

 Clock frequency

= 1 / Cycle time= 1 / 2 ns= 0.5 gigahertz

### ****For Processor P2:****

 Cycle time

= Max { 1 ns, 1.5 ns, 1.5 ns, 1.5 ns }= 1.5 ns

 Clock frequency

= 1 / Cycle time= 1 / 1.5 ns= 0.67 gigahertz

### ****For Processor P3:****

Cycle time= Max { 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns }= 1 ns

 Clock frequency= 1 / Cycle time= 1 / 1 ns= 1 gigahertz

### ****For Processor P4:****

Cycle time= Max {0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns} = 1.1 ns

 Clock frequency= 1 / Cycle time= 1 / 1.1 ns= 0.91 gigahertz

 Clearly, Process P3 has the highest peak clock frequency.

Thus, Option (C) is correct.

1. **Consider a 3 GHz (gigahertz) processor with a three-stage pipeline and stage latencies T1, T2 and T3 such that T1 = 3T2/4 = 2T3. If the longest pipeline stage is split into two pipeline stages of equal latency, the new frequency is \_\_\_\_ GHz, ignoring delays in the pipeline registers.**

**Solution-**

 Let ‘t’ be the common multiple of each ratio, then-

T1 = t

T2 = 4t / 3,T3 = t / 2

### ****Pipeline Cycle Time-****

 Pipeline cycle time

= Maximum delay due to any stage + Delay due to its register

= Max { t, 4t/3, t/2 } + 0= 4t/3

**Frequency Of Pipeline-**

 Frequency

= 1 / Pipeline cycle time = 1 / (4t / 3) = 3 / 4t

 Given frequency = 3 GHz. So,

3 / 4t = 3 GHz,4t = 1 ns,t = 0.25 ns

### ****Stage Latencies Of Pipeline-****

 Stage latency of different stages are-

Latency of stage-01 = 0.25 ns

Latency of stage-02 = 0.33 ns

Latency of stage-03 = 0.125 ns

**Splitting The Pipeline-**

The stage with longest latency i.e. stage-02 is split up into 4 stages.

After splitting, the latency of different stages are-

Latency of stage-01 = 0.25 ns

Latency of stage-02 = 0.165 ns

Latency of stage-03 = 0.165 ns

Latency of stage-04 = 0.125 ns

### ****Splitted Pipeline Cycle Time-****

 Splitted pipeline cycle time

= Maximum delay due to any stage + Delay due to its register

= Max { 0.25, 0.165, 0.165, 0.125 } + 0

= 0.25 ns

### ****Frequency Of Splitted Pipeline-****

 Frequency =1/ splitted pipeline cycle time=1/0.25 ns=4 Ghz. Thus, new frequency =4 GHz