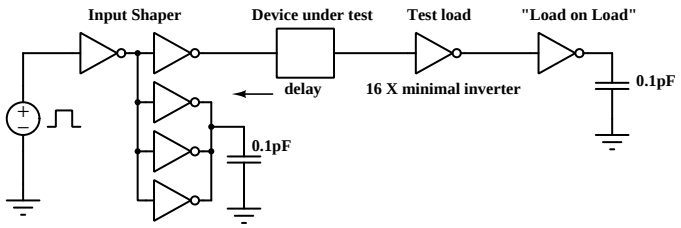
Monday	EE 671: VLSI Design	Due on
Oct.02, 2018	Assignment 3	Oct. 16, 2018

We want to model the performance of a 32 bit Kogge Stone adder.
To construct the adder, we shall design circuits using domino logic for generating G and P signals at different levels. These circuits should be laid out using the SCL process, back extracted and simulated to evaluate their delay. This delay will be used in a VHDL model. The Kogge Stone adder should be described structurally in VHDL and simulated with appropriate test vectors to find the worst case delay.

Q–1 Lay out domino Circuits for generating $A \cdot B$, $A + B$ and $A + B.C$. (These will have a dynamic circuit producing the inverted input, followed by static CMOS inverters). Geometries of n channel transistors in the dynamic gates are to be determined by applying series parallel rules to the minimum inverter nMOS size from the previous assignment. The p channel pull up of the dynamic gate should have the same size as used in the minimal inverter. The static inverter following the dynamic gates will be sized to 4X the minimal inverter size.

Back extract and evaluate the delay of these circuits using a circuit similar to the one used in assignment-2, as shown below.



One of the input can be held constant ('1' for AND, '0' for OR) while the other input is switched to evaluate the delay. In case of A + B.C, A should be held at '0', B at '1' and C should be switched to determine the delay.

Q–2 Now define VHDL entities for generating P and G values at different levels. At the first level,

$$P = A + B \qquad G = A \cdot B$$

For recursive generation of P and G for higher levels,

$$G_{i+1} = G_i + P_i \cdot G_{i-1} \qquad Pi + 1 = P_i \cdot P_{i-1}$$

Use the AFTER clause in these circuits to assign the delays as determined above. Use these as components in a 32 bit Kogge Stone adder and simulate its performance for various test vectors. Determine the test vector which will traverse the critical path and determine the worst case delay for the adder.