College of Engineering Trivandrum

Department of Electronics and Communication Engineering

ECL332 Communication Engineering Laboratory

Experiment No. 4

Hardware Implementation of BPSK Modulation and Demodulation

Name:	__________________	Date:	__________________
Roll No.:	__________________	Batch:	__________________

---

1. Aim

To design and set up a **BPSK modulator** and **BPSK demodulator** using discrete hardware blocks and verify the waveforms on a DSO.

2. Learning Outcomes

After completing this experiment, the student will be able to:

- Explain BPSK as a $\{0, \pi\}$ (or ± 1) phase modulation scheme and relate it to a constellation.
- Generate **carrier** and **inverted carrier** and use a switching/selection mechanism to form BPSK.
- Perform **coherent demodulation** using carrier-assisted detection, rectification, LPF, and thresholding.
- Identify and justify the role of each stage by observing intermediate waveforms on a DSO.

3. Prerequisites

- Inverting amplifier: gain and phase inversion
- Summing amplifier (adder) using op-amp
- Rectifier + RC low-pass filtering
- Comparator / threshold detector using reference from potentiometer
- Function generator + DSO operation (frequency, Vpp, triggering)

4. Apparatus / Components

Instruments:

- Dual-channel function generator (preferred) OR two synchronized generators
- Dual power supply (or equivalent arrangement to obtain ± 5 V)
- Digital Storage Oscilloscope (DSO) and probes
- Breadboard and connecting wires

ICs / Active devices:

- LM741 op-amp **(4 nos.)**
- CD4016 (bilateral switch) **(1 no.)**

- Diode 1N4007 **(1 no.)**

Passive components (typical as per circuit):

- Resistors: $10\,\mathrm{k}\Omega$ (multiple), $15\,\mathrm{k}\Omega$ (1), $1\,\mathrm{k}\Omega$ (2)
- Capacitor: $0.01\,\mu\mathrm{F}$ (1)
- Potentiometer (for threshold setting): ______________________________ (e.g., $10\,\mathrm{k}\Omega$)

5. Safety & Precautions

- Verify op-amp pinout and ensure correct ± 5 V connections **before** inserting ICs.
- Keep signal amplitudes within supply rails; avoid overdriving 741 inputs.
- Ensure **common ground** between power supply, function generator(s), and DSO.
- Use proper DSO probing and grounding to avoid short circuits/noisy readings.
- Coherent demodulation needs a **phase-aligned carrier**; use a dual-channel generator if possible.

6. Theory

6.1 BPSK principle

Binary Phase Shift Keying (BPSK) is a digital modulation scheme in which the information bit is conveyed by **two possible phases** of a sinusoidal carrier that differ by 180° (i.e., π radians). Hence, the carrier either appears in its original form or in an inverted form.

Let the binary data be mapped to a polar NRZ waveform $b(t) \in \{+1, -1\}$ such that

$$b(t) = \begin{cases} +1, & \text{bit } 1 \\ -1, & \text{bit } 0 \end{cases}$$

Then the BPSK signal is

$$s(t) = A\, b(t) \cos(2\pi f_c t),$$

where A is the carrier amplitude and f_c is the carrier frequency. When $b(t)$ changes sign, the transmitted signal becomes

$$s(t) = -A \cos(2\pi f_c t) = A \cos(2\pi f_c t + \pi),$$

which shows that a bit transition causes a π phase reversal.

Key features of BPSK:

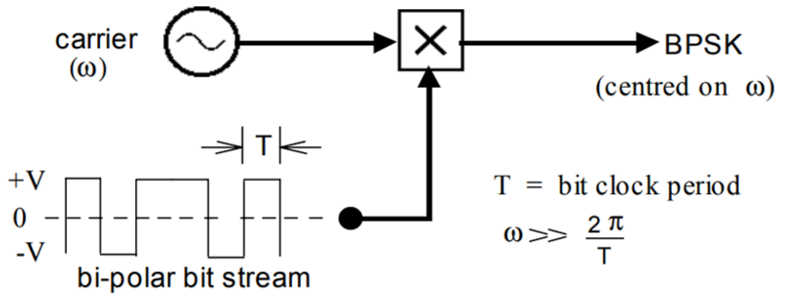
- **Constant envelope:** amplitude remains constant; only phase changes.
- **Two-point constellation:** points at $+A$ and $-A$ on the in-phase axis.
- **Robustness:** among PSK schemes, BPSK has the best noise performance for a given energy/bit.

6.2 Hardware realization idea

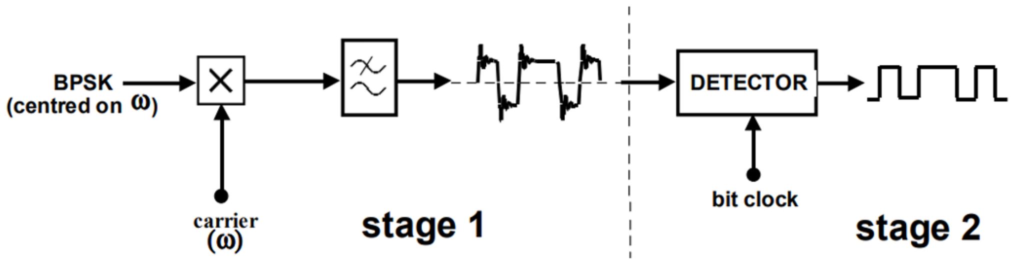
(a) BPSK Modulator

In the hardware implementation, BPSK can be realized by **selecting one of two carrier waveforms**: the carrier $c(t) = A\cos(2\pi f_c t)$ and its inverted version $-c(t)$.

- The **carrier** is generated using a function generator.
- An op-amp inverter produces the **inverted carrier** (180° phase-shifted).



(a) BPSK modulator



(b) BPSK demodulator

Figure 1: BPSK Block diagram

- The input data is applied as a **control signal** (and its complement is also generated if required).
- Using an **analog switch (CD4016)** / selection network:
  - If data corresponds to $b(t) = +1$, the switch selects $+c(t)$.
  - If data corresponds to $b(t) = -1$, the switch selects $-c(t)$.

  Thus, the modulator output is

$$s(t) = \begin{cases} +A\cos(2\pi f_c t), & b(t) = +1 \\ -A\cos(2\pi f_c t), & b(t) = -1 \end{cases}$$

which is precisely BPSK. On the DSO, the phase reversal can be clearly observed at the bit boundaries whenever the data changes state.

(b) BPSK Demodulator (Coherent Detection: Add-and-Detect Method)

Demodulation of BPSK requires a **reference carrier** that is frequency- and phase-aligned with the transmitter (*coherent detection*). In this experiment, the same carrier generator is used to provide the local reference, so that the phase alignment is maintained.

Adder stage idea: The received BPSK signal is added to the reference carrier:

$$v_a(t) = s(t) + A\cos(2\pi f_c t).$$

Now consider the two cases:

- If $s(t) = +A\cos(2\pi f_c t)$ (bit mapped to $+1$), then

$$v_a(t) = 2A\cos(2\pi f_c t) \quad \Rightarrow \quad \text{large amplitude.}$$

- If $s(t) = -A\cos(2\pi f_c t)$ (bit mapped to -1), then

$$v_a(t) = 0 \quad \text{(ideally)} \Rightarrow \text{very small amplitude.}$$

Hence, the **adder output amplitude** becomes a reliable indicator of the transmitted bit.

Rectifier + LPF: The adder output is then

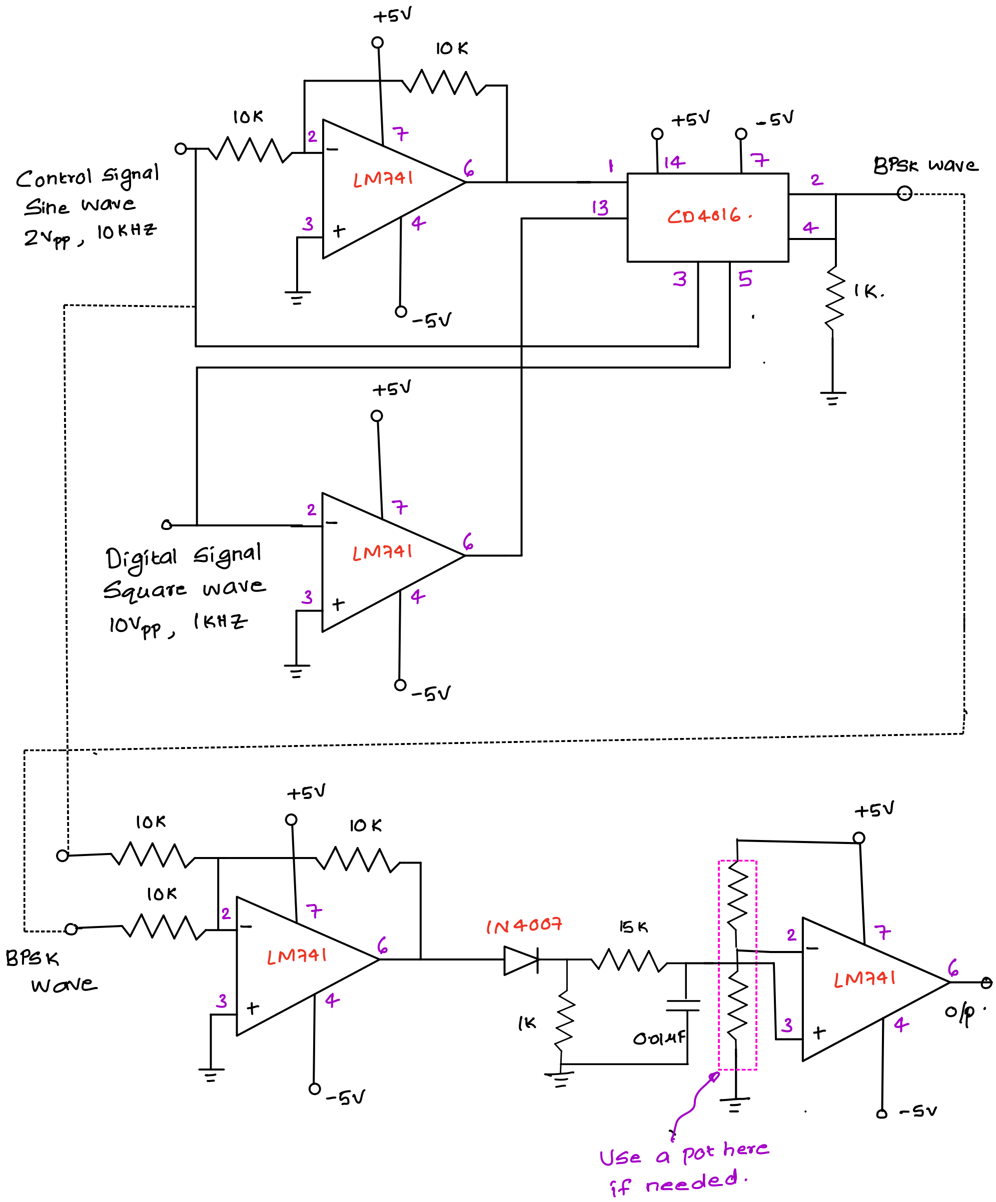
- **Rectified** (diode stage) to convert the sinusoidal amplitude difference into a unipolar waveform.
- Passed through a **low-pass filter (RC)** to extract the **envelope** (average level over each bit period) while removing carrier-frequency ripple.

Comparator/threshold decision: Finally, a comparator compares the filtered envelope with a reference level set by a potentiometer:

- If envelope > threshold ⇒ output logic "1"
- If envelope < threshold ⇒ output logic "0"

Important note: If the reference carrier is not phase-aligned, the "large" and "small" levels at the adder output will not be well separated, and the recovered data becomes distorted or erroneous. This is why coherent synchronization is critical in BPSK demodulation.

7. Circuit Diagram



8. Pre-Lab Questions (Answer in the space provided)

1. For a bit rate of $R_b = 1$ kHz ($T_b = 1$ ms) and carrier $f_c = 10$ kHz, compute the number of carrier cycles per bit.

2. Draw the expected BPSK waveform for the bit sequence 1 0 1 1 0 assuming bit "1" corresponds to a π phase reversal.

3. An inverting amplifier uses $R_{\text{in}} = 10\,\text{k}\Omega$ and $R_f = 10\,\text{k}\Omega$. (i) Find the voltage gain, (ii) state the phase shift introduced.

4. For the RC low-pass stage with $R = 15\,\text{k}\Omega$ and $C = 0.01\,\mu\text{F}$, compute the cutoff frequency $f_c = \frac{1}{2\pi RC}$, and comment whether it should pass the *bit-rate envelope* while rejecting the *carrier ripple.*

5. Explain (in 2–3 lines) why coherent demodulation requires a carrier that is frequency- and phase-aligned with the transmitter carrier.

9. Procedure

9.1 Power supply arrangement for ±5 V

1. Set the **fixed 5 V** section and the **0–30 V variable** section to **5 V**.
2. Connect the **+ terminal of fixed 5 V** to the **ground of the variable supply**. This becomes **common ground**.

3. Then: **variable + terminal** acts as +5 V and **fixed-supply ground** acts as −5 V.

9.2 Signal generation

1. Generate **digital data** using function generator: square wave, $f_b \approx 1$ kHz, $V_{pp} \approx 10$ V.
2. Generate **carrier**: sine wave, $f_c \approx 10$ kHz, $V_{pp} \approx 2$ V.
3. Ensure generator ground is common with circuit ground and DSO ground.

9.3 Modulator setup and checks

1. Build the modulator section as per circuit.
2. Verify and display on DSO:
   - Carrier and **inverted carrier**
   - Digital signal and **inverted digital signal** (if used)
   - Outputs from the switching/selection stage (e.g., CD4016 outputs)
3. Observe and store the **BPSK modulated waveform** at the modulator output.

9.4 Demodulator setup and checks

1. Connect the demodulator section as per circuit.
2. Feed **BPSK output** and the **carrier** into the adder stage.
3. Observe sequentially:
   - Output of **adder**
   - Output of **rectifier**
   - Output of **low-pass filter**
4. Adjust the **potentiometer/reference** in the comparator stage until a clean digital output is obtained.
5. Compare **input digital signal** and **demodulated signal** on DSO (dual trace).

10. Observations

10.1 Waveform checkpoints (sketch neatly)

Modulator:

(a) Carrier and inverted carrier

(b) Digital signal and inverted digital signal

(c) Switch outputs (e.g., CD4016 pin outputs)

(d) BPSK modulated waveform

Demodulator:

(e) Adder output

(f) Rectifier output

(g) LPF output

(h) Input digital vs demodulated digital

(i) BPSK vs demodulated digital

11. Calculations / Design Notes (show steps)

1. RC low-pass cutoff frequency: $f_c = \frac{1}{2\pi RC}$
   Given: $R =$ __________, $C =$ __________
   Computed: $f_c =$ ____________________

2. Threshold/reference used in comparator (from potentiometer):

   Observed reference voltage: ____________________ V

3. Note any phase delay between input and recovered data and possible reasons:

12. Result

- BPSK modulator circuit was implemented and the modulated waveform was observed on DSO.
- BPSK demodulator circuit was implemented and the digital data was recovered using coherent detection.

(Write a 2–3 line result statement in your own words based on your observation.)

13. Inference / Discussion (Answer briefly)

1. Where do you observe the 180° phase reversal in the modulated signal?

2. Why is rectification + LPF used before the comparator?

3. What happens if the carrier used in the demodulator is not phase-aligned?

14. Post-Lab / Viva Questions

1. What is the role of the analog switch (CD4016) in modulation?

2. Identify the purpose of each stage: adder, rectifier, LPF, comparator.

3. How will the choice of LPF cutoff affect the recovered data waveform?

4. Suggest two reasons for slight delay/phase shift in the demodulated output.

15. Troubleshooting Checklist

- No BPSK waveform: verify carrier/inverted-carrier and proper switching control signals.
- Demodulated output noisy: adjust DSO trigger, check diode orientation, verify LPF RC values.
- Wrong logic levels: re-check comparator reference (pot) and ensure correct grounding.
- Output stuck high/low: check adder stage connections and ensure carrier phase alignment.
